Surface Mount - Mounting Pad Dimensions and Considerations

Ceramic Capacitors
(including 0603, 0402, 0201 and ceramic arrays)

Tantalum Capacitors
(including low profile and large case (X & E) sizes and R case sizes)

Aluminum Capacitors
(including D, V, & X case sizes)

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The Institute for Interconnnecting and Packaging Electronic Circuits (IPC) has released IPC-SM-782, revision A. Many hours went into this revision. The committee that developed this document is very large and represents the leaders in many areas of the surface mount industry. The results are excellent, and we recommend you buy a copy. (The reference section of this bulletin lists the address and phone number for IPC.) This KEMET Bulletin is meant to supplement IPC 782A with focus on ceramic, tantalum and aluminum capacitors. KEMET Surface Mount Aluminum Capacitors are offered in some of the same case sizes as KEMET Surface Mount Tantalum Capacitors. See KEMET catalogs for availability.

The objectives of this KEMET Bulletin are:

- To introduce and summarize the methodology used in IPC 782A.
- To detail the land patterns for wave solder and reflow soldering using the methodology of IPC 782A for ceramic, tantalum and aluminum capacitors.
- To extend the methodology, and detail land dimensions for ceramic, tantalum and aluminum capacitor sizes not included in IPC 782A.
- To detail land patterns for capacitor arrays.
- To note some errors in IPC 782 and provide corrections.
- To show the impact of these corrections.
- To compare the new land patterns (IPC 782A methodology) to those previously presented in KEMET Engineering Bulletin F2100C.
- To discuss special care needed for small chips, such as 0603, 0402, 0201 and for capacitor arrays.
- To begin discussion of pads for 0201 size ceramic capacitors.

The discussion of this Bulletin is certainly in the spirit of IPC 782A. IPC 782A presents the equations and methodologies. Having said that, both the IPC and KEMET remind the user that they are responsible for additional modifications as needed that may result in a higher level of robustness.

THE BASICS: CALCULATIONS AND TOLERANCES

Introduction:

IPC 782A is a very thorough document. We suggest you review the total document, as it has much to offer. The discussions on grids, tolerances, dimension techniques and other aspects are very thorough and helpful in understanding the results. To jump directly to the land patterns and use them blindly is selling the total process short. The IPC also provides an excellent series of seminars to help you through the process.

We present the following synopsis as a baseline understanding. Figure 1 details the dimension letter callouts for pad design. Figure 2 details the equations for calculation of the pad dimensions and critical tolerances.

Calculations:

Calculation of three pad dimensions are needed. These are the width (X) of the pad, the overall length (Z) of the pad set, and the separation (G) between pads. The balance of the dimensions, including the length of the individual pad (Y), are calculated for reference. The equation that determines the spacing between the pads (G) uses the spacing between the part terminations (S_{max}), the minimum solder joint desired at the heel or inside joint (J_H), and the tolerances at the heel fillet (T_H). The equation that determines the overall length of the pads (Z) uses the minimum length of the component (L_{min}), the minimum solder joint desired (J_T)(this is the one you normally see), and the tolerances at the toe fillet (T_T). The equation that determines the width of the pads (X) uses the minimum width (W_{min}) of the termination, the minimum side solder fillet desired (J_S), and the tolerances at the width or side of the termination (T_S).

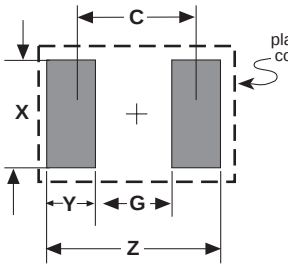
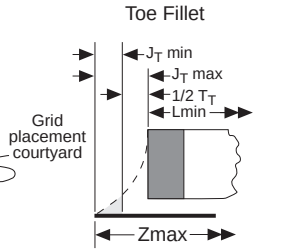
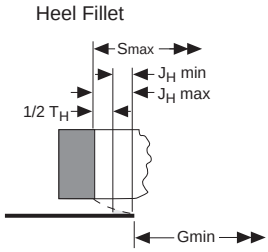


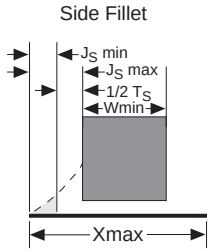
Figure 1.



Zmax = Lmin + $2J_T$min + T_T
Where:
$J_T$min = Minimum toe fillet
T_T = Combined tolerances at toe fillet



Gmin = Smax - $2J_H$min - T_H
Where:
$J_H$min = Minimum heel fillet
T_H = Combined tolerances at heel fillet



Xmax = Wmin + $2J_S$min + T_S
Where:
$J_S$min = Minimum side fillet
T_S = Combined tolerances at side fillet

Figure 2.

The IPC calculation for combination of tolerances always uses the “square root of the sum of the squares” method. This is a common engineering practice used when the tolerances vary independent of each other. Calculation of the tolerances about the toe of the part (T_T) incorporates the tolerance variation of the length of the part (C_L), the tolerance variation of the circuit board artwork and location of tooling holes (F), and the tolerance variations of the placement (P). IPC 782A makes assumptions for F = 0.2 mm and P = 0.2 mm. The document also suggests that these should be modified as appropriate by the experience of the user. Calculations of the tolerance variation of the part are in the dimensional table for each (C_L, C_W, and C_S). The subscripts of “C” refer to the dimension letter callout of the part (L, W, or S). Calculations of total tolerances use the “square root of the sum of the squares” method. For instance, if C_L = 0.2 mm, then $T_T = (0.2^2 + 0.2^2 + 0.2^2)^{0.5} = 0.35$. Other combined tolerances use the same calculation method. For T_S the dimensional tolerances of C_W are used, and for T_H the dimensional tolerances of C_S are used.

The calculation of S, the spacing between the inside edges of the terminations, is im-portant. The part manufacturers have not usually considered this dimension critical. In many cases it is not specified, and must be calculated with the use of termination and length dimensions. The standard for tantalum chip capacitors (EIA 535) specifies a min-imum S for all case sizes. The standard for ceramic chip capacitors (EIA 198) specifies a minimum S for the smallest case variations. This number is key in the calculation of G, one of the main pad dimension calculations. IPC 782A (paragraph 3.3.1) has determined that the worst-case calculation of S_{max} would not be representative of the true variations. Calculation of S_{max} also employs the “square root of the sum of the squares” method. The tolerances of the length (C_L) and the tolerance of the termination are used.

$S_{max} = S_{min} + (C_L^2 + \{T_{max} - T_{min}\}^2)^{0.5}$
$S_{min} = L_{min} - 2*T_{max}$, unless otherwise specified in the part standard.

PART DIMENSIONS

Figures 3 and 4 and Tables 1 and 2 detail the dimensions for ceramic and tantalum chip capacitors. The dimensions shown are those of standards EIA 198 for ceramic chips and EIA 535 for tantalum chips. These are also KEMET standard dimensions. When the dimensions differ from those in IPC 782, the table shows a footnote giving some comment or explanation. These tables also detail additional part sizes. These additional part sizes are denoted by an asterisk (*) next to the size callout.

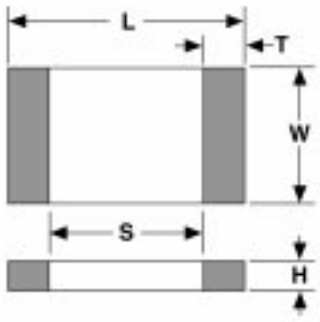


Figure 3.

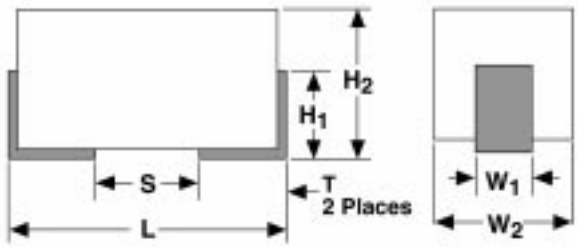


Figure 4.

Table 1 - Part Dimensions per EIA 198 Revision E - Ceramic Chip Capacitors

	Dimensions - mm									Calculations				
Dimension	**L**	**Lmin**	**Lmax**	**W**	**Wmin**	**Wmax**	**T**	**Tmin**	**Tmax**	**Smin**	**Smax**	**CL**	**CW**	**CS**
0201	0.60	0.57	0.63	0.30	0.27	0.33	0.15	0.10	0.20	0.20	0.35	0.06	0.06	0.15
0402	1.00	0.90	1.10	0.50	0.40	0.60	0.25	0.10	0.40	0.30	0.77	0.20	0.20	0.47
0603	1.60	1.45	1.75	0.80	0.65	0.95	0.35	0.20	0.50	0.70	1.22	0.30	0.30	0.52
0805	2.00	1.80	2.20	1.25	1.05	1.45	0.50	0.25	0.75	0.75	1.56	0.40	0.40	0.81
1206	3.20	3.00	3.40	1.60	1.40	1.80	0.50	0.25	0.75	1.50	2.31	0.40	0.40	0.81
1210	3.20	3.00	3.40	2.50	2.30	2.70	0.50	0.25	0.75	1.50	2.31	0.40	0.40	0.81
1812	4.50	4.20	4.80	3.20	2.90	3.50	0.60	0.25	0.95	2.30	3.46	0.60	0.60	1.16
1825	4.50	4.20	4.80	6.40	6.00	6.80	0.60	0.25	0.95	2.30	3.46	0.60	0.80	1.16
2220*	5.60	5.20	6.00	5.00	4.60	5.40	0.60	0.25	0.95	3.30	4.57	0.80	0.80	1.27
2225*	5.60	5.20	6.00	6.30	5.90	6.70	0.60	0.25	0.95	3.30	4.57	0.80	0.80	1.27
Footnotes									(1)	(2)	(3)			(4)

Calculation Formula
CL = Lmax - Lmin
CW = Wmax -Wmin
CS = Tmax - Tmin
Smin = Lmin - 2Tmax
Smax = Smin + $(CL^2 + 2CT^2)^{.5}$

Footnotes
1. Tmax for 0402 is 0.3 max in IPC 782A. This impacts the calculation of Smax. See Footnote 3.
2. Smin is specified in EIA 198D for 0402, 0603 and 0805 sizes. These are the values listed in this table.
3. Smax for 0402 is impacted by the difference in Tmax. See Footnote 1.
4. CS dimensions are different in the IPC 782 table. A spreadsheet error likely exists.

Table 2 - Part Dimensions per EIA 535 Issue 2 - Tantalum Chip and Aluminum Capacitors

		Dimensions - mm									Calculations				
Case Size	**Dimension**	**L**	**Lmin**	**Lmax**	**W1**	**W1min**	**W1max**	**T**	**Tmin**	**Tmax**	**Smin**	**Smax**	**CL**	**CW1**	**CS**
R*	2012	2.00	1.80	2.20	1.20	1.10	1.30	0.50	0.20	0.80	0.30	1.24	0.40	0.20	0.94
S*	3216L	3.20	3.00	3.40	1.20	1.10	1.30	0.80	0.50	1.10	0.80	1.74	0.40	0.20	0.94
A	3216	3.20	3.00	3.40	1.20	1.10	1.30	0.80	0.50	1.10	0.80	1.74	0.40	0.20	0.94
T*	3528L	3.50	3.30	3.70	2.20	2.10	2.30	0.80	0.50	1.10	1.10	2.04	0.40	0.20	0.94
B	3528	3.50	3.30	3.70	2.20	2.10	2.30	0.80	0.50	1.10	1.10	2.04	0.40	0.20	0.94
C	6032	6.00	5.70	6.30	2.20	2.10	2.30	1.30	1.00	1.60	2.50	3.54	0.60	0.20	1.04
U	6032L	6.00	5.70	6.30	2.20	2.10	2.30	1.30	1.00	1.60	2.50	3.54	0.60	0.20	1.04
D	7343	7.30	7.00	7.60	2.40	2.30	2.50	1.30	1.00	1.60	3.80	4.84	0.60	0.20	1.04
V	7343L	7.30	7.00	7.60	2.40	2.30	2.50	1.30	1.00	1.60	3.80	4.84	0.60	0.20	1.04
X*	7343H	7.30	7.00	7.60	2.40	2.30	2.50	1.30	1.00	1.60	3.80	4.84	0.60	0.20	1.04
E	7260	7.30	7.00	7.60	4.10	4.00	4.20	1.30	1.00	1.60	3.80	4.84	0.60	0.20	1.04
	Footnotes				(5)	(5)	(5)							(6)	

Calculation Formula
CL = Lmax - Lmin
CW1 = W1max -W1min
CS = Tmax - Tmin
Smin = Smin from EIA
Smax = Smin + $(CL^2 + 2CT^2)^{.5}$

Footnotes
5. The nominal and tolerances for W1 are as specified in EIA 535.
   IPC 782 tables list tighter tolerances.
6. The calculated CW1 here represents the tolerance of the termination.
   The CW in IPC 782A represents the tolerance of the body, it should
   be of the termination.

Figure 5 and Table 1.1 detail the dimensions for ceramic capacitor arrays. These are standard dimensions as established by the EIA P2.1 committee. Part dimensions L, W, H, and S are as specified. Part tolerance variation C_L, C_S, and C_W are calculated from dimensions; for example, $C_L = L_{max} - L_{min}$.

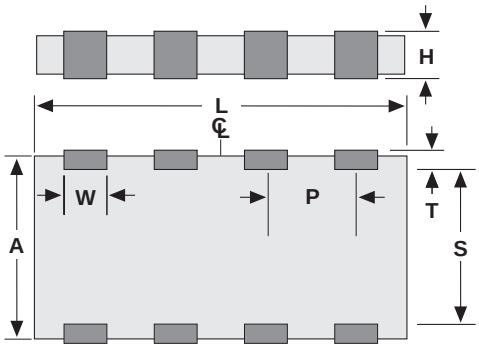


Figure 5. Capacitor Array

Table 1.1 - Part Dimensions per EIA 198 Revision D - Ceramic Chip Capacitor Arrays

Dimensions - mm													Calculations					
Dimension 3216	**L** 3.20	**Lmin** 3.00	**Lmax** 3.40	**W** 0.40	**Wmin** 0.30	**Wmax** 0.50	**T** 0.30	**Tmin** 0.10	**Tmax** 0.50	**Amax** 1.80	**Amin** 1.40	**Smin** 0.40	**Smax** 1.09	**CL** 0.40	**CW** 0.20	**CS** 0.69	**P** 0.80

Calculation Formula
CL = Amax - Amin
CW = Wmax -Wmin
CS = Smax - Smin
Smin = Amin - 2Tmax
Smax = Smin + $(CL^2 + 2CT^2)^{.5}$

Corrections:

A comparison of the dimensions for ceramic and tantalum capacitors in the published copy of IPC 782A with the part standards indicates some inconsistencies. In addition, some publishing errors were present for the calculated values. For use in this Bulletin, notations of the inconsistencies are in the footnotes of the table and corrected as appropriate. Further discussion of the effect on the pad dimensions is in the Appendix.

There is good news, however; IPC has a wonderful net site, “http:///www.ipc.org.” In this site you can find the IPC-SM-782 calculator. Many of these errors have been corrected. After you’ve enjoyed the KEMET Bulletin, you might want to visit this site.

OTHER FACTORS AND CONSTANTS

Other factors in the equations include:

- F - the accuracy of circuit board elements, such as tooling hole location, artwork, etc.
- P - the accuracy of placement
- The minimum desired solder joints for toe, heel, and side locations.
  J_T - the size of the desired fillet at the outside solder joint.
  J_H - the size of the desired fillet at the heel or inside solder joint.
  J_S - the size of the desired fillet at the side of the termination.

IPC 782A Table 3.4 details these assumptions. These all appear appropriate; however, it is again recommended that the user apply his own experience to the numbers and adjust them accordingly. The one modification that we recommend is for the small ceramic chip sizes (0201, 0402 and 0603). The use of these small chips increases the likelihood of “tombstoning” if the parts are not placed on the pads accurately. Thus, we believe it is important that both the circuit board and placement processes have greater accuracy than for normal production. We suggest modifying F

and P from 0.2 to 0.1mm for 0603 and 0402 and to 0.05mm for 0201. This has been done in the pad design calculations. Table 3 details the constants.

Table 3 - Constants

Placement Accuracies	P	0.20
Ceramic (0402 & 0603) & Arrays		0.10
Ceramic (0201)		0.05
Circuit Board Accuracies	F	0.20
Ceramic (0402 & 0603) & Arrays		0.10
Ceramic (0201)		0.05
Solder Toe Fillet	JT min	
Ceramic		0.50
Tantalum		0.60
Solder Heel Fillet	JH min	0.00
Arrays		0.00
Solder Side Fillet	JS min	0.05
Arrays		-0.01

PAD DESIGNS: CERAMIC, TANTALUM AND ALUMINUM CAPACITORS

Tables 4 and 5 detail the pad designs for ceramic, tantalum and aluminum chip capacitors. Calculations for the pads use the methodology, formula, and constants presented in IPC 782A. The part dimensions also are as noted in Tables 1 and 2, modified only as mentioned above.

Again, when pad dimensions are not consistent with those of IPC 782A, the table includes a footnote. The Appendix further discusses the effects of these inconsistencies.

Table 4 - Land Pattern Dimensions - Ceramic Chip Capacitors - mm**

	Reflow Solder					Wave Solder				
Dimension	**Z**	**G**	**X**	**Y(ref)**	**C(ref)**	**Z**	**G**	**X**	**Y(ref)**	**Smin**
0201	1.66	0.18	0.46	0.74	0.92	Not Recommended				
0402	2.14	0.28	0.74	0.93	1.21					
0603	2.78	0.68	1.08	1.05	1.73	3.18	0.68	0.80	1.25	1.93
0805	3.30	0.70	1.60	1.30	2.00	3.70	0.70	1.10	1.50	2.20
1206	4.50	1.50	2.00	1.50	3.00	4.90	1.50	1.40	1.70	3.20
1210	4.50	1.50	2.90	1.50	3.00	4.90	1.50	2.00	1.70	3.20
1812	5.90	2.30	3.70	1.80	4.10	6.30	2.30	2.60	2.00	4.30
1825	5.90	2.30	6.90	1.80	4.10	Not Recommended				
2220*	7.00	3.30	5.50	1.85	5.15					
2225*	7.00	3.30	6.80	1.85	5.15					
Footnotes		(A)	(B)	(C)	(C)					

Calculation Formula
Z = Lmin + 2Jt + Tt
G = Smax - 2Jh -Th
X = Wmin + 2Js + Ts
Tt, Th, Ts = Combined tolerances

Footnotes
A. G is different from G in IPC 782A tables because of Smax impact mentioned in Footnote 3.
B. X is different for case sizes of 1210 and greater due to an apparent spread sheet error in the X column of IPC 782A tables.
C. Y(ref) = (Z - G)/2, the difference in G being reflected in Y(ref). C(ref) = Z - Y(ref), with the same differences.
** The tables of IPC 782A round the primary dimensions (Z,G, & X) to make them compatible with grid layouts in CAD design. These dimensions have also been rounded to the nearest 0.1mm. Because dimensions for 0201,0402 and 0603 are critical to prevent "tombstoning," that have not been rounded.
*** Wave solder processing is not recommended for chips greater than 1210 (See KEMET application bulletin for additional information. Some attempt the process for 1812. This should be done with extreme caution. These pads are presented for that occasion.

Table 5 - Land Pattern Dimensions - Tantalum and Aluminum Chip Capacitors - mm**

		Reflow Solder					Wave Solder				
Case Size	**Dimension**	**Z**	**G**	**X**	**Y(ref)**	**C(ref)**	**Z**	**G**	**X**	**Y(ref)**	**C(ref)**
S*	3216L	4.70	0.80	1.50	1.95	2.75	5.10	0.80	1.10	2.15	2.95
A	3216	4.70	0.80	1.50	1.95	2.75	5.10	0.80	1.10	2.15	2.95
T*	3528L	5.00	1.10	2.50	1.95	3.05	5.40	1.10	1.80	2.15	3.25
B	3528	5.00	1.10	2.50	1.95	3.05	5.40	1.10	1.80	2.15	3.25
C	6032	7.60	2.50	2.50	2.55	5.05	8.00	2.50	1.80	2.75	5.25
U	6032L	7.60	2.50	2.50	2.55	5.05	8.00	2.50	1.80	2.75	5.25
D	7343***	8.90	3.80	2.70	2.55	6.35	9.70	3.80	2.70	2.95	6.75
V	7343L	8.90	3.80	2.70	2.55	6.35	9.30	3.80	1.90	2.75	6.55
X*	7343H***	8.90	3.80	2.70	2.55	6.35	9.70	3.80	2.70	2.95	6.75
E*	7360***	8.90	3.80	4.40	2.55	6.35	9.70	3.80	4.40	2.95	6.75
	Footnotes			(D)							

Calculation Formula
Z = Lmin + 2Jt + Tt
G = Smax - 2Jh -Th
X = Wmin + 2Js + Ts
Tt, Th, Ts = Combined tolerances

Footnotes
D. X is significantlly different from that of the tables of IPC 782A. The reason lies with the error made in CW (see footnote 6), and in the error made in dimension W1 (see footnote 5).
** The tables of IPC 782A round the primary dimensions (Z, G & X) to make them compatible wwith grid layouts in CAD design.
*** In general, tantalum capacitors can be wave soldered. The larger case sizes are more difficult and it is not recommended that these be waved soldered. Pad designs are presented for the adventurous.

Process Considerations:

Reflow Solder and Wave Solder Pad Designs

The general desire of circuit board layout designers would be to have one set of pad designs regardless of the soldering process. However, capacitor manufacturers believe it is important to modify the pad design for wave solder processing. Subsection 8.1 of IPC 782A includes a supporting note as follows. “Note: If a more robust pattern is desired for wave soldering devices larger than 1608 (0603), add 0.2mm to the “Y” dimension, and consider reducing the “X” dimension by 30%. Add a “W” suffix to the RLP number, e.g. 103W."

Ceramic chip capacitors are susceptible to mechanical breakage if the circuit board is flexed after soldering (reference 5). One of the ways to minimize this effect is to minimize the volume of the solder fillet. To accomplish this, most manufacturers recommend a re-duced width mounting pad when the part is to be wave soldered.

Wave Soldering Tantalum Capacitors

Tantalum chip capacitors are capable of wave solder processing as well as reflow solder processing. The termination of the tantalum chip does not go up the entire side of the body. One of the concerns in wave solder processing is shadowing, which is the wave not coming in contact with the termination. To prevent skipping, the solder must have an opportunity to wet to the solder pad and then the termination. To accomplish this, the pad is normally extended in length. KEMET does not recommend wave soldering the larger case tantalum capacitors. Pad designs, however, are included for the adventurous. Calculations of wave solder pad designs for tantalum chip capacitors use the IPC 782A criterion mentioned above. For the large case (D,X,E) tantalum we have extended the pad length by 0.4mm and kept the pad width at the full calculated dimension. We believe this will result in a more robust pad.

Reflow Only (?) for Some Ceramic Capacitors

Some ceramic chip sizes are not recommended for wave soldering. The small 0201, 0402 and capacitor arrays should not be wave soldered as the solder will likely bridge the termination. The 0603 can be wave soldered if the glue dots can be accurately placed, and if the wave is controlled to prevent bridging. Even for 0603, reflow soldering should be the first choice. Ceramic capacitors larger than 1210 should not be wave soldered. Thermal robustness issues are involved, as well as board flex problems. Some existing design layouts have required wave soldering of the 1812 size. These should be done with extreme caution. See KEMET Application Bulletin (reference 4) for more information. The pads for wave soldering 1812 size capacitors are included in the table for that rare, special occasion. Ceramic capacitors are being manufactured today with many, very thin, dielectric layers. While manufacturers state that wave soldering is OK, the stresses are high. Reflow soldering should be the first choice for ceramic capacitors with voltage ratings of 16 and below.

Special Considerations for Small Chips

The very small 0402 and 0603 chip sizes require special consideration. The pad designs presented in this Bulletin use the same formula and methodology as all the other chip sizes. The two exceptions to this are the use of a tighter tolerance for P and F constants (0.1mm in place of 0.2mm, and the elimination of mathematical rounding normally used to bring the dimensions on a CAD grid). These considerations are unique from the published IPC 782A document. The use of 0402 and 0603 size chips is a more precise application than the use of larger chips. These chips are much more susceptible to off-pad errors, movement during solder processes, and the dreaded “tombstoning.” In

addition, repair of missing parts or solder joints is much more difficult than for larger size chips. The repair of anything regarding 0402s is almost impossible. For this reason, the user should experiment with the pad designs.

Special Considerations for 0201

Let's start by pointing out that at the time of this writing there is little industry experience with placing these extremely small chips. The information presented in this Bulletin is to be considered "a place to start". The formula and methodology are the same as for all other designs presented. First calculations using the same exceptions as those for 0402 and 0603 above indicated little space between pads ("G" dimension). F and P constrants (Table 3) were further reduced to ±0.05 mm, placing real emphasis on accuracy of design and placement. The designer should also pay close attention to the next paragraph.

Special Considerations for Tombstoning

The “mathematics” behind tombstoning is shown in Figure 6. Tombstoning results when one of the terminations wets prior to the other and the counteracting forces are insufficient to overcome the force of wetting. The counteracting forces include the

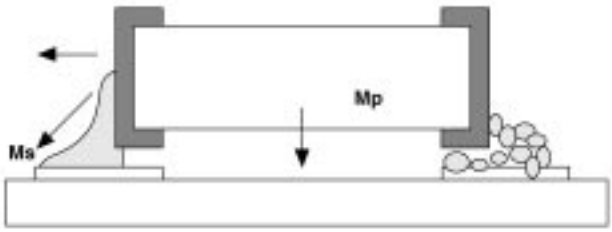


Figure 6.

$Ms = Fo (\cos \varnothing) t$
$Mp = g (L/2)$

Fo = Solder adhesive force = 500 dynes
$\varnothing$ = Solder fillet angle = 45°

Capacitors	Solder Fo (gf)	Moment s Fo*cos 45*t (*10-3)	Moment p g*1/2 (*10-3)	Tombstone Ratio (MsMp)	Weight (mg)
3216 (1206)	0.08	5.09	1.92	2.7	12.00
2012 (0805)	0.0625	3.98	0.65	6.1	6.50
1608 (0603)	0.04	2.26	0.28	8.1	3.50
1005 (0402)	0.025	0.88	0.07	12.6	1.40

weight of the part and the adhesion of the bottom of the termination to the solder paste. The pad design can be modified to enhance the counteracting force of adhesion. The goal is to design the pad to get the maximum area of the termination on the pad, without greatly increasing the end termination wetting force. To minimize tombstoning for 0201, 0402 and 0603 pads, two changes are recommended. The first is to round off all corners of the pads (Figure 7). This is a technique employed for pads of fine pitch ICs (see IPC 782A). The amount of rounding is process dependent. However, a good

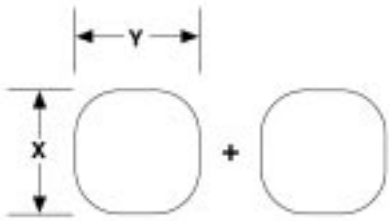


Figure 7.

starting point would be 0.25mm radius. The second recommendation is to minimize the solder paste by using a stencil opening less than the pad area. This is another technique commonly employed when soldering “fine pitch” integrated circuits. It is easily argued that 0201, 0402 and possibly 0603s have pads very similar to fine pitch parts. The stencil opening is the same in the “Y” direction, and is reduced by 1/3 in the “X” direction, and centered on the pad. Of course, the best pad designs will not prevent tombstoning if the solder process is not in control. The best solder process would result in the solder paste reflowing simultaneously in both pads.

PADS FOR CAPACITOR ARRAYS

Capacitor arrays have recently been introduced. These provide the user with some interesting options. A capacitor array consists of multiple capacitor elements in a single multilayer chip. The first introduction is the 1632 chip with 4 capacitors each. See Figure 5 and Table 1.1 for dimensions.

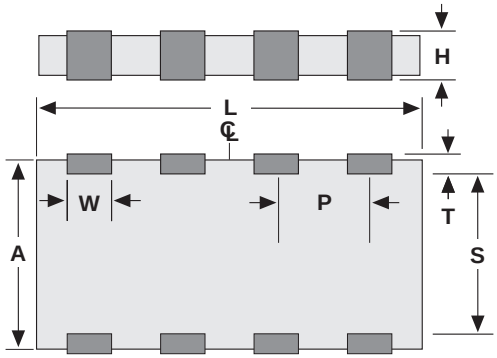


Figure 5. Capacitor Array

Table 1.1 - Part Dimensions per EIA 198 Revision D - Ceramic Chip Capacitor Arrays

Dimensions - mm												Calculations					
Dimension 3216	**L** 3.20	**Lmin** 3.00	**Lmax** 3.40	**W** 0.40	**Wmin** 0.30	**Wmax** 0.50	**T** 0.30	**Tmin** 0.10	**Tmax** 0.50	**Amax** 1.80	**Amin** 1.40	**Smin** 0.40	**Smax** 1.09	**CL** 0.40	**CW** 0.20	**CS** 0.69	**P** 0.80

Calculation Formula
CL = Amax - Amin
CW = Wmax -Wmin
CS = Smax - Smin
Smin = Amin - 2Tmax
Smax = Smin + $(CL^2 + 2CT^2)^{.5}$

The pad designs for reflow soldering of capacitor arrays presented here are calculated in two steps. The first step is to calculate the pads for a single element using the formula of IPC 782A. The calculations of C_L, C_W, and C are shown in Table 1.1. After the pad dimensions are calculated, multiple sets of these are placed on the same centerlines of pitch (P) as the terminations of the parts. The pad dimensions are shown in Table 4.1 and Figure 8.

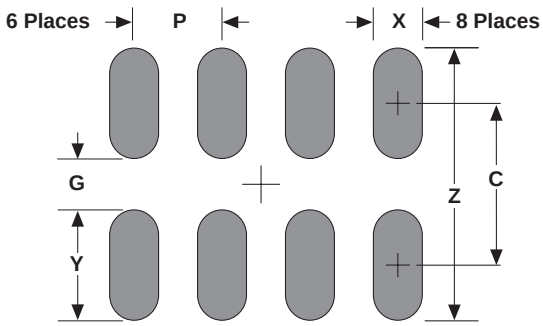


Figure 8. Pad Design - Ceramic Capacitor Arrays

Table 4.1 - Land Pattern Dimensions - Ceramic Chip Capacitor Arrays - mm

	Reflow Solder					
Dimension 3216	**Z** 2.80	**G** 0.40	**X** 0.52	**Y(ref)** 1.20	**C(ref)** 1.60	**P** 0.80

Calculation Formula
Z = Lmin + 2Jt + Tt
G = Smax - 2Jh -Th
X = Wmin + 2Js + Ts
Tt, Th, Ts = Combined tolerances

The capacitor array is very nearly a “fine pitch” product. Figure 8.1 shows an inset with one set of pads and the resulting space between pads. In keeping with fine pitch technology, we recommend rounding of the pads. In addition, we suggest that the solder stencil opening be reduced by approximately 20% (See Figure 8.2). It is thought that both of these will aid in the self-alignment during relow solder. When referencing arrays to fiducials for pick and place calculations, the center of the chip and pad design should be used. This will place the terminations nearest to the pads.

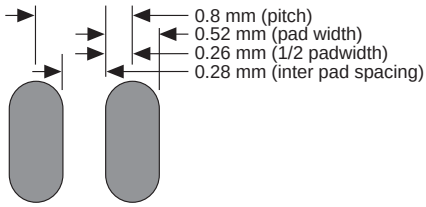


Figure 8.1 1632 Dimensions for Reference

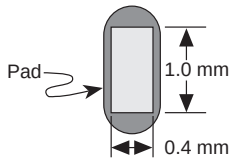


Figure 8.2 1632 Suggested Solder Stencil Openings

APPENDIX
PAD DESIGN COMPARISONS

This Bulletin Compared to Published IPC 782A

The publication of IPC 782A has been a great boon for standardization. The IPC pad designs are available on disc, and in Computer Aided Design (CAD) format for the designer. Many of the CAD software packages come complete with standard pad designs, and we can expect them to be those of IPC 782A.

Most board design work is being done with CAD, and many are being designed at con-tracted design houses. In addition, more and more design and board layout work is be-coming the responsibility and forte of sub-contract assembly companies. So it is not difficult to see that most pads will soon be those of the standard IPC 782A. This is as it should be, and we support this direction.

The IPC 782A group has done a very thorough job in putting together this standard. The corrections needed are small, and as mentioned before, many have already been corrected on the IPC internet site.

Until the IPC 782A standard can be corrected, some boards designed to the published criteria may have pads different from those shown in Tables 4 and 5. Tables 6 and 7 present these differences. These tables show the pad dimensions of Table 4 and 5, the published IPC 782A pad dimensions, and the delta’s between them.

Table 6 - Comparison Table 4 to Published IPC 782A Designs - Ceramic Chip Capacitors - mm

	Table 4 Calculation					IPC 782A Published					Table 4 - Published =				
Dimension	Z	G	X	Y(ref)	C(ref)	Z	G	X	Y(ref)	C(ref)	Z	G	X	Y(ref)	C(ref)
0402	2.14	0.28	0.74	0.93	1.21	2.20	0.40	0.80	0.90	1.30	-0.06	-0.12	-0.06	0.90	1.30
0603	2.78	0.68	1.08	1.05	1.73	2.80	0.60	1.20	1.10	1.70	-0.02	0.08	-0.12	1.10	1.70
0805	3.30	0.70	1.60	1.30	2.00	3.20	0.60	1.60	1.30	1.90	0.10	0.10	0.00	1.30	1.90
1206	4.50	1.50	2.00	1.50	3.00	4.40	1.20	2.00	1.60	2.80	0.10	0.30	0.00	1.60	2.80
1210	4.50	1.50	2.90	1.50	3.00	4.40	1.20	1.60	1.60	2.80	0.10	0.30	1.30	1.60	2.80
1812	5.90	2.30	3.70	1.80	4.10	5.80	2.00	1.80	1.90	3.90	0.10	0.30	1.90	1.90	3.90
1825	5.90	2.30	6.90	1.80	4.10	5.80	2.00	4.40	1.90	3.90	0.10	0.30	2.50	1.90	3.90
Footnotes												(E)	(F)		

Footnotes
E. For sizes larger than 0805, the IPC published pads have less separation distance, due to the impact of Cs detailed in Footnote 4 of Table 1.
F. For sizes 1210 and larger, the IPC published pads are significantly narrower, due to the impact of the error detailed in Footnote B of Table 4.

Table 7 - Comparison Table 5 to Published IPC 782A Designs - Tantalum Chip Capacitors - mm – Reflow Solder

		Table 5 Calculation					IPC 782A Published					Table 5 - Published =				
Case Size	Dimension	Z	G	X	Y(ref)	C(ref)	Z	G	X	Y(ref)	C(ref)	Z	G	X	Y(ref)	C(ref)
A	3216	4.70	0.80	1.50	1.95	2.75	4.80	0.80	1.20	2.00	2.80	-0.10	0.00	0.30	-0.05	-0.05
B	3528	5.00	1.10	2.50	1.95	3.05	5.00	1.00	2.20	2.00	3.00	0.00	0.10	0.30	-0.05	0.05
C	6032	7.60	2.50	2.50	2.55	5.05	7.60	2.40	2.20	2.60	5.00	0.00	0.10	0.30	-0.05	0.05
D	7343	8.90	3.80	2.70	2.55	6.35	9.00	3.80	2.40	2.60	6.40	-0.10	0.00	0.30	-0.05	-0.05
	Footnotes													G		

Footnotes
G. The published pads of IPC are significantly narrower, due to the error in using W instead of W1, detailed in Footnote D of Table 5.

Table 6 (ceramic chip capacitors) indicates that the main differences will appear in two areas.

The published IPC 782A pads (for chips larger than 0805) will have narrower separation (G) between pads than those in Table 4. This results from the errors made in calculation of C_S mentioned in footnote 4 of Table 1. The magnitude of this is small.

The published IPC 782A pads for 1210 and larger chips will have significantly narrower pads (X) than those of Table 4. This results from the calculation error detailed in footnote B of Table 4. This will result in pads as small as one half the correct width. As long as there are no “very near traces” or components, the solder joint will be sufficient. The parts may move more than with the correct pads.

Table 7 (tantalum chip capacitors) indicates that the differences appear in one area. The width of the IPC 782A pads will be less (by .3mm) than that of those in Table 5. This occurs because of the error in using the body width dimension (W) instead of the termination width (W1) in calculation C_W (footnote D in Table 5.). This reduction in width is small, and should have limited impact.

All other minor errors noted in the footnotes of Table 1, 2, 4, and 5 have had little impact on the pad designs, either because of the larger impact of other errors, or because of the minor nature of the error.

This Bulletin Compared to Previous KEMET Engineering Bulletins

Those of you who have used pad designs from previous revisions of this Bulletin may be interested in comparing the new IPC 782A pads with previous designs.

In general, the pads described in the previous bulletin are spaced further apart (with Z and G being larger), and they are wider (greater X) than those designed with the IPC 782A methodology. The reasons lie primarily with the design philosophy. The philosophy of the previous KEMET Bulletin was to present a pad that would result in 100% of the termination being on the pad nearly 100% of the time. For this reason, the maximum tolerances were used and added together. The philosophy of the IPC 782A methodology is to design pads using the “square root of the sum of the squares” of tolerances as they vary independently. This reduces the additive effect of the tolerances. In addition, the methods used in the previous KEMET Bulletin targeted the desired solder fillet length (E) to the approximate termination height. The solder fillet was 0.7mm for ceramics and 1.0mm for tantalum. This resulted in a slightly larger solder fillet.

Tables 8 and 9 repeat the part dimensions and resulting pads. A comparison of these and the pad designs of Table 4 and 5 is presented in Tables 10 and 11 of this Appendix. Discussions of the differences are also included in the footnotes of these tables. Of course, the newly added parts are not included.

Table 8 - Part Dimensions & Pad Dimensions (Previous Bulletin F-2100C) - Ceramic Chip Capacitors

Part Dimensions - mm										Reflow Pad Designs			
										Dnom	Cnom	Anom	Bnom
Dimension	**L**	**Lmin**	**Lmax**	**W**	**Wmin**	**Wmax**	**T**	**Tmin**	**Tmax**	**Z**	**G**	**X**	**Y(ref)**
0603	1.60	1.45	1.75	0.80	0.65	0.95	0.35	0.20	0.50	3.25	0.80	1.15	1.23
0805	2.00	1.80	2.20	1.25	1.05	1.45	0.43	0.25	0.68	3.85	0.89	1.95	1.48
1206	3.20	3.00	3.40	1.60	1.40	1.80	0.64	0.25	1.02	5.05	1.67	2.30	1.69
1210	3.20	3.00	3.40	2.50	2.30	2.70	0.64	0.25	1.02	5.05	0.67	3.20	1.69
1812	4.50	4.20	4.80	3.20	3.00	3.50	0.64	0.25	1.02	6.45	2.97	4.00	1.74
1825	4.50	4.20	4.80	6.40	6.00	6.70	0.64	0.25	1.02	6.45	2.97	7.20	1.74
2225*	5.60	5.20	6.00	6.30	5.90	6.70	0.64	0.25	1.02	7.65	4.07	7.20	1.79
Footnotes									(7)				

Footnotes
7. The main differences in dimensions are the bandwidth dimensions T.
These dimensions were typical of KEMET, the dimensions in Table 1 are the industry standards.

Table 9 - Part Dimensions & Pad Dimensions (Previous Bulletin F-2100C) - Tantalum Chip Capacitors

Part Dimensions - mm												Reflow Pad Designs			
							Fmax	K	Kmin	Kmax		Dnom	Cnom	Anom	Bnom
Case Size	**Dimension**	**L**	**Lmin**	**Lmax**	**W1**	**W1min**	**W1max**	**T**	**Tmin**	**Tmax**	**Snom**	**Z**	**G**	**X**	**Y(ref)**
A	3216	3.20	3.00	3.40	1.20	1.10	1.30	0.90	0.70	1.10	0.80	5.65	1.35	1.80	2.15
B	3528	3.50	3.30	3.70	2.20	2.10	2.30	1.10	0.70	1.30	0.80	5.95	1.65	2.80	2.15
C	6032	6.00	5.70	6.30	2.20	2.10	2.30	1.40	1.20	1.60	1.30	8.55	3.15	2.80	2.70
D	7343	7.30	7.00	7.60	2.40	2.30	2.50	1.50	1.30	1.70	1.30	9.85	4.45	3.00	2.70
E	7260	7.30	7.00	7.60	4.10	4.00	4.20	2.10	1.90	2.30	1.30	9.85	4.45	4.70	2.70
X	7343	7.30	7.00	7.60	2.40	2.30	2.50	1.50	1.30	1.70	1.30	9.85	4.45	3.00	2.70
	Footnotes									(8)					

Footnotes
8. The main differences in dimensions are the termination height K.
These dimensions were typical of KEMET, the dimensions in Table 1 are the industry standards.

Table 10 - Comparison Table 4 to Previous Bulletin F-2100C - Ceramic Chip Capacitors - mm – Reflow Solder

Dimension	Table 4 Calculation				Previous Revisions (F-2100C)				Table 4 - Previous =			
IPC 782A Comparison	**Dnom**	**Cnom**	**Amin**	**Bnom**	**Dnom**	**Cnom**	**Amin**	**Bnom**				
Case Size	**Z**	**G**	**X**	**Y(ref)**	**Z**	**G**	**X**	**Y(ref)**	**Z-nom**	**G-nom**	**X-Amin**	**Y-Bnom**
0603	2.78	0.68	1.08	1.05	3.25	0.80	1.15	1.23	-0.47	-0.12	-0.07	-0.17
0805	3.30	0.70	1.60	1.30	3.85	0.89	1.95	1.48	-0.55	-0.19	-0.35	-0.18
1206	4.50	1.50	2.00	1.50	5.05	1.67	2.30	1.69	-0.55	-0.17	-0.30	-0.19
1210	4.50	1.50	2.90	1.50	5.05	1.67	3.20	1.69	-0.55	-0.17	-0.30	-0.19
1812	5.90	2.30	3.70	1.80	6.45	2.97	4.00	1.74	-0.55	-0.67	-0.30	-0.06
1825	5.90	2.30	6.90	1.80	6.45	2.97	7.20	1.74	-0.55	-0.67	-0.30	-0.06
2225*	7.00	3.30	6.80	1.85	7.65	4.07	7.20	1.79	-0.65	-0.77	-0.40	-0.06
Footnotes									(H)	(I)	(J)	

Footnotes
H. Dnom is larger than Z due to the selection of the size of the solder fillet Jt, and the use of the sum of all tolerances, opposed to the use of the square root of the sum of squares method.
I. Cnom is larger than G due to the difference in the termination (T) (see footnote 7 in Table *), and the use of the sum of all tolerances, opposed to the use of the square root of the sum of squares method.
J. Amin is larger than W due to the use of 2 times the placement and artwork tolerance (Z), and the use of the sum of all tolerances, opposed to the use of the square root of the sum of squares method.

Table 11 - Comparison Table 4 to Previous Bulletin F-2100C - Tantalum Chip Capacitors - mm – Reflow Solder

Dimension		Table 4 Calculation				Previous Revisions (F-2100C)				Table 5 - Previous =			
Case Size	**IPC 782A Comparison**	**Dnom**	**Cnom**	**Amin**	**Bnom**	**Dnom**	**Cnom**	**Amin**	**Bnom**				
		Z	**G**	**X**	**Y(ref)**	**Z**	**G**	**X**	**Y(ref)**	**Z-nom**	**G-nom**	**X-Amin**	**Y-Bnom**
A	3216	4.70	0.80	1.50	1.95	5.65	1.35	1.80	2.15	-0.95	-0.55	-0.30	-0.20
B	3528	5.00	1.10	2.50	1.95	5.95	1.65	2.80	2.15	-0.95	-0.55	-0.30	-0.20
C	6032	7.60	2.50	2.50	2.55	8.55	3.15	2.80	2.70	-0.95	-0.65	-0.30	-0.15
D	7343	8.90	3.80	2.70	2.55	9.85	4.45	3.00	2.70	-0.95	-0.65	-0.30	-0.15
	Footnotes									(K)	(L)	(M)	

Footnotes
K. Dnom is larger than Z due to the selection of the size of the solder fillet Jt, and the use of the sum of all tolerances, opposed to the use of the square root of the sum of squares method.
L. Cnom is larger than G due to the use of Maximum Separation of terminals (the tables of IPC 782 reduce this by use of square root of sum of squares), and the use of the sum of all tolerance, opposed to the use of the square root of the sum of squares method.
M. Amin is larger than W due to the use of 2 times the placement and artwork tolerances (Z), and the use of the sum of all tolerances, opposed to the use of the square root of the sum of squares method.

Another Approach for 100% Termination on the Pads

Tables 12 and 13 detail pad designs for those designs where the customer requires that 100% of the terminations be on the pads 100% of the time. These pad designs use the formula developed in previous KEMET Bulletins, along with the industry standard dimensions presented in Tables 1 and 2.

Table 12 - Land Pattern Dimensions - Ceramic Chip Capacitors - mm**
(KEMET Bulletin Formula, Standard Dimensions)

	Reflow Solder					Wave Solder				
Dimension	**Z**	**G**	**X**	**Y(ref)**	**C(ref)**	**Z**	**G**	**X**	**Y(ref)**	**Smin**
0201	1.73	0.20	0.53	0.77	0.97	Not Recommended				
0402	2.20	0.40	0.80	0.90	1.30					
0603	2.85	0.80	1.15	1.03	1.83	3.25	0.80	0.80	1.23	2.03
0805	3.90	0.90	1.70	1.50	2.40	4.30	0.90	1.20	1.70	2.60
1206	5.10	2.10	2.00	1.50	3.60	5.50	2.10	1.40	1.70	3.80
1210	5.10	2.10	2.90	1.50	3.60	5.50	2.10	2.00	1.70	3.80
1812	6.50	3.20	3.70	1.65	4.85	Not Recommended				
1825	6.50	3.20	7.00	1.65	4.85					
2220*	7.70	4.30	5.60	1.70	6.00					
2225*	7.70	4.30	6.90	1.70	6.00					
Footnotes										

Calculation Formula
Z = Lmax + 2Jt + z
G = L - 2T - z
X = Wmax + 2z
Yref = (Z - G)/2
Cref = Z - Yref
Jt = 0.7, (0.5 for 0201, 0402 & 0603)
z = 0.25

Calculation Formula
Z = Lmax + 2Jt + 2*0.2
G = L - 2T - z
X = (Wmax + 2z)0.7*
Yref = (Z - G)/2
Cref = Z - Yref
Jt = 0.7, (0.5 for 0402 & 0603)
z = 0.25

** The IPC 782A rounds the primary dimensions (Z,G, & X) to make them compatible with grid layouts in CAD design. These dimensions have also been rounded to the nearest 0.1mm. Because dimensions for 0603 and 0402 are critical to prevent "tombstoning," that have not been rounded.

Table 13 - Land Pattern Dimensions - Tantalum Chip Capacitors - mm**
(KEMET Bulletin Formula, Standard Dimensions)

		Reflow Solder					Wave Solder				
Case Size	**Dimension**	**Z**	**G**	**X**	**Y(ref)**	**C(ref)**	**Z**	**G**	**X**	**Y(ref)**	**C(ref)**
R*	2012	3.90	0.80	1.80	1.55	2.35	4.30	0.80	1.26	1.75	2.55
S*	3216L	5.10	1.40	1.80	1.85	3.25	5.50	1.40	1.26	2.05	3.45
A	3216	5.70	1.40	1.80	2.15	3.55	6.10	1.40	1.26	2.35	3.75
T*	3528L	5.40	1.70	2.80	1.85	3.55	5.80	1.70	1.96	2.05	3.75
B	3528	6.00	1.70	2.80	2.15	3.85	6.40	1.70	1.96	2.35	4.05
C	6032	8.60	3.20	2.80	2.70	5.90	9.00	3.20	1.96	2.90	6.10
U	6032L	8.60	3.20	2.80	2.70	5.90	9.00	3.20	1.96	2.90	6.10
D	7343	9.90	4.50	3.00	2.70	7.20	10.30	4.50	2.10	2.90	7.40
V	7343L	9.90	4.50	3.00	2.70	7.20	10.30	4.50	2.10	2.90	7.40
X*	7343H	9.90	4.50	3.00	2.70	7.20	10.30	4.50	2.10	2.90	7.40
E	7260	9.90	4.50	4.70	2.70	7.20	10.30	4.50	3.29	2.90	7.40
	Footnotes										

Calculation Formula
Z = Lmax + 2Jt + z
G = L - 2T - z
X = W1max + 2z
Yref = (Z - G)/2
Cref = Z - Yref
Jt = 1.0, (0.7 for S,T,U & V)
z = 0.25

Calculation Formula
Z = Lmax + 2Jt + z +2*0.2
G = L - 2T - z
X = (Wmax + 2z)*0.7
Yref = (Z - G)/2
Cref = Z - Yref
Jt = 1.0, (0.7 for S,T,U & V)
z = 0.25

** IPC 782A rounds the primary dimensions (Z, G & X) to make them compatible with grid layouts in CAD design. These dimensions have also been rounded to the nearest 0.1mm.
*** In general Tantalum Capacitors can be wave soldered. The larger case sizes are more difficult and it is not recommended that these be wave soldered. Pad designs are presented for the adventurous.

REFERENCES

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   The Institute for Interconnecting and Packaging Electronic Circuits
   2215 Santers Road, Northbrook, IL
   60062-6135
   Phone: 847-509-9700
   Fax: 847-509-9798
   Internet http:///www.IPC.org

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