

# PCB DESIGN PERFECTION: THE CAD LIBRARY SERIES PART 2: SOT (SMALL OUTLINE TRANSISTORS)

CONTENT ACKNOWLEDGEMENT: TOM HAUSHERR, DEVELOPER OF THE LP WIZARD (NOW XDM LAND PATTERN CREATOR), AND FORMER EDA LIBRARY PRODUCT MANAGER AT MENTOR GRAPHICS.

## ABSTRACT

This paper, the second in a series dedicated to CAD library quality, describes each aspect to consider when creating SOT (Small Outline Transistor) component library parts. It also describes the impact each feature has in the PCB process.



P A D S

W H I T E P A P E R

## THE UNITS

Today, 90% of all component manufacturers list their component package dimensions in metric units. Accordingly, this paper utilizes metric units for CAD library development.

## THE CALCULATIONS

The examples in this document are calculated utilizing the nominal environment as defined in IPC-7351B's standard 3-tier CAD library system: See Figure 1.

- Level A = Most – for military and medical applications.
- Level B = Nominal – for controlled environment desktop.
- Level C = Least – for cell phones and hand-held devices.



**Level A**  
Very Robust  
Solder Joint



**Level B**  
General Purpose  
Solder Joint



**Level C**  
Minimal Solder Joint  
for  
High Density Applications

*Figure 1: IPC-7351B's 3-tier solder goal density levels*

## SOT (SMALL OUTLINE TRANSISTOR) COMPONENTS

The SOT23 is the most popular of this component family. It has 3, 5, 6, and 8 pin variations and three popular pin pitches.

- 0.50 mm Pitch - See Figure 2
- 0.65 mm Pitch
- 0.95 mm Pitch

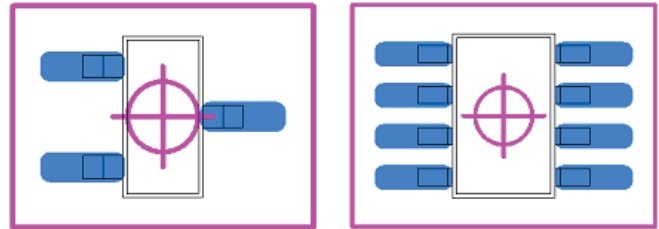


Figure 2: 0.5 mm pitch SOT23 3-pin and 8-pin examples

Figure 3 illustrates four different 0.5mm pitch 3-pin SOT23 land pattern via fanout techniques. The SOT23 parts are placed on a 0.5 mm grid system and all the vias snap to a 1 mm grid.

This spacing supports two 0.1 mm traces with 0.1mm clearance spacing on all layers. The via land size is 0.5 mm, hole size is 0.25 mm, and plane anti-pad is 0.7mm

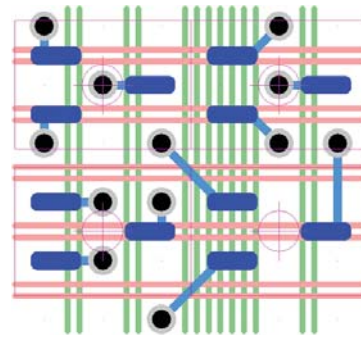


Figure 3: Four different 3-pin, 0.5mm pitch SOT23 fanout examples

Figure 4 illustrates four different 0.5mm pitch 8-pin SOT23 land pattern via fanout techniques. The SOT23 parts are placed on a 0.5 mm grid system and all the vias snap to a 1 mm grid. This allows two 0.1 mm trace/space technology on all layers.

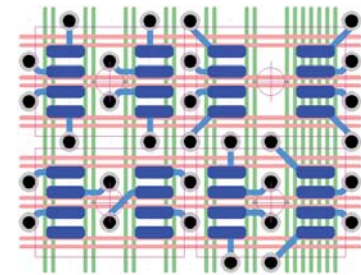


Figure 4: 8-pin, 0.5 mm pitch SOT23 fanout examples

Figure 5 illustrates four different 0.65 mm pitch SOT23 3, 5, 6, and 8-pin examples.

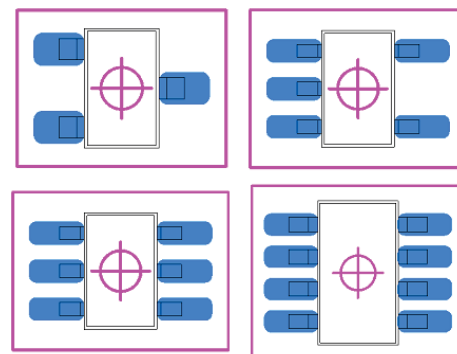


Figure 5: 0.65 mm pitch SOT23 3, 5, 6, and 8-pin examples

Figure 6 illustrates five different 0.65mm pitch 3, 5, 6, and 8-pin SOT23 land pattern via fanout techniques. The SOT23 parts are placed on a 0.5 mm grid system and all the vias snap to a 1 mm grid. This allows two 0.1 mm trace/space technology on all layers with 0.5 mm via land.

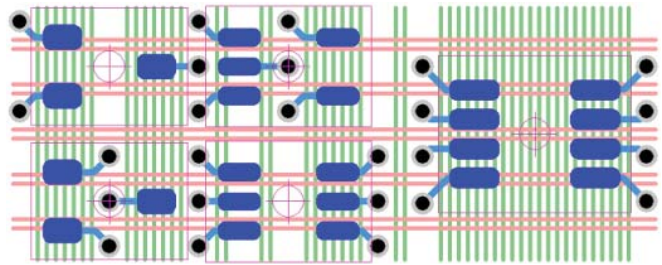


Figure 6: 0.65 mm pitch SOT23 fanout examples

Figure 7 illustrates 0.95 mm pitch SOT23 3, 5, 6, and 8-pin examples.

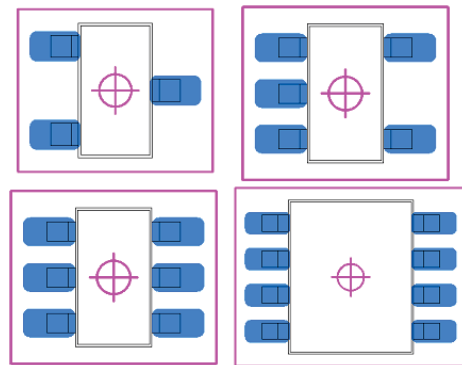


Figure 7: 0.95 mm pitch SOT23 3, 5, 6, and 8-pin examples

Figure 8 illustrates five different 0.95mm pitch 3, 5, 6, and 8-pin SOT23 land pattern via fanout techniques. The SOT23 parts are placed on a 0.5 mm grid system and all the vias snap to a 1 mm grid. This allows two 0.1 mm trace/space technology on all layers with 0.5 mm via land.

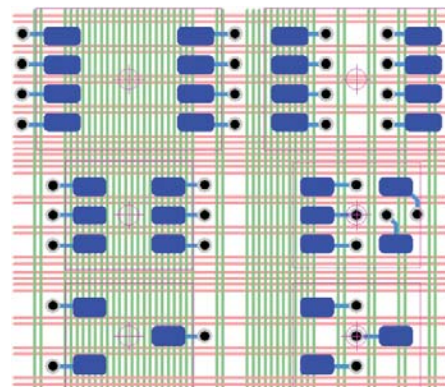


Figure 8: 0.95 mm pitch SOT23 fanout examples

The SOT223 is the second most popular SOT component. It has 4, 5, and 6-pin variations and three popular pin pitches.

- 1.27 mm Pitch - See Figure 9.
- 1.50 mm Pitch
- 2.30 mm Pitch

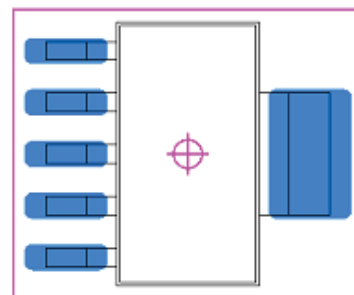


Figure 9: 6-pin 1.27 mm pitch SOT223 land pattern

Figure 10 shows the 6-pin 1.27 mm pitch SOT223 land pattern via fanout using a power via with a 1 mm land and a 0.5 mm hole snapped to a 1 mm grid. The signal trace/space rules are 0.1 mm.

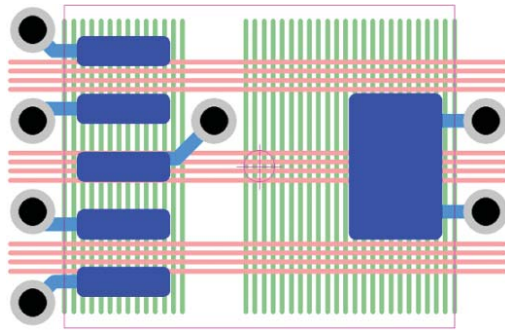


Figure 10: Typical via fanout for 6-pin 1.27 mm pitch SOT223

Figure 11 shows the 5-pin 1.5 mm pitch SOT223 land pattern.

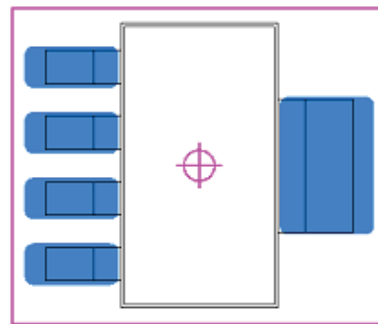


Figure 11: 5-pin 1.5 mm pitch SOT223

Figure 12 shows the 5-pin 1.5 mm pitch SOT223 land pattern via fanout using a power via with a 1 mm land and a 0.5 mm hole snapped to a 1 mm grid. The trace/space rules are 0.1 mm.

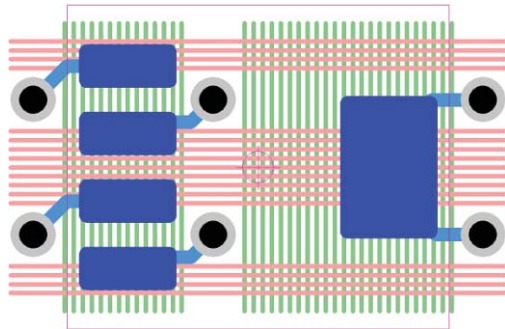


Figure 12: Typical via fanout for 5-pin 1.5 mm pitch SOT223

Figure 13 shows the 4-pin 2.3 mm pitch SOT223 land pattern.

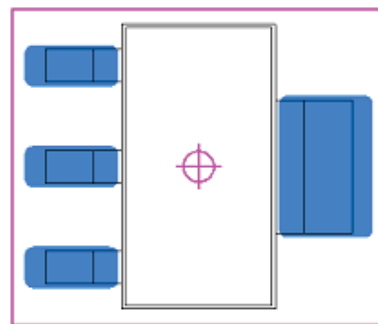


Figure 13: 4-pin 2.3 mm pitch SOT223

Figure 14 shows the 4-pin 1.5 mm pitch SOT223 land pattern via fanout using a power via with a 1 mm land and a 0.5 mm hole snapped to a 1 mm grid. The trace/space rules are 0.1 mm but the routing grid is 0.05 mm.

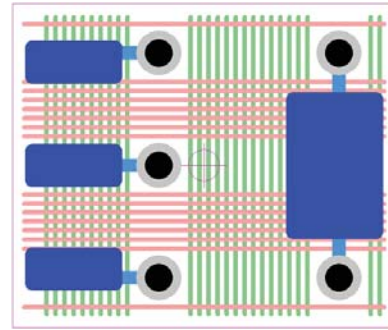


Figure 14: 4-pin 1.5 mm pitch SOT223

The SOT143 is another popular SOT component. It has four pins with a larger Pin 1. The pin pitch is 1.9 mm. See Figure 15.

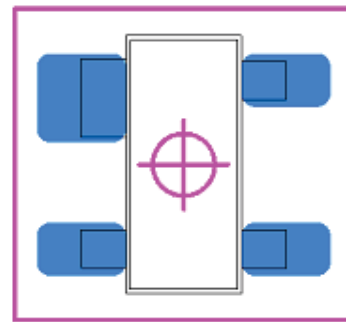


Figure 15: SOT143

Figure 16 shows the 4-pin 1.9 mm pitch SOT143 land pattern via fanout using a via with a 0.5 mm land and a 0.25 mm hole snapped to a 1 mm grid. The trace/space rules are 0.1 mm and the routing grid is 0.1 mm.

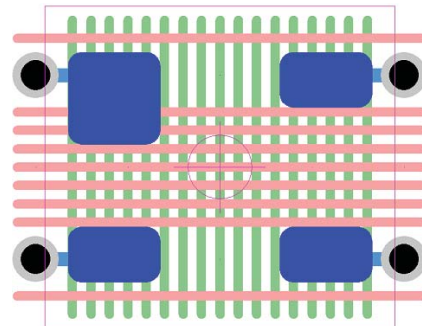


Figure 16: 4-pin 1.9 mm pitch SOT143

The SOT343 is also popular. It has four pins with a larger Pin 1. See Figure 17.

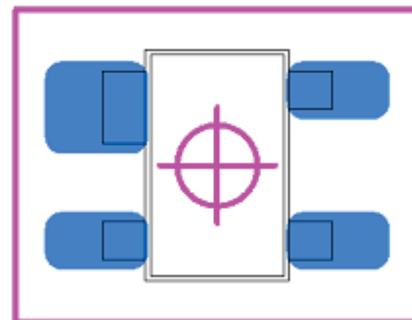


Figure 17: SOT343

Figure 18 shows the 4-pin 1.3 mm pitch SOT343 land pattern via fanout using a via with a 0.5 mm land and a 0.25 mm hole snapped to a 1 mm grid. The trace/space rules are 0.1 mm and the routing grid is 0.1 mm. The via fanout direction depends on which layer needs more routing channels.

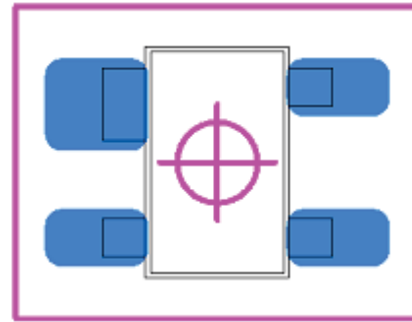


Figure 18: 4-pin 1.3 mm pitch SOT343

The SOT component family uses a Gull Wing component lead. All Gull Wing leaded components have four different sets of land pattern rules. The following examples are for the "Nominal Environment."

- Pin pitch less than 0.625mm (side goal is -0.02 mm) considered "fine pitch"
- Pin pitch greater than 0.625 mm (side goal is 0.03 mm)
- Outward Flat Ribbon with pin pitch less than 0.625mm (heel goal is 0.15 mm and side goal is -0.02 mm)
- Outward Flat Ribbon with pin pitch greater than 0.625mm (heel goal is 0.15 mm and side goal is 0.03 mm)

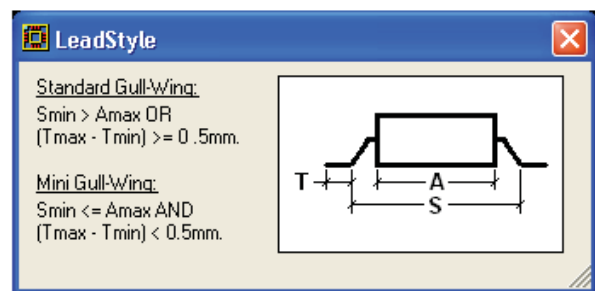


Figure 19: Gull Wing - Standard and Mini formulas

The formula to calculate the difference between Gull Wing and Outward Flat Ribbon (Mini Gull Wing) is shown in Figure 19.

## SOT ASSEMBLY AND SILKSCREEN GRAPHIC CONSIDERATIONS

It's important to note that the Lands (pads) do not get added to the assembly drawing layer for small parts. The two most important things on the assembly drawing are the Ref Des and Component Outline. If the part is too small and the Lands interfere with the Ref Des, then do not add the Top Assembly Lands to the padstack. However, if the Lands do not interfere with the Ref Des then the Top Assembly Lands should be added to the padstack.

Here are some of the various assembly outlines for the 0.95 mm pitch SOT23 component family. See Figure 20 for the 3, 5, & 6-pin versions of the Assembly Outline, Ref Des, and Polarity Marker for pin 1 location and Lands (pads). Note that the polarity marker shape is a triangle in the corner because the component is too small for the standard circle polarity marker.



Figure 20: 3, 5, & 6-pin - 0.95 mm pitch SOT23 examples

Here are some of the various assembly outlines for the SOT223 component family. See Figure 21 for the 4, 5, & 6-pin versions of the Assembly Outline, Ref Des, and Polarity Marker for pin 1 location and Lands (Pads).



Figure 21: Assembly outlines for 4, 5, & 6-pin versions

Here are some of the assembly outlines for the SOT143 component family. See Figure 22 for the standard and reverse pin versions of the Assembly Outline, Ref Des, and Polarity Marker for pin 1 location and Lands (Pads). Note that the polarity marker shape is a triangle in the corner because the component is too small for the standard circle polarity marker.



Figure 22: SOT143 examples

Here are some of the various silkscreen outlines for the SOT component families. See Figure 23 for the SOT23, SOT223, and SOT143 versions of the Silkscreen Outline, Polarity Marker, and 0.5 mm Post Assembly Inspection Dot for pin 1 location and Lands (Pads). Note that the SOT23 and SOT143 do not have a polarity marker inside the silkscreen outline because the component is too small. The Post Assembly Inspection Dot will be the Polarity Marker.

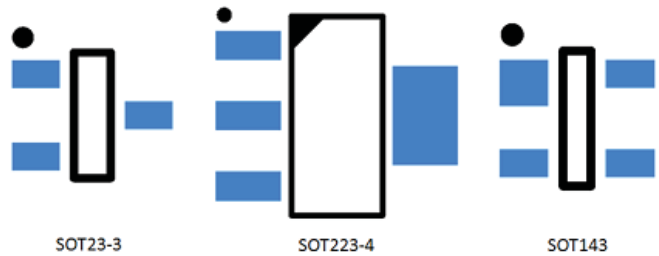


Figure 23: SOT silkscreen outline examples: 0.50 mm pitch, 0.65 mm pitch, and 0.95 mm pitch.



## CONCLUSION

When creating SOT components, every aspect of the design should be considered including the impact that each land pattern feature has in the PCB design process. The land pattern is the starting point that affects every process from PCB layout through PCB manufacturing and assembly. There are dozens of things to consider when creating a CAD library that are often overlooked; this paper discussed the factors to consider when creating molded body component library parts. Each factor can directly affect the quality of the part placement, via fanout, trace routing, post processing, and fabrication and assembly processes.

## DID YOU KNOW?

PADS, Mentor Graphics' Personal Automated Design System, includes everything you need in order to create your component library. PADS provides a highly integrated library and component management environment that meets designers' and engineers' needs in creating and maintaining PCB design libraries.

### PADS LIBRARY MANAGEMENT COMBINES:

- A starter library containing more than 10,000 ready-to-use, IPC-compliant, proven parts provided by Optimum Design Associates for a quick start to new design projects.
- Web access to component supplier data with an ability to load contents into PADS
- A central library for maintaining up-to-date design data. The central library contains all library elements in the same location, and is available at all design stages. PADS makes it possible to maintain an up-to-date library in real time, without any compilation, and includes all library elements (e.g., symbols, part data, footprints, simulation models, drawing items, and part common-property definitions).
- A component management system, integrated with schematic design and library management environments.
- A built-in consistency check of library data to make sure your library is constantly in-sync.
- Live verification of symbols placed in your schematic against the latest component and library data to eliminate costly redesigns and quality problems that might otherwise go undetected until late in the design cycle.
- A land pattern creator for quick creation of IPC-standard footprints.
- A migration path for 3rd-party libraries and component databases.

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