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Maintain thermal stability for power-MOS devices

POWER MOSFETs CAN EXPERIENCE DESTRUCTIVE THERMAL EFFECTS AT RELATIVELY LOW DRAIN VOLTAGES AND CURRENTS THAT ARE WELL WITHIN TRADITIONAL, SAFE BOUNDARIES. HOWEVER, DESIGNERS CAN USE BASIC SPICE-MODEL PARAMETERS TO PREVENT THERMAL INSTABILITY IN THESE DEVICES.

Power MOSFETs can experience destructive thermal effects at relatively low drain voltages and currents that are well within the traditional SOA (safe-operating-area) boundaries. For typical SOA curves, in which gate-to-source voltage is larger than the threshold voltage, the increasing on-resistance of the MOS device dominates and effectively limits thermal runaway. Destructive failure can result, however, if the device is biased at a low gate-to-source voltage, such that sensitivity to the decreasing threshold voltage overwhelms the increasing channel resistance as temperature rises. You can use basic Spice-model parameters to estimate the minimum gate drive to prevent thermal instability and resultant damage to the device.

MOSFETs IN THE SATURATION REGION

For a MOSFET in the saturation region,

$$I_D = \frac{\mu C_{OX}}{2}\frac{W}{L}(V_{GS}-V_T)^2, \qquad (1)$$

where I_D is drain current, μ is electron mobility, V_T is the threshold voltage, V_{GS} is the gate-to-source voltage, C_{OX} is the oxide capacitance, W is the gate width, and L is the gate length. Electron mobility and threshold voltage are the significant temperature-dependent terms.

The threshold of thermal stability occurs at the $V_{GS}-V_T$ value, where the rate of change of drain current with temperature is zero:

$$\frac{\partial I_D}{\partial T} = \frac{\partial \mu}{\partial T} \times \left\{\frac{C_{OX}}{2}\frac{W}{L}(V_{GS}-V_T)^2\right\} - \frac{\partial V_T}{\partial T} \times \left\{\mu C_{OX}\frac{W}{L}(V_{GS}-V_T)\right\}. \qquad (2)$$

Substituting for I_D,

$$\frac{\partial I_D}{\partial T} = \frac{\partial \mu}{\partial T} \times \left\{\frac{I_D}{\mu}\right\} - \frac{\partial V_T}{\partial T} \times \left\{\frac{2I_D}{(V_{GS}-V_T)}\right\} = I_D \times \left\{\frac{1}{\mu}\frac{\partial \mu}{\partial T} - \frac{2}{(V_{GS}-V_T)}\frac{\partial V_T}{\partial T}\right\}. \qquad (3)$$

Recognizing that both $\partial\mu/\partial T$ and $\partial V_T/\partial T$ are negative, **Equation 2** shows that drain current increases or decreases with temperature, depending on the magnitude of $V_{GS}-V_T$. Setting this rate of change to zero gives $V_{GS}-V_T$ at the threshold of stability:

$$\frac{1}{\mu}\frac{\partial \mu}{\partial T} = \frac{2}{(V_{GS}-V_T)}\frac{\partial V_T}{\partial T}, \qquad (4)$$

or

$$V_{GS}-V_T = 2\mu \times \frac{\partial V_T / \partial T}{\partial \mu / \partial T}. \qquad (5)$$

$V_{GS}-V_T$ must be greater than the value in **Equation 5** to ensure thermal stability, $-\partial I_D/\partial T$. Note that the rate of change with temperature is proportional to I_D, but the threshold of thermal stability depends only on mobility and the temperature coefficients of mobility and threshold voltage. You can derive the mobility value for a typical MOS power device, the NTD60N02, from the Spice-model-file parameter for K′ on the manufacturer's Web site: $K'=\mu\times C_{OX}$, and $C_{OX}=\epsilon_{OX}/t_{OX}$. With $K'=18.1\ \mu A/V^2$ from the model file, permittivity that standard texts define, and an oxide thickness of 400 angstroms, mobility is $\mu=206(cm^2/V\times sec)$ for this process. Mobility varies with temperature in a manner proportional to T^{-n}, where n is typically about 1.5 (**Reference 1**). You determine an expression for mobility as a function of temperature by setting $206=C\times T^{-1.5}=C\times 300^{-1.5}$ at room temperature, where T=300K). This calculation equates to a proportionality constant of $C=(206/300^{-1.5})=2.86\times 10^6$. The rate of change of mobility with temperature (**Reference 2**) for this case is then:

$$\frac{\partial \mu}{\partial T} = -N \times C \times T^{-N-1} = -1.5 \times (1.1 \times 10^6) \times 300^{-2.5} = -1.06\frac{CM^2 / V \times sec}{°K}. \qquad (6)$$

Typical values for threshold-voltage variation with temperature are in the range of $(\partial VT/\partial T)=-2[(mV)/°K]$. Using these values of mobility and temperature variation:

$$V_{GS}-V_T = 2 \times 550 \times \left(\frac{-0.002}{-2.75}\right) = 0.8V \qquad (7)$$

for a MOS device with the mobility $[550(cm^2/V\times sec]$ operating in the saturated region. You can then add the Spice-model value for V_T to the above result to determine the minimum gate-to-source voltage necessary for thermal stability.

MOSFETs IN THE LINEAR REGION

You can apply the same analysis to the drain-current expression for a MOS device in the linear region of operation:

$$I_D = \mu C_{OX} \frac{W}{L}\left\{(V_{GS}-V_T)\times\left(V_{DS}-\frac{V_{DS}^{\ 2}}{2}\right)\right\}, \qquad (8)$$

where the $V_{DS}^{\ 2}$ term is small enough for you to ignore in **Equation 9**:

$$\begin{aligned}\frac{\partial I_D}{\partial T} &= \frac{\partial\mu}{\partial T}\times\left\{C_{OX}\frac{W}{L}(V_{GS}-V_T)\times V_{DS}\right\}-\frac{\partial V_T}{\partial T}\times\\ &\left\{\mu C_{OX}\frac{W}{L}V_{DS}\right\}=\frac{\partial\mu}{\partial T}\times\left\{\frac{I_D}{\mu}\right\}-\frac{\partial V_T}{\partial T}\times\left\{\frac{I_D}{(V_{GS}-V_T)}\right\}= \qquad (9)\\ &I_D\times\left\{\frac{1}{\mu}\frac{\partial\mu}{\partial T}-\frac{1}{(V_{GS}-V_T)}\frac{\partial V_T}{\partial T}\right\}.\end{aligned}$$

Again, the drain-current rate of change with temperature shows that drain current increases or decreases with temperature, depending on the magnitude of $V_{GS}-V_T$. Setting this rate of change to zero yields **Equation 10** or **11**:

$$\frac{1}{\mu}\frac{\partial\mu}{\partial T}=\frac{1}{(V_{GS}-V_T)}\frac{\partial V_T}{\partial T}, \qquad (10)$$

or

$$V_{GS}-V_T=\mu\times\frac{\partial V_T/\partial T}{\partial\mu/\partial T}, \qquad (11)$$

which differ from the expression for a device in saturation, **equations 4** and **5**, by a factor of two. Thus, for the same device-channel mobility of 550(cm²/V×sec), the minimum gate drive to maintain thermal stability in the linear region is half that in saturation, or $V_{GS}-V_T=0.4V$.

You can find Spice models for many discrete power MOSFETs on the manufacturers' Web sites. These models are usually more basic than the BSIM3 models designers commonly use for IC simulation, so the U0 value for mobility may default to the value of 600(cm²/V×sec), which Spice simulator references use (**Reference 3**).EDN

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