THE POWER DIP (16+2+2, 12+3+3) PACKAGES

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INTRODUCTION

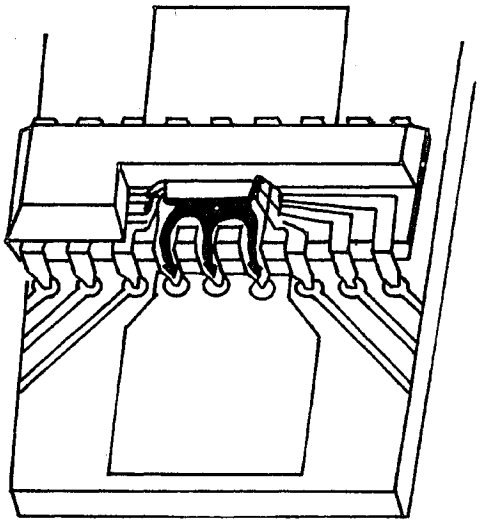
This Application Note is aimed to give a complete thermal characterization of the (16+2+2) power DIP (modified 20 lead DIP with 4 heat transfer leads) and of the (12+3+3) power DIP (modified 18 lead DIP with 6 heat transfer leads) in association with thermal modules integrated on the PCB.

Characterization is performed according with recomendations included in G32-86 SEMI guideline, by means of a dedicated test pattern developed by SGS-THOMSON. It refers to:

1. Junction to pin thermal resistance Rth(j-p)
2. Junction to ambient thermal resistance Rth(j-a)
3. Thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techiniques.

Figure 1. POWER DIP application on PC board



Experimental conditions

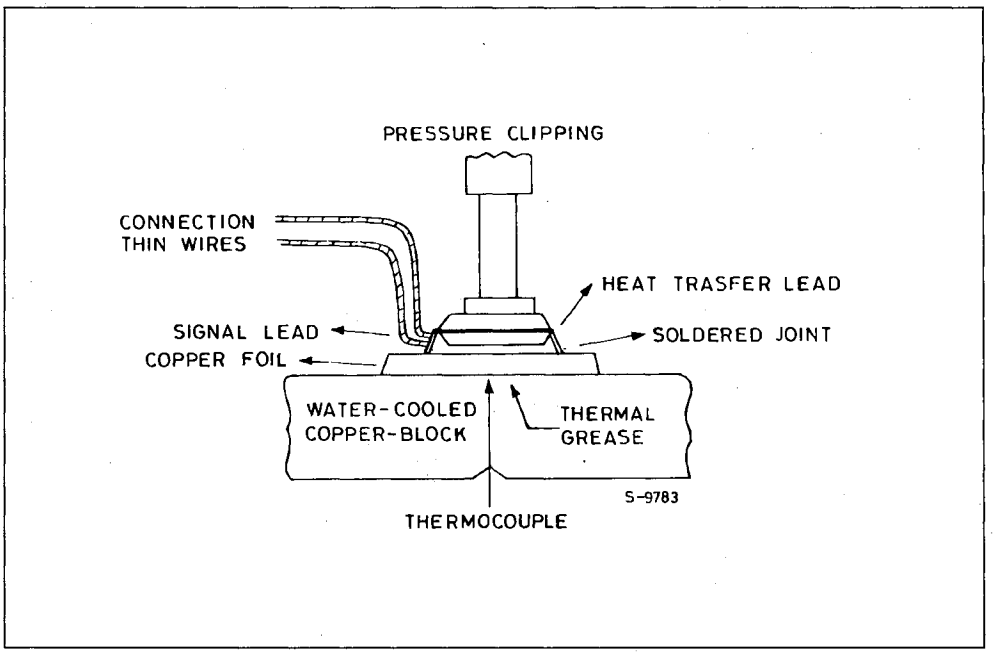
The thermal evaluation was performed by means of the test pattern P638, which is a 80x80 *mils*^{2} die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 3000 *mils*^{2}, with a power capability of 20 W. Measurement method is described in Appendix. A.

Samples with the indicated characteristics were prepared:

Package	DIP (16+2+2)	DIP (12+3+3)
Frame Material	Copper	Copper
Frame Thickness	0.4*mm*	0.4*mm*
Frame Thermal Conductivity	3.9*W/cm*°C	3.9*W/cm*°C

Measurement of junction to pin thermal resistance Rth(j-p) is performed by holding the package (with the heat transfer leads soldered on a copper plate) against a water cooled heat sink, according with fig. 2. A thermocouple placed in contact with the plate measures the reference temperature.
For junction to ambient thermal resistance Rth(j-a) the samples are suspended horizontally in a one cubic foot box, to prevent drafts.
The effect of "on board" external heat sinks shown in fig. 1 is quantified, using a test board which has two 4 x 4 cm^2 dissipating areas, one of each side of the package. These areas are mechanically reduced in order to study the effect of their size on thermal performance.
The measurement circuit shown in fig. A3 is used for all of the thermal evaluations.

Figure 2. Measurement of Rth(j-p)



JUNCTION TO PIN THERMAL RESISTANCE

The dependance of Rth(j-p) on the dissipated power is negligeable compared to the absolute value: starting from 1 Watt to 10 Watts the Rth(j-p) increases of about 0.5C/W due to the lowering of silicon thermal conductivity with the increasing of temperature. An important contribution to Rth(j-p) is given by the silicon die and in fig. 3,4 is showed the relationship between Rth(j-p) and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

In the figures two curves area reported: the lower one is referring the Rth(j-p) measured at the pin stand-off, the upper one is referring to the Rth(j-p) measures at 1.5 mm from the pin stand-off (1.5 mm is the typical thickness of FR4 board).

The upper curve must be used for the application in which the heat sink is placed in the lower side of PCB and the lower curve must be used when the heat sink is placed on the upper side of PCB.

Figure 3 - POWER DIP 16+2+2 $R_{th(j-p)}$ vs on die dissipating area

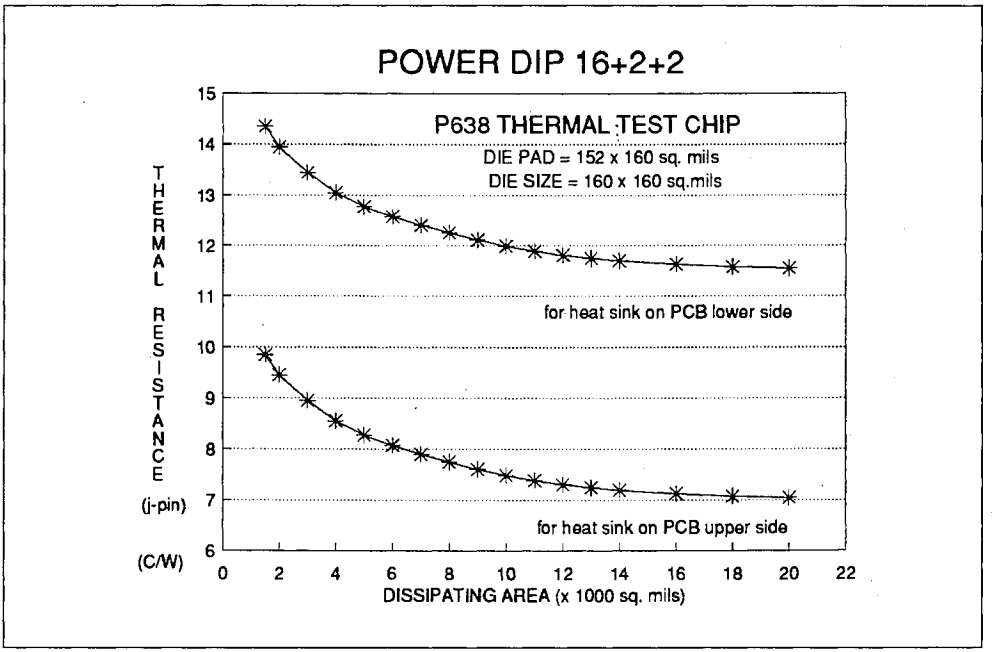
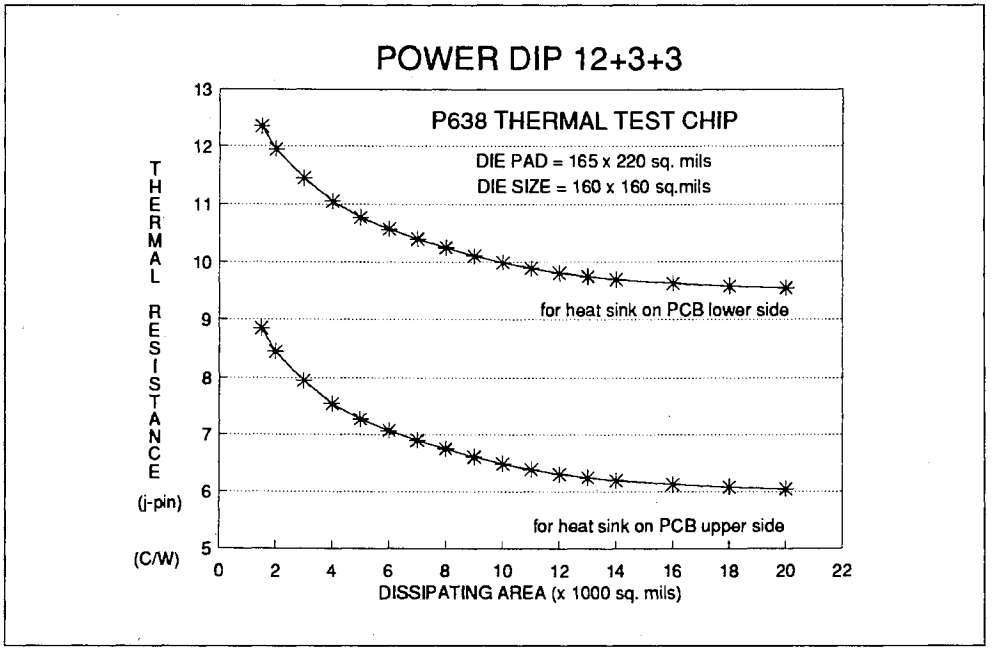


Figure 4 - POWER DIP 12+3+3 $R_{th(j-p)}$ vs on die dissipating area



JUNCTION TO AMBIENT THERMAL RESISTANCE

Fig. 5,6 give the junction to ambient thermal resistance Rth(j-a) of the package vs dissipated power; it evidences the effect of the board in improving the exchange of the heat towards the ambient. The upper curve refers to samples suspended in air, with eight thin wire connecting the dissipating transistors and the sensing diode. The lower curve is obtained with a very large heat sink (35 µm thick 4 x 4cm^2 copper area for each side) while the other curve refers the packages mounted on board with no heat sink.

Rth is decreasing when power is increased, due to a better heat transfer efficiency at higher temperature.

Figure 5 - $R_{th(j-a)}$ of DIP (16+2+2) package vs dissipated power

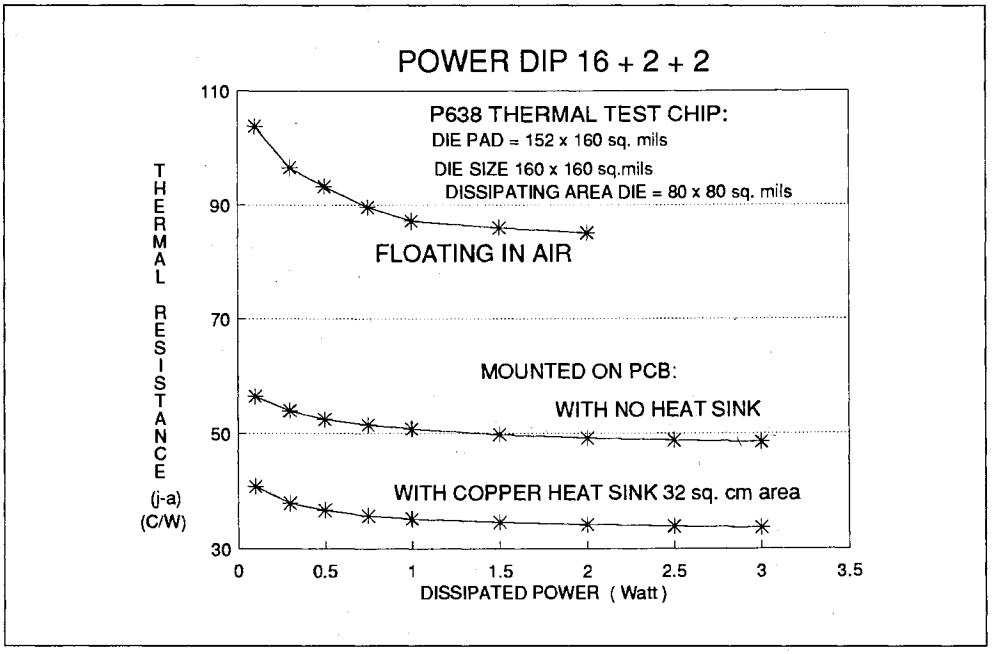
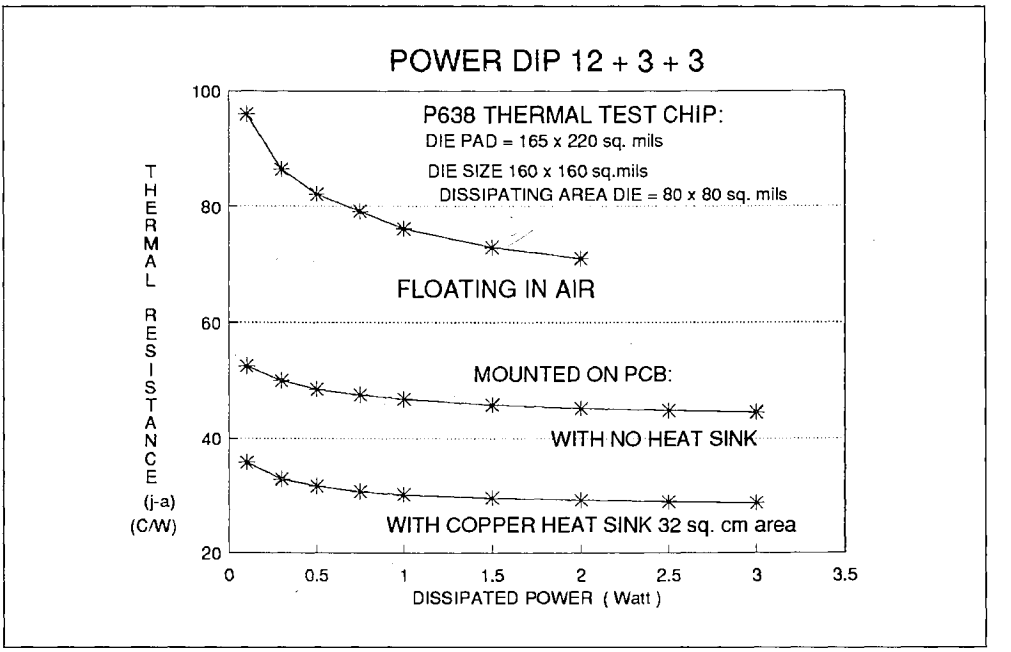


Figure 6 - Rth(j-a) of DIP (12+3+3) package vs. dissipated power



The effect of on board heat sinks with different size is summarized in fig. 8,9; thermal resistance in given vs the side l of the two thick copper squares, obtained in the lower side of the test board and dedicated to heat dissipation (see fig. 7 for test board). Standard thickness of 35µm was used for the characterization as the most part of PCb application but a large improvement can be easily obtained with a thicker copper heat sink on board: 70µm and 105µm (respectively 2 and 3 oz.) are strongly increasing the thermal performances of the considered POWER DIP application. These solutions can be attractive for low complex PC board with a cost saving in avoiding large external heat sink or forced ventilation.

Figure 7 - Test board with two "on board" square heat sinks vs side l

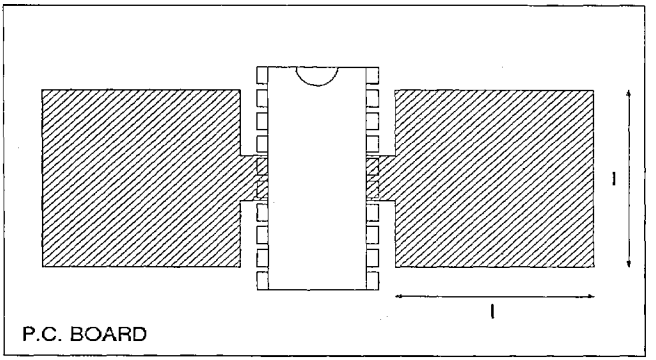


Figure 8 - $R_{th(j-a)}$ of POWER DIP 16+2+2 vs side I for heat sink on the PCB lower side

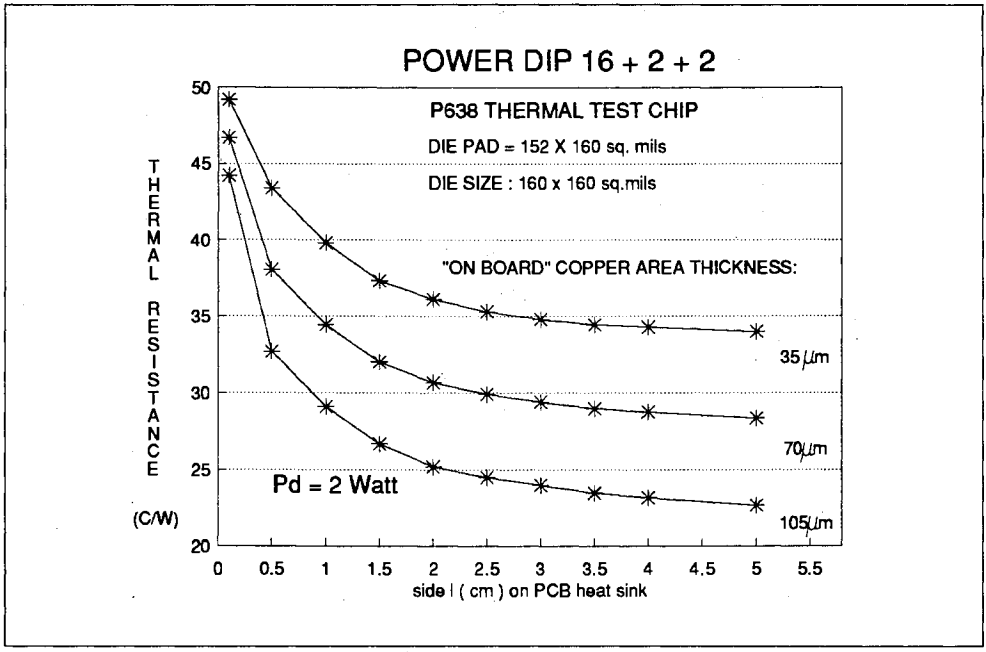
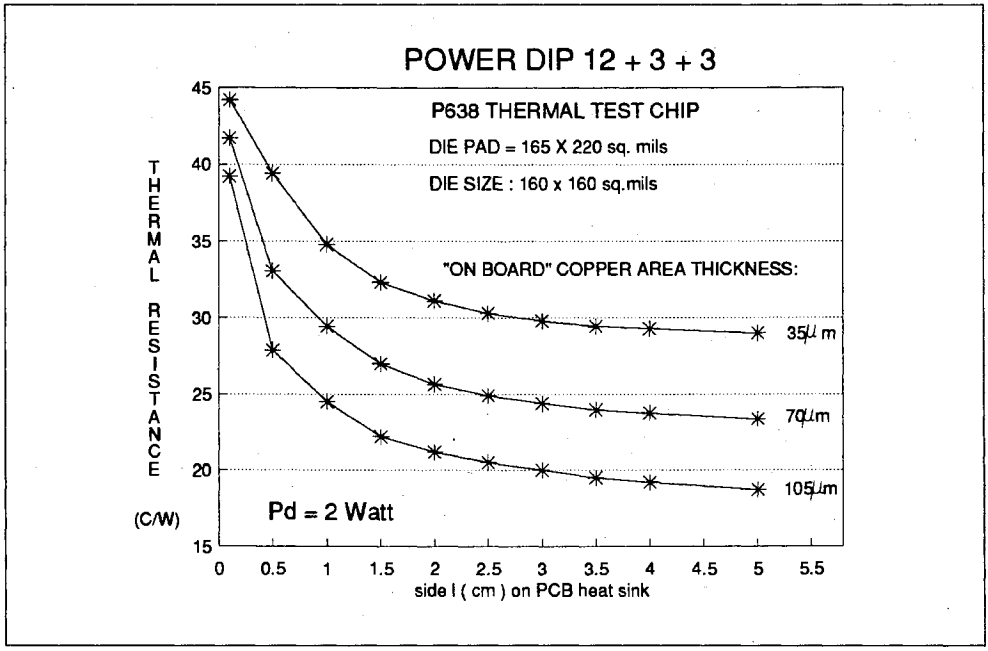


Figure 9 - $R_{th(j-a)}$ of POWER DIP 12+3+3 vs side I for heat sink on the PCB lower side



TRANSIENT THERMAL RESISTANCE

The effect of single pulse of different length and height, is shown in fig. 10,11 for POWER DIP 16+2+2 and 12+3+3. Thicker copper heat sink on PCB is effective also for short pulse width (less 1 sec.). Due to a significant thermal capacitance a correspondingly long risetime, single pulse up to 10W can be delivered to the system for 1s with acceptable junction temperature increase.

Figure 10 - DIP 16+2+2 Transient thermal resistance for single pulses

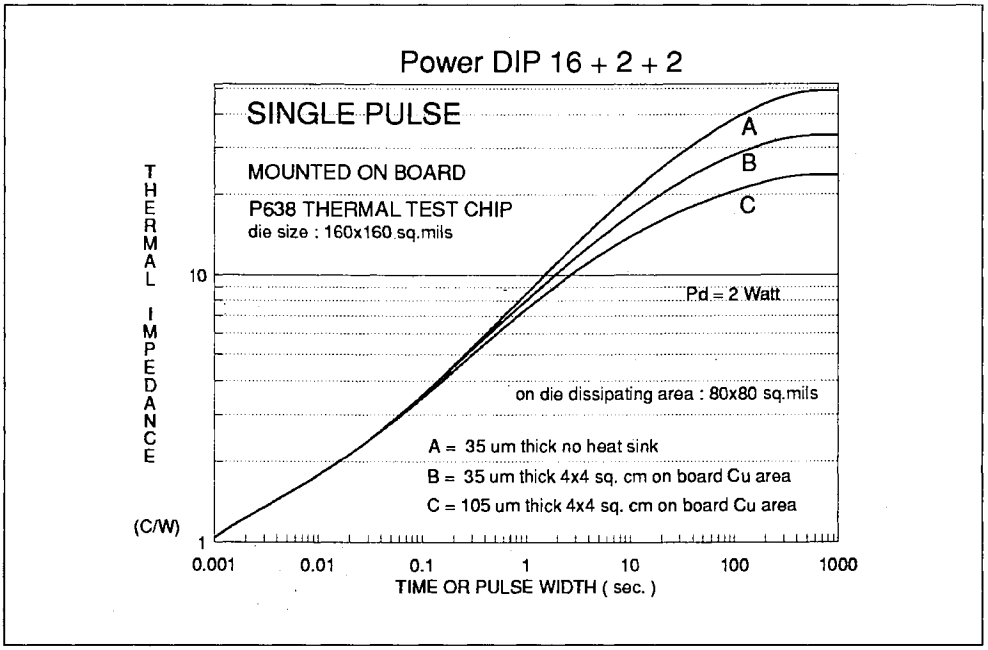
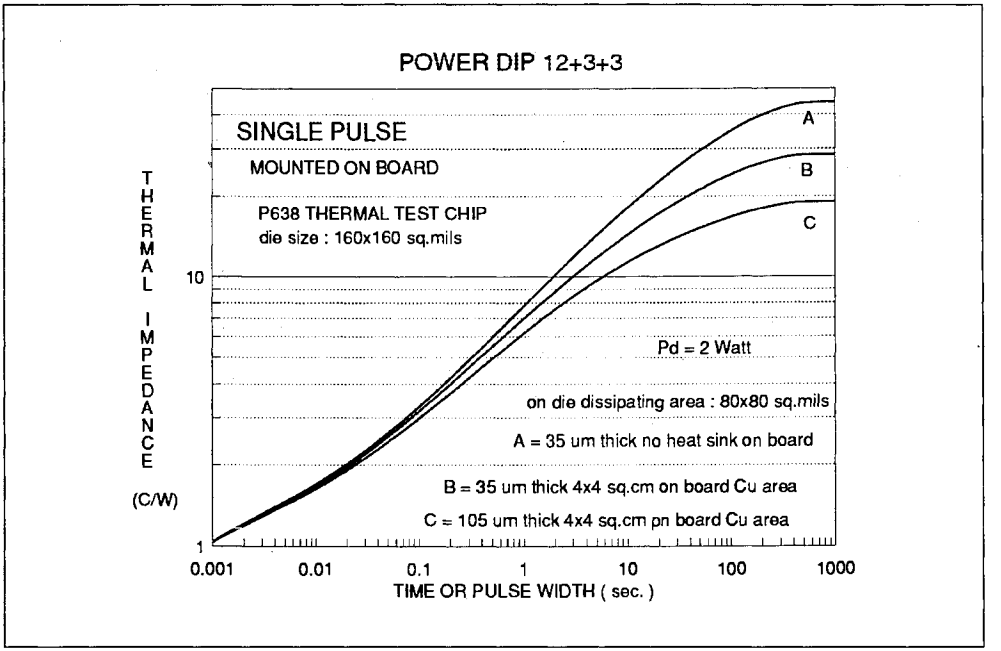


Figure 11 - DIP 12+3+3 Transient thermal resistance for single pulses



Repeatition of pulses with defined Pd, period and duty cycle DC (ratio between pulse length and signal period), gives rise to an average temperature increase:

$\Delta T_{avg} = Rth \times Pd_{avg} = Rth \times Pd \times DC$

Junction temperature is oscillating about the mean value as qualitatively shown in fig. 12. The transient thermal resistance corresponding to the upper limit (peak transient thermal resistance) is reported in fig. 13,14 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

Figure 12

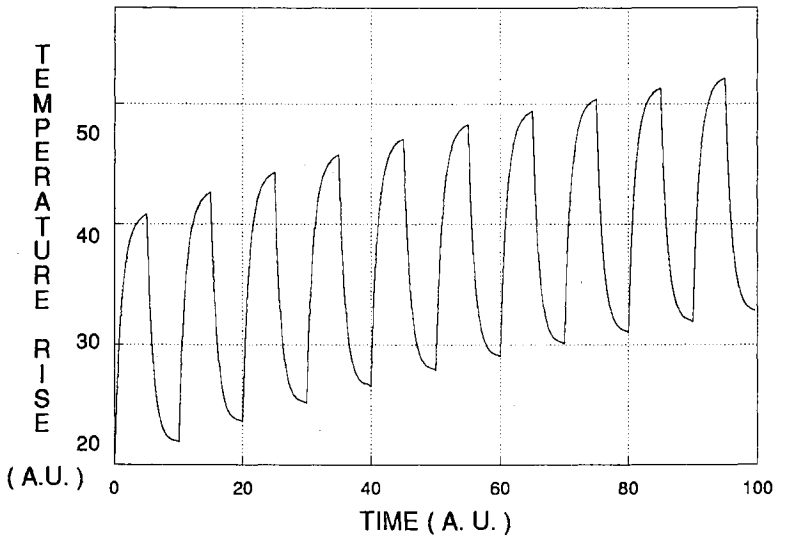


Figure 13 - Peak Transient Thermal resistance of DIP (16+2+2)

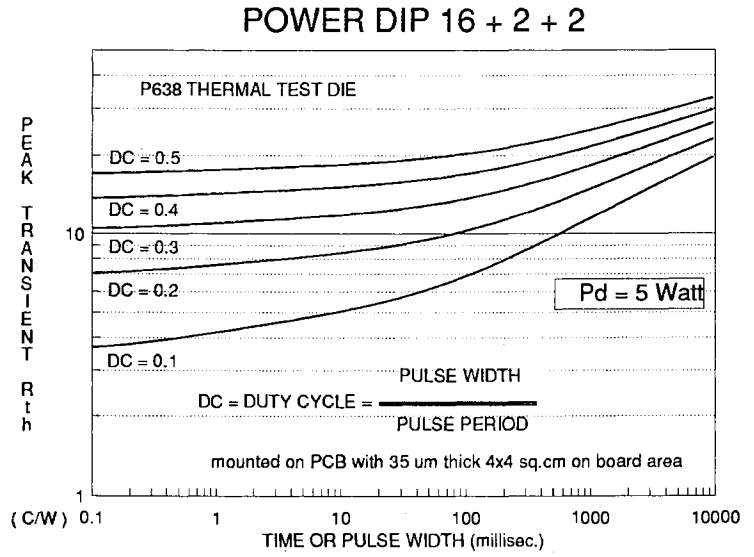
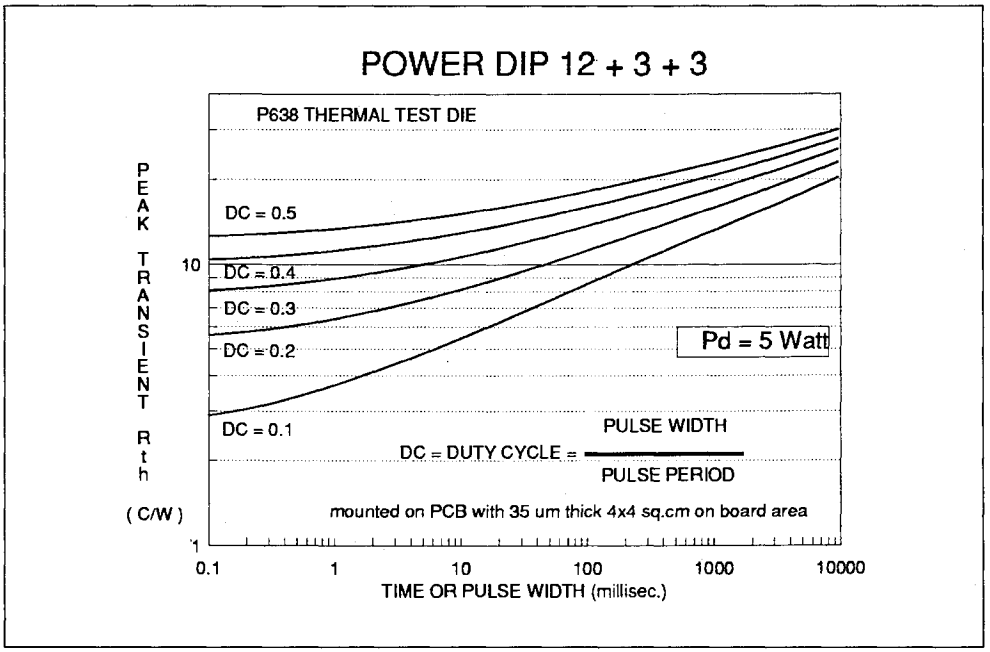


Figure 14 - Peak transient thermal resistance of DIP (12+3+3)



APPENDIX

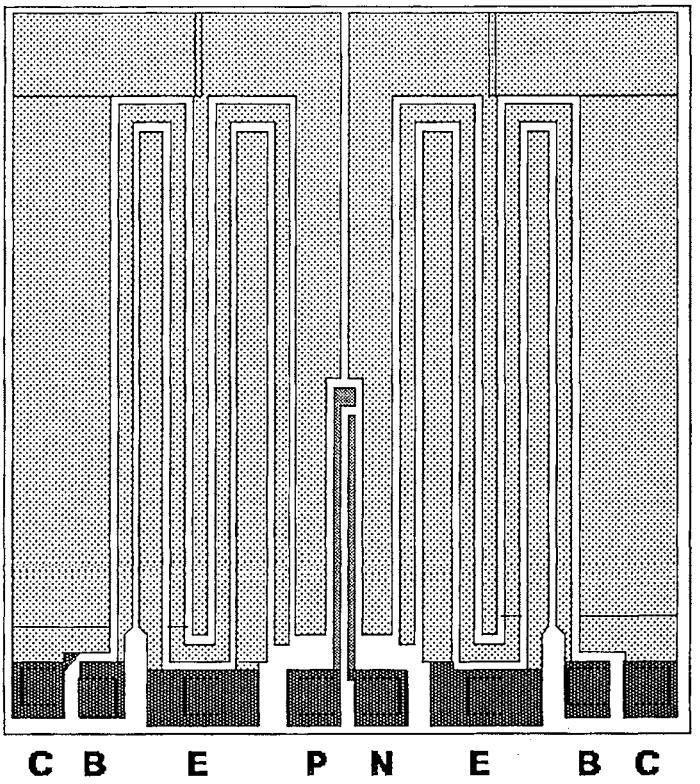
TEST PATTER P638

For thermal measurement

Test patterm P638 is designed for thermal measurement following SEMI guideline G32 (see SEMI Standard Handbook, 1986/87).

It has two bipolar power transistor with area of about 3000 sq. mils and one sensing diode (see Fig. A1). The lay-out is optimized in order to have a uniform temperature, once the two transistors are powered: the sensing diode is placed at the center of this area.

Figure A1 - P638 test pattern



Die size of single unit is 80 x 80 sq. mils; wafer thickness is about 280 microns.

The relationship between the forward voltage V_f of the diode at a constant current of **100** μA and the temperature is linear, with a coefficent **K = 1.85 mV/C** (see Fig. A2).

Therefore changes ΔT_j in junction temperature of the dissipating element formed by the two transistors, can be easily obtained from the diode forward voltage drop:

$$\Delta T_j = \frac{(V_{f1} - V_{f2})}{K}$$

(V_{f2} is the diode forward voltage at ambient temperature and V_{f1} is the voltage when the transistors are dissipating).

For thermal resistance evaluation the measurement circuit is showed in Fig. A3.

Figure A2 - Calibration curve (sensig diode).

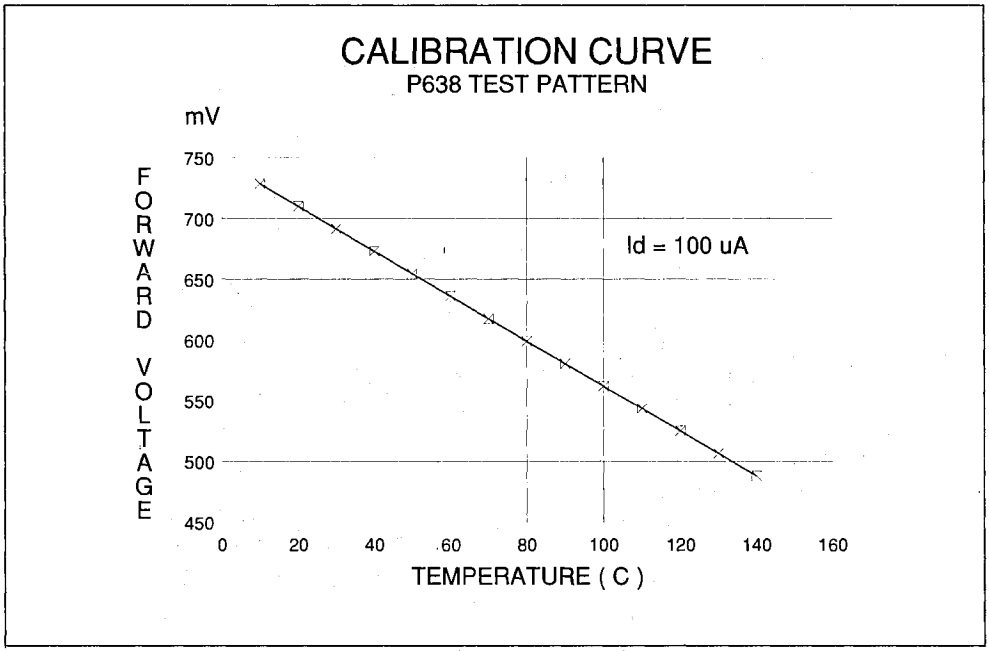
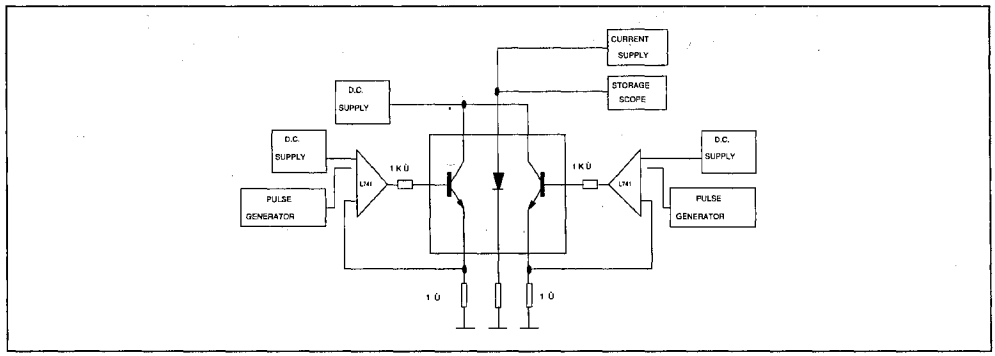


Figure A3 - Measurement System



Tipical conditions are:

P_d (Watt)	V_{ce} (Volt)	I_c (mA)
0.1	1.0	100
0.2	2.0	100
0.3	3.0	100
0.5	5.0	100
0.75	7.5	100
1.0	10.0	100
1.5	15.0	100
2.0	20.0	100
3.0	15.0	200
5.0	25.0	200
10.0	25.0	400

Each transistor is able to dissipate up to 10 Watt due to presence of second breakdown.