MAKING THE MOST OF LOGIC IC'S

PART TWO—By R. W. COLES

PRACTICAL RTL DICE

ARMED with the basic facts of RTL from Part 1, we can now consider a simple "novelty" application, an electronic dice unit, which will take the place of the usual cube of dots used in so many games of chance.

Anyone interested in RTL will find plenty to get his teeth into, as the design employs the main elements of this family as well as interface circuits and a multivibrator.

This article will describe the design of a small electronic unit which will replace the conventional playing dice.

It must be appreciated that this is intended purely as an exercise in the use of RTL; it is possible to design a more simply way of simulating dice.

The system is designed around RTL logic integrated circuits, and serves as a useful introduction to the use of these versatile devices, which are now available quite cheaply from several different advertisers in this magazine.

OPERATION OF THE SYSTEM

The operation of the system is quite simple: a free running astable multivibrator is used as the input to a binary counter, which is programmed to divide by six. The six separate states of the counter are decoded by a system of gates, and are used to illuminate six miniature lamps, only one of which will be on at a given time.

Each of the bulbs is assigned a decimal value between one and six, and the bulb which is illuminated at the end of the count represents the "up" side of the dice.

The element of chance is introduced by allowing the "thrower" to control the input to the counter by means of a push button. The multivibrator, or "clock", speed is arranged to be fast enough to prevent the eye from following the count, which will be "frozen" when the button is released.

The unit employs a total of five integrated circuits: two ML914 dual two-input negative logic NAND gates and three ML923 JK bistable flip-flops. These i.c.s are also shown as μL914 and μL923 in suppliers' lists. In addition, eight *npn* silicon bulb-driver stages, ten resistors, and two capacitors are employed.

The "clock" is made by a.c. coupling a dual gate to form a multivibrator which oscillates at approximately 1kHz, and gives a square-wave output to drive the counter. The circuit of the ML914, with the two resistors and two capacitors which set the frequency and pulse width of the output, is shown in Fig. 2.1. To enable the clock to be switched on and off, a push button switch is connected in its positive supply line.

BINARY COUNTER

The divide by six counter is formed from three JK bistables, with feedback to prevent it cycling in unwanted states (because a three-stage counter would normally have eight separate states), each stage dividing by two. The "text-book" way to make a divide by six counter is to force a divide by eight counter to reset to zero when a count of seven is decoded by an AND gate. However, by using JK flip-flops, the same result can be achieved in a simpler way, with the added advantage that bulb decoding gating can also be made simpler than would be the case with a conventional binary divider.

The simplest way to set about designing a counter which is not required to divide to a binary multiple (two, four, eight, 16, etc.), is to divide the required divisor by two until the lowest odd integer is obtained. A counter, with feedback, is then designed to divide by this number, followed by (or preceded by) a number of divide by two stages, to make the final divisor up to the required number.

Our divide by six counter can be constructed by using a divide by three counter followed by one divide by two stage. A further divide by two stage would turn it into a divide by 12 counter, and so on. The advantage of using this method is that it is much simpler to arrange the feedback for resetting a divide by three counter than for a complete divide by six counter.

There is a disadvantage which could be important in some other applications, the counter outputs are not in the natural binary code, as can be seen from the truth tables of the two types of counter discussed (see Fig. 2.2).

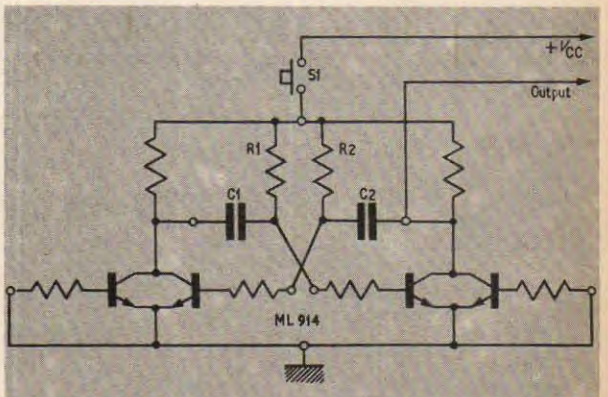

Fig. 2.1. Clock pulse generator made up from two 2-input NAND gates with C1, C2, R1 and R2 added to make up an astable multivibrator. R1=R2=1kΩ. C1=C2=0·68μF

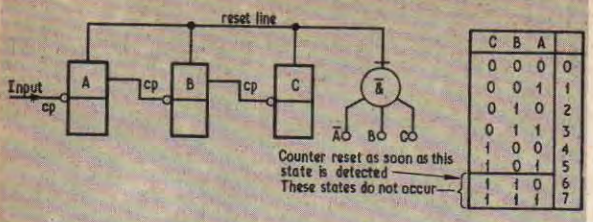

Fig. 2.2a. Conventional ÷6 counter

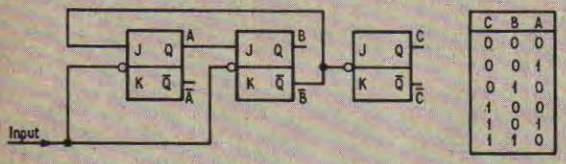

Fig. 2.2b. This ÷6 counter is used in the dice system

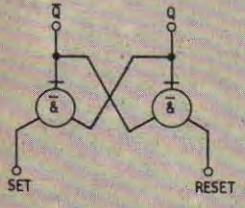

Fig. 2.3a. Simple latch bistable

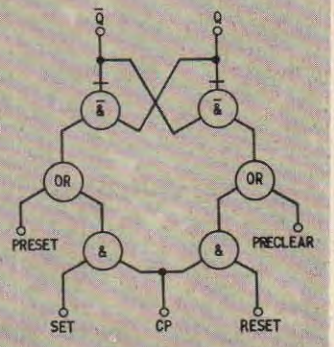

Fig. 2.3b. Shift register bistable

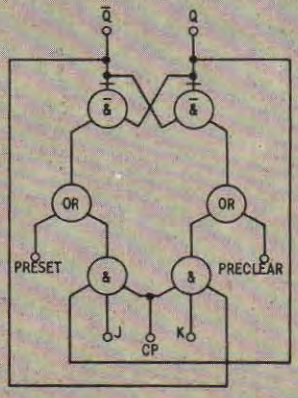

Fig. 2.3c. Simplified logic diagram of a JK bistable

VERSATILE JK

Perhaps it might be as well to consider the way in which the JK has developed to become the "do-anything" device, suitable for use in memory circuits, shift registers, and various forms of counters, used in logic circuitry today.

The simplest form of bistable is the set/reset or latch, which is formed simply from two NAND or NOR gates, as in Fig. 2.3a. The inputs to this circuit must be complementary, and there is no provision for a clock input, so its use is limited and confined to simple memory applications.

The first step in improving the set/reset type is to add AND gates to the inputs, enabling information to be gated in synchronism with a clock pulse, which is common to both gates. The asynchronous inputs of the simple latch can be retained if required by adding an OR gate between the bistable and the AND gates. A circuit of this type is shown in Fig. 2.3b.

This is a useful circuit which may be used in shift registers, but the inputs must still be complementary to ensure proper operation. To enable the circuit to be self-complementing, feedback can be provided from the collector outputs of the bistable to the inputs of the AND gates, ensuring that if two "ones" are present at the inputs of the AND gates, the bistable will change state. This circuit is the basis of the JK flip-flop, and is shown in Fig. 2.3c.

It must be appreciated that this is a simplified representation, and there are some problems which have not been considered in this treatment.

DICE COUNTER

The complete logic system of the electronic dice is shown in Fig. 2.4. A divide by three synchronous counter is made up from the JK flip-flops A and B. The third JK flip-flop C is a divide by two stage. The complete counter conforms to the truth table given in Fig. 2.2.

The decoding of the six separate states of the counter is likely to appear very complicated to those unfamiliar with the "dodges" which are often used in this type of circuitry. A knowledge of Boolean algebra is necessary to design such circuits, but a simple explanation will be given here. By using this in conjunction with the truth table a constructor should be able to sort out exactly what is going on.

The transistors used to drive the bulbs are also used as a form of AND gate. This is possible as a transistor requires both that its base be taken positive, and that its emitter be grounded, before it will turn on, assuming *npn* transistors are used.

Therefore, if we let bistable C control the grounding of the emitters of the bulb drivers, we can see from the truth table that output C is down for three counts. Output $\overline{C}$ is down for the other three counts, enabling the emitters of bulb drivers 1, 2 and 3 to be connected together and ground them through another transistor, whose base is controlled by the $\overline{C}$ output. Drivers 4, 5, and 6 can be similarly controlled by the C output.

Having dealt with the C bistable, A and B can be decoded having gone through two complete counts of three in any count of six. The bases of drivers 1 and 4, 2 and 5, 3 and 6 can be connected together in pairs and driven from the decoded states, which represent the three separate states of bistables A and B.

The decision as to whether 1 or 4, 2 or 5, 3 or 6 is illuminated is carried out by bistable C, switching on only one emitter of each pair.

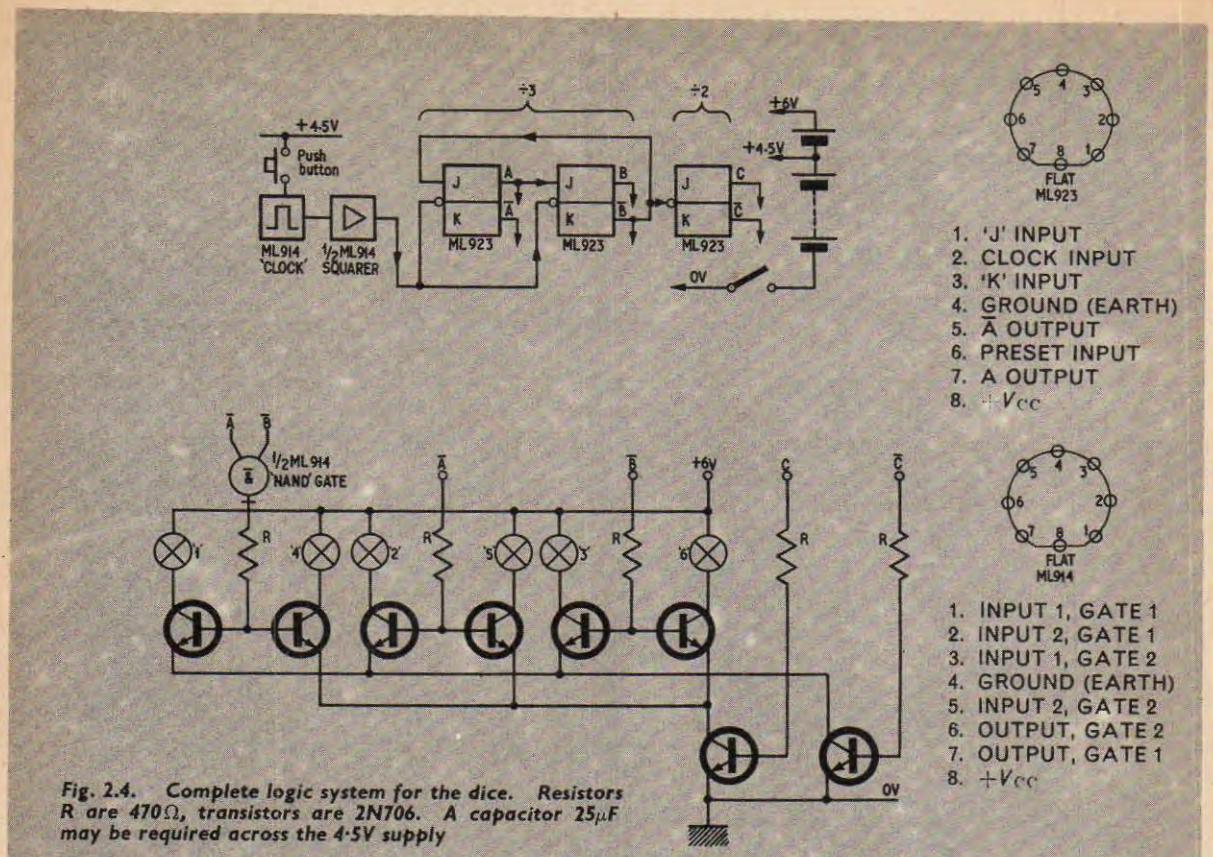

Fig. 2.4. Complete logic system for the dice. Resistors R are 470Ω, transistors are 2N706. A capacitor 25μF may be required across the 4·5V supply

The decoding of each of the three states of A and B is rendered simple by the type of counter employed. The first state has to be described in terms of A and B, but states 2 and 3 are described merely by deciding whether the A output or the B output is "up". A gate is only necessary to decode counts 1 and 4; counts 2 or 5 can be driven by the NOT output of bistable A, as this is positive only during these two states. Similarly, counts 3 and 6 can be driven by the $\bar{B}$ output.

The gate used to decode the first stage of the counter uses half of an ML914, used as a 2-input negative logic NAND gate, its inputs being A and $\bar{B}$, which are both negative at a count of one only.

As a bit of light relief, let us see what has happened to the spare half of the ML914, left over from the decoding circuit. It is in fact being used as an amplifier, with both its inputs connected together, to square up the edges of the clock waveform.

This is necessary, as the JK flip-flop needs a very fast negative edge on the clock input, for it to operate correctly; our clock multivibrator cannot be relied upon to produce such edges.

PRACTICAL DETAILS

This completes the circuit description, except for a few practical details. The supply voltage used poses a bit of a problem, the RTL i.c.s. specified are designed for a supply voltage of 3·6 volts. Since this is not easily obtained from dry batteries, a compromise is used of 4·5 volts, and an extra cell is used to boost this to 6 volts for the bulb circuitry.

The bulbs used must be low consumption types, requiring in the region of 50mA at 6V. Although they will be slightly under-run, due to the saturation voltages of the two driver transistors appearing in series with each of them, this is not a bad thing from the point of view of reliable readout.

The actual layout of the circuit can be safely left to the constructor, as there are no special problems involved, but perhaps a few hints would be useful. There are several kinds of perforated baseboard suitable for the support of this kind of circuit on the market. Veroboard is one which can be used for this particular application.

Using this type of board in the 0·1in matrix size the integrated circuits can be directly inserted, but due to the component density, a good deal of the connections will have to be made using "jumper" wires to realise a compact unit.

The i.c. leads can be left at least ½in long, if desired, but to be sure of re-use of the i.c.s, Lektrokit board can be used. In this case a ring of terminal pins can be used for the i.c.s, which can be mounted upside down on the board, wiring being carried out underneath.

A miniature soldering iron is a virtual necessity when working on this sort of layout, unless the constructor possesses a very steady pair of hands.

The completed unit can be accommodated in a small plastics box, the only controls being the on/off switch, the push button, and a row of six miniature lamp holders.

Next month's article in this series will look into Diode Transistor Logic or DTL.