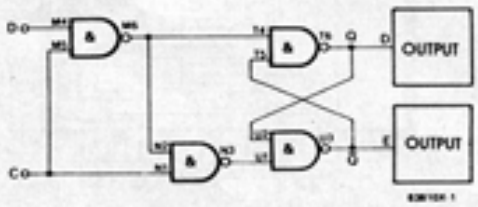
Digi-Course II

Chapter 3

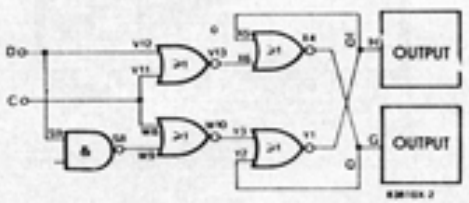
Chapter 2 of our Digi-Course II had described different versions of the set-reset Flipflop. Operation of the D-Flipflop was described in-detail. The gates M and N are wired in such a way that the condition of the C input decides whether or not the input D will be passed on to output Q or blocked. The actual Flipflop part consists of gates T and U.

1



The NOR-version of the D-Flipflop is shown in figure 2. In this circuit, the value present at input D is stored by the Flipflop on the "0" to "1" transition of the signal on the C input.

2



The truth tabe and the timing diagram for the D-Flipflop is given below for reference.

3

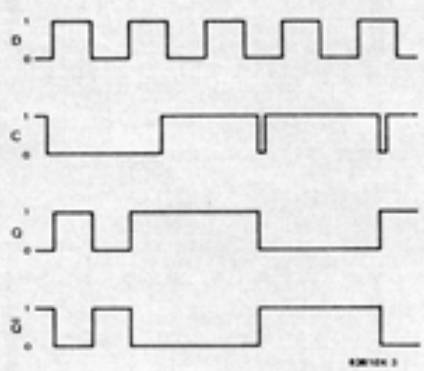


Table 1.

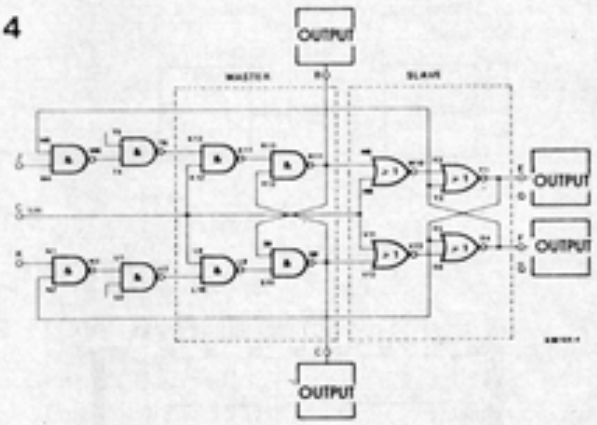
C	D	Q	Q̄
0	0	1	0
0	1	0	1
1	0	0/1	1/0
1	1	0/1	1/0

From the truth table we can see that the Q and $\overline{Q}$ outputs are not the same here, as we had in our original circuit that we started with, in Chapter 1. It is reversed in this case and we interchange Q and $\overline{Q}$.

In practice, this simple D-Flipflop does not meet all the requirement of an advanced design for functioning as a storage element. In the application of Digital technology, storage elements are required which take up and retain information in a precisely defined time frame. In a D-Type Flipflop the moment of storing the input signal level is precisely defined, but before that moment, the output Q takes on all the values that appear at the input.

Practically this problem is solved by using an additional Flipflop. This additional intermediate Flipflop takes on all the values appearing at the input, but passes on the value to the output Flipflop ony when a command to do so is given to it. This combination of Flipflop is called a Master Slave JK Flipflop.

4



The figure 4, given above shows one such complicated circuit. This circuit requires all the gates so far installed on our Digilex Board. The contents inside the dotted rectanles are actually two independent RS Flipflops, with status control. Two output indicators are used for each Flipflop and the conditions of both Master and Slave Flipflops can be seen simultaneously on these LEDs. A logical "1" on the C input (L9) causes all the values at the inputs J and K to be taken up by the first Flipilop.

The second Flipflop reacts only to the values provided by the first Flipflop at the time when input C goes to "0" from "1". The actual response of this circuit can be studied by observing the conditions of the output indicator LEDs B/C and E/F.

The control signal at C (L9) is also called the 'Clock' signal. As the Flipflop reacts only at the moment when input C goes to "0" from "1", it is said to be edge-triggered, triggered by the negative going edge of the input clock. As the edge defines an exact point of time during the sequence of events, this type of arrangement is practically very useful. In the computer technology, mostly the triggering is done on the positive or negative going edge of control signals. Some computers are so fast in operation, the rise time and fall time of the positive or negative going edge also matter and affects the operation.

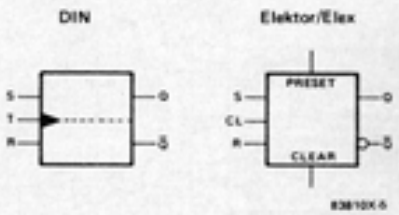
A few trials on the circuit will be enough to clarify the actual operation of the JK Flipflop. The circuit functions properly only when the data remains stable during the clock pulse. For proper operation data must be placed on the inputs before the clock pulse is applied, and should remain unchanged during the clock pulse.

The input conditions 0/0 on J/K do not affect the output, the condition 1/1 on J/K reverses the output conditions on Q/$\bar{Q}$ at every clock pulse.

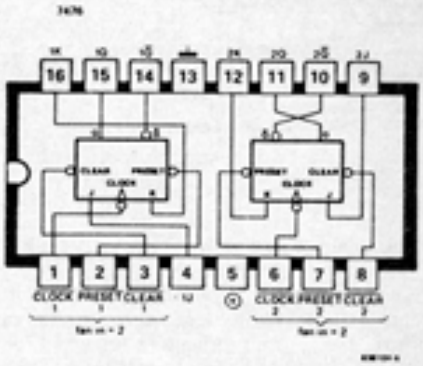
For a practical application, one need not construct the JK Flipflop using so many descrete gates. A single chip containing two such JK Flipflops is commercially available. The number of the TTL IC is 74L576.

The circuit symbols for a Flipflop are shown in figure 5 and the pin diagram and internal connections are illustrated in figure 6.

5



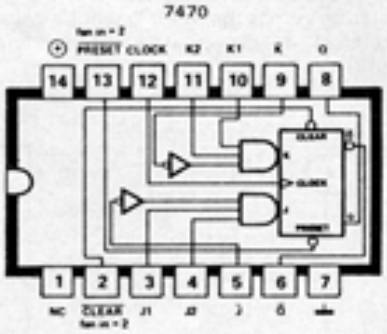
6



In addition to the known inputs J, K and C of our original Flipflop circuit, this IC has two more inputs. $\overline{\text{PRESET}}$ and CLEAR inputs, as their names indicate, are used to Preset or clear the Q output to "1" or "0". The bars on PRESET and CLEAR indicate that the desired effect is achieved when the original on one of these inputs is "0". These ICs can be installed in the sockets (IC & and IC7) provided for them on the Digilex board.

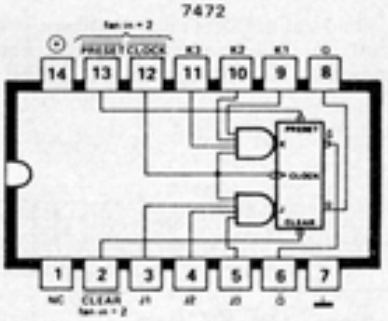
Figure 7 shows the Pin diagrams and internal connections of some other TTL Flipflop ICs.

7470



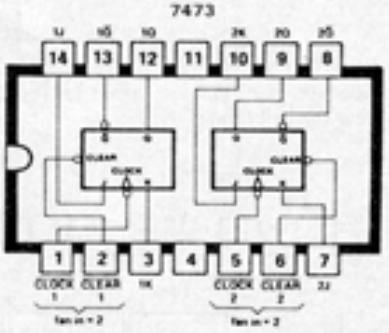
JK Flipflop with three inputs, $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$.

7472



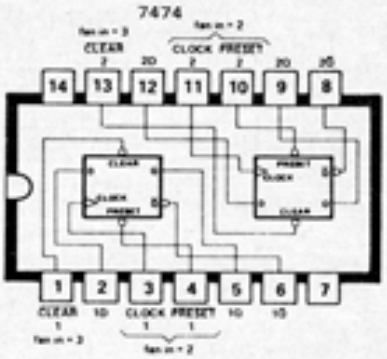
JK Flipflop with three inputs, $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$.

7473



Dual JK Flipflop with only one J/K input and $\overline{\text{CLEAR}}$

7474



Dual-D Flipflop with D input, $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$.