Interconnection of logic elements

The transmission line, t.t.l. and tri-state devices

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This article outlines the concepts required when designing a complex logic system and describes the fundamental principles of connection between basic logic gates.

A digital system is composed of logic gates and interconnections between them. To ensure correct functioning of the system it is important to consider a model of this connection. The simplest case is a logic gate driving another single gate with no fanout as shown in Fig. 1. It is impossible to consider the interconnection without a ground or V_{cc} return path, and when this is present there is a distributed capacitance and inductance which forms a transmission line.

Properties of a transmission line

To characterise a transmission line a step propagating along a two-wire line is considered as shown in Fig. 2. Using Faraday's law of $V = d\phi/dt$ around loop abcd, L is defined as the inductance per unit length of the wire pair so $L = \phi/i$. In time t, the step will advance a distance s so that $s/t = c$ and the change of flux will be $\phi = L\,s\,i$. Substitution into Faraday's law gives the voltage applied to the line to overcome back e.m.f; $V_{AD} = L\,i\,ds/dt = L\,i\,c$. From $Q = VC$, $i = vCc$ where C is the capacitance per unit length of the wire pair, so $c = \pm 1/\sqrt{LC}$ and $v/i = Z_0 = \sqrt{L/C}$. Therefore, a step may propagate in either direction.

The two parameters which characterise a transmission line are the velocity of propagation c, and the impedance Z_0 which relates the voltage difference across the line to the current in the line. Thus, $v = iZ_0$ where Z_0 is a property of the geometry, and medium, μ and ϵ, in which the wires are embedded.

To use the formulae for Z_0 and c it is necessary to calculate L and C for any geometry that may be used. In general it is impossible to solve analytically for L and C and so other methods are used. Values for most practical cases are in the literature. It is common to represent a lossless transmission line as the model shown in Fig. 3 which allows the equations of step propagation to be derived. This method has little to recommend it especially as it appears to lead to a spurious high frequency cut-off. There is, of course, no high frequency cut-off inherent in any transmission line geometry and the only factor which can cause this is a frequency dependent behaviour of the dielectric. If the dielectric is vacuum, there is no frequency dependence and no cut-off.

The sinewave concept can be very misleading in digital electronics and it is invalid to think of a single step as being composed of a superposition of sinewaves. The diagram in Fig. 4 shows a step which is propagating along a transmission line with velocity c ($c = 1/\sqrt{\mu\epsilon}$), the velocity of light in the medium surrounding the conductors. A true sinewave signal is infinite in both time and distance, i.e. it can only exist in an infinitely long transmission line, and any practical situation is an approximation to this ideal. Because the step is travelling at the velocity of light there can be no energy or information ahead of it and there can be no effect at any point P in front of the step. This consideration alone is sufficient to demonstrate that such a step cannot be analysed into a superposition of sine-

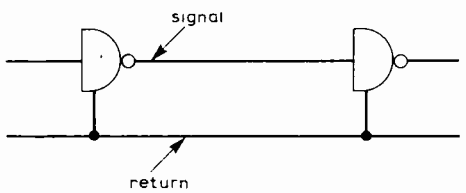
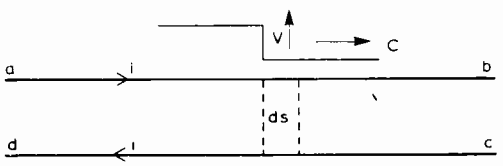


Fig 1. *Simple example of a logic gate driving another gate.*

Fig 2. *A step propagating along a two-wire line.*



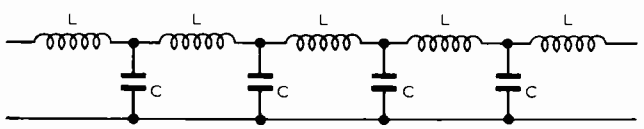
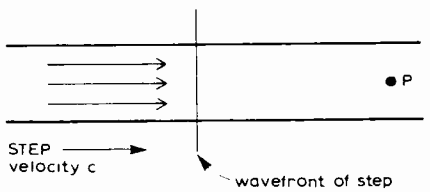


Fig 3. *Model of a lossless transmission line.*

Fig 4. *A simple step should not be considered as a superposition of sinewaves.*



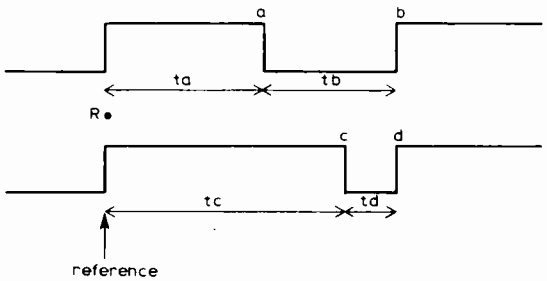


Fig 5. *Two digital signals, illustrating edges as separate events in time.*

waves because these sinewaves would have to exist both ahead of and behind the step. Also, if the transmission lines were cut before the step arrived at P, any effect which was already at P would have to vanish instantaneously, again impossible. Mathematics indicate that if we superpose many sinewaves of appropriate amplitudes and phase relationships we would obtain a step waveform. This is undeniably true but its converse, that we can analyse a step into a superposition of sinewaves, does not follow logically and is in fact not true. The sinewave is responsible for much confusion particularly in the discussion of factors affecting the choice of capacitors for logic decoupling. It is important to remember that a step is a shock wave, formed by a transverse electromagnetic wave front travelling at the speed of light, and all digital signals are combinations of either positive or negative going edges. Any observer can only see the signal as it passes him on the transmission line.

The important parameter of the two digital signals in Fig. 5 is the time delay between the edges. Each edge a, b, c or d must be considered as a separate event in time which is completely unconnected with any other transition. A logic gate connot predict the arrival of any edge until the shock wave actually arrives. It then responds to the amplitude of the signal and by the time the next shock wave arrives it has settled down to the steady state condition.

Transistor transistor logic

Before discussing t.t.l. circuits it is worth considering the evolutionary process which lead up to them. In early d.t.l., transistors were only capable of sustaining a 1mA collector current which resulted in the circuit arrangement shown in Fig. 6 where a 10kΩ resistor was used in the collector. One problem with this circuit is its inability to drive stray capacitance. Consider the output waveform in Fig. 7 which is obtained when a pulse is applied to the input. The transistor switches on and the stray capacitance is discharged through the saturated transistor to produce a rapid falling edge. When the transistor switches off it cannot supply current so the stray capacitance charges through the 10kΩ resistor to produce an exponential rise which corresponds to a time constant of RC. Therefore, this type of gate is not very good at driving long signal lines. In practice the load is not strictly capacitive, but is a transmission line with a characteristic impedance of around 100Ω. However, in this case because R is much greater than 100Ω it makes very little difference and the slow edge masks any transmission line effects.

Logic designers attempted to circumvent this problem by using a "push-pull" output stage to give rapid transitions in both directions as shown in Fig. 8. Here the output is driven by a "phase splitter" so that while the top transistor

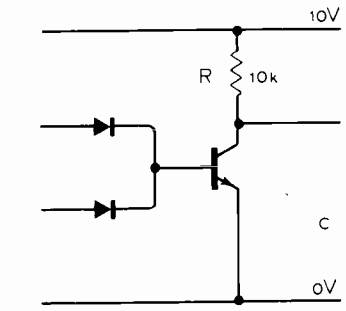


Fig 6. *Early form of logic, diode-transistor logic.*

Fig 7. *Output waveform from d.t.l. in Fig 6.*

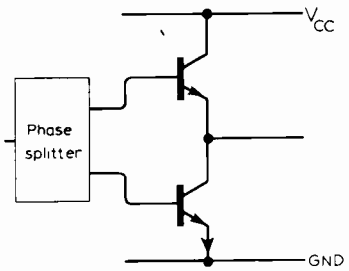


Fig 8. *Push-pull output stage to give rapid transitions.*

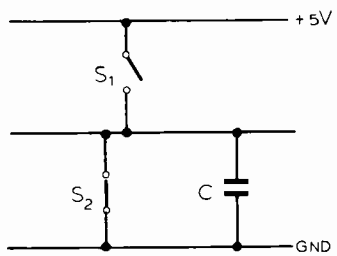


Fig 9. *Basis of t.t.l. circuit required to drive a capacitive load.*

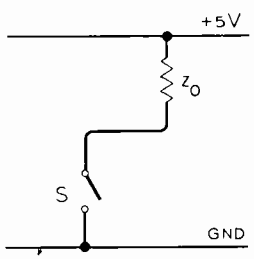


Fig 10. *Only one switch required for a resistive load.*

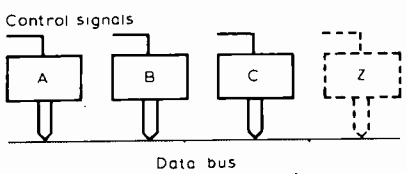


Fig 11. *Tri-state devices connected to a bus.*

is on the bottom one is off and vice versa, but in practice there is an overlap of a few ns. This causes a low impedance across the supply rails which produces a current spike. This type of output was used in the unpopular 73 series of logic. The final step in the evolution of t.t.l. was the insertion of a series limiting resistor in the collector of the upper transistor.

Unfortunately, during the evolution of t.t.l the way impedance levels and device speeds have changed has not been considered fully. While d.t.l. worked initially with a 10kΩ output impedance we now have t.t.l. devices with an internal pull-up resistor of around 100Ω. This means that the transmission line behaviour cannot now be ignored. In fact, when the connection to a t.t.l. device is considered as a transmission line the upper transistor in the output is redundant and serves no useful purpose. A capacitive load requires a circuit as shown in Fig. 9 because, to produce a voltage across the capacitor, a charge must be fed into it via S_1. Discharge of the capacitor must take place through S_2. As already mentioned, a t.t.l. gate must drive a transmission line with an impedance of about 100Ω. The current and voltage are related by $V = iZ_0$ where V is the voltage applied to the line and i is the resulting current. In this case the load is essentially resistive and only one switch is required as shown in Fig. 10. When S is closed the output is low and when it is open the output is high. If the interconnection is terminated with a resistor $R = Z_0$, effects due to stray capacitance and inductance will not affect the output rise or fall times. Therefore, under certain conditions the t.t.l. "push-pull" configuration is unnecessary and an open collector gate will suffice.

Tri-state devices

Common data-bus structures are widely used in mini computer systems but because conventional t.t.l. cannot be wire-ORed it cannot be used. To overcome this limitation tri-state devices have been produced and are rapidly becoming standard components for bus drivers and memory outputs. A tri-state device has an additional control input which determines whether or not the device is enabled. When enabled, its outputs are in the high or low states as normal. When disabled, its outputs assume the high-impedance or off state and the device behaves almost as though its outputs are disconnected from the package pins. In this system only the device which is driving the bus is enabled, so active pull-up is achieved with the benefits of wire ORing. However, even with these apparent advantages it must be considered whether tri-state t.t.l. is necessary and desirable.

With regard to its necessity, the answer is definitely no. Any function which is possible with tri-state devices can be implemented more simply with

open-collector t.t.l. Tri-state is an unfortunate development caused by a misunderstanding of the requirements for transmission line driving. The answer is also no for desirability because it has a failure mode which can lead to the progressive collapse of all the tri-state devices driving a bus. For example, in Fig. 11 if device A becomes enabled at the wrong time due to a fault in the circuitry it could place all lows on a bus to which another device is quite legitimately outputting all highs. This leads to catastrophic power dissipation in the good device and the process can then repeat until all of the devices are destroyed. For the Ti 74365 hex bus-driver, power dissipation in this failure mode can be calculated as follows. The output short-circuit current is specified as 40-130mA so the power dissipation per gate for a 15V rail will be between 0.2 and 0.65W, and the total dissipation for a package of six gates will be 1.2 to 3.9W. The quiescent power dissipation of 0.3 to 0.4W per package means that the total worst case figure is 4.3W. This is about ten times the rated dissipation of a d.i.p. and will destroy the device. □

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