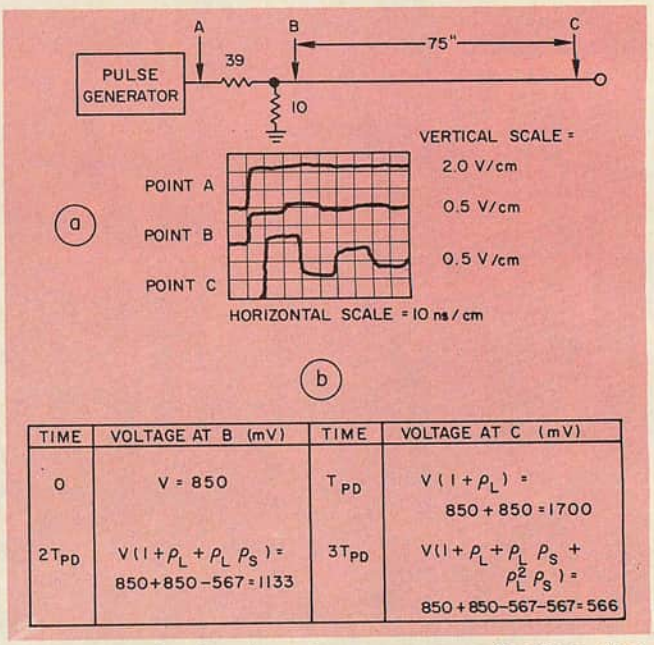
Improve fast-logic designs. Terminated lines reduce reflections to overcome line-length and fanout limitations. Crosstalk and noise are restricted, too.

Designers faced with the fairly restrictive rules on line lengths and fanouts for today's high-speed, emitter-coupled logic (ECL) families might conclude that they really can't use the speeds available—gate propagation delays of 2 ns and less. But it's possible to design a high-speed ECL digital system without restrictions on interconnection line lengths or fanout. And the same techniques can be used to restrict crosstalk and system noise to limits well below the tolerance levels of the circuits. The trick is to use transmission lines with parallel terminations that minimize reflections.

Actually every signal path connecting any two integrated circuits is already a transmission line, with such properties as characteristic impedance and propagation delay. The length of the line and propagation delay relate to the amount of ringing, or noise, that occurs on a line for a given signal rise time. Characteristic impedance is important because it appears as a load to the driving circuit and can be used to determine optimum line termination.

When the propagation delay time exceeds the signal rise time, the line appears as a resistive load to the driving circuit. The value of this load equals the characteristic impedance and is independent of the capacitive loading at the end of the line. For shorter lines, the driving circuit sees a combination of the characteristic impedance and the line load. The effect of the line impedance on the driving circuits lasts only for the duration of the initial signal and any following reflections. After the signal has stabilized to a dc level, the circuit does not see the line impedance and drives only the dc load added to the line.



TIME	VOLTAGE AT B (mV)	TIME	VOLTAGE AT C (mV)
0	V = 850	T_{PD}	$V(1+\rho_L) =$ 850 + 850 = 1700
$2T_{PD}$	$V(1+\rho_L+\rho_L\rho_S) =$ 850+850−567 = 1133	$3T_{PD}$	$V(1+\rho_L+\rho_L\rho_S+\rho_L^2\rho_S) =$ 850+850−567−567 = 566

1. **Changes in line impedance cause reflections** that result in ringing, as seen in a simple test setup simulating an ECL gate driving a 75-inch line (a). The amplitudes of the reflections are calculated in b.

Cause of reflections

Reflections on a conductor result when the signal on the line sees a change in line impedance. The test circuit and waveforms in Fig. 1 show the effects of such reflections. In the circuit, a high-speed pulse generator drives a 75-inch line. The 39-Ω and 10-Ω resistors together approximate the 50-Ω load required by the pulse generator. The 10-Ω resistor simulates the low output impedance of a high-speed ECL driving circuit. A 75-inch line gives a 10-ns propagation time, so that reflections can be easily observed. Nothing happens at the receiving end of the line, point C, until one propagation time (one oscilloscope division) after the signal is sent from point B.

As the signal travels down the line, a current flows in the line equal to the signal amplitude divided by the line's characteristic impedance. When this current reaches the far end of the line, it sees an open circuit, with the result that all the current reflects back toward the sending end. This reflection causes the voltage at the receiving end of the line to double. Hence the signal at point C is twice as large as that at point B.

Two propagation delays later the reflected signal returns to point B and is seen as the small step in the point-B waveform. The step is

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small because the 10-Ω resistance is much smaller than the 50-Ω line impedance.

A second reflection results that is equal to the difference between the small signal at point B and the initial reflection from point C. This reflection is seen at point C three propagation delays after the initial signal.

These reflections bounce back and forth, getting smaller as they progress, and cause ringing. As shown in Fig. 1, ringing consists of a series of square waves. However, it normally appears as a decreasing sine wave, because usually the driving signal has slower rise times, the line is shorter and the oscilloscope sweep speed is slower.

Use reflection coefficients

Reflection coefficients are used to determine reflection amplitudes on a signal line. The reflection coefficient at the receiving, or load end, of the line, ρ_L, depends on the line's characteristic impedance and the load resistance at the end of the line:

$$\rho_L = \frac{R_L - Z_o}{R_L + Z_o}.$$

For the example, in Fig. 1, where the open-circuit load impedance is extremely large, the reflection coefficient is approximately 1. The reflection coefficient at the sending end of the line, ρ_S, is a function of the line's characteristic impedance and the output impedance of the driving circuit. Its value is found to be $\rho_S = (10 - 50)/(10 + 50) = -0.67$. With these reflection coefficients, the reflection amplitudes given in Fig. 1b are calculated.

A common method to control ringing limits the length of the signal line. Reflections then occur during the rise time of the driving signal and are of reduced amplitude. For acceptable design performance, limit the line length so that propagation delay is one-half the signal rise time or less.

This technique is known as designing with short lines,[1] in which a short line length, ℓ, is defined by its maximum value

$$\ell_{max} \leq t_R/2t_{PD},$$

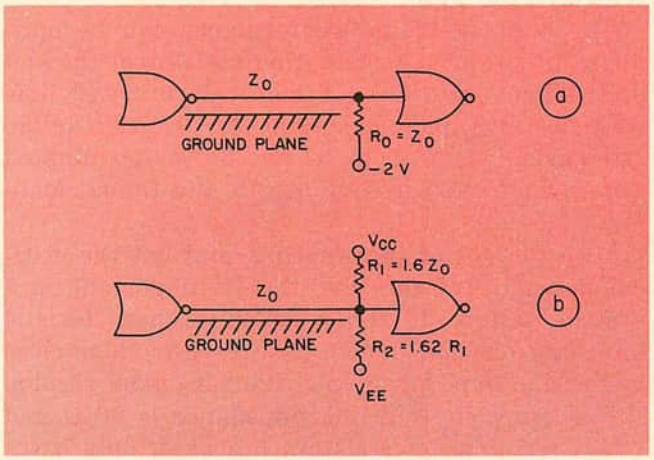
where t_R = rise time of the logic family and t_{PD} = propagation delay per unit length.

Fanout loads decrease line lengths

Since the propagation time of a line increases with capacitive loading, the maximum line length becomes shorter as fanout load is increased. With ECL 10,000 edge speeds—typically 3.5 ns from 10 to 90%—the maximum line length with the short-line method of design is normally between four and nine inches, depending on line impedance and fanout. Many of the recommended wiring rules suggested for high-speed logic are based on short-line design techniques.

The key to controlling reflections without line-length and fanout restrictions is the elimination of the first reflection at the load end of the line. If the reflection coefficient at the load end of the line, ρ_L, were zero, there would be no reflections and hence no waveform distortion. To achieve a reflection coefficient of zero, it's necessary to match the line's characteristic impedance with a resistance load at the end of the line. Methods for terminating a signal line when using high-speed ECL circuits are shown in Fig. 2.

All ECL 10,000 and MECL III circuits are specified with 50-Ω loads, both for dc logic levels and ac performance.[2] When the circuits are used in the conventional manner—positive ground on V_{CC} and −5.2 V dc on V_{EE}—the 50-Ω load is terminated to a −2-V-dc supply called V_{TT} or termination voltage. When operating from a



2. **Terminations can eliminate reflections.** The possible termination techniques include resistor $R_O \approx Z_O$ connected to a termination voltage (a) or the use of an equivalent resistor network (b).

+5-V-dc supply, V_{TT} should be +3 V dc. Or termination may be accomplished with an equivalent resistor network (Fig. 2b) if use of a separate V_{TT} supply is not practical.

The 50-Ω load specification for high-speed ECL —a worst-case specification—does not preclude using the logic with higher impedance lines. Many systems are designed in the 75-to-100-Ω impedance range for manufacturing convenience and lower system power. For such cases, improvements in waveshapes can be obtained by using proper termination-resistor values.

The results of using a ground plane and a termination are shown in Fig. 3. An ECL-10,000 gate drives an eight-inch unterminated line on a circuit board without a ground plane (Fig. 3a). The fanout is one gate at the end of the line. The upper waveform corresponds to the end of the line and the input to the receiving gate; the lower trace corresponds to the output of the receiving gate.

Because of the absence of a ground plane, the

line impedance is high (> 150 Ω) and somewhat undefined along the path. The waveform at the end of the line has excessive ringing, with the result seen at the output of the receiving gate. Although the circuit is functioning, the ringing significantly exceeds recommended design limits.

Ground plane reduces ringing

With a ground plane beneath the eight-inch line (Fig. 3b), characteristic impedance becomes a well-defined 75 Ω. Thus loading has less of an effect on the line, and faster signal propagation speed can be obtained. The result: much less ringing at the end of the line, even though the line is not terminated. The amplitude of the ringing represents a conservative short-line design, and no ringing couples into the output of the receiving gate.

The eight-inch line performance can be optimized by use of a termination resistor at the end of the line (Fig. 3c). With the terminated line, no reflections and no ringing occur. And unlike the waveforms of Figs. 3a and 3b the terminated line is unaffected by line length and fanout loading.

It is the act of terminating, and not the critical matching of the line, that is important in a system design. If the exact line characteristic impedance is not known, any resistor value close to the line impedance will give very good results.

For example, if a line impedance is 90 Ω and 100-Ω termination resistors are used, only 5.3% of the signal would be reflected. This would cause a small signal overshoot that would not affect system operation and that would be much preferred to the 100% reflection of an unterminated line.

Terminated lines increase speed

In addition to controlling ringing, the use of low-impedance transmission lines can lead to faster system performance. The effects of fanout loading on propagation delay time is a function of the line characteristic impedance. The amount of current flowing in a signal line determines the time it takes to charge any stray or fanout-load capacitance. And a high-impedance line conducts less current than a low-impedance line for a given signal amplitude.

The propagation delay time of a loaded line, T_{PD}', may be expressed as

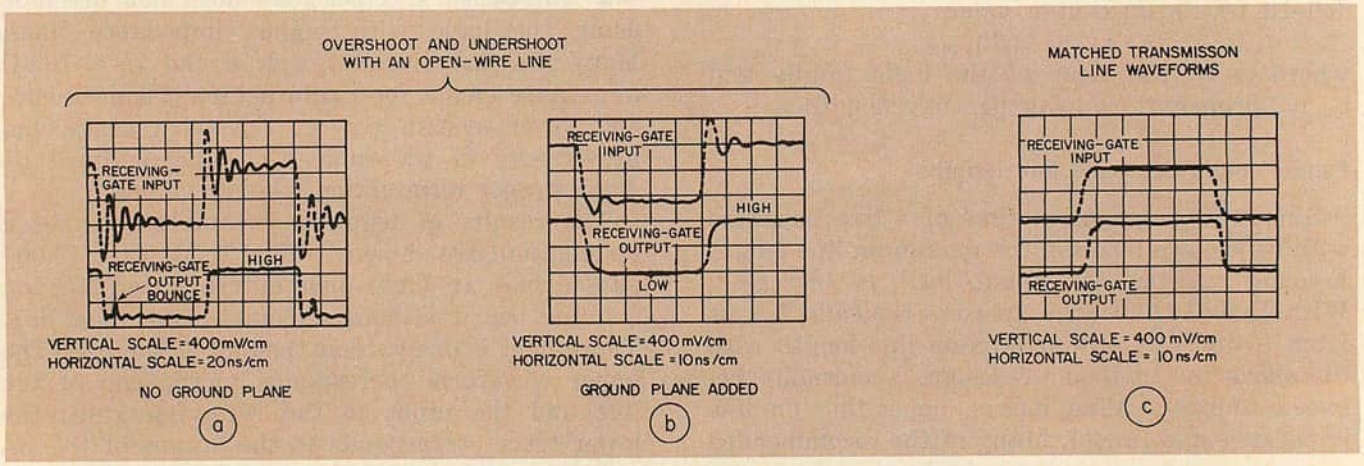
$$T_{PD}' = T_{PD}\sqrt{1 + \frac{C_D}{C_o}},$$

where T_{PD} is the unloaded line speed (about 0.15 ns per inch for a circuit-board line), C_D is the distributed load capacitance on the line (about 3 pF per ECL-10,000 fanout) and C_o is the intrinsic capacitance of the line (about 150 L/Z_o, where L is the line length in inches).

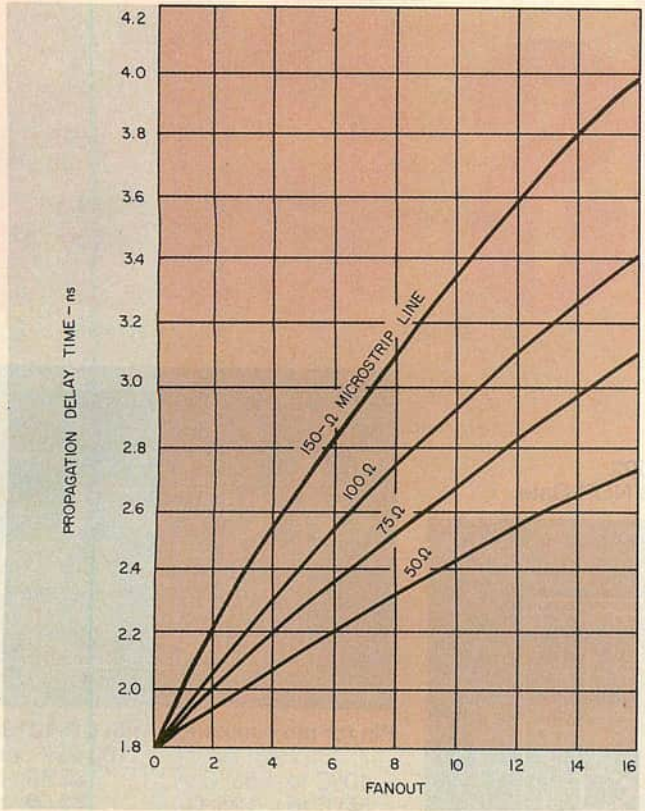
Calculations of loaded line speed illustrate the performance gain when designing the low-impedance transmission lines. A six-inch, 50-Ω line on a circuit board, for example, would have a propagation delay time of 1.27 ns when loaded with a fanout of 6. A similarly loaded six-inch, 150-Ω line would have a 1.8-ns propagation delay. This small speed difference is more than one-fourth of a gate delay and represents a 30% improvement in wire-propagation delay time.

The line-propagation delay times for 12-inch microstrip lines, as functions of fanout loading and line impedance, are shown in Fig. 4. The use of low-impedance lines can have a significant effect on over-all system speed when all the line delays are added together.

In many designs the conversion to transmission-line operation is easy. Very good microstrip interconnections are formed simply by the addition of a ground plane to a standard circuit board. Added to a system backplane, the ground plane provides point-to-point interconnections with a characteristic impedance between 80 and 130 Ω, and they can be terminated. Moreover Wire-Wrap interconnections can still be used



3. **Waveforms show reduced ringing** when a ground plane is used (a and b). Further improvements are obtained when the line is terminated with a resistor (c). This case eliminates ringing as well as reflections.



4. **Low-impedance lines also result in reduced delay times,** or higher speeds. Curves show the propagation time for a 12-inch lump-loaded microstrip line as a function of fanout.

with the fast edge speeds of ECL-10,000.[3]

For longer interconnections, ribbon cable or twisted-pair lines can be used. If every other wire in a ribbon cable is grounded or ribbon cable with a ground shield is used, the cable has a defined characteristic impedance (about 75 Ω) that can be terminated for signal integrity. Twisted-pair lines can be operated differentially with ECL gates and line receivers and have high-noise immunity over long distances.

Usually the hardware of a transmission-line system remains the same as that for a lower-speed system. But the system grounding is more carefully designed, resulting in greatly reduced crosstalk amplitudes. Crosstalk energy is coupled into the ground plane rather than into an adjacent signal line. Tests have shown that without a ground plane crosstalk on a circuit board is 2-1/2 times larger than on a similar board with a ground plane.

Finally, when designing with transmission lines, a system can be completely characterized on paper. ■■

References

1. *MECL System Design Handbook*, Motorola, Inc., 1971.

2. *MECL Integrated Circuits Data Book*, Motorola, Inc., 1972.

3. "Interconnection Techniques for Motorola's MECL 10,000 Series Emitter Coupled Logic," *AN-556* Motorola, Inc., 1972.