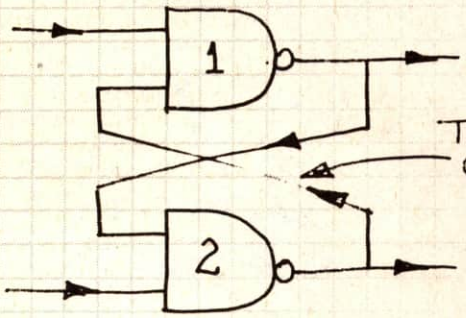
FLIP FLOPS

THE FLIP FLOP WAS INTRODUCED IN FRAMES 17 TO 21 AND THEY SHOWED HOW A NOR GATE & NAND GATE COULD BE WIRED TO PRODUCE A FLIP FLOP.

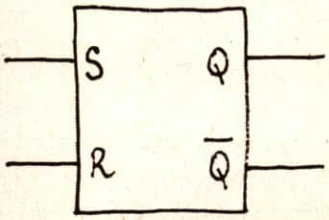
A FLIP FLOP IS AN IMPORTANT BUILDING BLOCK AS IT IS A BASIC STORAGE CELL — IT HAS A MEMORY.

IN THIS SECTION WE WILL EXTEND FLIP FLOP THEORY AND INTRODUCE SPECIALIZED TYPES OF FLIP-FLOPS.

A FLIP FLOP CAN BE MADE FROM 2 NAND GATES OR 2 NOR GATES FIRSTLY WE WILL DISCUSS THE NAND GATE FLIP FLOP.



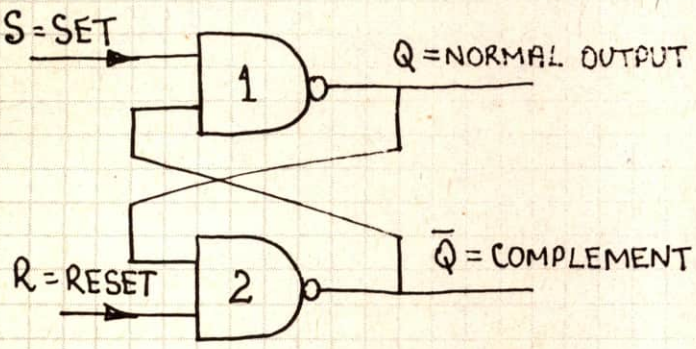
NAND FLIP FLOP



R-S FLIP FLOP

THE 2 GATES ARE WIRED SO THAT EACH OUTPUT FEEDS INTO ONE INPUT OF THE OPPOSITE GATE.

THE INPUT & OUTPUT LINES ARE IDENTIFIED WITH LETTERS:

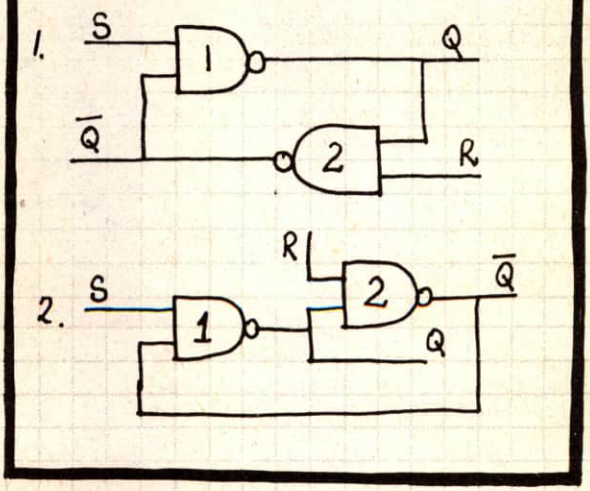


A FLIP-FLOP HAS ONLY 2 STABLE STATES

1. GATE 1 ON: GATE 2 OFF.
2. GATE 1 OFF: GATE 2 ON.

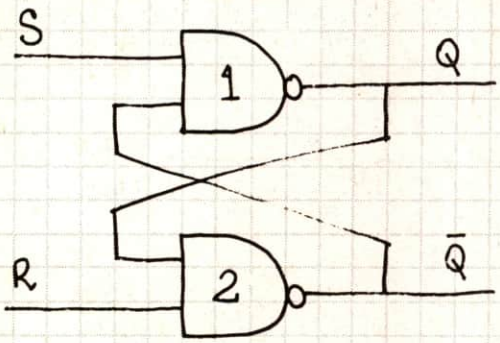
DURING THESE STATES THE FLIP FLOP IS CAPABLE OF STORING A PIECE OF BINARY INFORMATION.

2 OTHER WAYS OF DRAWING A FLIP FLOP:



IN ONE OF THE STATES THE FLIP FLOP WILL STORE A BINARY 1 & IN THE OTHER STATE IT WILL STORE A BINARY 0. IT WILL HOLD THIS INFORMATION AS LONG AS THE POWER IS APPLIED TO THE AND GATES.

THE SIMPLEST TYPE OF FLIP FLOP IS THE LATCH. WE WILL DRAW THE LATCH WITH THE CROSS-COUPLING LINES TO SHOW HOW BOTH GATES ARE INTER-CONNECTED.



A SIMPLE LATCH.

THE LATCH HAS 2 INPUTS, LABELED S FOR SET & R FOR RESET. THE S INPUT IS USED TO SET THE LATCH & THUS STORE A BINARY 1, IN THE FLIP FLOP.

THE R INPUT IS USED TO RESET THE FLIP FLOP & THUS STORE A BINARY 0.

THESE LETTERS GIVE THE FLIP FLOP ITS MOST COMMON NAME:
RS FLIP FLOP [FOR RESET-SET FLIP FLOP]

THE OUTPUT ARE LABELED Q & $\bar{Q}$ (Q-BAR OR Q COMPLEMENT) AND REFER TO THE NORMAL OUTPUT (Q) AND THE COMPLEMENT OUTPUT ($\bar{Q}$)

THE VALUE STORED IN THE FLIP FLOP IS GIVEN BY THE READING ON THE NORMAL OUTPUT.

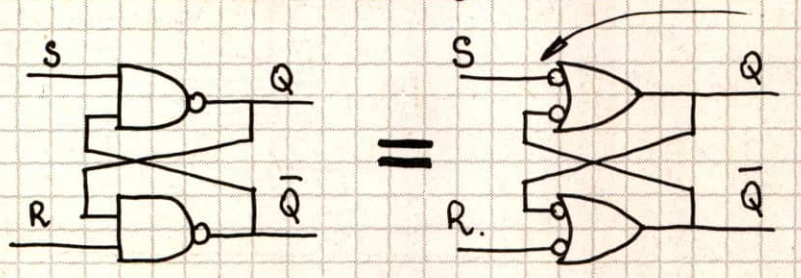
THE $\bar{Q}$ IS AN OUT-OF-PHASE VALUE & IS USED WHEN DESIGNING COMPLEX LOGIC DIAGRAMS. IT CAN, HOWEVER, BE USED TO DETERMINE THE STATE OF THE FLIP FLOP:
IF $\bar{Q}$ IS HIGH (BINARY 1) THE FLIP FLOP IS RESET.
IF $\bar{Q}$ IS LOW (BINARY 0) THE FLIP FLOP IS SET.

THE MAIN FEATURE OF A NAND GATE IS THIS! THE OUTPUT GOES LOW WHEN BOTH INPUTS ARE HIGH. THIS MEANS THE LOW IS THE CONTROLLING INFLUENCE FOR A NAND GATE FLIP FLOP AND EACH GATE REQUIRES A LOW FOR ITS STATE TO CHANGE.

NAND

INPUTS		OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

FROM THE ARTICLE ON "BUBBLES" WE CAN REDRAW THE NAND GATE FLIP FLOP AS DUAL NEGATED INPUT OR GATES:

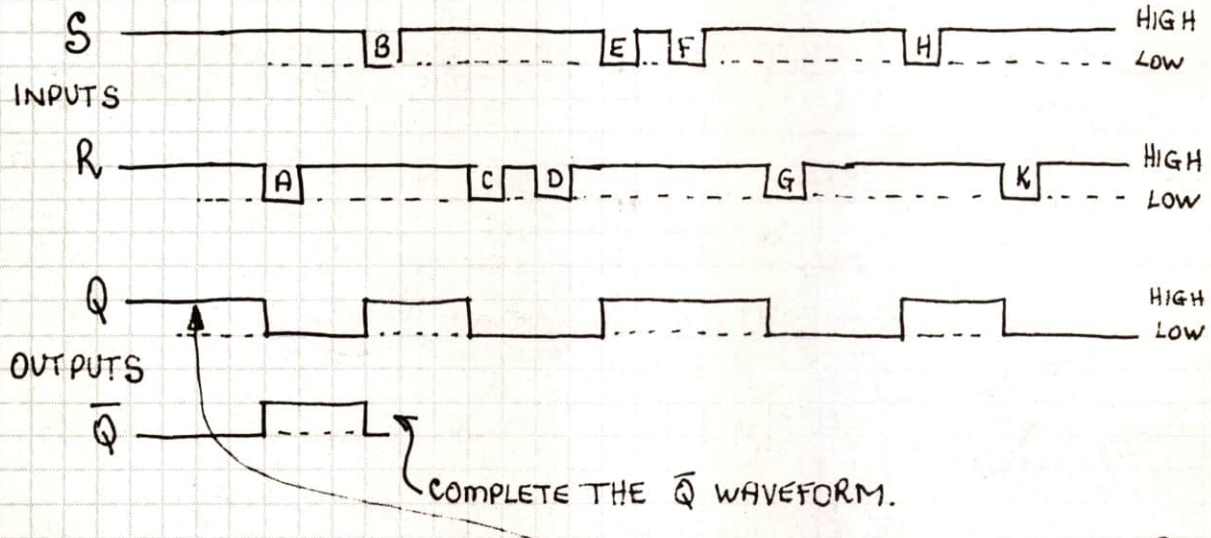


THIS BUBBLE INDICATES THE GATE IS ACTIVE WHEN THE INPUT LINE IS LOW.

THIS WILL HIGHLIGHT THE FACT THAT A LOW IS REQUIRED TO CHANGE THE STATE OF A NAND GATE R-S FLIP FLOP

A LOW ON THE S INPUT WILL SET THE FLIP FLOP.
A HIGH ON THE S INPUT WILL DO NOTHING AS THE INPUT IS ONLY ACTIVATED BY A LOW SIGNAL (THAT IS A SIGNAL CHANGING FROM A HIGH VALUE TO A LOW VALUE)
A LOW ON THE RESET LINE WILL RESET THE FLIP FLOP & THIS LINE CANNOT SET THE FLIP FLOP BY GOING HIGH. ONLY LOWS ACTIVATE THE FLIP FLOP

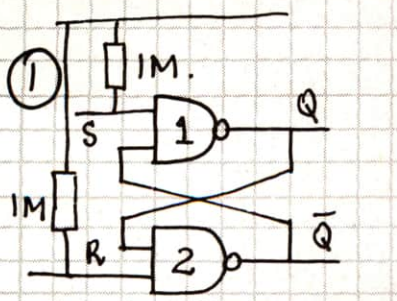
THE FOLLOWING DIAGRAM SHOWS HOW THE FLIP FLOP RESPONDS TO THE INPUT PULSES: THE FLIP FLOP IS INITIALLY SET (IN OTHER WORDS IT IS PRODUCING A HIGH ON OUTPUT Q).



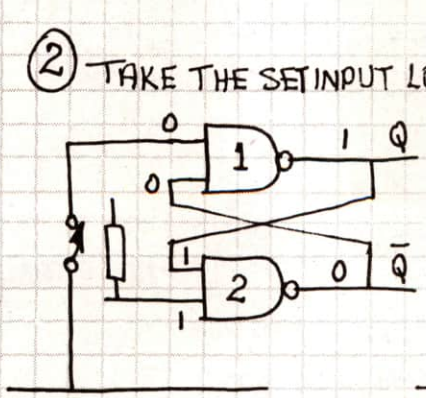
THE FLIP FLOP IS INITIALLY SET? THE LOW ON THE RESET LINE AT A RESETS THE F-F. THIS CONDITION CONTINUES UNTIL THE SET PULSE B IS RECEIVED TO SET THE F-F. RESET PULSE C RESETS THE F-F & PULSE D HAS NO EFFECT AS IT IS ALSO A RESET PULSE. PULSE E SETS THE F-F & PULSE F IS ALSO A SET PULSE AND DOES NOT ALTER THE F-F. PULSE G RESETS THE F-F AND PULSE H SETS IT AGAIN. FINALLY PUSE K RESETS F-F.

THIS SIMPLE TYPE OF FLIP FLOP SUFFERS FROM ONE TYPE OF PROBLEM WHICH WE HAVE NOT SHOWN IN THE ABOVE DIAGRAM.

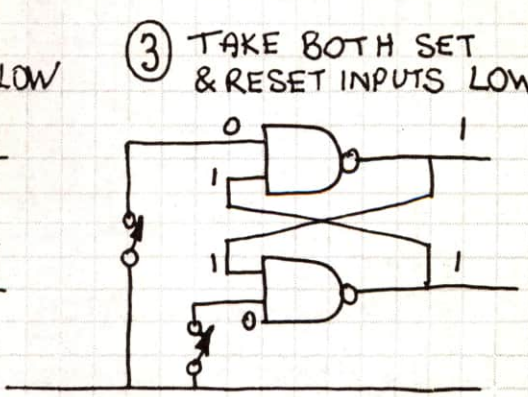
FOLLOW THROUGH THESE DIAGRAMS AND SEE THIS LIMITATION:



THE INPUTS ARE NORMALLY HIGH & WE HAVE ASSUMED THE FLIP FLOP IS IN THE RESET STATE



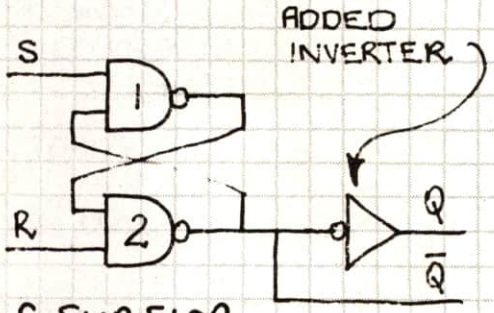
FLIP FLOP 1 IS SET AND THE NOMAL OUTPUT IS HIGH.



BOTH OUTPUTS GO HIGH!

IF BOTH INPUTS ARE TAKEN LOW, THE OUTPUTS PRODUCE A HIGHLY UNDESIRABLE CONDITION. THEY BOTH BECOME HIGH! WE LOSE OUR FEATURE OF Q & $\overline{Q}$ BEING COMPLEMENTARY & WE MUST INTRODUCE MEASURES TO AVOID THIS SITUATION.

THIS THIRD CONDITION IS CALLED "LIMBO" & ONE METHOD OF ELIMINATING IT IS TO PLACE AN INVERTER ON ONE OF THE OUTPUTS. THIS ENSURES THE Q & $\overline{Q}$ WILL BE COMPLEMENTARY EVEN WHEN BOTH INPUTS GO LOW. THE INVERTER CAN BE ADDED TO EITHER Q OR $\overline{Q}$ OUTPUT WITH THE SAME RESULT.



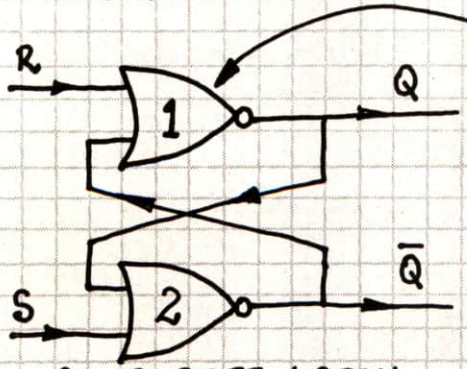
SUMMARY OF THE NAND LATCH – ALSO R-S FLIP FLOP

INPUTS		OUTPUTS		
SET	RESET	Q	$\overline{Q}$	
0	0	1	1	PROHIBITED OR LIMBO CONDITION
0	1	1	0	SET CONDITION
1	0	0	1	RESET CONDITION
1	1	X	$\overline{X}$	THE X MEANS EITHER SET OR RESET & THE $\overline{X}$ MEANS RESET OR SET.

THIS IS A LOW TO THE SET LINE

THIS IS A LOW TO THE RESET LINE

A SECOND TYPE OF R-S FLIP FLOP CAN BE CONSTRUCTED WITH NOR GATES. IT OPERATES IN A SIMILAR MANNER EXCEPT THAT IT REQUIRES A HIGH ON THE SET OR RESET LINES TO CHANGE THE STATE OF THE FLIP FLOP.



A NOR-GATE LATCH.

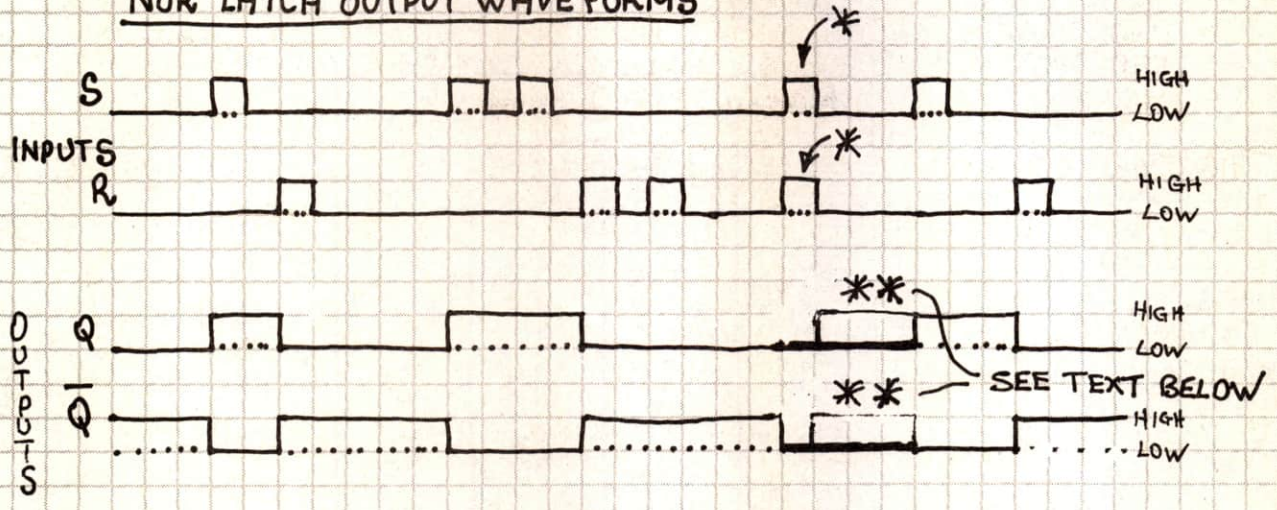
NOR

INPUTS		OUTPUT
0	0	1
0	1	0
1	0	0
1	1	0

TRUTH TABLE - NOR GATE

THE FIRST POINT TO NOTE IS THE LABELING OF THE R&S LINES. THEY ARE IN REVERSE TO THE NAND FLIP FLOP. IN THE NOR LATCH A HIGH ON THE SET LINE WILL PRODUCE A HIGH ON THE Q OUTPUT. A HIGH ON THE RESET LINE WILL PRODUCE A LOW ON THE Q OUTPUT.

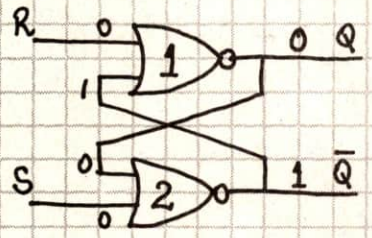
NOR LATCH OUTPUT WAVEFORMS



* THE TWO PULSES OCCUR ON THE SET & RESET LINES AT THE SAME TIME. THE RESULT IS THE Q & $\bar{Q}$ OUTPUTS GO LOW AT THE SAME TIME TO PRODUCE THE UNWANTED RESULT WE DISCUSSED PREVIOUSLY. THIS IS THE ONE LIMITATION OF THE R-S LATCH & INTRODUCES THE NEED FOR AN IMPROVED LATCH.

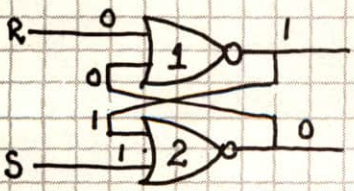
** THE UNWANTED STATE ABOVE IS SHOWN IN THE OUTPUT BY **. AFTER THE SET & RESET PULSES GO LOW TOGETHER, A RACE OCCURS IN THE FLIP FLOP FOR THE FIRST OUTPUT TO GO HIGH. THIS COULD BE EITHER THE NORMAL OR COMPLEMENTARY OUTPUT. THIS UNKNOWN STATE CAN BE CLEARED UP BY PROVIDING A SET PULSE OR RESET PULSE, AFTER WHICH THE LATCH FUNCTIONS PREDICTABLY.

(1) THE NOR LATCH CAN START UP IN ANY STATE WHEN BOTH INPUTS ARE LOW. — ASSUME IT STARTS UP RESET.

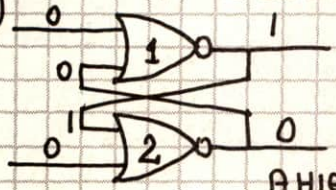


THE "0's" & "1's" ARE HIGHS & LOWS.

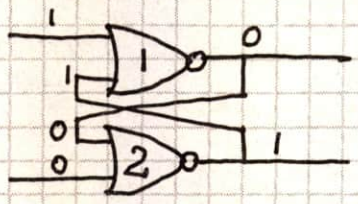
(2) A SET PULSE WILL SET THE FLIP FLOP:



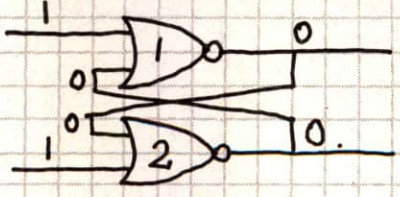
(3) REMOVING THE SET PULSE WILL NOT AFFECT THE F-F BECAUSE THE FEEDBACK FROM THE Q OUTPUT TAKES OVER WITH A HIGH INTO F-F #2.



(4) A RESET PULSE (HIGH) WILL RESET THE FLIP FLOP.

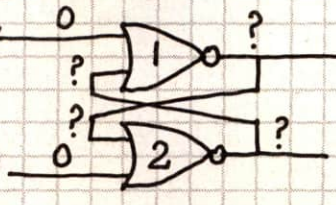


(5) IF THE RESET PULSE REMAINS & A SET PULSE IS APPLIED:



BOTH OUTPUTS GO LOW!

(6) IF BOTH S&R PULSES ARE REMOVED TOGETHER, A RACE EXISTS FOR THE FIRST OUTPUT TO GO HIGH — & EITHER CAN GO HIGH.



SUMMARY OF THE NOR LATCH (R-S FLIP FLOP)

A HIGH ON THE RESET LINE

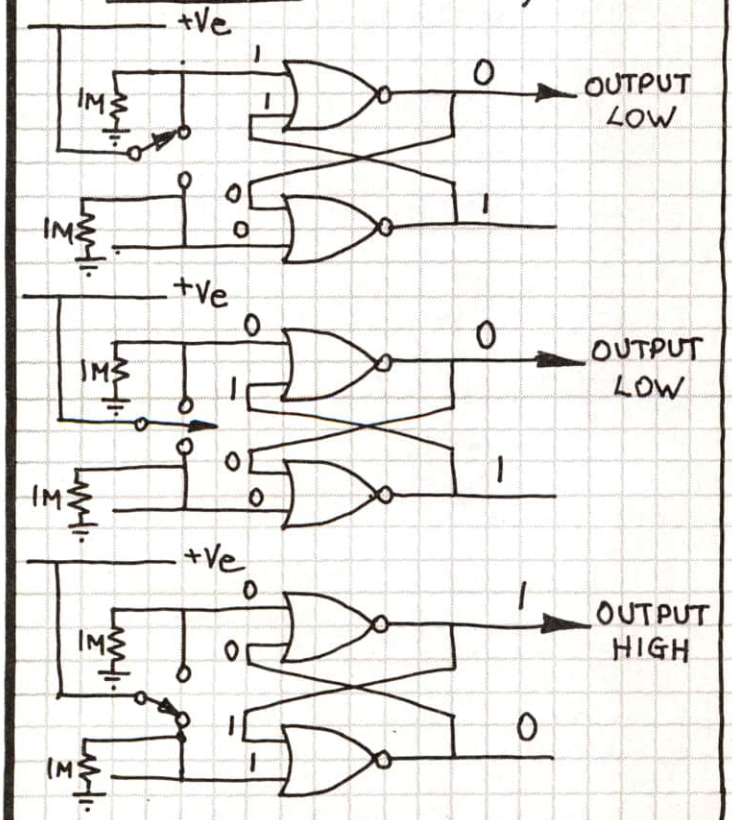
A HIGH ON THE SET LINE.

INPUTS		OUTPUTS		
SET	RESET	Q	$\overline{Q}$	
0	0	X	$\overline{X}$	— EITHER SET OR RESET
0	1	0	1	— RESET CONDITION
1	0	1	0	— SET CONDITION
1	1	0	0	— UNDESIRABLE CONDITION.

DEBOUNCING A SWITCH

THE NAND & NOR LATCHES CAN BE SUCCESSFULLY USED AS DEBOUNCE CIRCUITS FOR MECHANICAL SWITCHES. THE IMPORTANT FEATURE OF THESE CIRCUITS IS THE FACT THAT THEY DO NOT CHANGE STATE WHEN THE SWITCH IS OPENED BUT ONLY ON CLOSING THE CONTACTS.
NEITHER DOES IT CHANGE STATE ON RE-CLOSING THE CONTACTS BACK TO THE SAME GATE.

NOR LATCH — (CD4001)



NAND LATCH — (½ CD 4011)