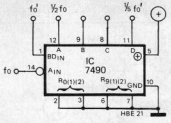
66

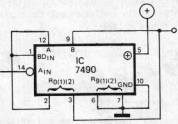


division by 2,5 and 10

The 7490 contains two independent (except for reset function) counters, a divide-by-two (flip-flop) and a divide-by-five counter. These may be used separately, or cascaded to form a divide-by-ten counter.
For use as a divide-by-two counter, the input count is fed into input A (pin 14) and the output is taken from output A (pin 12). For a divide-by-five counter the input is to pin 1, and a binary output sequence is obtained at pins 8, 9 and 11.

There are two methods of connecting the IC as a divide-by-ten counter. The divide-by-two counter may be connected before the divide-by-five counter (pins 12 and 1 linked, and the input connected to pin 14). In that case a BCD count sequence is obtained at pins 8, 9, 11 and 12, in accordance with the truth table. If a symmetrical square-wave output is required for frequency synthesizer or other applications then the divide-by-two stage is connected after the divide-by-five stage. In that case input BD (pin 1) receives the input count. The D output (pin 11) is connected to input A (pin 14) and the symmetrical square-wave output is obtained from the A output (pin 12).
In order for the counter to function the reset 0 and reset 9 inputs (pins 2, 3, 6 and 7) must be grounded.

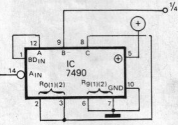
67



division by 3

For division by 3 the counter must reset to 0 when the BCD output is 3 (i.e. 0011). The counter is therefore connected in the BCD (non-symmetrical) divide-by-ten mode, but the reset 0 inputs (pins 2 and 3) are connected to the A and B outputs, pins 12 and 9 respectively. The reset 9 inputs remain grounded. Asymmetric divide-by-three output, pin 9.

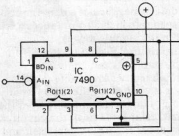
68



division by 4

Division by 4 requires the counter to be reset to 0 when the output reaches 4 (BCD 0100). The reset 0 inputs are thus both connected to the C output (pin 8). On the fourth count pulse output C will momentarily become '1', but the counter will then immediately reset to zero. Asymmetric divide-by-four output, pin 9.

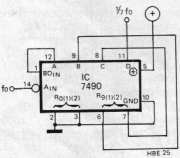
69



division by 6

As with division by 3 and by 4, the DCBA output of a 7490 can be exploited to give a reset to 0000 at every sixth count. The binary output at this count is DCBA = 0110; i.e. C and B are both '1' for the first time. Outputs B and C are thus connected to pins 2 and 3 respectively. Asymmetric divide-by-six output, pin 8.

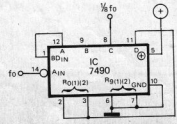
70



division by 7

Since in BCD code 7 is 0111 it is impossible to provide a reset every 7 input pulses using only the 2 reset 0 inputs, since using only 2 of the bits in the code would lead to confusion with 3, 6 or 5. It is, however, possible to achieve a divide-by-seven function, though not with a BCD output sequence. Use is made of the reset 9 inputs, and the reset 0 inputs are grounded. The C and B outputs are connected to pins 6 and 7 respectively. The counter will now count 9, 0, 1, 2, 3, 4, 5, 9, 0 . . . . and so on. An asymmetric divide-by-seven output may be obtained from either output C or output D.

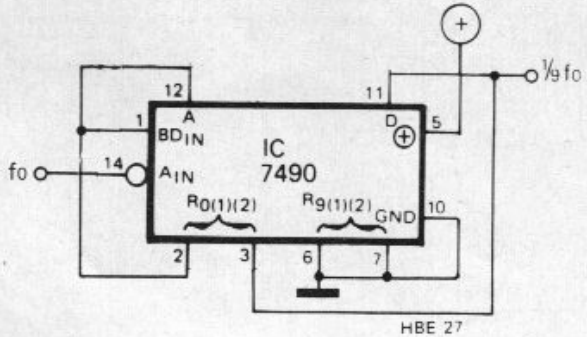
71



division by 8

This simply entails connecting output D (pin 11) to the reset 0 inputs. Asymmetric divide-by-eight output from output C.

72



division by 9

Since the BCD code for 9 is 1001 outputs A and D must be connected to pins 2 and 3 respectively. Asymmetric divide-by-nine output from output D.

73

use of 7493 instead of 7490

The 7493 may be use for division ratios up to 16 since it contains a divide-by-two and a divide-by-eight counter. The pin connections are identical to those of the 7490 except that no reset 9 inputs are provided. The following additional division ratios can be obtained with no external gating.

Division by 12

Outputs C and D connected to the reset inputs, pins 2 and 3 respectively. Asymmetric divide-by-twelve output, pin 11.

Division by 16

Counter connected as for 7490 in divide-by-10 mode.