TTL decade counter divides by any integer

In many applications a pulse train must be divided by a fixed integer. For example, digital clocks often divide the line frequency by 50 to obtain a 1Hz output, and time-base generators divide a crystal oscillator frequency down to several stable low frequency outputs. If the integer is 10 or less, just one 7490 TTL decade counter can handle the division.

Usually frequency division in TTL circuits is accomplished by using binary counters and logic gates. To divide by

OPERATION OF 7490 IC AS A DIVIDE-BY-N COUNTER

DIVISOR N	INPUT PIN No.	OUTPUT PIN No.	EXTERNAL CONNECTIONS
2	14	12	PIN 2 OR 3 LOW
3	1	8	PIN 8 TO PIN 2 PIN 9 TO PIN 3
4	1	8	PIN 11 TO PINS 2 AND 3
5	1	11	PIN 2 OR 3 LOW
6	14	8	PIN 12 TO PIN 1 PIN 9 TO PIN 2 PIN 8 TO PIN 3
7	1	12	PIN 11 TO PIN 14 PIN 12 TO PIN 2 PIN 9 TO PIN 3
8	14	8	PIN 12 TO PINS 1 PIN 11 TO PINS 2 AND 3
9	14	11	PIN 12 TO PINS 1 AND 2 PIN 11 TO PIN 3
10	14	11	PIN 12 TO PIN 1 PIN 2 OR 3 LOW

N—i.e., to get one output pulse for every N input pulses—the logic gates are connected so that the counter is reset when the Nth pulse is counted. The most significant bit is used as the output, because it makes the high-to-low clocking transistion only once for every N input pulses. If it is necessary to have an output pulse of a specific length, then a monostable may be triggered when the Nth pulse is detected.

The disadvantage of this division technique is that even for divisors less than 10, two ICs are required, a binary counter and a gate. But a pulse train can be divided by any integer between 2 and 10 by use of just one 7490 TTL decade counter IC, owing partly to its divide-by-2 and divide-by-5 stages and partly to its internal ANDed reset, which lets it reset only when both pin 2 and pin 3 are high.

The counter can be made to reset on any count from 2 to 10 by appropriate connections of the pins. The necessary interconnections for each value of N are shown in the table. For example, if division by 7 is desired, the 7490 is wired as shown in the figure. The input and output pulse trains for this configuration are also shown. If a larger division is required, it is only necessary to cascade several stages together, provided the divisor has factors that are all less than 10.

(By T. Durgavich and D. Abrams, in "Electronics").