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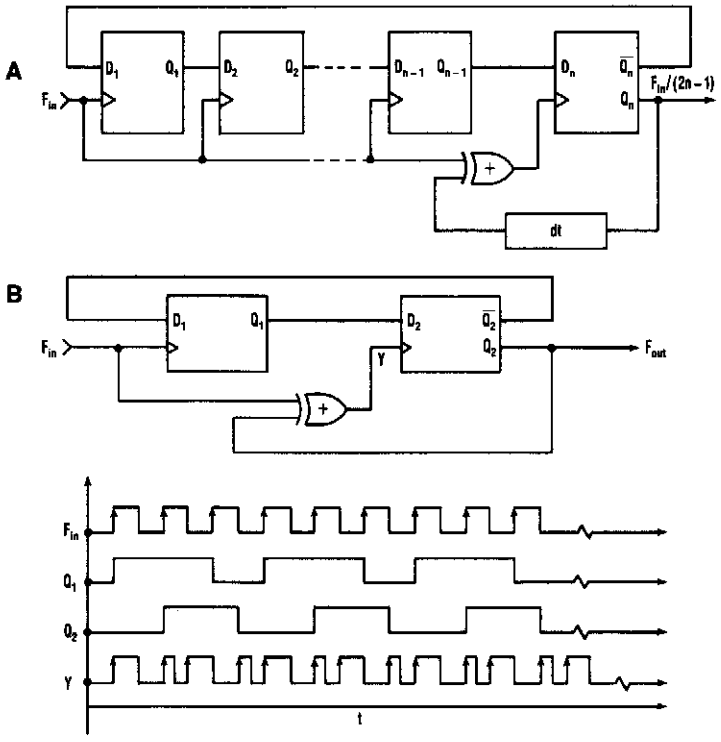
Dividers

The sources of the following circuits are contained in the Sources section, which begins on page 665. The figure number in the box of each circuit correlates to the entry in the Sources section.

Clock Input Frequency Divider
Programmable Frequency Divider
Divide-by-Odd-Number Counter
7490 ÷ N Circuits
Divide-by-2-or-3 Circuit
1+-GHz Divide-by-N Counter
Divide-by-$N+1/2$ Circuit

CLOCK INPUT FREQUENCY DIVIDER



1. THE INPUT CLOCK frequency fed into this circuit is divided by 2n – 1. The circuit consists of n clocked flip-flops and one exclusive-OR gate. The dt delay is zero in most cases.

2. THIS CIRCUIT CONFIGURATION divides the input frequency by three (a). The circuit's timing diagram verifies the division (b).

ELECTRONIC DESIGN

Fig. 26-1

ICA, R1 through R3, and Q1 form a current source. The current that charges C1 is given by:

$$I = \frac{(V_D \times R_1)}{(R_1 + R_2) \times R_3}$$

$$= \frac{(15 \times 3\ \text{k}\Omega)}{(3\ \text{k}\Omega + 12\ \text{k}\Omega) \times 470\ \text{k}\Omega}$$

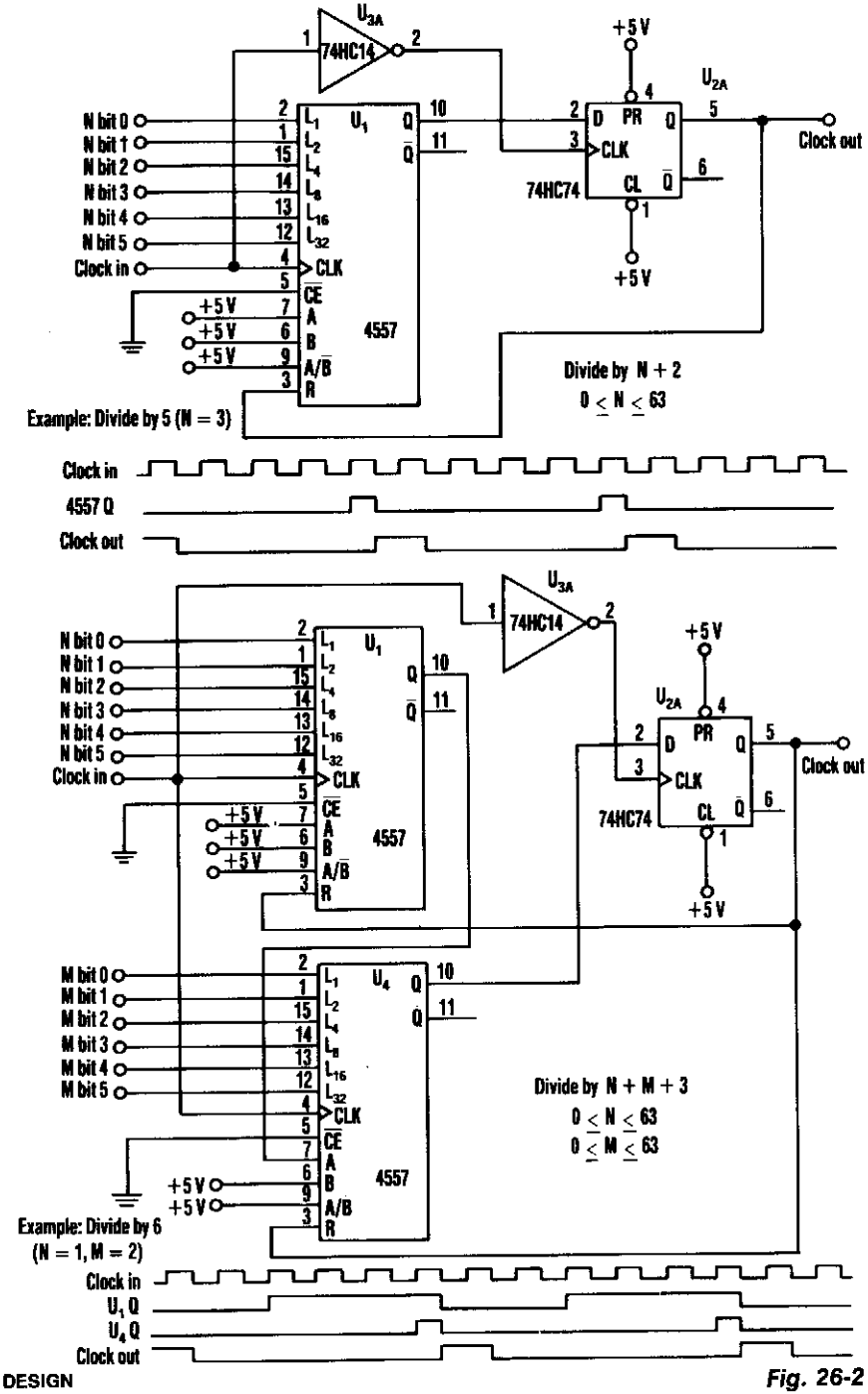
$$= 6.4\ \mu\text{A}$$

The input signal drives ICD. Because ICD's positive input (V+) is slightly offset to +0.1 V, its steady-state output will be near +13 V. This voltage is sent to ICC through D2, setting ICC's output to +13 V. Therefore, point D is cut off by D1, and C1 is charged by the current source. Assuming the initial voltage on C1 is zero, the maximum voltage (VC_{max}) is given by:

$$tw_{clk} > tp_{ff} + dt + tp_{xr} + tw_{ff}$$

The right side of the inequality should be the minimum pulse width (either up time or down time) of the input clock. The circuit, when constructed with standard 74F-type parts, operates without any added delay in the exclusive-OR feedback path and with an input frequency of up to 22.5 MHz. The circuit's output signal will have the same duty cycle as the input clock.

PROGRAMMABLE FREQUENCY DIVIDER



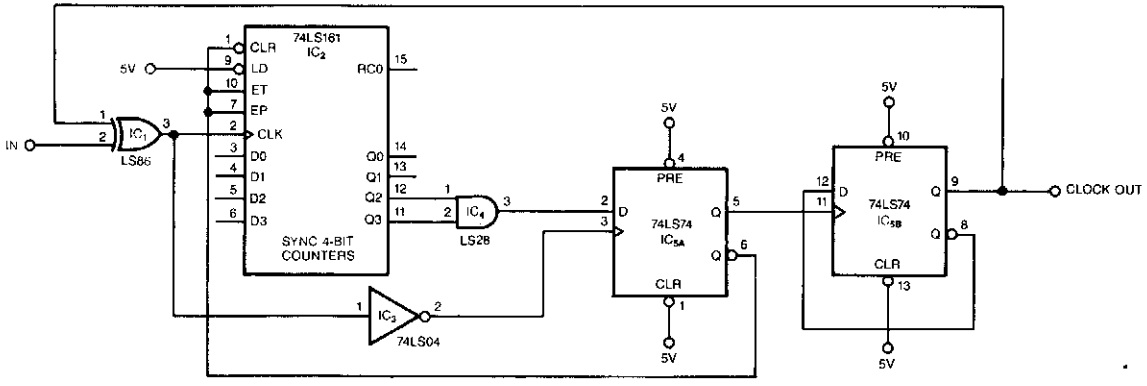
ELECTRONIC DESIGN

Fig. 26-2

PROGRAMMABLE FREQUENCY DIVIDER (*Cont.*)

This divider uses a variable-length shift register, a type-D flip-flop, and an inverter. The clock feeds the flip-flop clock input and the output of the shift register feeds the D input of the flip-flop. The FF output is tied back to the reset input of the shift register so that each clock pulse shifts a "1" into the 4557. $N+1$ cycles after the reset pulse is removed. The first "1" will propagate through the register output. The "1" is latched into the FF on the clock's next falling edge and fed back to the 4557 reset pin, which resets the shift register to zero. When a zero is clocked into the flip-flop on the next falling clock edge, the reset is removed, restarting the process. The divide ratio is $(N+2)$, where N = the binary number that is programmed into 4557.

DIVIDE-BY-ODD-NUMBER COUNTER



EDN

Fig. 26-3

This circuit symmetrically divides an input by virtually any odd number. The circuit contains $n+1/2$ clocks twice to achieve the desired divisor. By selecting the proper n, which is the decoded output of the 74LS161 counter, you can obtain divisors from 3 to 31. This circuit divides by 25; you can obtain higher divisors by cascading additional LS161 counters.

The counter and IC5A form the $n+1/2$ counter. Once the counter reaches the decoded counts, n, IC5A ticks off an additional 1/2 clock, which clears the counter and puts it in hold. Additionally, IC5A clocks IC5B, which changes the clock phasing through the XOR gate, IC1. The next edge of the input clocks IC5A, which reenables the counter to start counting for an additional $n+1/2$ cycles.

Although the circuit has been tested at 16 MHz, a worst-case timing analysis reveals that the maximum input frequency is between 7 and 8 MHz.

7490 ÷ *N* CIRCUITS

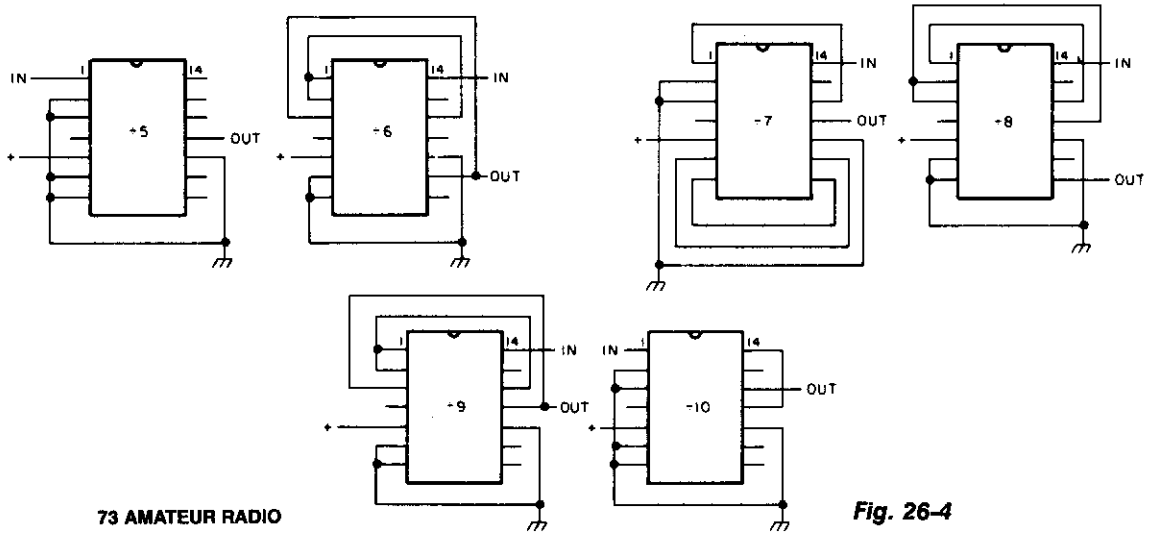


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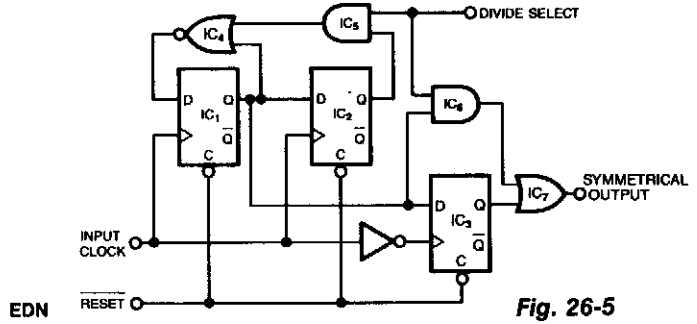
Fig. 26-4

A 7490, 74LS90, 74C90, etc., is a decode divider, but it can be configured to divide by any *N* up to 10. The above figures illustrate the connections necessary to divide by *N* from 5 to 10.

DIVIDE-BY-2-OR-3 CIRCUIT



EDN

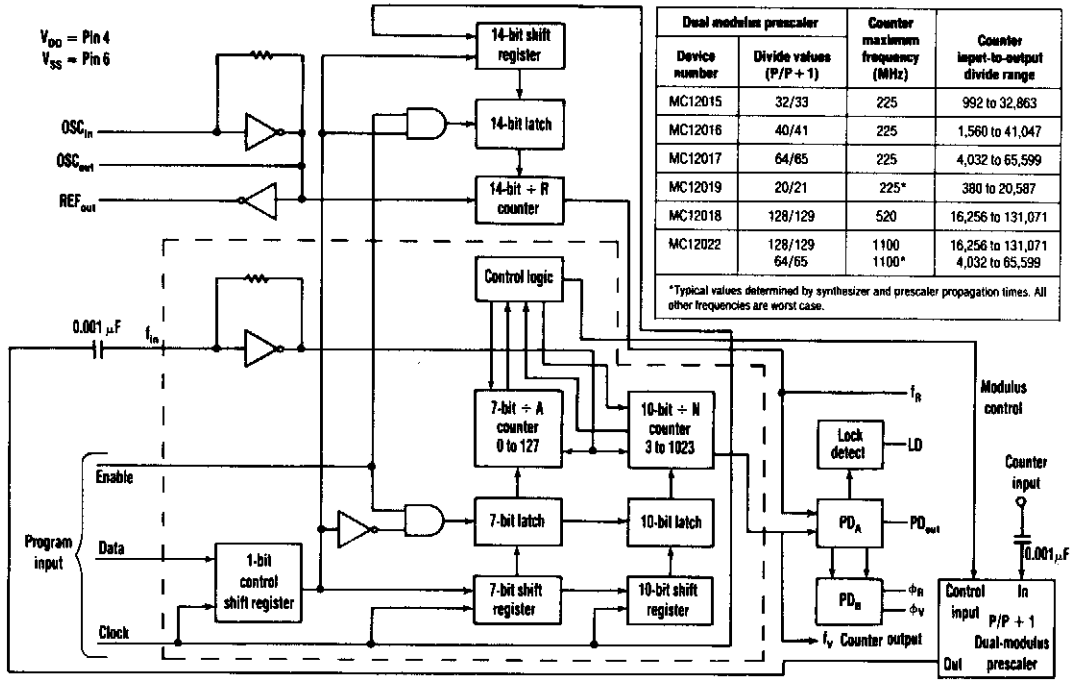
Fig. 26-5

This circuit produces a symmetrical waveform when dividing by either 2 or 3. The Divide Select input controls the division factor. When Divide Select is high, flip-flops IC1 and IC2, along with associated gates, form the classical divide-by-3 circuit.

When divide select is low, however, the output of the AND gate, IC5, goes low. Consequently, the NOR gate, IC4, inverts the feedback signal and passes it to the D input of the flip-flop, IC1. Now, IC1 acts like a toggle flip-flop and produces a divide-by-2 output.

IC3, which is, in effect, a negative-edge-triggered flip-flop, provides symmetrical output signals. When you select division by 2 (Divide Select is low), the output and AND gate IC6 is low, and IC3 simply clocks out the divider's output, delayed by one clock period. When you set Divide Select high, the path to the output through the AND and OR gates, IC6 and IC7, is enabled. This path means that the output goes high on the leading edge of IC3's input (not its output) and produces a symmetrical divide-by-3 output.

1 + -GHz DIVIDE-BY-*N* COUNTER



Dual modulus prescaler		Counter maximum frequency (MHz)	Counter input-to-output divide range
Device number	Divide values (P/P + 1)		
MC12015	32/33	225	992 to 32,863
MC12016	40/41	225	1,560 to 41,047
MC12017	64/65	225	4,032 to 65,599
MC12019	20/21	225*	380 to 20,587
MC12018	128/129	520	16,256 to 131,071
MC12022	128/129 64/65	1100 1100*	16,256 to 131,071 4,032 to 65,599

*Typical values determined by synthesizer and prescaler propagation times. All other frequencies are worst case.

ELECTRONIC DESIGN

Fig. 26-6

Counter speeds for CMOS- and TTL-programmable counters are limited to under 100 MHz. ECL-type devices can approach a few hundred MHz, but with significant current requirements. However, coupling the dual-modulus-prescaling technique with the available phase-locked-loop synthesizer chips that control the prescaler circumvents these frequency and power-drain constraints.

With this approach, designers can also choose various counter-programming schemes (serial, parallel, or data bus), in addition to achieving higher frequency capabilities. Low-power drain (less than 75 mW) and low-cost devices can also be selected. Moreover, only two ICs are necessary to achieve divide values above 131 000.

Maximum input frequency and dividing range for the counter are controlled by choosing an appropriate 8-pin dual-modulus prescaler. The counter's output appears at synthesizer pin F_V (see the figure). The total input-to-output divide value is governed by the equation:

$$N_{TOTAL} = N \times P + A$$

N and A represent the value programmed through the serial port into the divide-by-N and divide-by-A counters. P is the lower dual-modulus value that is established by the synthesizer's modulus-control signal.

Typically, A varies from zero to $P-1$ to achieve steps within the system's divide range. N must be equal to or greater than A. $N>A$ then sets a lower limit on N_{TOTAL}, which is dictated by $A_{MAX}=P-1$.

DIVIDE-BY-$N+1/2$ CIRCUIT

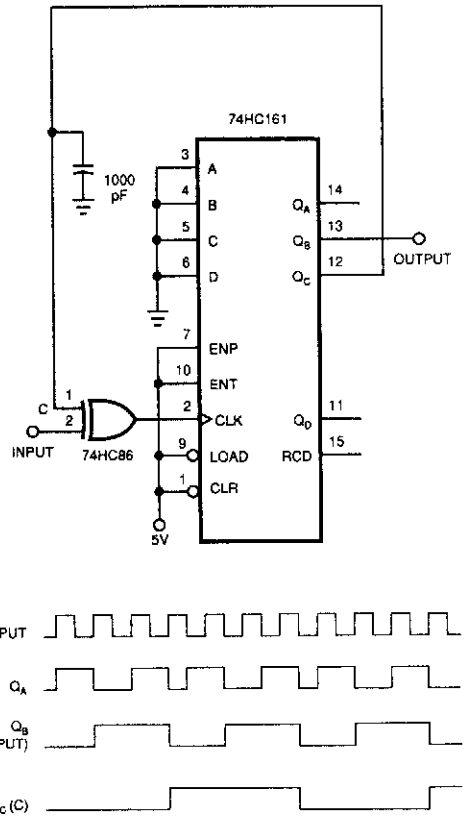


Table 1—XOR feedback signals for N+½ divider

Divide number	Feedback signal(s)			
N = 1.5	Q_1			
N = 2.5	Q_0	Q_2		
N = 3.5	Q_2			
N = 4.5	Q_0	Q_3		
N = 5.5	Q_0	Q_1	Q_3	
N = 6.5	Q_1	Q_3		
N = 7.5	Q_3			
N = 8.5	Q_0	Q_4		
N = 9.5	Q_0	Q_2	Q_4	
N = 10.5	Q_0	Q_1	Q_2	Q_4
N = 11.5	Q_0	Q_1	Q_4	
N = 12.5	Q_1	Q_4		
N = 13.5	Q_1	Q_2	Q_4	
N = 14.5	Q_2	Q_4		
N = 15.5	Q_4			
N = 16.5	Q_0	Q_5		
N = 17.5	Q_0	Q_3	Q_5	
N = 18.5	Q_0	Q_2	Q_3	Q_5
N = 19.5	Q_0	Q_2	Q_5	
N = 20.5	Q_0	Q_1	Q_2	Q_5

EDN

Fig. 26-7

This circuit, instead of dividing by an integer, divides the input signal by $N+1/2$. With the feedback connections exactly as the figure shows, the circuit divides by 3.5. Point C ultimately controls when the input clocks the 74HC161 4-bit counter. When $C=0$, the positive edge of the input triggers the counter. If $C=1$, the negative edge of the input triggers the counter. Each time that point C changes level, the circuit shortens the output pulse width of the counter by half of an input cycle. Thus, the counter's divisor depends on how many changes occur at point C during one output period.

Although the figure divides by 3.5, feeding back different counter outputs produces different divisors. Generally, an m-bit binary counter with pure exclusive-OR (XOR) feedback can form an $N+1/2$ counter, where N ranges from $2^{m-2}+1/2$ to $2^{m-1}-1/2$. The divided output is available at the m-1 bit of the counter.