S/PDIF-to-TTL-Converter

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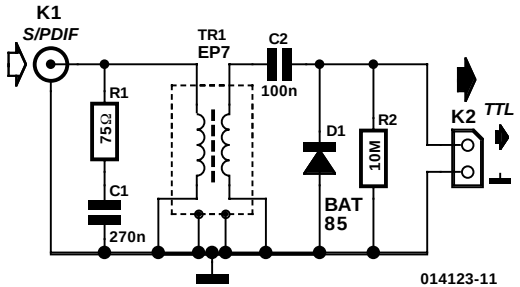
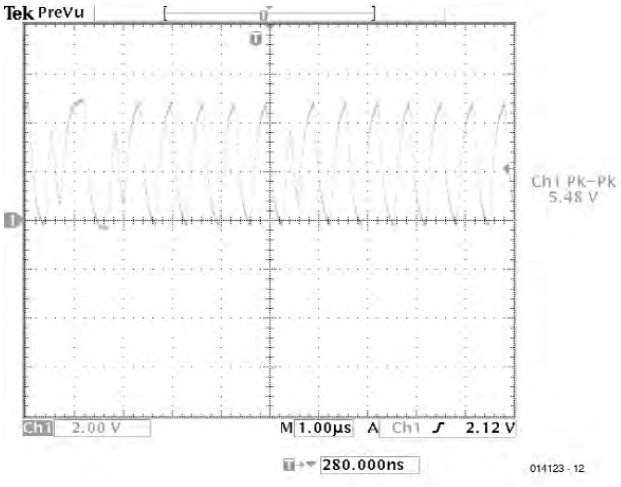


The idea for this circuit came from the question whether there was a simple method for connecting a digital audio output to the TTL input of, for example, a sound card. A typical S/PDIF signal has a level of 0.5 V_{pp} at 75 Ω. This level is of course much too low to drive an input that works at TTL levels. The simplest way to obtain the correct voltage is to use a small transformer to step up the voltage. The input impedance of the circuit should be 75 Ω in order to keep distortion of the signal as low as possible.

The transformer we've used has an EP7 core with an accompanying former, since it is very small; the outer dimension are only 10.7 mm by 8.5 mm. A core material of T38 was chosen (available from Farnell), which gives the transformer an A_L of 5200 nH. Since the windings (copper is diamagnetic) form a large part of the transformer, we find that in practise the A_L-value is a lot lower (30 to 40 % less).



The primary winding consists of 15 turns of 0.2 mm diameter enamelled copper wire. This is wound in one layer from a pin at the corner to a pin at the other corner. The secondary winding consists of 150 turns of 0.1 mm diameter enamelled copper wire and is wound similarly between two corner pins. Be very careful with the coil former whilst joining the halves of the core with the metal clip: it is very easily broken. The clip also shields the transformer. The coil former can be fixed in place during the winding using

a 3.5 mm drill-bit and a piece of paper.

In order to keep the input impedance linear and constant within an as wide as possible bandwidth, the 75 Ω terminating resistor has a 270 nF capacitor connected in series. At the secondary is a clamping circuit (C2 and Schottky diode D1), which gives the correct DC offset to the AC signal. The screenshot of the oscilloscope shows the output signal. This was taken at a sampling frequency of 48 kHz. It is clear that this is the limit at which this circuit can be used, at 96 kHz the logic '1' level will become too small.

A second possible method would be to have a potential divider between 5 V and earth, set to be exactly in the middle of the two logic levels. An AC-coupled S/PDIF signal ($1\ V_{pp}$ open circuit) should be large enough to be accepted at the logic input. A third method could be a combination of the previous two. With a winding ratio of 1:5 the quality of the signal (especially the bandwidth) will be much better and could give a better performance when used with the potential divider.

The aim was to keep this circuit completely passive, avoiding the need for an external power supply. This has in fact been achieved, albeit with a limited performance. No doubt a different core material and a larger core should give better results. The converter still has plenty of scope for home experimentation!

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