Low-Cost, Low-Power Level Shifting in Mixed-Voltage (5 V, 3.3 V) Systems

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ABSTRACT

Many applications require bidirectional data transfer between 5-V and 3.3-V systems. Two methods of maintaining the lowest possible total system power consumption and safe operation with mixed-mode signal translation are compared. The methods are: 1) split-rail or dual 3.3-V and 5-V devices, and 2) completely 5-V tolerant, pure 3.3-V V_{CC} components.

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Introduction

The increasing demand for lower system power consumption has brought many new design challenges. Among them is the problem of safely and efficiently interfacing the various switching levels in mixed 3.3-V and 5-V systems, while maintaining the lowest possible total system power consumption. Two competing methods of accomplishing this mixed-mode signal translation have emerged:

- Split-rail or dual 3.3-V and 5-V V_{CC} devices
- Completely 5-V tolerant, pure 3.3-V V_{CC} components

This application report deals with the pros and cons of using both device types and offers additional suggestions for even greater system power savings.

Split-Rail Level Shifters

Split-rail level shifters are a class of transceiver devices that have both a 5-V and 3.3-V V_{CC} rail. These transceivers are specifically suitable for bidirectional data transfer between the 5-V CMOS interface and 3.3-V systems. Products in this class can be used effectively as level shifters and data-path voltage translators, but the following precautions usually are recommended:

- Some dual-V_{CC} rail devices typically have strict power sequencing requirements to prevent leakage or even damage to the devices in the event that one V_{CC} rail ramps faster than the other.
- Having a 5-V V_{CC} pin does not necessarily ensure that the device actually switches all the way to the 5-V rail. Switching to 5 V is one way to reduce the power consumption in 5-V memories or other pure 5-V CMOS circuits that are driven by a level-shifter device (this application report demonstrates others as well).

The data sheet for the product in question reveals whether the part drives all the way to the 5-V rail. If the output high-voltage (V_{OH}) minimum is around 4.44 V, it does drive to the rail (for example, LVC and AHC). Five-volt level shifters with TTL-compatible outputs typically drive only to around 3.6 V (for example, ABT).

5-V Tolerant, Pure 3.3-V V_{CC} Components

A second class of products created to meet these design challenges offers similar voltage translation and level-shifting capabilities as the split-rail devices previously mentioned. These transceivers are not suitable for bidirectional data transfer between the 5-V CMOS interface and the 3.3-V LVTTL side. Using a single V_{CC} source, they avoid the power-sequencing problems and are offered in a number of functions, bit widths, and storage options. The one potential drawback of these single 3.3-V V_{CC} products is that the outputs do not pull all the way to the 5-V V_{CC} rail. A comparison of 5-V ABT and 3.3-V LVT families is provided in the following sections to see if this is a true drawback.

The LVT series of devices rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT devices. Figure 1 shows a simplified LVT output and shows the mixed-mode signal drive designed into the output stage. This combination of a high-drive TTL stage with the rail-to-rail CMOS switching gives the LVT devices extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices (see Figure 2), providing the dc drive needed for existing 5-V backplanes and allowing for a simple solution to reduce system power via the migration to 3.3-V operation.

Not only can LVT devices operate as 3-V-to-5-V level translators by supporting input or I/O voltages of 5.5 V with V_{CC} = 2.7 V to 3.6 V, the inputs can withstand 5.5 V even when V_{CC} = 0 V. This permits the devices to be used under partial system power-down applications or when live insertion is required.

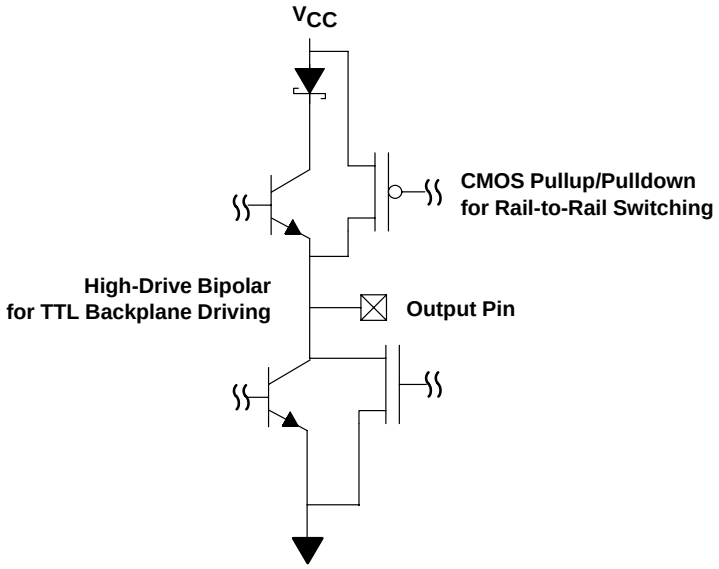

Figure 1. Simplified LVT Output Structure

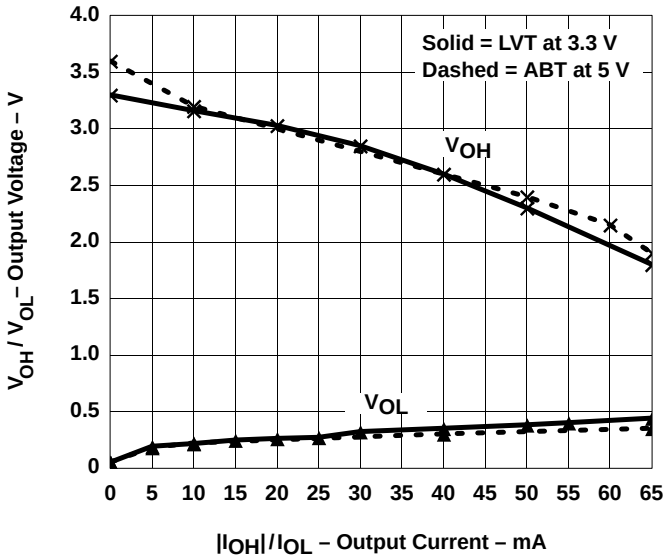

Figure 2. ABT Versus LVT Output Drive Comparison

The Misconception About ΔI_{CC}

The component selection of a level shifter affects two major aspects of total system-power dissipation:

- The effect the V_{OH} level of the driving part (A, in Figure 3) has on the power dissipation of the receiving device (B, in Figure 3), commonly known as ΔI_{CC}
- The power of the device itself

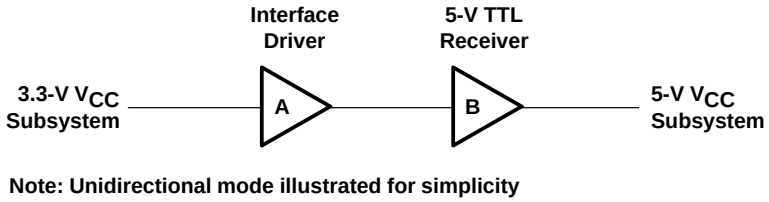

Figure 3. Basic Logic Data Transceiver

ΔI_{CC} is the added power dissipation induced into a TTL-compatible 5-V device (B, in Figure 3) due to the V_{OH} level of the driving device (A, in Figure 3). It would be correct to expect that a TTL-compatible 5-V product would have higher power dissipation if it were driven by a device with a V_{OH} of 3.6 V, rather than if that same device was driven by a 5-V V_{OH} driver.

Figure 4 shows a typical 5-V CMOS input stage and the ΔI_{CC} current associated with switching the device through the input voltage range from 0 to V_{CC}.

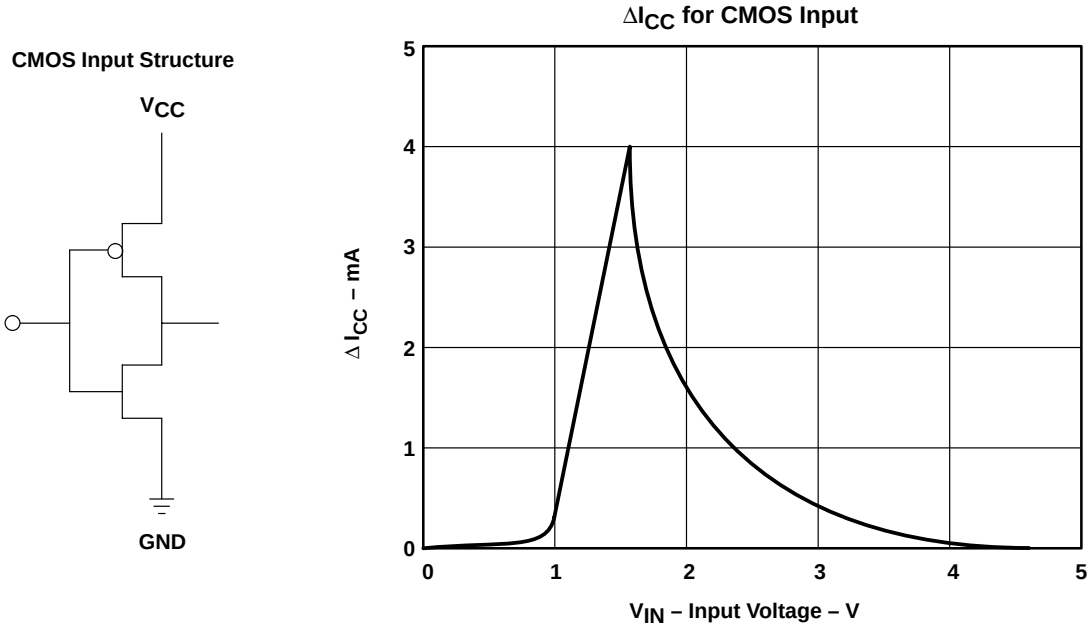

Figure 4. Basic CMOS Input Structure and Typical ΔI_{CC} Current

As expected, the ΔI_{CC} current approaches zero at the V_{CC} and ground rails and peaks in the TTL-threshold region of 1.5 V.

Figure 5 is a graph of the ΔI_{CC} (i.e., additional I_{CC}) that is induced into a 16-bit device (all outputs switching) as a function of V_{OH} of the driving device and frequency.

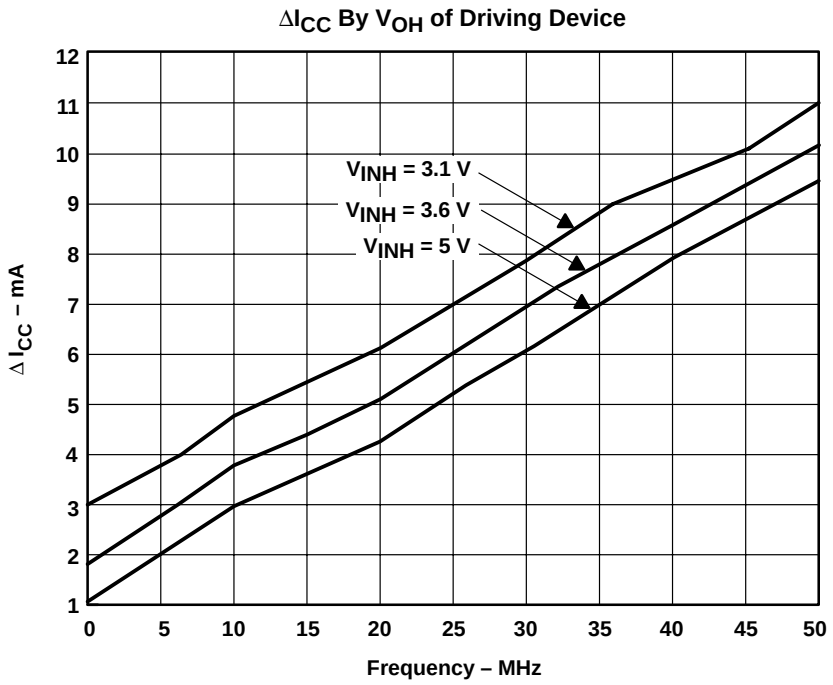

Figure 5. ΔI_{CC} – 16-Bit Device

As shown in Figure 5, ΔI_{CC} is, in fact, 2 mA to 3 mA higher for the case where V_{OH} is only 3.1 V, than for the same device driven to the 5-V rail by a pure 5-V CMOS device. From this, one might conclude that the best possible solution would be to always select a part that switches all the way to the 5-V rail, but this conclusion fails to consider the impact of system power on the driving device.

Figure 6 shows the V_{OH} of two devices: the FCT164245 split-rail device from Integrated Device Technology, Inc. (IDT™) and the 'LVTH16245A from TI.

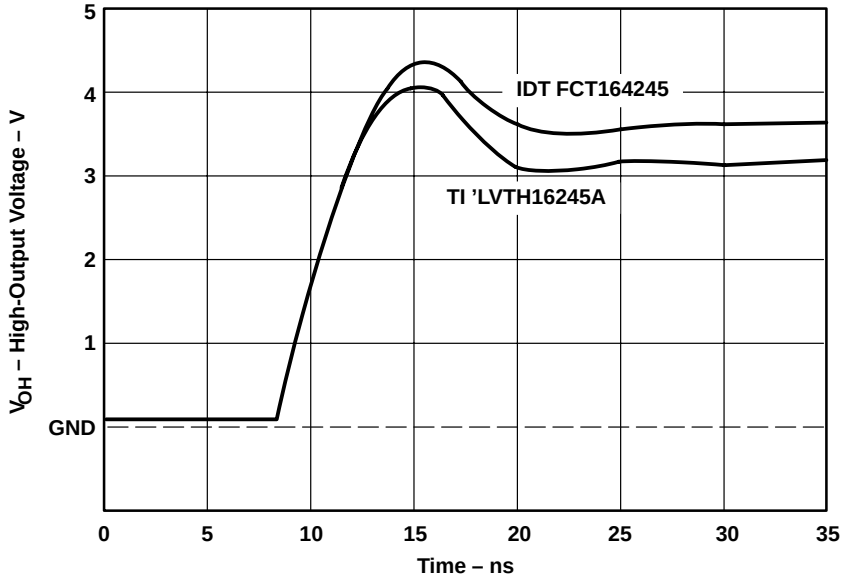

Figure 6. V_{OH} of FCT164245 and 'LVTH16245A

From Figure 6, it can be concluded correctly that the induced ΔI_{CC} current in a part driven by the LVT part would be higher than the FCT device. The problem with this conclusion is that, from a system standpoint, ΔI_{CC} is only one of the two components of total system power dissipation that is affected by the selection of a level-shifter device.

Figure 7 shows the total power dissipation of the same IDT split-rail device, the TI 'LVTH16245A, and the worst-case ΔI_{CC} (V_{OH} = 3.1 V) plotted on the same vertical scale.

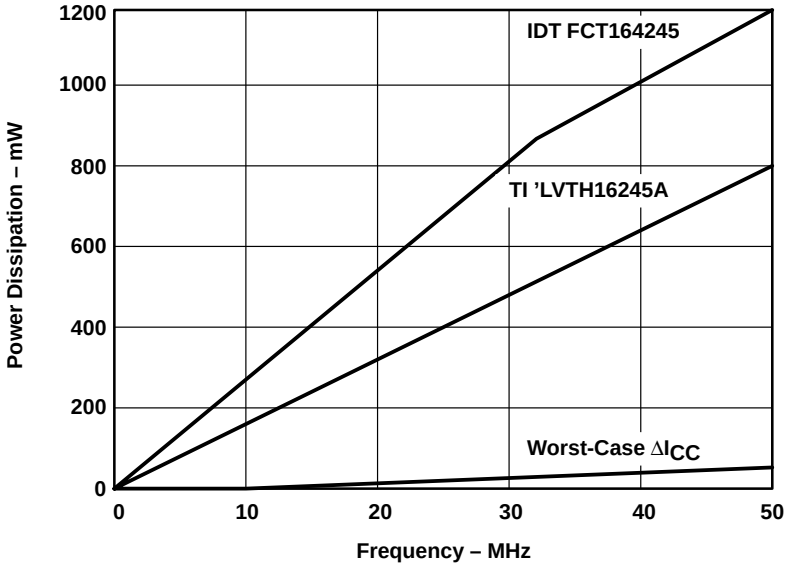

Figure 7. Total-System Power-Dissipation Impact

From Figure 7, it can be seen that, even if a split-rail device pulls all the way to the 5-V rail (which the IDT part does not), the power savings in ΔI_{CC} is more than offset by the huge switching currents that the split rail draws from the 5-V rail.

More Savings Are Possible

Some systems use a means of power savings known as partial power down. In partial power-down mode, a system basically shuts off the V_{CC} to some unused circuits during inactivity, thus eliminating even low standby currents. All of the members of TI's LVT product line offer a parametric specification I_{off}, which ensures that the output pins of the parts remain in the high-impedance state when the supply voltage is at 0 V. This prevents an inactive LVT device from dragging down the bus of an active part in the system and allows the LVT part to become a partition for the partially powered-down unused subsystem. The LVT device still functions as a level shifter and voltage translator when power is restored to the inactive subsystem.

Another aspect of system power dissipation is the use of passive resistor pullups to keep a local bus from floating and causing damage to the devices on the bus. Pullups were sufficient for the older desktop systems where power consumption was not as much of a concern, but pullup resistors in portable equipment can have a serious impact on battery life and, as such, must be addressed.

Products like the ’LVTH16245A (and others) from TI have a circuit feature called a bus-hold cell (shown in Figure 8). This cell eliminates these passive components and all of the procurement costs, board space, bus parasitics, and power dissipation associated with them. This circuitry provides for a typical holding current at ±100 μA that is sufficient to overcome any CMOS-type leakages. Since this is an active circuit, it does take current – approximately ±500 μA – to toggle the state of the input. This current is negligible when compared to the magnitude of current that is needed to charge a capacitive load and does not affect the propagation delay of the driving output.

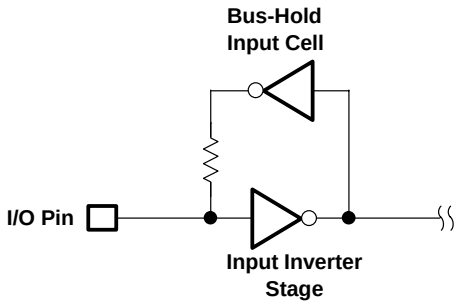

Figure 8. LVT Bus-Hold Cell

Conclusion

As an interface between a 5-V CMOS and a 3.3-V system, the split-rail level shifter with rail-to-rail output switching is a good choice. Both split-rail level shifters and 5-V-tolerant single 3.3-V V_{CC} devices can be used for bidirectional data transfer between the 5-V LVTTL interface and 3.3-V systems. When optimizing the cost and power for a total system, many issues should be considered. A device that contributes less ΔI_{CC} power might not always contribute to more efficient system power consumption. Although the IDT FCT164245 had less ΔI_{CC} power contribution than the TI LVTH16245A, overall system power consumption was better with the LVTH16245A.

Acknowledgment

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