Connecting digital ICs within the same logic family will rarely cause any problems, as long as such things as fan-out and parasitic line and input capacitance are taken into account. It is quite a different matter, however, to try to use the different logic families, TTL (standard, LS and ALS) and CMOS, together. There is a great temptation to do just this as the possibilities for combinations becomes even greater with logic families continually being expanded. The new family of high speed CMOS (HCMOS) recently released onto the market prompts even more questions about the compatibility of its two variations with existing logic circuits. Maybe a lot of problems will be solved if we simply answer the question 'How digital is digital?'.

mating logic families

it was all very easy when there was only TTL

The popularity of digital electronics is very easy to understand. What could be simpler than a system in which there are only two values, '1' or '0'? Certainly this makes design and fault finding much simpler, but there are also some other considerations. As long as the elements of a design are kept 'in the family', with only TTL or only CMOS, for example, the manufacturers have already sorted out the problem of matching different gates. The logic levels are well defined and the input and output currents are virtually the same. Combining different logic families, however, is a completely different kettle of fish. Then our old friend Murphy appears with a vengeance and seems to have taken a personal dislike to your design, whatever it is. With a bit of determination, however, even Murphy can be defeated (temporarily at least).

How the families compare

There are, of course, some advantages to having different logic families. It becomes easier, for instance, to combine speed with economy. The appearance of different logic families is largely based on the attempts to achieve ever shorter switching times and smaller power consumption. Within the scope of a short article we cannot deal with all logic families, and this would, in any case be overdoing it a bit as we are only interested in logic elements that are already, or will soon be, readily available. A summary of the families to be dealt with and their most notable characteristics is shown in table 1. These data should only be considered as an indication and not as exact values. The only function of this table is to aid the general comparison so the values can vary depending on the circuit and even the manufacturer.

The values of logic '1' and '0' have to be specified as a certain voltage and the symbols we will use to make this definition are shown in figure 1.

In order for the circuit to operate under the least favourable conditions (the worst case) U_{OH} must always be larger than U_{IH} and U_{OL} must be smaller than U_{IL}. A summary of the voltages needed for the various logic families is given in table 2. The CMOS levels are only given at 5 V because we want to ensure compatibility with TTL.

Table 1

	TTL			CMOS		
series	7400	74LS	74ALS	4000	74HC	74HCT
supply voltage	5 V	5 V	5 V	3...18 V	2...6 V	5 V
dissipation per gate	10 mW	2 mW	1 mW	2.5 nW	2.5 nW	2.5 nW
gate delay time	10 ns	9.5 ns	4 ns	40 ns	9 ns	9 ns

1

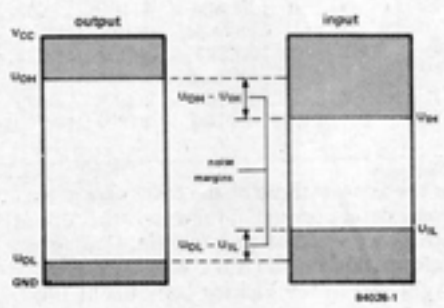

Figure 1. Here we define the logic levels as fixed voltages. Between 'high' and 'low' is a 'no man's land'.

Possibilities for combination

First we will see which families are matched purely on the basis of input and output levels. Most notable is the fact that interconnecting elements within the TTL group causes no problems. In one case the noise margin is even improved; this happens if LS or ALS is used in place of standard TTL.

Connecting TTL to HCTMOS is no problem either as this version of high speed CMOS is TTL compatible. Furthermore the user does not even need to know he is working with CMOS because its gates appear to be extra-efficient LSTTL devices. The supply voltage tolerance with HCTMOS is larger than with TTL (10% instead of 5%), which simply means that the

Table 2.

	TTL	LSTTL	ALSTTL	CMOS	HCTMOS	HCMOS	
V_{CC}	5 V ± 5%	5 V ± 5%	5 V ± 5%	3 . . . 18 V	5V ± 10%	2 . . . 6 V	
				5 V		5V ± 10%	3 V
U_{IH} - logic 1 input level (min.)	2.0 V	2.0 V	2.0 V	3.5 V	2.0 V	3.15 V	2.1 V
U_{IL} - logic 0 input level (max.)	0.8 V	0.8 V	0.8 V	1.5 V	0.8 V	1.1 V	0.6 V
U_{OH} - logic 1 output level (min.)	2.4 V	2.7 V	2.7 V	4.5 V	3.7 V	3.7 V	2.2 V
U_{OL} - logic 0 output level (max.)	0.5 V	0.5 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V
I_{IL} - input sink current (max.)	-1.6 mA	-0.36 mA	-0.2 mA	0.005 µA			
I_{IH} - output source current (max.)	40 µA	20 µA	20 µA	0.005 µA			
I_{OL} - output sink current (min.)	16 mA	8 mA	4 mA	0.4 mA	4 mA	4 mA	4 mA
I_{OH} - output source current (min.)	-400 µA	-400 µA	-400µA	-0.4 mA	-4 mA	-4 mA	-4 mA

TTL supply can be used for HCTMOS but the reverse is not necessarily true.
It is not quite so easy to connect TTL to CMOS. The U_{OH} in TTL is lower than the U_{IH} in CMOS with a supply of 5 V. This means that a logic 1 at a TTL output will not be interpreted as 'high' by a CMOS input.
The same applies if we want to use HCMOS and TTL with a supply of 5 V. In this case U_{IH} (for HCMOS) is a minimum of 3.15 V, which is much too high for TTL. All is not lost, however, as the supply voltage for HCMOS can be anywhere between 2 and 6 V. If the HCMOS section of a circuit is operating on a supply of 3 V then U_{IH} is 2.1 V (70% of 3 V). Now TTL can provide a logic 1, with a margin of 0.3 V. One situation that can arise here, however, is that the TTL output level can be higher than the HCMOS supply voltage. In this case the current flowing through the 150 Ω input resistor and the input protection diode is limited by the resistor and by the collector resistance in the output circuit of the TTL gate. As long as the input current does not exceed 20 mA nothing untoward should happen. What logic 0 means in this case is three things: U_{IL} is a maximum of 0.6 V (20% of 3 V), while the U_{OL} for TTL is 0.5 V which leaves a margin of 0.1 V. Fortunately it is not such a problem to drive TTL from CMOS or HCMOS, as long as the supply is 5 V. The input levels for TTL do not have to be very precise; U_{IL} is relatively high and U_{IH} fairly low. The CMOS output voltages are therefore quite suitable for the TTL inputs, but care must be taken to ensure that the CMOS can handle the relatively high TTL input current. This applies particularly to driving standard TTL from ordinary CMOS, we will deal with this further under 'fan-out'.
If the CMOS is operating at a higher supply level then obviously a level adapter circuit is needed at the connection to TTL or HCTMOS

Fan out

As regards input current a distinction must be made between TTL and CMOS. The input of a TTL gate consists of a (multi-emitter) transistor whose base is connected to V_{CC} via a resistor, as shown in figure 3. Consequently a floating input is always seen as a logic 1. The output is logic 0 if the input is earthed, then a current, the sink current, flows from the input. The sink current is 1.6 mA in standard TTL, 0.4 mA for LSTTL and 0.2 mA with ALSTTL. These values are also stated in table 2. The output of the driving gate must be able to handle this current. This, of course, presents no problems for TTL as the outputs are designed with this in mind, but CMOS is a different matter. Within the CMOS family the outputs are not expected to deliver large currents. The only current that will flow is the charging current for the input capacitance (and otherwise only the input leakage current) which has a value of a few nA.
As a general rule the fan out, even between different families, can be calculated by dividing the maximum output current by the required input current. These currents are defined for both logic levels (see table 2 again). Because of the set-up of the

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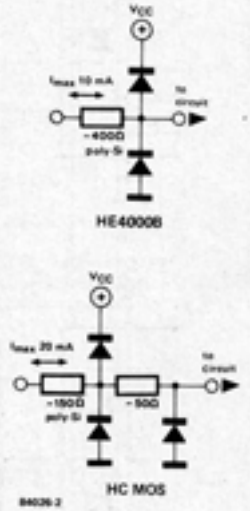
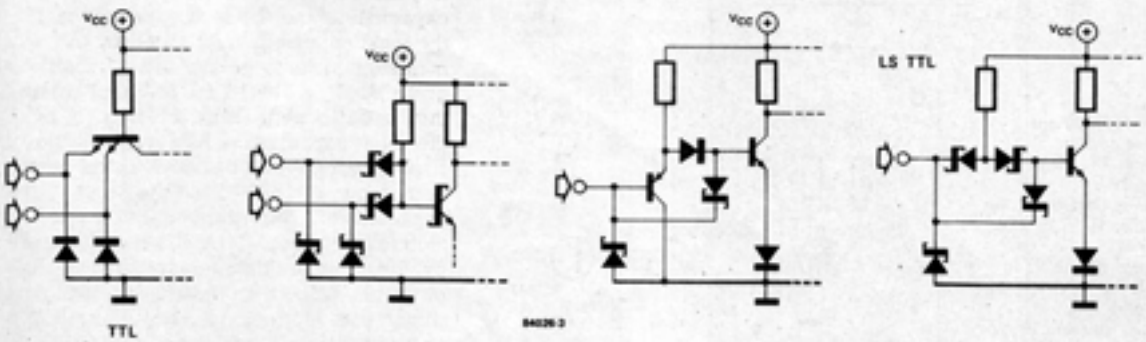


Figure 2. Input protection circuits for HCMOS and CMOS circuits.

Figure 3. Various configurations of (LS) TTL inputs. If the input is made 'low' a relatively large current flows from the input (the sink current).

3



TTL input circuit I_{IL} is considerably greater than I_{IH}. As a consequence of this lack of symmetry the fan out at both logic levels must be calculated and the smaller value taken as the limit.
Using the data in table 2, the fan out for various different combinations is easily found. A separate table (table 3) has been drawn up to show a summary of the results. This fan out is only shown for the combinations whose logic levels adapt directly to each other, as indicated by table 4.

Table 3.

from \ to	TTL	LS TTL	ALS TTL	HCT MOS	HC MOS	CMOS
TTL (1)	10	20	20			
LS TTL (1)	10	20	20			
ALS TTL	10	20	20			
HCT MOS (2)	100	100	100			
HC MOS (2) (5 V)	100	100	100			
CMOS (3) (5 V)		20	40			

1) with 74 and 74LS buffers the fan out is three times as large.
2) 74HC and 74HCT ICs with bus driver outputs have a fan out 1 x times as large.
3) Normally CMOS cannot handle the normal TTL sink current but this depends on make and type.
4) Theoretically infinite, but in practice limited by the maximum permissible delay times.
5) Direct connection not possible because of different logic levels.
6) May only be combined if the HCMOS section works from a supply of 3 V.

Because of its large sink current, TTL can be heavily driven. The fan out, for driving normal TTL, is, as a rule, low. Not even CMOS can handle the sink current of 1.6 mA. As a result of this it is not possible to connect CMOS directly to TTL, even though their voltage levels are similar. There are, however some CMOS ICs available with buffered outputs that can sink a current of 1.6 mA. Otherwise the CMOS outputs could also be connected in parallel until the I_{IL} required is reached. The data sheets from the relevant manufacturer should be studied for more details about this.
There are less problems with driving LSTTL and ALSTTL because of their smaller sink current. CMOS can also drive LSTTL and ALSTTL directly.
The input requirements of all the MOS families are so modest that the fan out is theoretically very high (several thousand). In practice this is limited by the input capacitance and the lead capacitance. If the maximum frequency stated by the manufacturer is to be attained (generally given by C_L = 10, 15, 50, or 100 pF), then the fan out is defined by dividing C_L by the input capacitance. As a general rule 10 pF per input can be taken as the norm. Remember, of course, that the input capacitance is very dependent on the technology used; CMOS ICs manufactured by metal gate techniques have a larger input capacitance than those made using silicon gate technology. Also, a length of ribbon cable or a track on a printed cir-

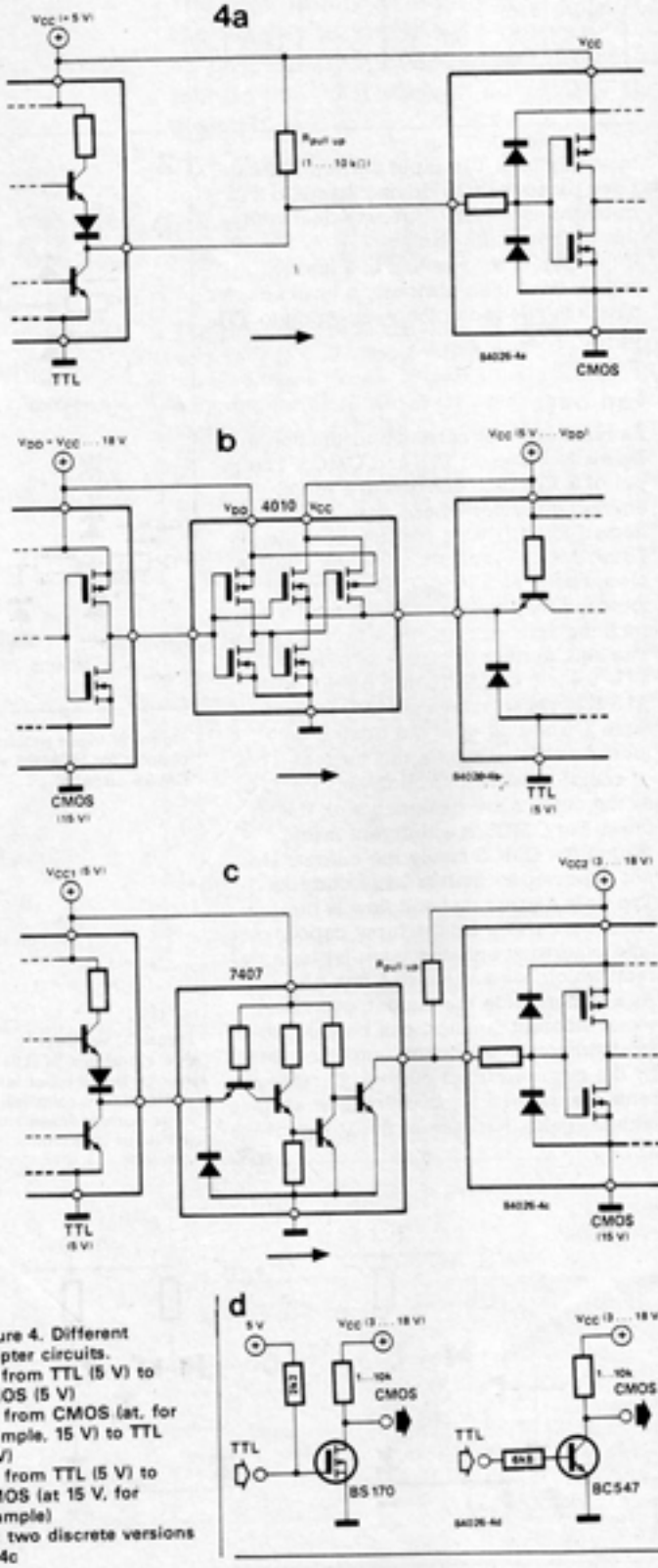


Figure 4. Different adapter circuits.
4a: from TTL (5 V) to CMOS (5 V)
4b: from CMOS (at, for example, 15 V) to TTL (5 V)
4c: from TTL (5 V) to CMOS (at 15 V, for example)
4d: two discrete versions of 4c

cuit board can form a considerable capacitance. In all these cases it is up to the user to set an acceptable delay time and therefore the fan out.

Adapter circuits

In order to connect TTL (standard, LS and ALS) to 5 V supplied CMOS and HCMOS, the TTL must be able to provide the logic 1 level needed by the CMOS (at least 3.5 V). This is simply done using a pull up resistor, as figure 4 shows. A small value results in a high speed as parasitic capacitances are then charged more quickly. The minimum resistance possible is decided by the maximum load for the output. In theory the number of inputs driven by this output must also be taken into account, but if they are MOS inputs, which have negligible input current, that can simply be ignored. The minimum value of the pull up resistor is defined by:

$$R(min.) = [V_{CC}(min.) - U_{OH}]/[I_{OL} - \Sigma I_{IL}]$$

The second term in the denominator, the sum of the input currents, can be neglected if we are talking about MOS inputs.
There is also a maximum permissable value for the pull up resistor. Because of leakage currents at the output (if, for example, several open collector outputs are connected together) and the input, there is a voltage drop across the pull up resistor at logic 1. As the output voltage may never be less than U_{IH}, the maximum value of the pull up resistor is defined by:

$$R(max.) = [V_{CC}(min.) - U_{OH}]/[\Sigma I_{OH} + \Sigma I_{IH}]$$

Here again the second term of the denominator can be ignored for MOS inputs.
What all this means, in effect, is that the pull up resistor must have a value of 1 . . . 10 kΩ. Generally these formulae can be applied to the pull up resistors of open collector outputs whether they drive CMOS or HCMOS or not.
The situation is quite different if one logic device operates at a different supply level, which also means different logic levels. A single 4009, 4010, 4049 or 4050 buffer can be used as a high-low adapter, for example from 15 V CMOS to 5 V TTL. Each package contains six buffers, and in the case of the 4009 and 4049 they are also inverters. These buffers, which can drive up to 2 TTL inputs or 9 LSTTL inputs, can also be used, for example, to drive standard TTL from CMOS.
And so to the last combination possibility: from 5 V TTL to CMOS working at a higher level, or HCMOS at 6 V. This is also fairly straightforward if we are working with open collector outputs. In some cases the output transistor's U_{CE} is higher than V_{CC}. Examples of this are the 7406 and 7407 with 30 V open collector outputs and the 7416 and 7417 with 15 V open collector outputs. The value of the pull up resistor must be carefully chosen so that the sink current does not become too large.
The fan out of the 74XX buffers listed above is three times the standard fan out, so the pull up resistor is unlikely to be too small. The disadvantage of this is that unnecessarily small pull up resistors can draw a much larger current for a negligible increase in speed.
A discrete buffer stage could, of course, be built using a transistor and two resistors to drive CMOS from TTL. This effectively creates an open collector output. Two possibilities for this are shown in figure 4d, the first having the advantage of a faster switching time.

Table 4.

mating logic families

from \ to	TTL	HCT MOS	HC MOS (5 V)	CMOS (5 V)	CMOS (>5 V)
TTL	●	●	2) ○		
HCT MOS	●	●	●	●	3)
HC MOS (5 V)	●	●	●	●	
CMOS (5 V)	1) ○	●	●	●	
CMOS (>5 V)		3)			●

1) Logic levels are right but sink currents must be taken into account. Buffers are needed.

2) Possible as long as the HCMOS section has a supply of 3 V.

3) Not possible without extra adapter circuitry.

Finally

It is not a good idea to leave unused TTL inputs floating, even though they normally act as if they were logic 1. If, for example, a certain LSTTL IC with a floating input is changed for its HCTMOS equivalent this causes problems. The very high input impedance means that the logic level will not be defined and the circuit will not work (properly). The moral of this is that unused inputs should always be tied to one logic level; for TTL use a pull up resistor (1 . . . 10 kΩ) to V_{CC}, connect directly to earth or to an input that is used (LS inputs can be connected directly to +5 V). With all MOS versions connect unused inputs to V_{CC}, earth or an input that is used.
It is virtually impossible to list how to interconnect all the various logic families from different manufacturers who specify different testing conditions for their gates. However, that was never our intention, and we think that this summary of the present possibilities should at least enlighten the hobbyist as to what can be done with what is available today. ▶

ECL
Emitter Coupled Logic, fast unsaturated logic.

TTL (7400 series)
Transistor Transistor Logic, circuits with transistors in saturation. Slower than ECL.

HTTL (74H series)
High speed TTL.

LTTL (74L series)
Low power TTL.

STTL (74S series)
Schottky TTL. The use of Schottky diodes prevents the transistors from being driven too far into saturation. This increases the switching speed.

LSTTL (74LS series)
Low power Schottky TTL.

ALSTTL (74ALS series)
Advanced Low power Schottky TTL.These are the fastest and most economical TTL devices.

CMOS (4000 series)
Complementary Metal Oxide Semiconductor, fairly slow but very economical logic family.

HCMOS (74HC series)
High speed CMOS, CMOS with LSTTL switching times.

HCTMOS (74HCT series)
High speed TTL compatible CMOS, low power consumption.