Hexadecimal encoder debounces keyboard

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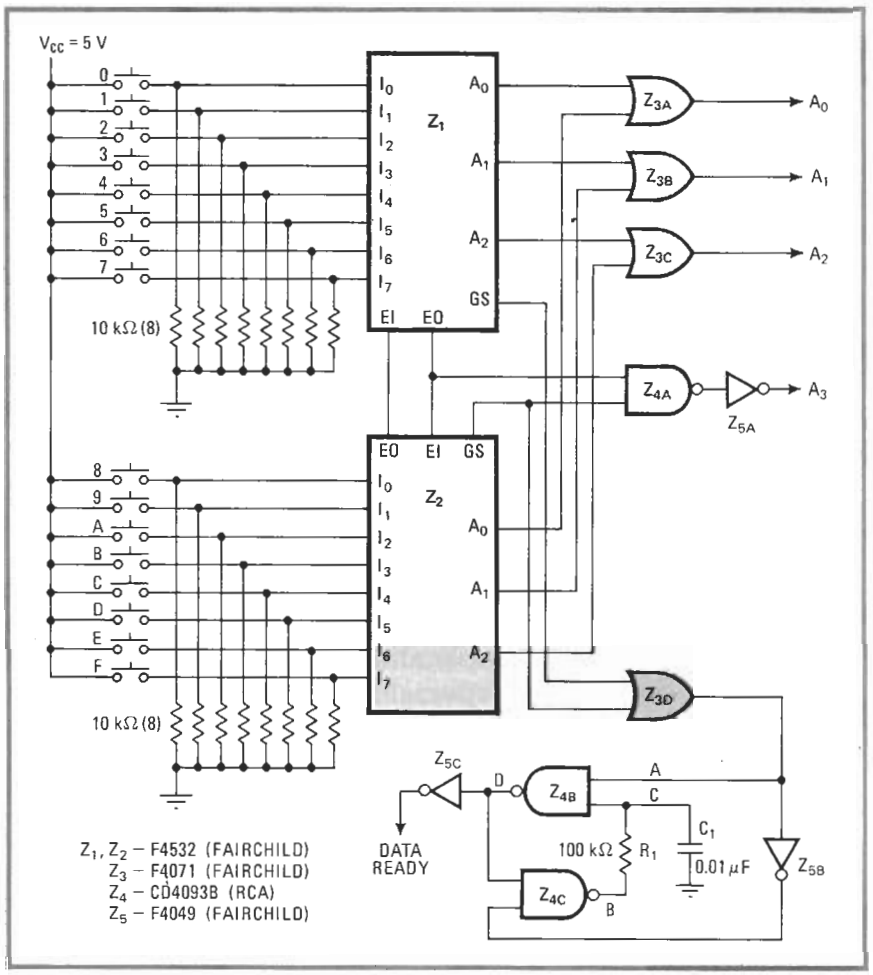
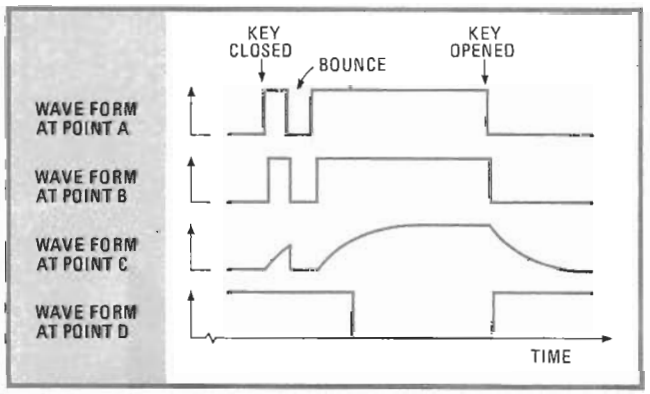
Programs and instructions for microprocessors are commonly written in hexadecimal machine code (0, 1, . . . 9, A, B, . . . F), but must be fed into memory in binary code. In the 16-key encoding keyboard circuit described here, the unique application of two eight-input priority encoders provides the user with key lockout—if he accidentally presses two keys to one encoder simultaneously, only the higher value is encoded, and oper-



1. Encodes and debounces. Pressing any one of the 16 hexadecimal-digit keys produces the corresponding 4-bit binary output through the two priority encoders Z_1 and Z_2. Key debounce is provided by the Schmitt trigger delay latch Z_{4B}/Z_{4C}, as illustrated in Fig. 2. This keyboard is a convenient interface to microprocessors or other binary devices for which instructions may be written in hexadecimal code.



2. Less bounce to the ounce. Wave forms at four points in delay latch illustrate how R_1C_1 delay and Schmitt trigger action prevent key-bounce from generating multiple outputs.

ation of one encoder automatically disables the other.

Another unique feature of the circuit is a delay latch, which debounces the keys. Only when the key contacts have settled down to a steady closed or open position can the microprocessor read the code.

As Fig. 1 shows, the circuit accepts the hexadecimal input over 16 keys and translates it into 4-bit binary outputs for parallel feed to a computer. The priority encoders provide the basic encoding.

The keys are arranged in two groups, 0 through 7 and 8 through F. Each subgroup is encoded in 3-bit binary code; if two keys in the same subgroup are pressed, the code output corresponds to the highest-priority key depressed. Lockout between subgroups is accomplished by cross-coupling the enable-input (EI) and enable-output (EO) pins, so that the output code is decided by which subgroup is accessed first. Encoding for the fourth bit is accomplished by an AND gate between the low-order enable-output and the high-order group-select (GS). The composite output code then consists of the subgroup output bits ORed together for the lower three bits, and the fourth bit output.

The keys are debounced by delay latch Z_{4B}/Z_{4C}. The basic ingredients of the latch are the CD4093B Schmitt trigger elements and an RC delay (R_1 and C_1) in the feedback loop of the latch. The debounce wave forms in Fig. 2 show that a key must stop bouncing before the latch feedback, delayed by a time 0.85 R_1C_1, locks in the key action. Release of a key immediately resets the latch, with the input bypassing the delay loop. It is imperative that a Schmitt trigger be incorporated in the delay latch, but the use of C-MOS holds down the size and cost of the capacitor. The values of C_1 and R_1 are determined by the bounce characteristics of the push-button keys. The 0.01 microfarad and 100 kilohms shown in Fig. 1 will debounce almost any key. □

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