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BRIEF

# Device spacing on RS-485 buses

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## Introduction

The RS-485 bus is a distributed parameter circuit whose electrical characteristics and responses are primarily defined by the distributed inductance and capacitance* along the physical media. The media is defined here as the interconnecting cable(s) or conducting paths, connectors, terminators, and RS-485 devices added along the bus. The following analysis derives a guideline for the amount of capacitance and its spacing that can be added to the bus.

For a starting approximation, the characteristic transmission line impedance at any cut point in the unloaded RS-485 bus is defined by the following equation, where L is the inductance per unit length and C is the capacitance per unit length.

$$Z = \sqrt{\frac{L}{C}}$$

As capacitance is added to the bus in the form of devices and their interconnections, the bus impedance is lowered to Z′, causing an impedance mismatch between the media and the loaded section of the bus.

As the input signal wave arrives at this mismatch in impedance, an attenuation (or amplification) of the signal will occur. The signal voltage at an impedance mismatch is $V_{L1} = V_{L0} + V_{J1} + V_{R1}$, where $V_{L0}$ is the initial voltage, $V_{J1}$ is the input signal voltage, and $V_{R1}$ is the reflected voltage. The voltage reflected back from the mismatch is $V_{R1} = \rho_L \times V_{J1}$, where

$$\rho_L = \frac{Z' - Z}{Z' + Z}$$

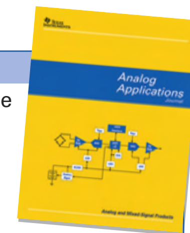
and is the coefficient of reflection commonly used in transmission line analysis. The voltage equation can now be written as $V_{L1} = V_{L0} + V_{J1} + \rho_L \times V_{J1}$.

With fast transfer rates and electrically long** media, it becomes essential to achieve a valid input voltage level on the *first* signal transition from an output driver anywhere

* All capacitances are differential in this article. The differential is approximately one-half of the single-ended capacitance.

** "Electrically long" is defined here as $\tau > \frac{t_{10\text{-}90\%}}{3}$

where t is the one-way time delay across the bus and $t_{10\text{-}90\%}$ is the 10% to 90% transition time of the fastest driver output signal.



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on the bus. This is called incident-wave switching. If incident-wave conditions are not achieved, reflected-wave switching must be used. To achieve a valid logic voltage level, reflected-wave switching depends upon reflected energy occurring some time after the first transition arrives.

Assuming that the bus is terminated at both ends with the nominal media impedance and no fail-safe offset, an RS-485 driver will create a high-to-low voltage change from at least 1.5 V to –1.5 V, or a $V_{J1}$ of –3 V. The signal voltage at the load, $V_{L1}$, should go below the minimum receiver input voltage threshold of –0.2 V.

$$-0.2 > 1.5 + (-3) + \rho_L \times (-3)$$

$$\rho_L > \frac{-0.2 - 1.5 + 3}{-3} = -0.43$$

Now we can solve for Z′:

$$\rho_L = \frac{Z' - Z_0}{Z' + Z_0} > -0.43$$

$$Z' - Z_0 > -0.43(Z' + Z_0)$$

$$Z'(1 + 0.43) > Z_0(1 - 0.43)$$

$$Z' > 0.4Z_0$$

If the loaded bus impedance is no less than $0.4Z_0$, the minimum threshold level should be achieved on the incident wave under all allowed cases.

What bus configuration rules should be used to keep the loaded bus impedance above $0.4Z_0$?

In the derivation of the minimum loaded-bus impedance, we treat the addition of devices and their capacitances in a distributed model. As such, the loaded-bus impedance can be approximated by

$$Z' = \sqrt{\frac{L}{C + C'}}$$

where $C'$ is the added capacitance per unit length.

If we knew the distributed inductance and capacitance of the media, we could calculate $Z'$ directly. Unfortunately, manufacturers do not commonly specify these; but they generally do specify the characteristic impedance, $Z_0$, and the capacitance per unit length, C. With these and the relationship

$$Z_0 = \sqrt{\frac{L}{C}}$$

we can solve for L, as $L = Z_0^2 C$. Then we can substitute into the equation for $Z'$ and simplify:

$$Z' = \sqrt{\frac{Z_0^2 C}{C + C'}} = Z_0 \sqrt{\frac{C}{C + C'}}$$

$C'$ is the distributed device capacitance ($C_L$) divided by the distance (d) between devices:

$$C' = \frac{C_L}{d}$$

Substituting this into the equation, we can solve for d:

$$Z' = Z_0 \sqrt{\frac{C}{C + \frac{C_L}{d}}}$$

$$\left(\frac{Z'}{Z_0}\right)^2 = \frac{C}{C + \frac{C_L}{d}}$$

$$C\left(\frac{Z_0}{Z'}\right)^2 = C + \frac{C_L}{d}$$

$$d = \frac{C_L}{C\left[\left(\frac{Z_0}{Z'}\right)^2 - 1\right]}$$

Now substituting our minimum $Z'$ of $0.4Z_0$ gives us d in meters (if C is pF/m) or feet (if C is pF/ft):

$$d > \frac{C_L}{C\left[\left(\frac{Z_0}{0.4Z_0}\right)^2 - 1\right]}$$

$$d > \frac{C_L}{5.25C}$$

We now have a relationship for the minimum device spacing as a function of the distributed media and lumped-load capacitance. Figure 1 shows this relationship graphically.

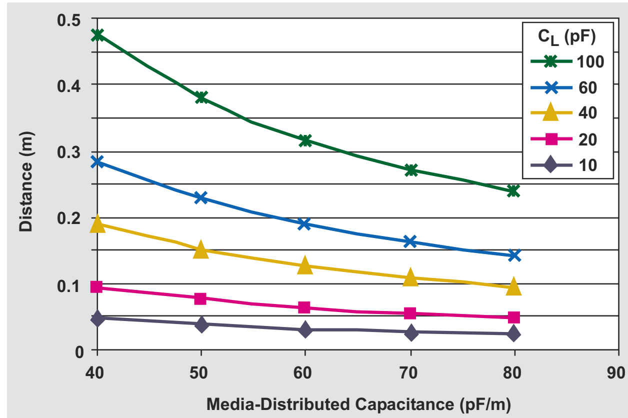


Figure 1: TPS79918 Internal Block Diagram

Load capacitance includes contributions from the RS-485 line circuit bus pins, connector contacts, printed-circuit-board traces, protection devices, and any other physical connections as long as the distance from the bus to the transceiver is electrically short. RS-485 5-V transceivers, such as the SN65HVD1176, have a capacitance of 7 pF. Transceivers with a 3-V supply, such as the SN65HVD11, have about twice the capacitance that 5-V transceivers have at 16 pF. Board traces add about 0.5 to 0.8 pF/cm depending upon their construction. Connector and suppression device capacitance can vary widely. Media-distributed capacitance ranges from 40 pF/m for low-capacitance, unshielded, twisted-pair cable to 70 pF/m for backplanes.

This derivation gives guidelines for spacing of RS-485 nodes along a bus segment based upon the lumped-load capacitance. The method is equally applicable to other multipoint or multidrop buses, such as CAN, RS-422, or M-LVDS, with appropriate adaptation of the parameter values.

| **References:** |
|---|
| Related Web sites |
| interface.ti.com |
| www.ti.com/sc/device/SN65HVD11 |
| www.ti.com/sc/device/SN65HVD1176 |