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Digital Design: How to Interface ICs

Connect ICs to the outside world with these hints from the author of "Digital Basics."

The reader response to my three-part series titled "Digital Basics" (*73*, September through November, 1982) was overwhelming even to an old tech-writing hack like myself. In addition to receiving more than a dozen positive letters (and no negative ones), I received a consulting offer; writing for *73* surely pays!

One theme which popped up in about one-third of the letters was digital interfacing. Readers wanted to know how to interface various digital IC logic families with each other and with the "outside world." In this extension of the original series, we will discuss interfacing techniques and how they can be applied in practical situations.

Logic Family Outputs and Inputs

Most readers will be using either the transistor-transistor-logic (TTL) or complementary-metal-oxide-semiconductor (CMOS) and related MOS families. These will be the devices discussed in this article.

Before we can become too deeply involved in any discussion on interfacing, we must become familiar with just *what* is being interfaced. For digital electronics, this means a review of the input and output circuits of the devices, since these are what will be connected together.

The TTL logic family operates from a single-polarity dc power supply of +5 volts dc and ground. This supply must be regulated to keep the voltage within a narrow range—4.75 to 5.2 volts. Some texts permit slightly broader limits, but practical experience indicates that voltages lower than +4.75 volts cause erratic operation, especially of complex function devices, while potentials over about +5.2 volts lead to premature failure of large numbers of chips. I personally prefer to keep the potential within the even narrower range of +4.9 to +5.05 volts dc.

The TTL output stage is a *current sink* to ground, while the TTL input is a *current source*. Figs. 1(a) and 1(b) show two popular forms of TTL output, while Fig. 1(c) shows a typical TTL input circuit. The high and low logic levels in TTL are specified in terms of the voltages that satisfy the input requirements.

The high level will be anything between +2.4 volts and +5.0 volts. In most TTL devices, the output will produce a potential greater than +2.4 volts for high, but considerably lower than +5 volts; potentials in the 3.0-to-4.0-volt range are most frequently found. The low condition is defined as any potential between 0.0 volts and 0.8 volts, i.e., 800 millivolts. The region between 0.8 volts and +2.4 volts is undefined and is therefore to be avoided. One problem seen in some interfacing situations is the creation of a circuit that will not bring the outputs to within the defined high and low limits, thereby creating an unpredictable situation.

One advantage of using IC logic elements is that we are free to avoid the problems of impedance matching (and other related headaches) when connecting the devices together in cascade. We can use the concepts of *fan-in* and *fan-out*. The term fan-in defines the load presented by any device in terms of standard TTL input loads. Since the TTL input is little more than a 1.6-milliampere current source, we define a fan-in of 1 as a current source of 1.6 mA, at standard TTL logic voltage levels. The fan-out is the drive capacity of a logic device defined in terms of the number of standard 1.6-mA TTL loads that the output will drive. In most devices, the fan-out is ten, so the device will successfully drive up to ten standard TTL loads. (In other words, it has

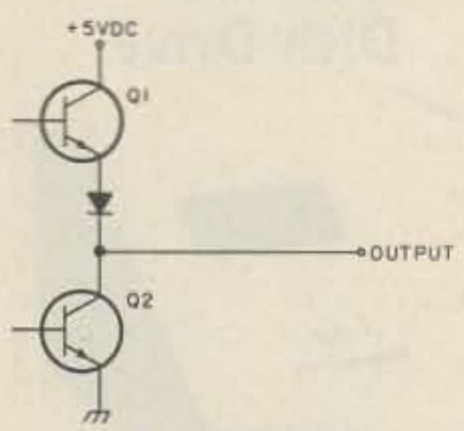

Fig. 1(a). TTL totem-pole output.

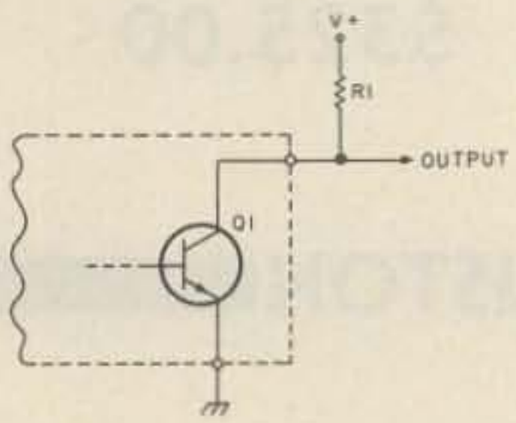

Fig. 1(b). TTL open-collector output.

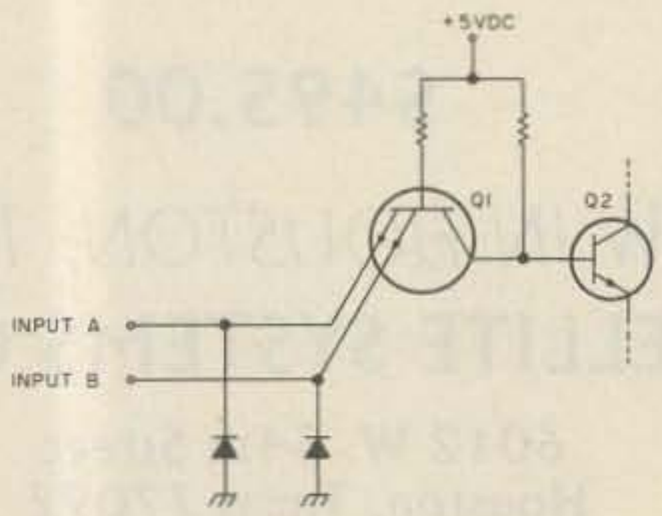

Fig. 1(c). TTL inputs.

a 16-mA output current sink capacity.) Some special devices called *buffers* or *line drivers* typically will have fan-outs of thirty, but up to one hundred are known.

Most TTL devices have an output circuit such as the one shown in Fig. 1(a). The output circuit is a totem-pole power amplifier consisting of two NPN transistors. A blocking diode prevents current flow from the output terminal through Q1 to the +5-volt power-supply line. When the output is low, transistor Q1 is turned off and Q2 is turned on. This places the output line at or near zero volts. The actual potential will be the Vce(sat) rating of Q2, which may be as much as 0.8 volts. In the opposite condition, when the output is high, the opposite occurs: Transistor Q1 is turned on and R2 is turned off. This places a potential on the output line that is the +5-volt power-supply voltage less the Vce(sat) rating of Q1 and the junction drop of the series diode (normally 0.6 to 0.7 volts).

An alternate form of TTL output is the *open-collector* circuit of Fig. 1(b). The open-collector device is used to drive external devices and is a prime tool in interfacing with other logic families as well as with the "outside world." Transistor Q1 will be connected to the V+ (which is not always +5 volts, even though the package power-supply voltage must be +5 volts dc) through a pull-up resistor or another form of load. Normally, if a simple pull-up resistor is used for the load, we will need 2000 to 3000 Ohms for +5-volt power supplies, and proportionally higher for higher potentials. TTL devices with open-collector outputs include the following hex inverters: 7405 (+5-volt supply only), 7406 (to +30 volts at up to 30 mA), 7416 (to +15 volts at up to 40 mA), and the following hex non-inverting buffers: 7407 (30 volts, 30 mA) and 7417 (15 volts, 40 mA). These devices are of prime concern for our interfacing chores. Note that certain other TTL devices also have open-collector outputs.

An example of a TTL input circuit is shown in Fig. 1(c). The device shown here is a two-input circuit as is found in each section of a device such as the 7400 two-input NAND gate. Each input will source up to 1.6 mA of current.

A CMOS inverter circuit is shown in Fig. 1(d). The typical CMOS device will have a pair of complementary MOSFET transistors connected in series with the output taken at the junction between the two. Transistor Q1 is a p-channel MOSFET, while Q2 is an n-channel MOSFET. These devices have opposite properties such that Q1 will be turned off (high-resistance channel) by a high applied to the input, while Q2 is turned on by a high on the input. Thus, for each different binary logic level, we will always have a series circuit consisting of a high resistance and a low (approximately 200 Ohms) resistance. For output-low conditions, there will be a high resistance to V+ (Q1 off) and a low resistance to V−(Q2 on). For the output-high condition, exactly the opposite occurs: there is a low resistance to V+ (Q1 on) and high resistance to V− (Q2 off).

Thus, we will see the CMOS output sink current on low and source current on high. Although this fact is not needed when interfacing CMOS-to-CMOS, it is useful for other interfacing chores.

The CMOS input is essentially an open circuit. CMOS devices operate using electrostatic fields derived in the channel from potentials applied to the gate terminal. This terminal is insulated by a thin metal-oxide layer and thus represents an immensely large resistance. Various

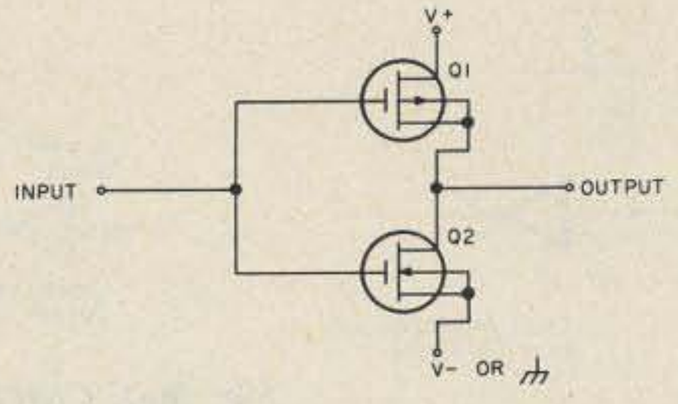

Fig. 1(d). CMOS inverter, showing inputs and outputs.

authorities quote not less than 1 megohm, with some going to 10^{12} Ohms. Thus, many CMOS devices can be driven from the same output with regard for current-driven capability. There may, however, be capacitance limitations, especially where a rapid rise time must be maintained.

Interfacing Between Logic Families

Fig. 2 illustrates some of the circuit situations required to interface between CMOS and TTL devices. Ordinarily, a single low-power (74L) or low-power Schottky (74LS) TTL device can be directly driven from a CMOS output, *provided* that the CMOS device is operated from a +5-volt power supply and ground. Normally, CMOS devices can operate with ±V of ±4.5 to ±15 volts dc; furthermore, these supplies need not be equal. We could, for example, operate from V+ =5 volts, and V− =0 volts (grounded). It is only this latter situation that will accommodate Fig. 2(a). Here the CMOS device will directly drive the 74L or 74LS TTL device. These TTL devices operate from lower current levels than does regular TTL.

Two specific CMOS devices will directly drive a single regular TTL input: the 4001 quad two-input NOR gate and the 4002 dual four-input NOR gate. See Fig. 2(b). Note that the B series CMOS (4001B) would probably drive more than one input.

Fig. 2(c) shows the use of the 4049 or 4050 devices. These devices are hex inverter and hex non-inverting buffers, respectively. They are specially designed to directly drive up to two regular TTL inputs (output current of 3.2 mA) *provided* that the 4049/4050 package is operated from +5 volts and ground, rather than some other V+/V− combination.

In Fig. 2(d) we see that a TTL output will drive a CMOS input (actually, several can be accommodated) provided that there is a current source. Recall that the TTL output wants to see a 1.6-mA to 16-mA current source for its load, while the CMOS input is an extremely high impedance. In order to keep the TTL device operating properly, we must pro-

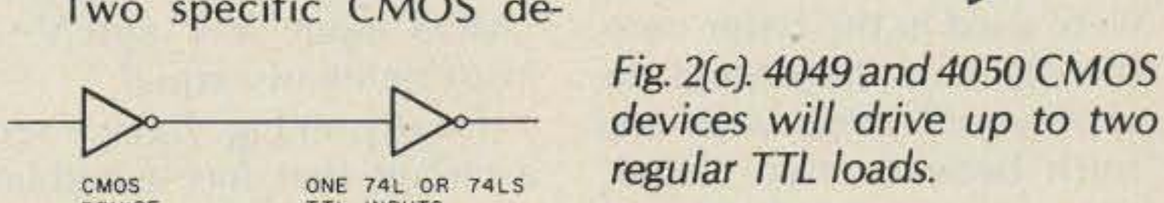

Fig. 2 (a). CMOS-to-74L or -74LS devices.

Fig. 2(b). 4001/4002 CMOS will drive one regular TTL load.

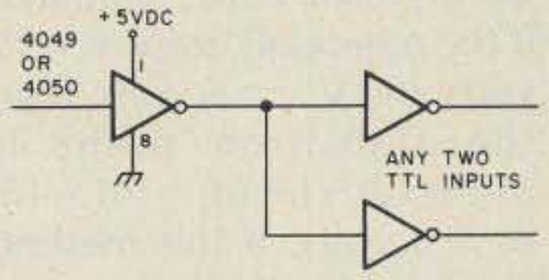

Fig. 2(c). 4049 and 4050 CMOS devices will drive up to two regular TTL loads.

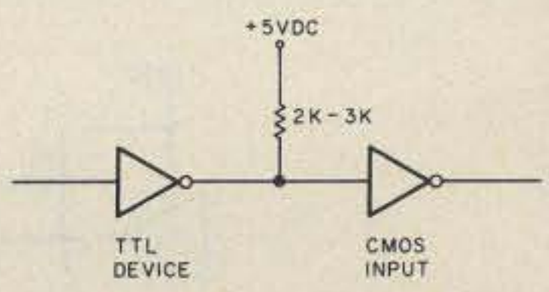

Fig. 2(d). TTL-to-CMOS (operated from +5 volt supply).

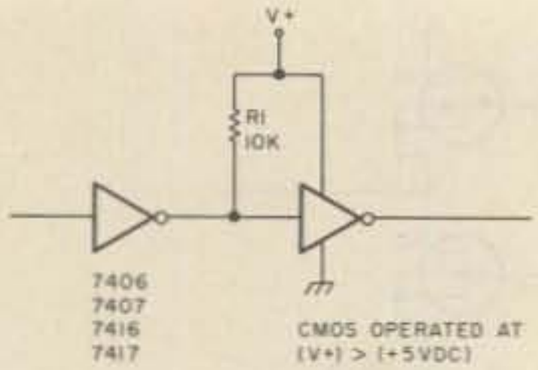

Fig. 2(e). TTL-to-CMOS (operated from V+ greater than +5 volts, and V− =0 volts).

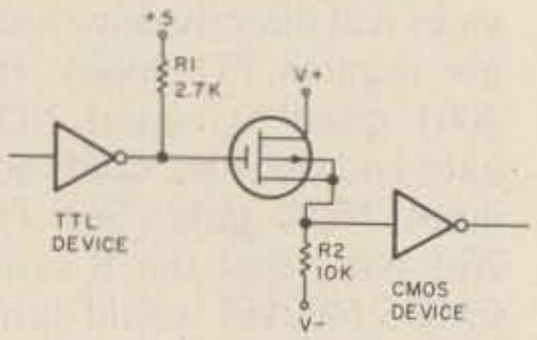

Fig. 2(f). TTL-to-CMOS (operated from ±V supplies).

vide a 2 to 3k-Ohm pull-up resistor between the TTL output and +5 volts dc. We must limit this method to those cases where the TTL voltage levels are compatible with the CMOS. If the CMOS device is operated from +5 volts and ground, then there is no problem.

Recall from the previous series on digital basics that the CMOS device output will go through a high/low or low/high transition when the input voltage is midway between the V+ and V− voltages. If, for example, the supplies are +5 volts and ground, then the transition occurs close to +2.5 volts. But, if the supplies are ±12 volts (or any other legal potential), then the transition occurs near zero. Similarly, if the potentials are V+ =12 volts and V− =6 volts, then the transition point is ½[(+12)−(−6)]=½(+18) or +9 volts. If this method were used in the latter case, the input of the CMOS device would jump back and forth between two "legal" low potentials, so the output would never toggle. In Fig. 2(e) we show you how to deal with that problem.

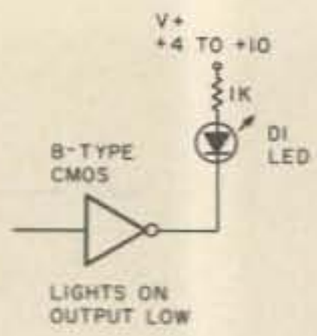

Fig. 3(a). CMOS light-on-output-low LED interfacing.

For those cases where the CMOS device operates from power-supply potentials other than +5 volts and ground, we will need a circuit such as the one in Fig. 2(e). Here we will use one of the "high-voltage" hex inverter IC devices discussed at the beginning of this article: 7406, 7407, 7416, and 7417 are candidates; 7405 can operate only from +5 volts, so it is ruled out. Note that the package power-supply voltage for these TTL devices *must* remain at +5 volts only, but the voltage applied to the open-collector output transistor via the pull-up resistor can be up to the CMOS V+ limit of +15 volts dc. A 10k-Ohm pull-up resistor will suffice.

Fig. 2(f) shows how to interface the TTL device with CMOS devices that are operated from bipolar power supplies instead of V− = 0. In this circuit, we use a MOSFET transistor (or one section of the CMOS 4007 device) in between the two logic devices. Resistor R1 provides a current source for the TTL output, while R2 limits the MOSFET current to a safe value and develops the potential applied to the CMOS input. V+ and V− must be nearly equal.

Finally, in Fig. 2(g) we see a circuit that has a certain universality. In most cases,

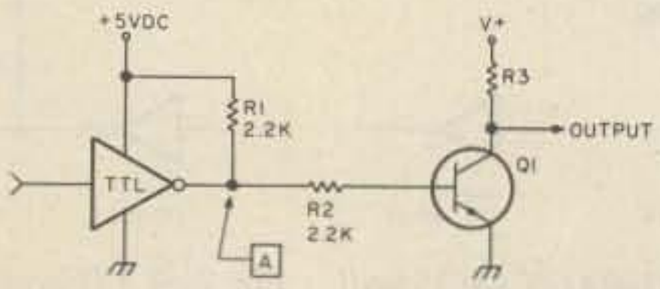

Fig. 2(g). Universal TTL to other logic devices.

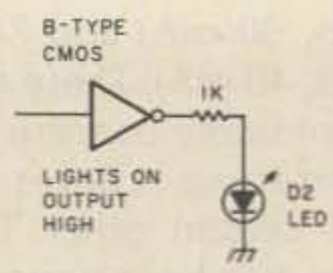

Fig. 3(b). CMOS light-on-output-high interfacing.

the function of this circuit will be to interface TTL to certain other higher-voltage logic families (such as CMOS operated from supplies over +5 volts, HNIL, HTL, etc.) In the majority of such instances, you will use a 7406, 7407, 7416, or 7417 device in place of transistor Q1, but this circuit may prove useful in some situations.

For example, in an existing device, there may be too little room to add an IC, but plenty of room to kludge on a 2N2222 or similar transistor. This situation turned up one time when I worked for a medical school electronics laboratory. It seems that one of the researchers had an elderly frequency/period counter that used zero and +12 volts as the logic levels, yet she wanted to interface this counter to a modern instrument that provided TTL output levels. The solution was to kludge R1–R3 and Q1 onto the PC board inside of the older instrument, and create a new input.

Register R1 is used, regardless of whether open-collector logic is used, and serves to provide a current for the TTL output to sink. When the TTL output is low, point A in Fig. 2(g) will be at zero potential, so the base of Q1 is turned off. Under this condition, the output is high (inverted). Similarly, when the output of the TTL device is high, the potential at point A is 3 to 4 volts, so it can bias the base of Q1 on. Under this condition, the transistor is saturated and will produce a low output. This method is useful so long as an inverted output is sufficient. Otherwise, cascade two similar stages. I

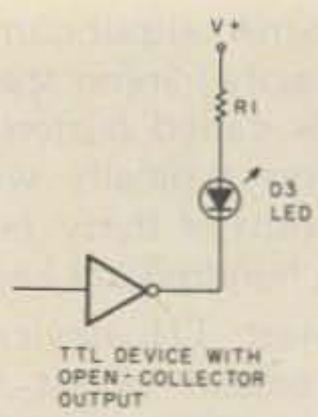

Fig. 3(c). TTL open-collector LED interfacing (circuit will also drive very-low-current lamps).

suspect, however, that any situation where cascading two Q1 stages is feasible will also permit the kludge of a 14-pin DIP, thereby making the use of the hex inverter the preferred method.

Interfacing Lamps and LEDs

Incandescent lamps and light-emitting diodes (LEDs) are often used in digital instruments to indicate logic status or to signal some event like the completion of a process, etc. The B series CMOS devices can often be interfaced directly with light-emitting diodes, provided that no more than about 15 mA of current will light the LED to an acceptable brightness (the usual case). The A series devices are not able to do this neat trick because they have as little as one-third the current sinking/sourcing capability of the B series devices.

Figs. 3(a) and (b) show the use of direct interfacing between a B series CMOS device and the low-current LED. The circuit in Fig. 3(a) uses the LED as a pull-up between the CMOS output and the positive power supply and will cause the LED to light on any output-low condition. The CMOS output in this case operates as a current source to ground. In Fig. 3(b), the LED is connected between the CMOS output and ground and will light only on output-high conditions. In this case, the CMOS output is used as a current source.

Fig. 3(c) shows the use of an open-collector TTL device to drive the LED. If V+

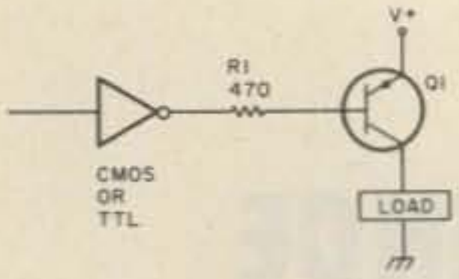

Fig. 3(d). Incandescent lamp interfacing with PNP transistor.

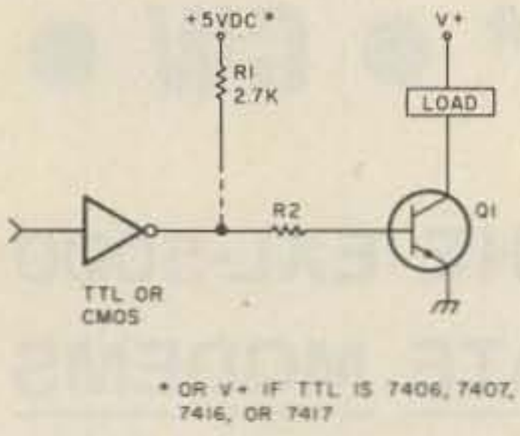

Fig. 3(e). Incandescent lamp interfacing with NPN transistor.

is +5 volts, then the 7405 device may be used. The 7406, 7407, 7416, and 7417 devices may also be used at +5 volts or any potential up to the rated potential for the specific device (+15 or +30, depending upon type). Resistor R1 is used to limit the current through the LED and the TTL output to a safe value, usually 15 mA. The value of R1 is given by Ohm's law: $R1=(V+)/I_{LED}$ or V+/0.015 if the 15-mA figure is acceptable. In this circuit, the TTL device operates as a current sink for the LED and will light on output-low.

Incandescent lamps typically draw a lot more current than LEDs. Some small current lamps ("grain-of-wheat" lamps) will operate directly from the 7417 TTL device, but most require too much current for safe operation directly from TTL. We can, however, use the TTL (or CMOS) device to drive a transistor switch that will, in turn, operate the lamp or other load. This situation is depicted in Figs. 3(d) and 3(e). In Fig. 3(d) we see the use of a PNP transistor to turn on the load. When the base of Q1 is made low, then the base-emitter potential is proper to turn on transistor Q1; current will flow in the c-e path to the load. If, however, the logic output is high, then the base-emitter voltage is nearly zero, so the transistor is cut off.

Fig. 3(e) shows the use of an NPN transistor for Q1. While the lamp in Fig. 3(d) will turn on for output-low, the circuit shown in Fig. 3(e) turns on for output-high. Again, either TTL or CMOS devices can be used, within certain limitations. One limitation applied to TTL devices is that a pull-up resistor (R1) be provided so that the TTL output sees a current source. For CMOS devices, we must use a transistor that has a high enough beta gain that it will saturate with the current available from the CMOS output. Resistor R2 is used to limit the current applied to the base of Q1. When the IC output is high, then a current flows in R2 that will turn on the transistor. Under that condition Q1 is saturated, so its collector will be at or near ground potential. This condition makes the load see a current flow, so if it is a lamp then it will light up.

Large loads, i.e., those of high current but limited voltage, can be accommodated with the circuit of Fig. 4. Here we extend Fig. 3(e) to account for the higher currents of the load. There are two transistors used in this circuit. In most cases, we will use a "driver" transistor such as the 2N3053 for Q1 and a "power" transistor such as the 2N3055 for Q2. Note that some semiconductor manufacturers offer TO-3 packages containing both Q1 and Q2 and term the combination "Darlington" transistors after the fact that the circuit in which these transistors are connected is called a "Darlington amplifier" or "Darlington pair."

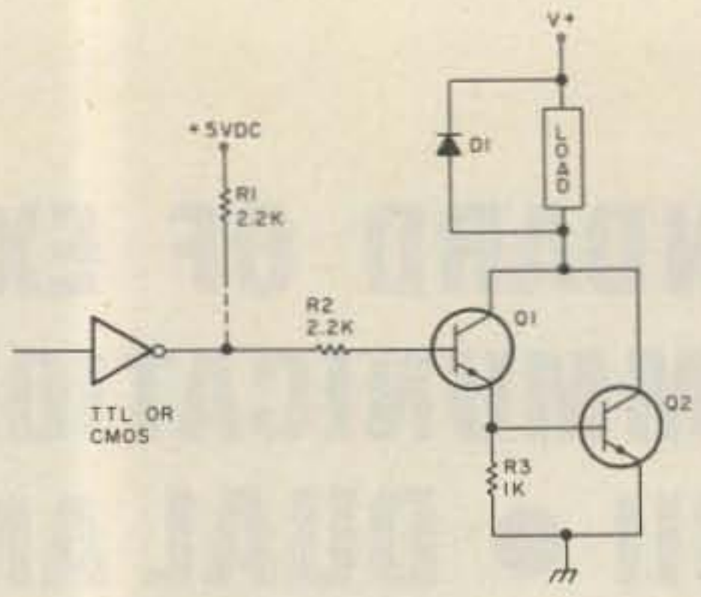

Fig. 4. Driving large loads using Darlington-pair transistors.

The advantage of this circuit is the amplification of beta (H_{fe}) that occurs. The total beta is the product of the individual beta ratings, or: $H_{fe(total)} = H_{fe(Q1)} \times H_{fe(Q2)}$. If you recall your basic transistor theory, the beta is defined as the collector current divided by the base current, or I_c/I_b. For example, if the beta of Q1 is 80 and the beta of Q2 is 50, then the total beta is (80)(50) or 4,000. The implication of this is that the drive current need only be 1/4000 of the load current! Let's assume that there will be approximately 1.2 mA available to drive the Darlington pair when the TTL output is high. With a beta of 4000, the load current will be more than 4 Amperes! Of course, a transistor must be selected for Q2 that will "hack" the current of the load.

The diode shown in parallel with the load is advisable for all creative (capacitive or inductive) loads, and for most very high current loads. It is especially necessary in inductive-load circuits, for example, when the load is a relay or solenoid coil. The problem is the inductive spike produced by an inductor energized with dc when the circuit is interrupted. Under this circumstance, the energy stored in the magnetic field around the inductor will collapse and the counter-electromotive force generated will be opposite the polarity of V+ and will have a very high value (kilovolts are possible). If you have studied calculus, then you will see that V = L(dI/dt) can reach a very high number in the situation where the current flow is abruptly terminated (dI/dt is negative and has a rapid fall time).

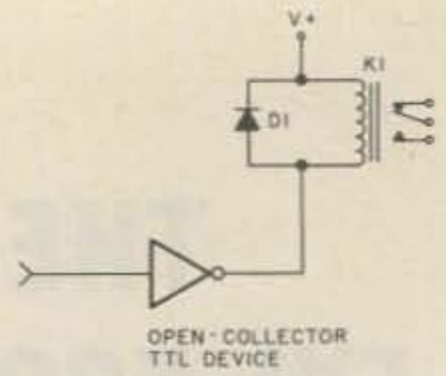

Fig. 5(a). Interfacing open-collector TTL to low-current relays.

The diode is reverse-biased most of the time but will conduct when the CEMF potential is applied. Since the potential can easily reach hundreds of volts in practical situations, the diode must have a piv rating of 1000 volts or more. I recommend 1N4007 for all but very heavy inductive loads; for heavier cases, use series-connected 1N4007 devices with each diode shunted by a 470k-Ohm-to-1-megohm, ½-Watt, carbon resistor.

Fig. 5 shows two situations where electromechanical relays—those workhorses of electricity/electronics left over from the 19th century but still viable—are interfaced with digital IC devices.

In Fig. 5(a) we see the use of an open-collector TTL device for directly interfacing with a low-current relay. Some manufacturers offer low-current (40-mA and under) relays, both in regular relay packages and in packages resembling IC packages (both metal-can and DIP packages are available). Keep in mind the voltage and current limitations of the 7406, 7407, 7416, and 7417 devices listed at the beginning of this article.

For heavier relays, we will

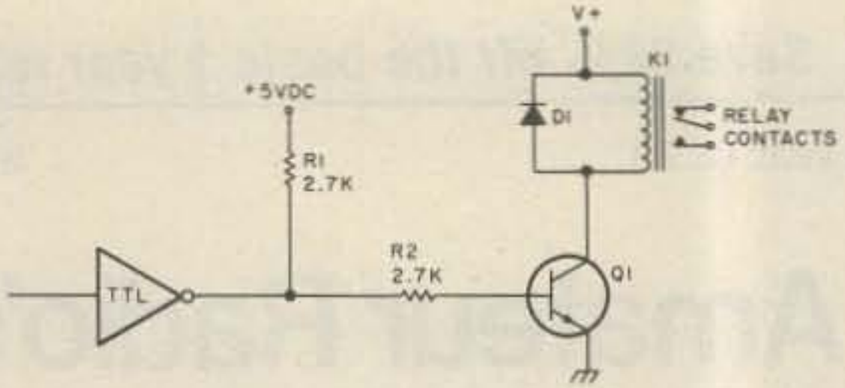

Fig. 5(b). Interfacing TTL or CMOS to higher-current relays.

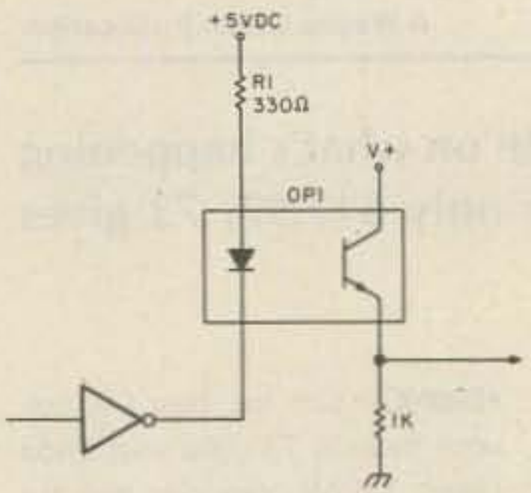

Fig. 6. Driving an isolated load.

use a switching transistor, as in Fig. 5(b). This is merely an extension of the earlier circuits. The diode transient suppressors are mandatory, however. If these are not used, especially in Fig. 5(a), the high voltage transient will blow the semiconductor.

Relays are used for many applications. Of course, if the current is too high to be conveniently handled by the semiconductor, then a relay is in order. But, today, we have numerous high-current power transistors and Darlington devices, so this application is fading. The isolation provided by the relay, however, makes it attractive whenever the logic device must be interfaced with a high-voltage circuit, or the ac power lines (115 volts ac).

Finally, we see one further method for providing isolation between a digital circuit and some outside-world load. There are devices called *optoisolators* (Fig. 6) available in which an LED and either a phototransistor or a photodiode are placed such that the LED will illuminate the transistor/diode (whichever). The pair is housed inside of an opaque DIP package that has the same 0.1" × 0.3" pinouts as the digital IC devices in the circuit. When the LED is turned on, i.e., when the logic device output is low, then the phototransistor base is illuminated, so the transistor is turned on. Under this condition, the output will be a potential close to V+. When the LED is extinguished, i.e., when the logic output is high, then the phototransistor base is turned off and there will be no voltage across the load resistor. In most cases, the dangerous isolated circuit will be on the transistor side of the optoisolator. In some cases, however, the dangerous side of the circuit will *send* the signal and thus will be on the LED side.

Conclusion

The advantages of digital logic are even greater when we can interface either between logic families or to the outside world. The techniques in this article allow us, among other things, to interface elderly digital equipment obtained on the surplus market to modern equipment, or to interface essentially non-digital circuits (control) that are still binary in nature to some digital instrument. For example, a trivial case would be the push-to-talk circuit on a transmitter. As another example, the transmitter control circuit on a linear power amplifier could be placed under control of a computer in which the digital interfacing is between a 3.2 mA (fan-out = 2) output port terminal and the radio equipment. Lots of luck.■