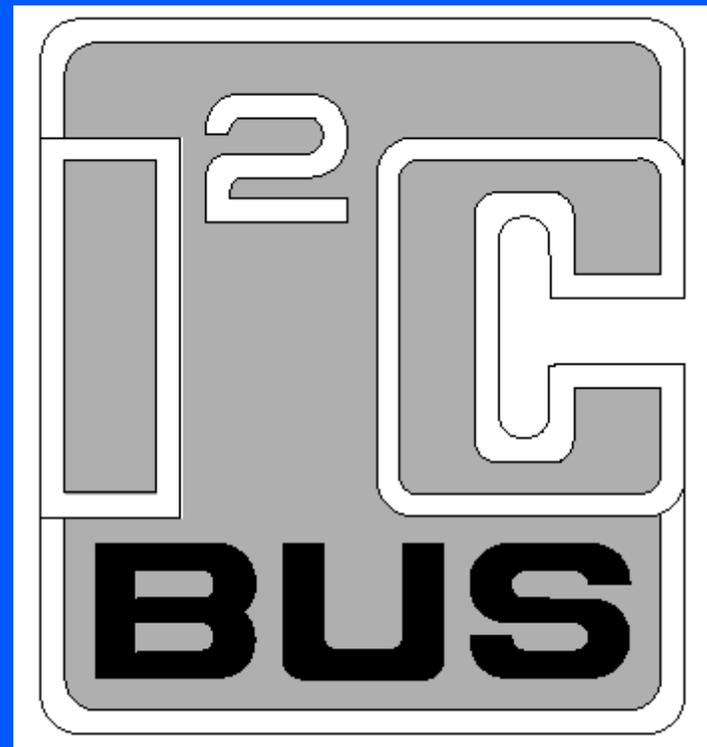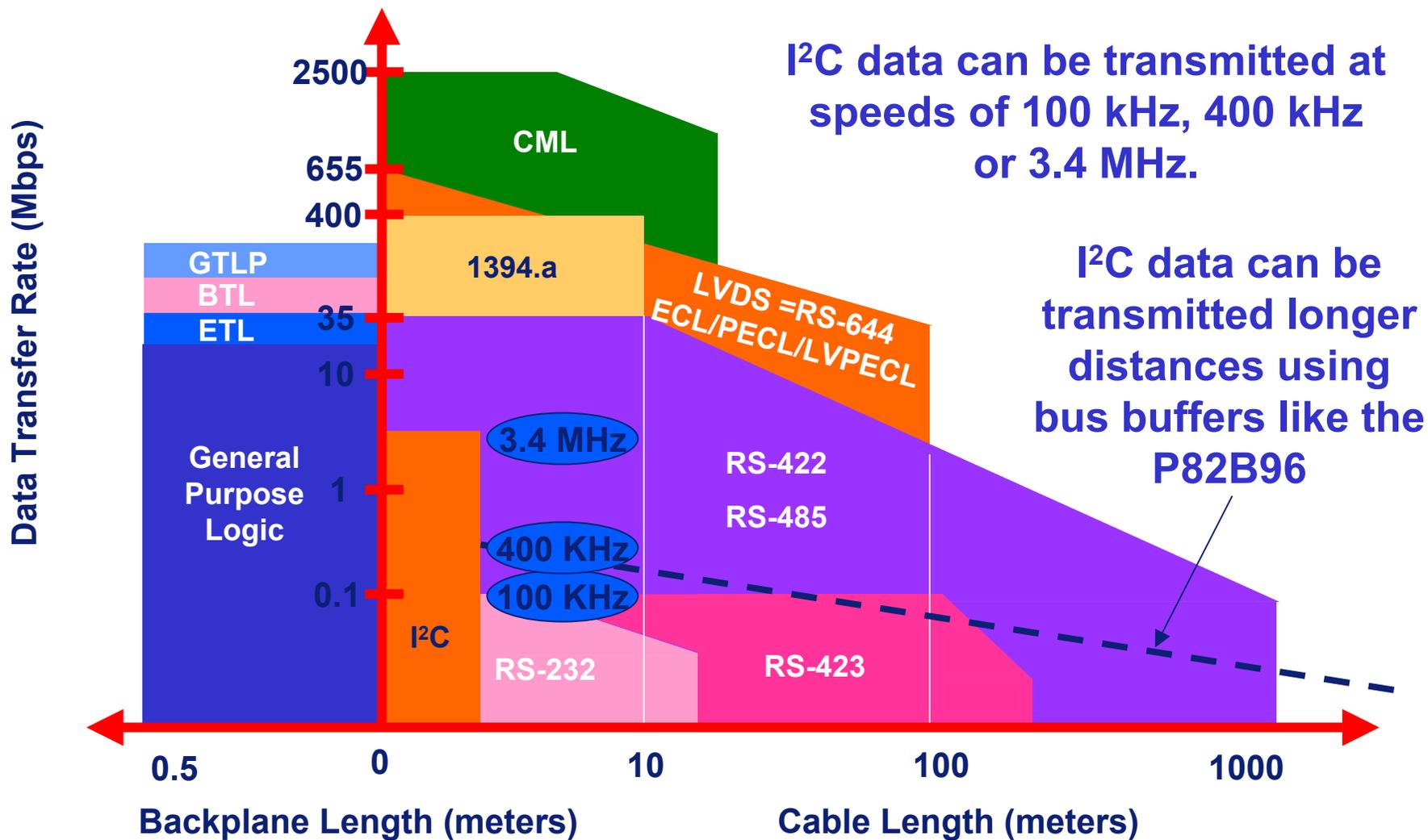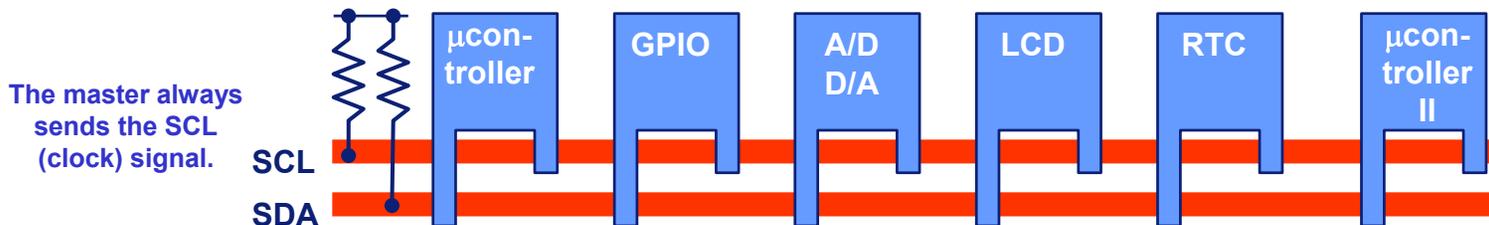# PHILIPS

I^{2}C Overview

2H 2003

Agenda

- **What is I^{2}C and why would you be interested in using the I^{2}C bus?**

- **What new I^{2}C devices are there and what are the typical applications?**

- **How are we going to help you design-in these devices?**

I^{2}C Bus Basics - Address and Data

μcon-troller | GPIO | A/D D/A | LCD | RTC | μcon-troller II

SCL
SDA

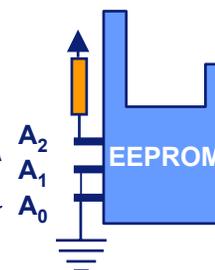**The master always sends the SCL (clock) signal.**

Each device is addressed individually by software with a unique address that can be modified by hardware pins.

The open drain/collector outputs provide for a "wired-AND" connection that allows devices to be added or removed without impact and always require a pull-up resistor.

$$1010A_2A_1A_0R/\overline{W}$$

$$1010100R/\overline{W}$$

A_2
A_1
A_0

EEPROM

New devices or functions can be easily 'clipped on to an existing bus!

Write data

S	slave address	$\overline{W}$	A	data	A	data	A	P

< n data bytes >

Master   Slave

| transmitter | | receiver |

Read data

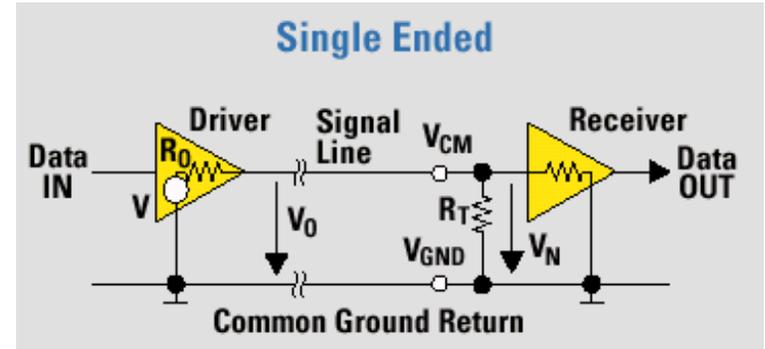| S	slave address	R	A	data	A	data	$\overline{A}$	P

< n data bytes > last data byte

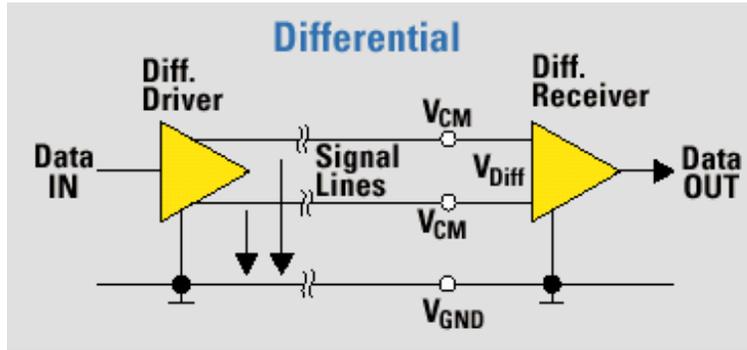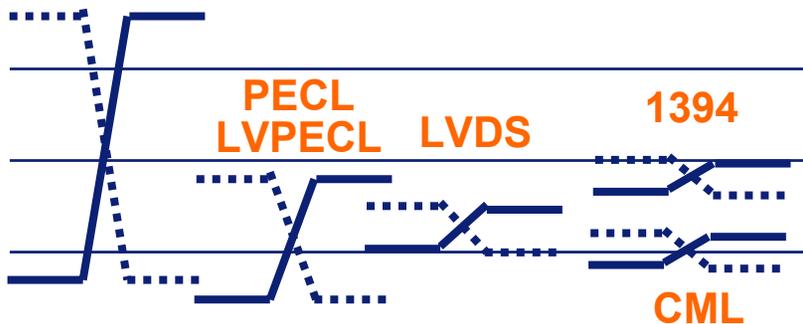| receiver | | transmitter |
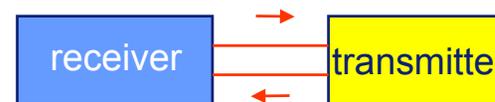
S = Start condition
A = Acknowledge
P = Stop condition

$R/\overline{W}$ = read / write not
$\overline{A}$ = Not Acknowledge

Semiconductors

Typical Signaling Characteristics
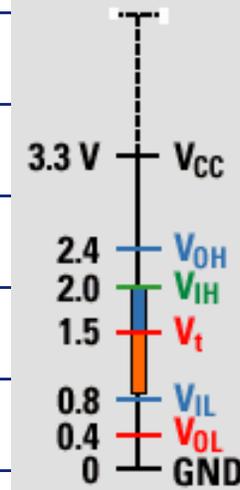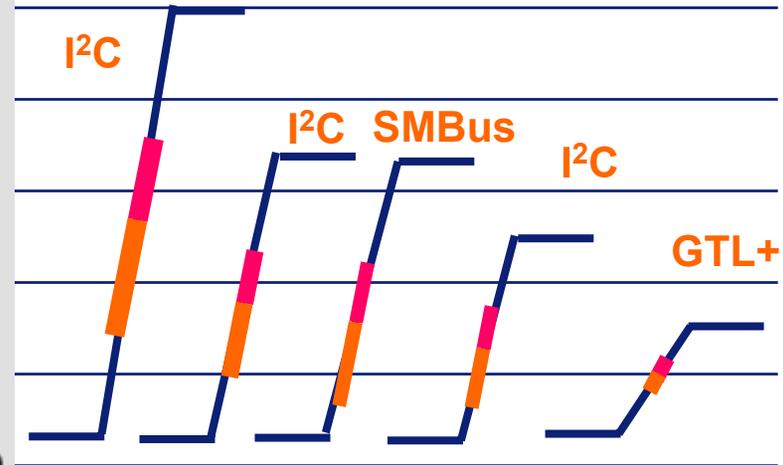
I^{2}C by the numbers

	Standard-Mode	Fast-Mode	High-Speed-Mode	
Bit Rate (kbits/s)	0 to 100	0 to 400	0 to 1700	0 to 3400
Max Cap Load (pF)	400	400	400	100
Rise time (ns)	1000	300	160	80
Spike Filtered (ns)	N/A	50	10	
Address Bits	7 and 10	7 and 10	7 and 10	

Rise Time

V_{DD}
V_{IH} — 0.7 $_x$ V_{DD}
V_{IL} — 0.3 $_x$ V_{DD}
V_{OL} — 0.4 V @ 3 mA Sink Current
GND

Semiconductors
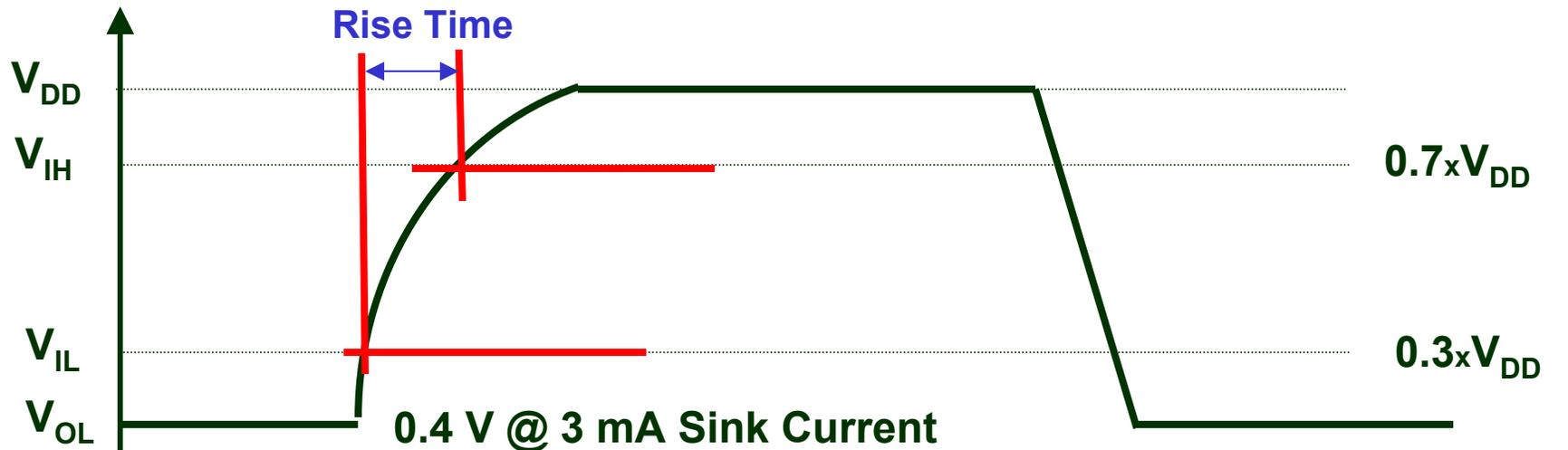
I^{2}C Bus Basics - Bus Operation
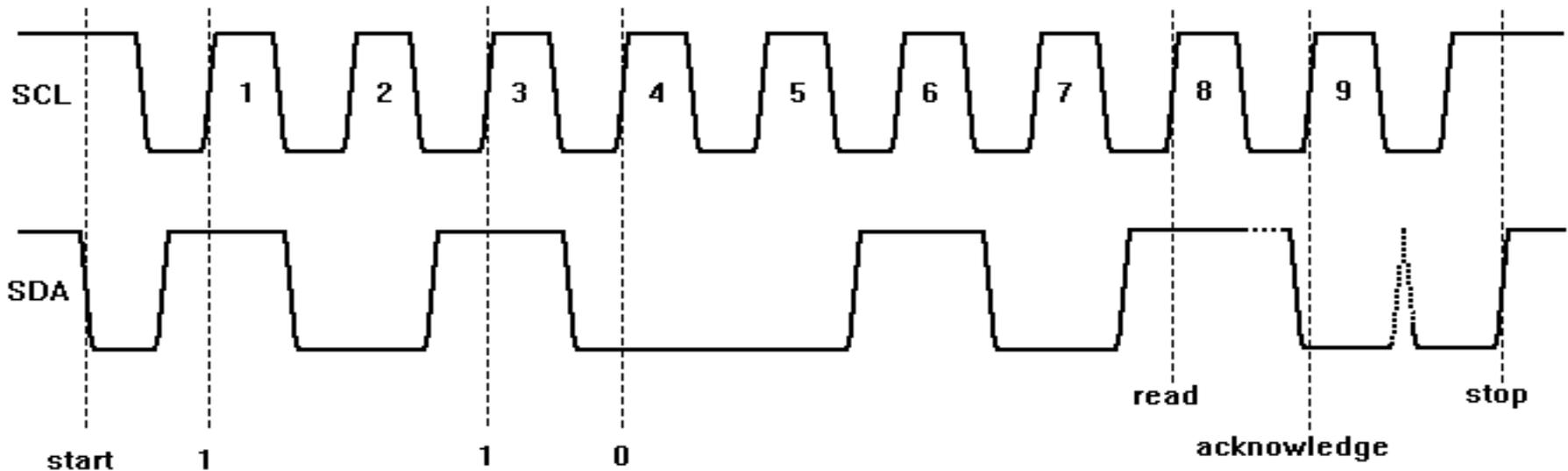
The SCL falling edge 'requests' data when reading, or 'advises' data coming when writing

The SDA data <u>changes</u> during the SCL low and is <u>used</u> during or just after the SCL rising edge

Typical bus communication waveforms

The I^{2}C specification and other useful application information can be found on Philips Semiconductors I^{2}C web site at
www.semiconductors.philips.com/i2c

I^{2}C Bus Features

• Only 2 bus lines required: data (SDA) and clock (SCL)

• Each device connected to the bus is software addressable by a unique address

• 2 modes: Master-Transmitter and as Master-Receiver

• Multi-master capable protocol:

> ➢ collision detection

> ➢ arbitration

• Serial bi-directional data transfers:

> ➢ 100 kbit/s   Standard-mode

> ➢ 400 kbit/s   Fast-mode

> ➢ 3.4 Mbit/s   High-speed mode

• Maximum bus capacitance = 400 pF (without repeaters) which is about 20 – 30 devices or 10 ft of wire (100 pF/meter)

I^{2}C Bus Benefits

- Well known bus:
    - Created and developed by Philips
    - More than 20 years of existence
    - Has become a world-wide standard
- Standard adopted by all the industry:
    - Computing   - Networking   - Automotive
    - Industrial   - Telecom   - Consumer
- Used in many types of applications:
    - PC   - DVD   - Cell Phones
    - Printers   - Set Top Boxes   - PDA
- Adopted by a lot of leading High-Tech companies
    - Intel   - IBM   - Compaq
    - Nokia   - Cisco   - HP
- Life of products: designed to stay in the market several years

I^{2}C Designer Benefits

• No need to design bus interfaces because the I^{2}C-bus interface is already integrated on-chip.

• Integrated addressing and data-transfer protocol allow systems to be completely software-defined.

• The same IC types can often be used in many different applications.

• ICs can be added to or removed from a system without affecting any other circuits on the bus.

• Fault diagnosis and debugging are simple; malfunctions can be immediately traced.

• Software development time can be reduced by assembling a library of reusable software modules.

I^{2}C Manufacturer Benefits

- Simplicity: 2 wire protocol
    - Minimum inter connections
    - Minimum footprint
    - Simpler, smaller and less expensive PCB
- Robustness of the protocol
    - Completely integrated protocol
    - No need for address decoding and "glue logic"
    - Interrupt oriented architecture
    - Multi-master capable
- Upgrade path:
    - Speed: 100 kHz → 400 kHz
    - Modular architecture allowing easy design and architecture updates and upgrades

I^{2}C Product Characteristics

- Package Offerings
  - Typically SO, TSSOP and HVQFN packages
- Frequency Range
  - Older devices 100 kHz operation
  - Newer devices operating up to 400 kHz
  - Graphic devices up to 3.4 MHz
- Operating Supply Voltage Range
  - 2.5 to 5.5 V or 2.8 to 5.5 V
  - Newer devices at 2.3 to 5.5 V or 3.0 to 3.6 V with 5 V tolerance
- Operating temperature range
  - Typically -40 to +85 ºC
  - Some 0 to +70 ºC
- Hardware address pins
  - Typically three (A_O, A_1, A_2) are provided to allow up to eight of the identical device on the same I^{2}C bus but sometimes due to pin limitations there are fewer address pins

TSSOP

HVQFN

SO

4 mm x 4 mm

24 pin 16-bit PCA9555 shown
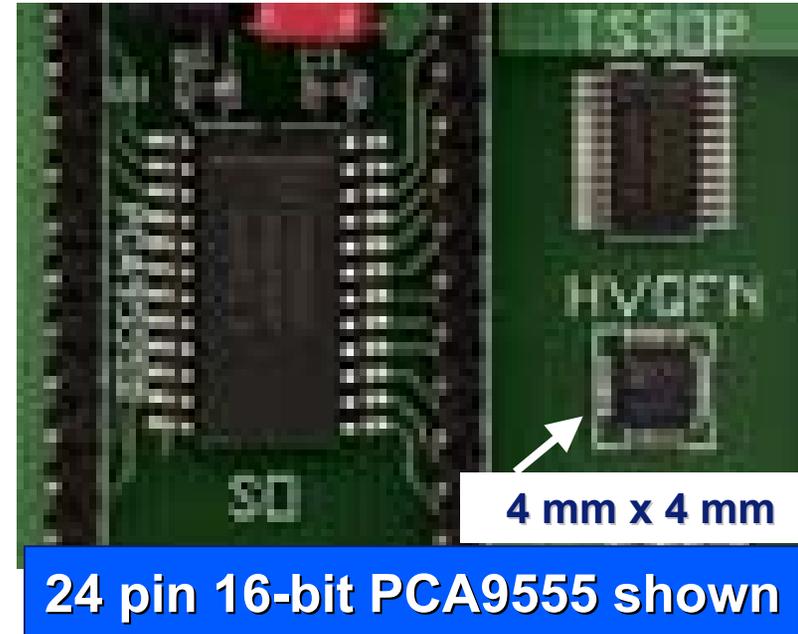
I^{2}C Patent and Legal Information

• The I^{2}C bus is protected by patents held by Philips. Licensed IC manufacturers that sell devices incorporating the technology already have secured the rights to use these devices, relieving the burden from the purchaser.

• A license is required for implementing an I^{2}C interface on a chip (IC, ASIC, FPGA, etc). It is Philips's position that all chips that can talk to the I^{2}C bus must be licensed. It doesn't matter how this interface is implemented. The licensed manufacturer may use its own know how, purchased IP cores, or whatever.

• This also applies to FPGAs. However, since the FPGAs are programmed by the user, the user is considered a company that builds an I^{2}C-IC and would need to obtain the license from Philips.

• Apply for a license or text of the Philips I^{2}C Standard License Agreement
    • US and Canadian companies: contact Mr. Piotrowski (I2C.Support at philips.com)
    • All other companies: contact Mr. Hesselmann (I2C.Support at philips.com)

Agenda

- **What is I^{2}C and why would you be interested in using the I^{2}C bus?**

- **What new I^{2}C devices are there and what are the typical applications?**

- **How are we going to help you design-in these devices?**

Philips Semiconductors I^{2}C Devices Overview

- **TV Reception**
- **Radio Reception**
- **Audio Processing**
- **SMART Card Interface**
- **DTMF**
- **LCD display control**
- **Clocks/timers**

- **General Purpose I/O**
- **LED display control**
- **Bus Extension/Control**
- **A/D and D/A Converters**
- **EEPROM/RAM**
- **Hardware Monitors**
- **Microcontroller**

I^{2}C devices are broken down into 14 different categories

**Philips offers over 400 different I^{2}C devices**

TV Reception

The SAA56xx family of microcontrollers are a derivative of the Philips industry-standard 80C51 microcontroller and are intended for use as the central control mechanism in a television receiver. They provide control functions for the television system, OSD and incorporate an integrated Data Capture and display function for either Teletext or Closed Caption.
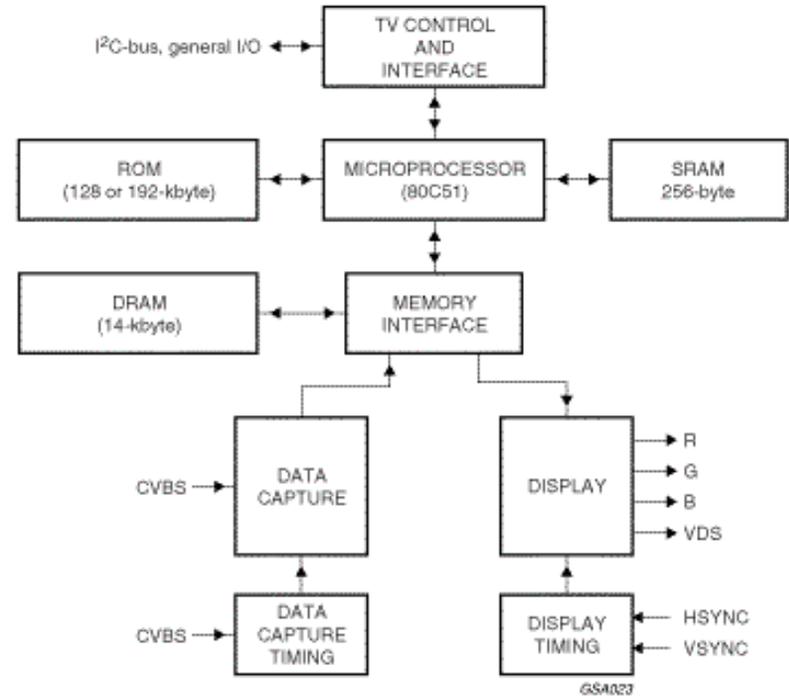
Additional features over the SAA55xx family have been included, e.g. 100/120 Hz (2H/2V only) display timing modes, two page operation (50/60 Hz mode for 16:9, 4:3), higher frequency microcontroller, increased character storage, more 80C51 peripherals and a larger Display memory. For CC operation, only a 50/60 Hz display option is available.

Byte level I²C-bus up to 400 kHz dual port I/O

Radio Reception
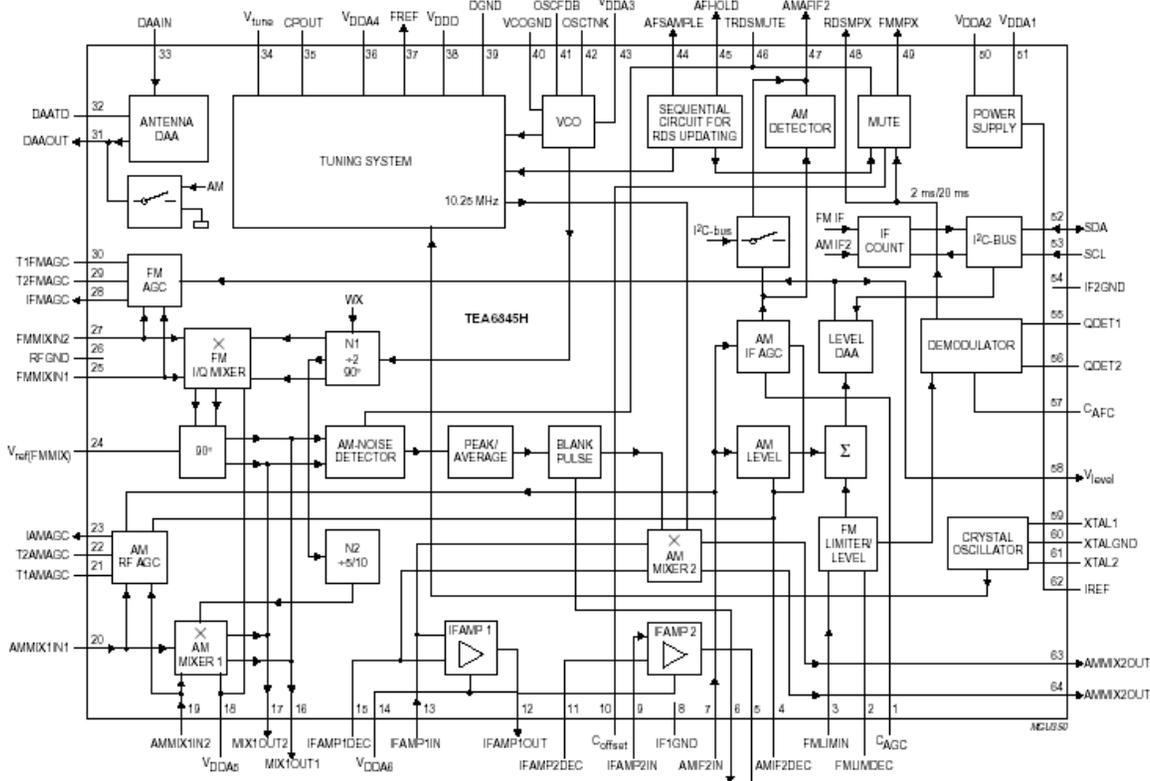
The TEA6845H is a single IC with car radio tuner for AM and FM intended for microcontroller tuning with the I²C-bus. It provides the following functions:

• AM double conversion receiver for LW, MW and SW (31 m, 41 m and 49 m bands) with IF1 = 10.7 MHz and IF2 = 450 kHz

• FM single conversion receiver with integrated image rejection for IF = 10.7 MHz capable of selecting US FM, US weather, Europe FM, East Europe FM and Japan FM bands.

Audio Processing

The SAA7740H is a function-specific digital signal processor. The device is capable of performing processing for listening-environments such as equalization, hall-effects, reverberation, surround-sound and digital volume/balance control. The SAA7740H can also be reconfigured (in a dual and quad filter mode) so that it can be used as a digital filter with programmable characteristics.
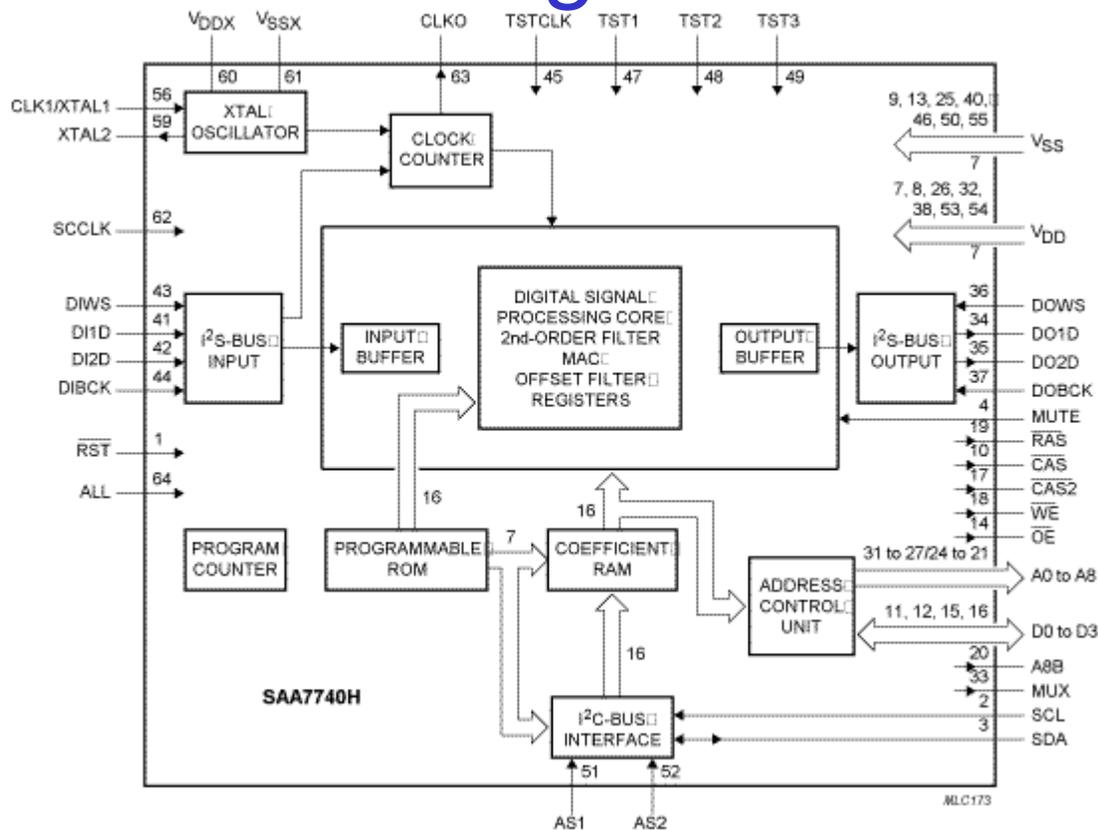
The SAA7740H realizes most functions directly in hardware. The flexibility exists in the possibility to download function parameters, correction coefficients and various configurations from a host microcontroller. The parameters can be passed in real time and all functions can be switched on simultaneously. The SAA7740H accepts 2 digital stereo signals in the I2S-bus format at audio sampling frequency (fast) and provides 2 digital stereo outputs.

SMART Card Interface - TDA8003
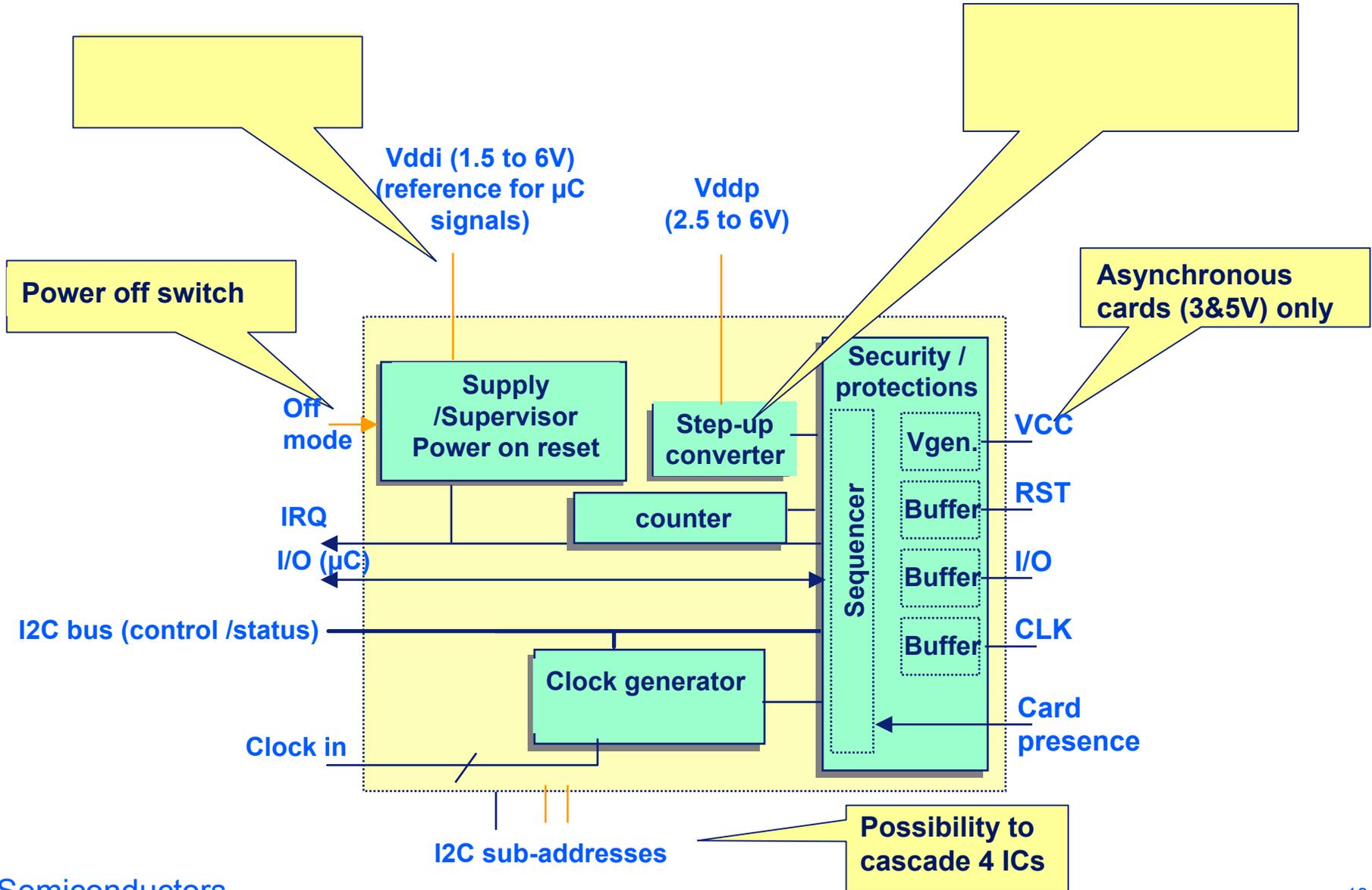
SMART Card Interface - OM5926HN

Reference voltage from the Host

Vddi (1.5 to 6V) (reference for µC signals)

Vddp (2.5 to 6V)

40000 clock cycles counter for ATR sequence

Power off switch

Asynchronous cards (3&5V) only

Off mode

Supply /Supervisor Power on reset

Step-up converter

Security / protections

Vgen.

Vcc

counter

Buffer

RST

Sequencer

I/O (µC)

Buffer

I/O

I2C bus (control /status)

Buffer

Clk

Clock generator

Clock in

SMART Card - Telecom Terminal Application

Single Slot application

| Single chip baseband — ISO UART | iso | TDA8003 or OM5926 | iso | SIM/WIM card |

or

| Single chip baseband | RS232 or I²C | TDA8029 | iso | SIM/WIM or banking card |

Dual slot application

Single chip baseband

| ISO UART | iso | TDA8003 or OM5926 | iso | SIM card |

| RS232 or I²C | TDA8029 | iso | Banking card |
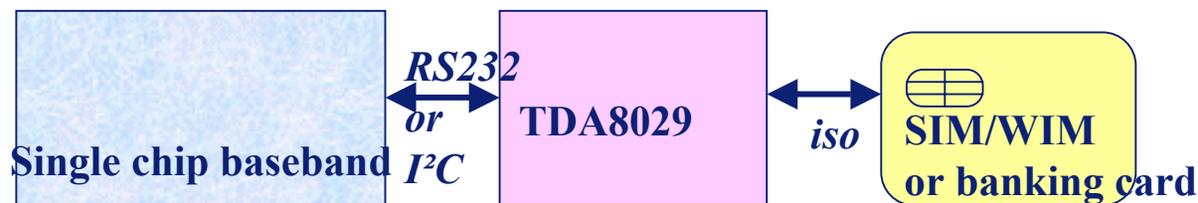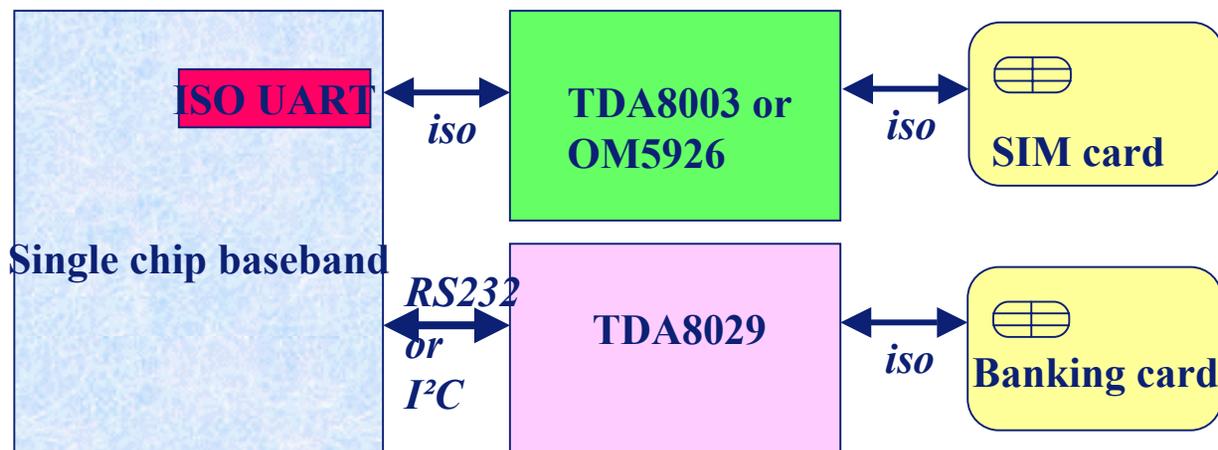
SMART Card Interface - TDA8023

SMART Card Interface - TDA8020

AVDD = 2.7V to 6V

reset delay

Supply /Supervisor Power on reset

Step-up converter

SCL
SDA
IRQ
A0
A1

I²C bus Control & Status

clock circuit

CLKIN1
CLKIN2

internal oscillator

I/O µC1
I/O µC2

Level shifters

$V_{DD}I$(1.8 to 6.5V)

clock circuit

Sequencer

V gen.
Buffer
Buffer
Buffer

VCC1
RST1
I/O1
CLK1
Card presence1
CGND1

Sequencer

V gen.
Buffer
Buffer
Buffer

VCC2
RST2
I/O2
CLK2
Card presence2
CGND2

Semiconductors

DTMF/Modem/Musical Tone Generators
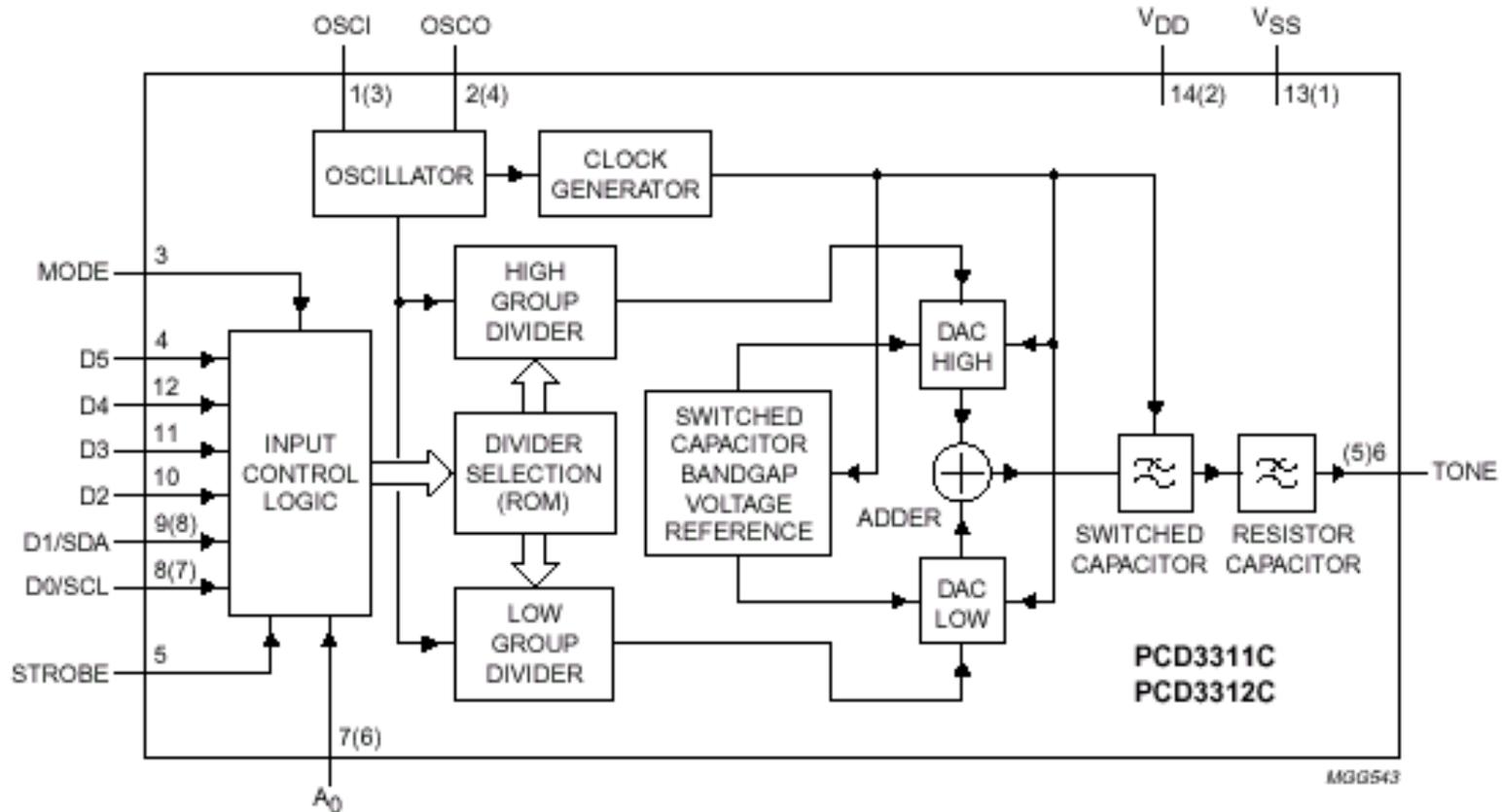
- Modem and musical tone generation
- Telephone tone dialing
  - DTMF > Dual Tone Multiple Frequency
- Low baud rate modem

I2C LCD Display and Segment Drivers

LCD Display Control

**Display size:
2 line by 12 characters +
120 icons**

21/03   16:27
WELCOME

Column driver
Row driver
Sequencer
DDRAM
CGRAM
CGROM
Control logic
Bias voltage generator
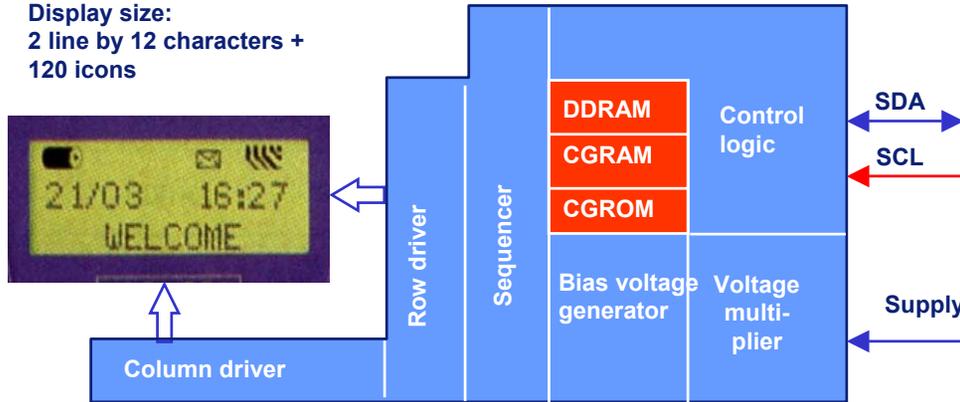Voltage multi-plier
SDA
SCL
Supply

The LCD Display driver is a complex device and is an example of how "complete" a system an I2C chip can be – it generates the LCD voltages, adjusts the contrast, temperature compensates, stores the messages, has CGROM and RAM etc etc.

LCD Segment Control

**Display sizes single chip: 1 x 24 … 2 x 40…
4 x 40 ... 16 x 24**

The LCD Segment driver is a less complex LCD driver (e.g., just a segment driver).

Control logic
SDA
SCL
RAM
Supply
Bias voltage generator
Sequencer
Backplane drivers
Segment drivers
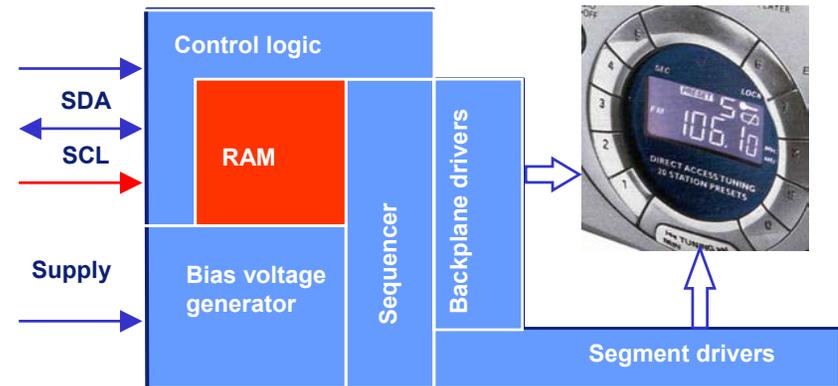
I²C LCD Display and Segment Drivers

LCD Character Driver

• PCF2104 LCD controller/driver

• PCF2113x LCD controllers/drivers

• PCF2116x LCD controller/drivers

• PCF2119x LCD controllers/drivers

LCD Graphic Black/White Driver

• OM6217 67 x 96 pixel matrix LCD driver

• PCF8531 34 x 128 pixel matrix driver

• PCF8535 65 x 133 pixel matrix driver

• PCF8548 65 x 102 pixels matrix LCD driver

• PCF8811M 80 x 128 pixels matrix LCD driver

• PCF8811 80 x 128 pixels matrix LCD driver

• PCF8813 67 x 102 pixels matrix LCD driver

• PCF8814 65 x 96 pixels matrix LCD driver

LCD Graphic Gray Scale Driver

• PCF8820 67 x 101 Grey-scale/ECB color dot matrix LCD driver

• OM6208 65 x 96 Grey-scale/ECB color dot matrix LCD driver

LCD Segment Driver

• OM4085 Universal LCD driver for low multiplex rates

• PCF8533 Universal LCD driver for low multiplex rates

• PCF8566 Universal LCD driver for low multiplex rates
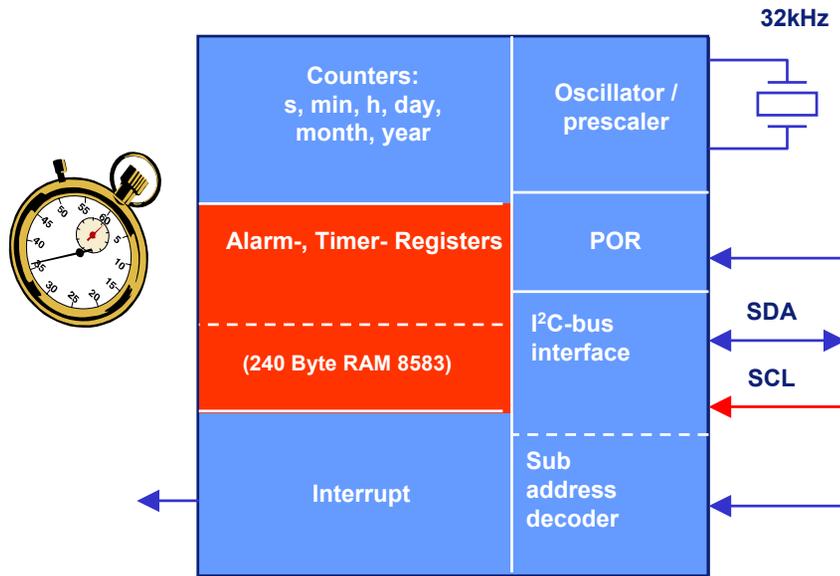
• PCF8576C Universal LCD driver for low multiplex rates

• PCF8576D Universal LCD driver for low multiplex rates

• PCF8577C Universal LCD driver for low multiplex rates

• PCF8578 LCD row/column driver for dot matrix graphic displays

• PCF8579 LCD column driver for dot matrix graphic displays

LED Segment Driver

• SAA1064 4-digit LED-driver with I²C-Bus interface

I^{2}C Real Time Clock/Calendar

Real-Time Clock / Calendar

Counters: s, min, h, day, month, year	Oscillator / prescaler	32kHz
Alarm-, Timer- Registers	POR	
(240 Byte RAM 8583)	I^{2}C-bus interface	SDA SCL
Interrupt	Sub address decoder	

The RTC is used to provide absolute timing to devices on the I^{2}C Bus.
The latest RTC is the PCF8565 which is the automotive temp range version of the PCF8563 low current consumption RTC.
The PCF8583 has 240 bytes 'scratchpad' RAM integrated with the RTC.

- PCA8565 Real time clock/calendar
- PCF8563 Real time clock/calendar
- PCF8573 Clock/calendar with serial I/O
- PCF8583 Clock/calendar with 240 x 8-bit RAM
- PCF8593 Low power clock/calendar

I2C Controlled Clock Generation

PCK2023 CK408 (66/100/133/200MHz) Spread Spectrum Differential System Clock Generator

The PCK2023 is a clock synthesizer/driver for a Pentium IV and other similar processors. The PCK2023 has three differential pair CPU current source outputs. There are ten PCI clock outputs running at 33 MHz and two 48 MHz clocks. There are six 3V66 outputs. Finally, there is one 3.3 V reference clock at 14.318 MHz. All clock outputs meet Intel's drive strength, rise/fall times, jitter, accuracy, and skew requirements.

I2C is used to turn options on/off, control edge rate, enable/disable I/O and switch clock input.

Supports platforms based on the Intel CK408 clock specification for the Almador (Intel 830) and Brookdale (Intel 845) chipsets.
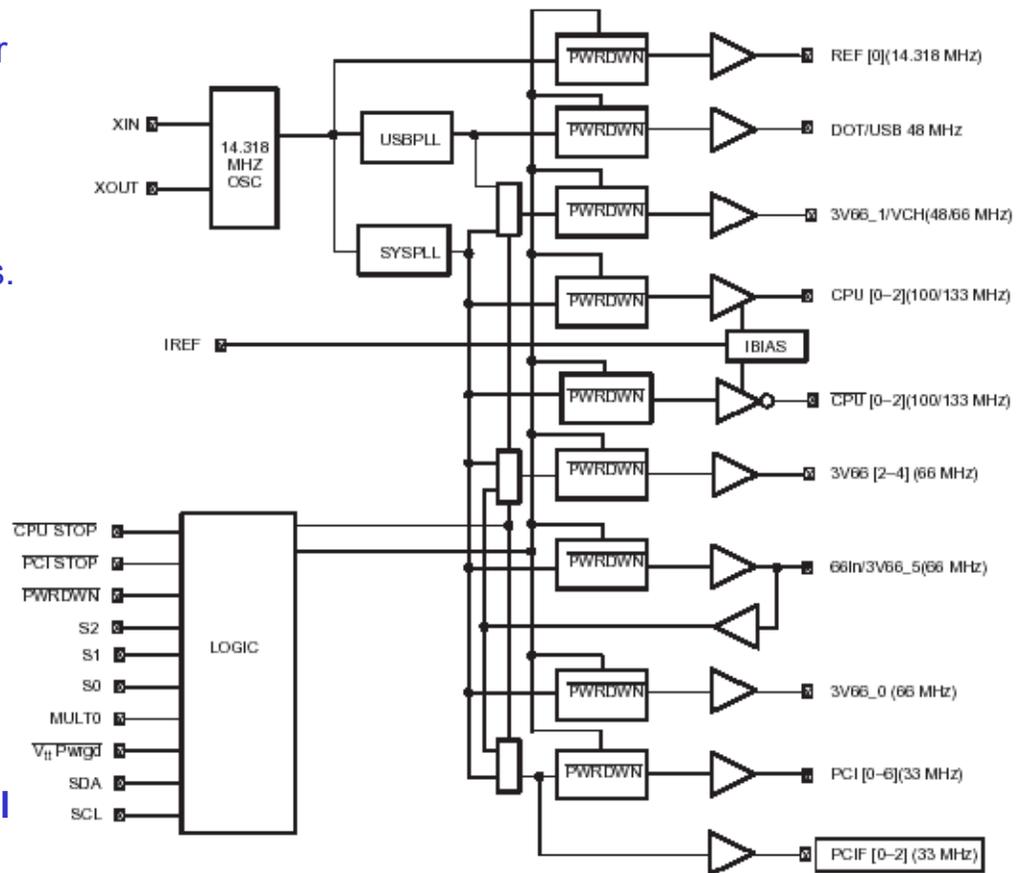
I^{2}C Controlled Clock Distribution

The PCK2001/2 are a LVTTL fanout buffers used for 133/100 MHz CPU, 66/33 MHz PCI, 14.318 MHz REF, or 133/100/66 MHz SDRAM clock distribution.

18 outputs are used to support up to 4 SDRAM DIMMS commonly found in desktop, workstation or server applications.

10 outputs of the mobile (M) version support 2 SDRAM DIMMS in notebook applications.

6 outputs of the registered (R) version support up to 4 registered SDRAM DIMMs commonly found in server applications.

I^{2}C is used to turn each individual I/O on/off
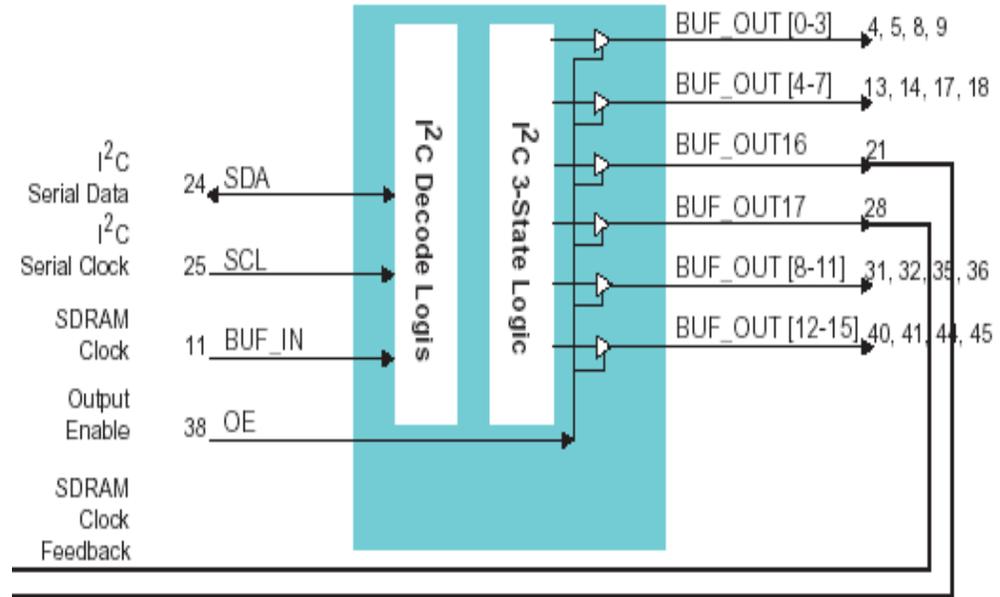

- **PCK2001**   14.318-167MHz I²C 1:18 SDRAM Clock Buffer
- **PCK2001M**   14.318-167MHz I²C 1:10 SDRAM Clock Buffer
- **PCK2001R**   14.318-133MHz I²C 1:6 SDRAM Clock Buffer
- **PCK2002**   0-300MHz I²C 1:18 SDRAM Clock Buffer
- **PCK2002M**   0-300MHz I²C 1:10 SDRAM Clock Buffer

I^{2}C Controlled Zero-Delay Clock Distribution

PCK2057 DDR Memory Clock Driver

• Optimized for clock distribution in DDR (Double Data Rate) SDRAM applications supporting DDR 200/266/300/333

• 1:10 differential clock distribution

• Jitter < 100 ps

• HCSL to SSTL_2 input conversion

• 2.5 V and 3.3 V I^{2}C support @ 100 kHz

• Test mode enables output buffers while enabling PLL

• Spread spectrum tolerant clock input

• 48-pin plastic TSSOP packaging

• Form, fit, and function compatible with CDCV850
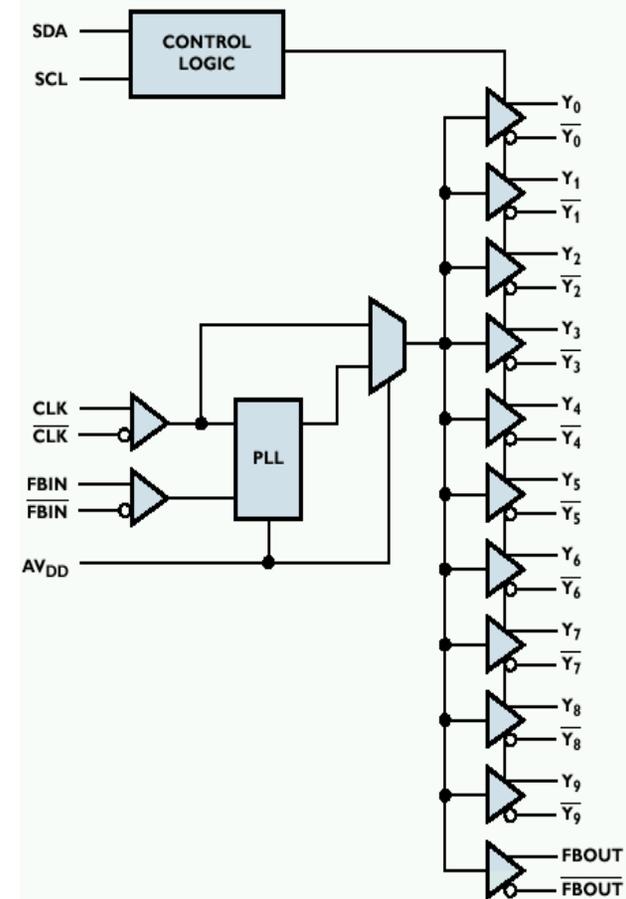
Clocking Solution for ServerWorks Grand Champion™ System I/O Switch

Quasi Output I²C I/O Expanders

General Purpose I/O

Supply

SDA

SCL

POR

I²C-bus interface

Sub address decoder

Interrupt

≠

Latches

Input/ output stages

alternative analog input configurations

KEY POINTS
-Transfers keyboard, ACPI Power switch, keypad, switch or other inputs to microcontroller via I²C bus
-Expand microcontroller via I²C bus where I/O can be located near the source or on various cards
-Use outputs to drive LEDs, sensors, fans, enable and other input pins, relays and timers
- Quasi outputs can be used as Input or Output without the use of a configuration register
-The PCA9501 has 6 address pins, allowing up to 64 devices to share the same I²C Bus.
-Application Note, AN469 GPIO Selection, discusses pros and cons of GPIOs
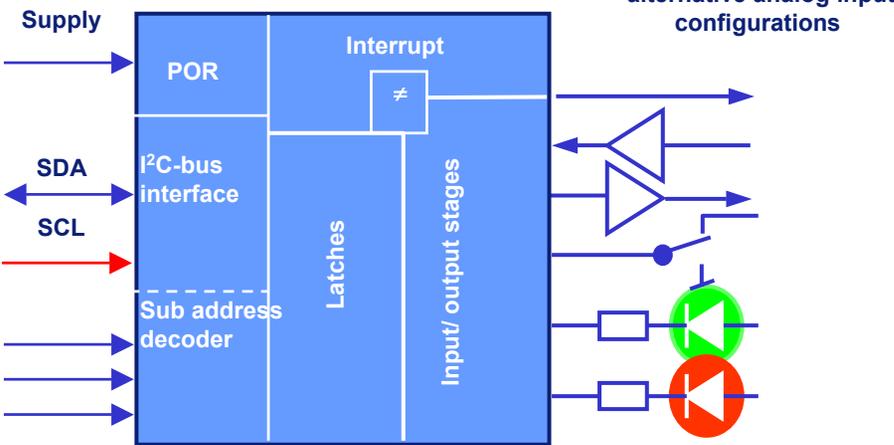
# of Outputs	Interrupt	2Kbit EEPROM	Interrupt and 2Kbit EEPROM
Quasi Output (20-25 ma sink and 100 uA source)			
8	PCF8574/74A	PCA9500/58	PCA9501
16	PCF8575/75C	-	-

Application Note AN469

Quasi Output I^{2}C I/O Expanders - Registers

• **To program the outputs**

S	Address	W	A	OUTPUT DATA	A	P

Multiple writes are possible during the same communication

• **To read input values**

| S	Address	R	A	INPUT DATA	$\overline{A}$	P

Multiple reads are possible during the same communication

• **Important to know**

– **At power-up, all the I/O's are HIGH (except PCF8575C); Only a current source to V$_{DD}$ is active**

– **Upper transistor is on for one clock cycle to provide strong pull-up and allow for faster rising edge rate**

– **I/O's should be HIGH before using them as inputs**

True Output I^{2}C I/O Expanders
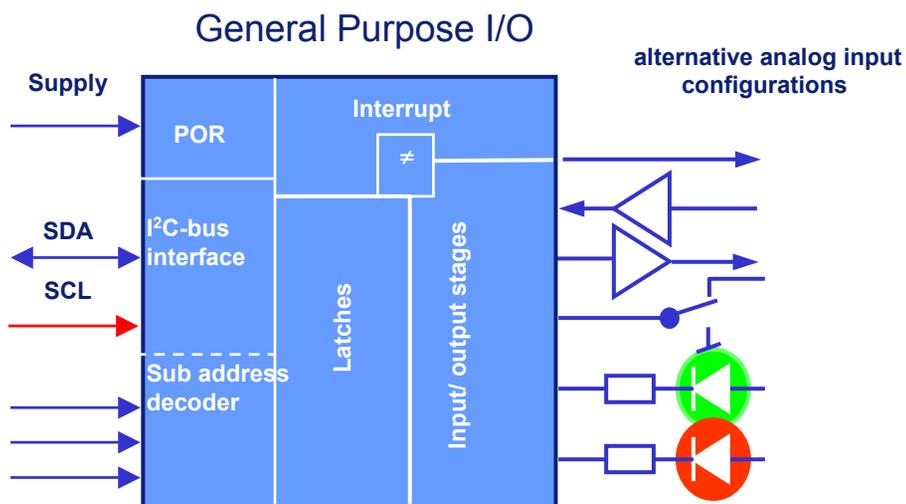
General Purpose I/O

alternative analog input configurations

KEY POINTS

-Transfers keyboard, ACPI Power switch, keypad, switch or other inputs to microcontroller via I^{2}C bus

-Use totem pole outputs to drive LEDs, sensors, fans, enable and other input pins, relays and timers

-Extra command byte needed for Input, Output, Polarity and I/O Configuration

-Application Note, AN469 GPIO Selection, discusses pros and cons of GPIOs

# of Outputs	Reset	Interrupt
True Output (20-25 ma sink and 10 mA source)		
8	PCA9556/57	PCA9534/54/54A
16	-	PCA9535/55

Application Note AN469

True Output I^{2}C I/O Expanders - Registers

- **To configure the device**

S	Address	W	A	03$_H$	A	CONFIG DATA	A

S	Address	W	A	02$_H$	A	POLARITY DATA	A	P
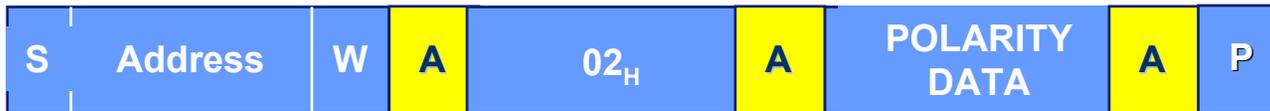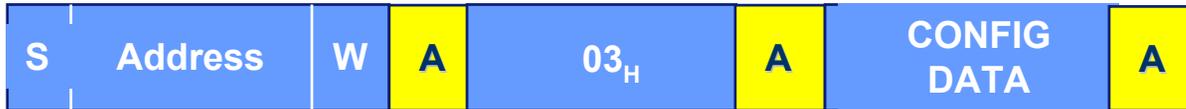
No need to access Configuration and Polarity registers once programmed

- **To program the outputs**

S	Address	W	A	01$_H$	A	OUTPUT DATA	A	P

Multiple writes are possible during the same communication

- **To read input values**

S	Address	W	A	00$_H$	A

S$_R$	Address	R	A	INPUT DATA	$\overline{A}$	P

Multiple reads are possible during the same communication

Semiconductors

34

True Output I^{2}C I/O Expanders - Example

Input Reg#		Polarity Reg#		Config Reg#		Output Reg#		I/O's
1		0		1		X	←	1
1		0		0		1	→	1
0		0		0		0	→	0
0		1		0		1	→	1
0		1		1		X	←	1
1		1		1		X	←	0
0		0		1		X	←	0
1		0		0		1	→	1
Read		**Read/ Write**		**Read/ Write**		**Read/ Write**		**I/O's**

I²C LED Dimmers/Blinkers

alternative analog input configurations

# of Outputs	Reset and POR
2	PCA9530/50
4	PCA9533/53
8	PCA9531/51
16	PCA9532/52

Application Note AN264
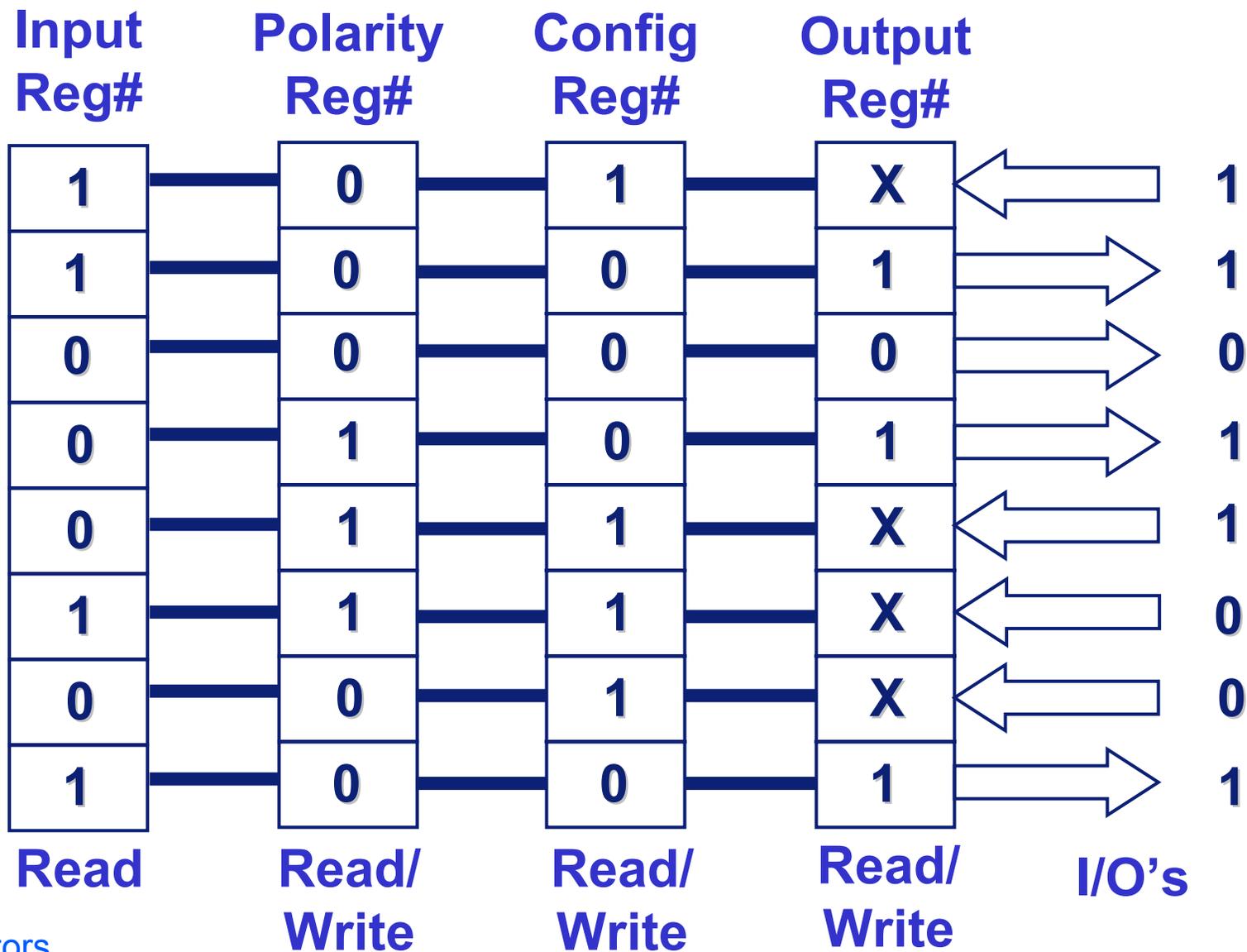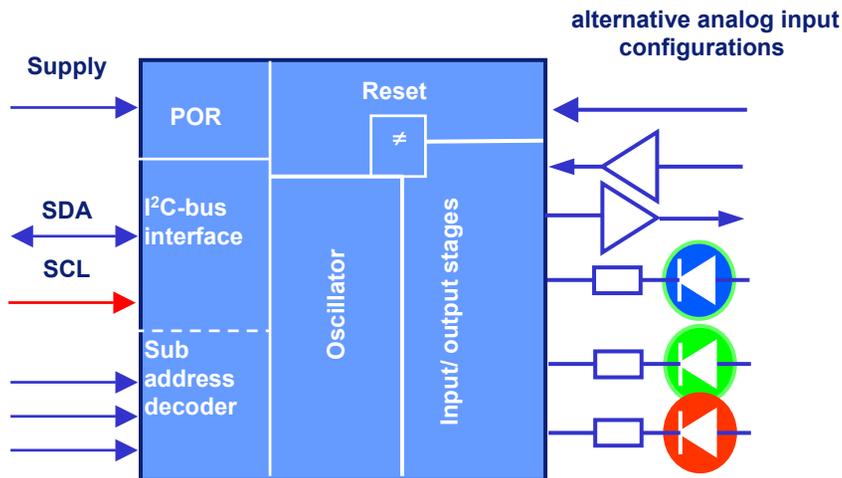
KEY POINTS

-I²C/SMBus is not tied up by sending repeated transmissions to turn LEDs on and then off to "blink" LEDs.

-Frees up the micro's timer

-Continues to blink LEDs even when no longer connected to bus master

-Can be used to cycle relays and timers

-Higher frequency rate allows LEDs to be dimmed by varying the duty cycle for Red/Green/Blue color mixing applications.

FEATURES

-25 mA open drain outputs

-Internal oscillator (+/- 15%)

-Two user definable blink rates and duty cycles adjustable between 160 Hz and 1.6 seconds (3x Dimmers) or 40 Hz and 6.4 seconds (5x Blinkers) in 256 steps

-Unused pins can be used for normal GPIO
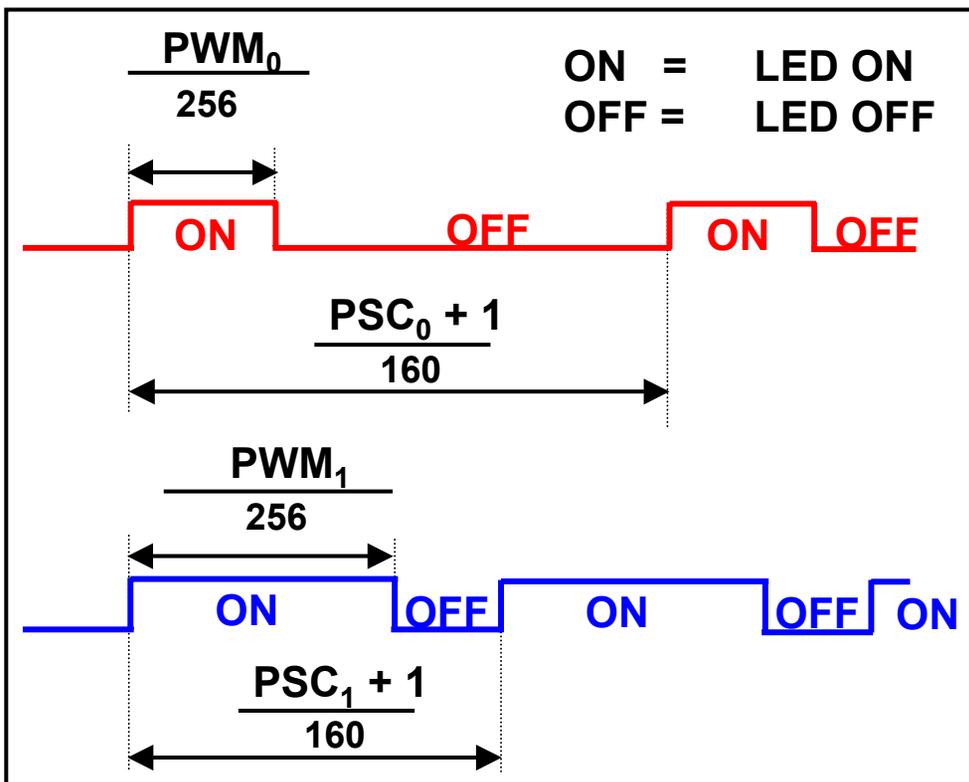
-Hardware Reset pin and Power On Reset (POR)

PCA953x I^{2}C LED Dimmers

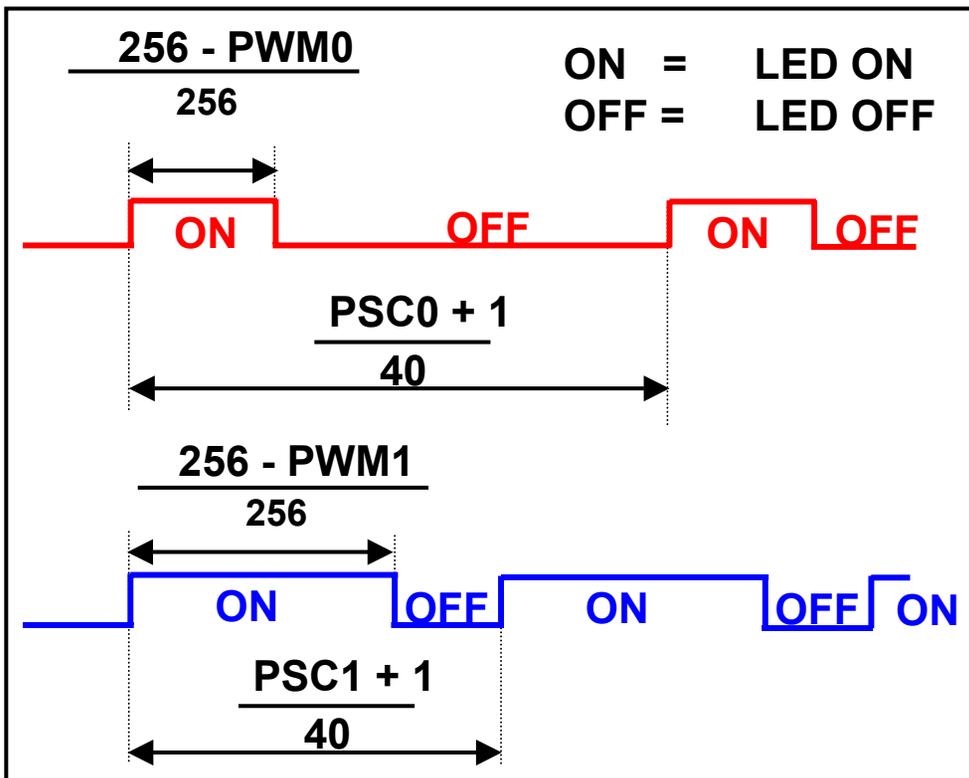|	0 (00$_H$)	255 (FF$_H$)
Frequency	160 Hz	1.6 s
Duty Cycle	0 %	99.6 %

State machine defaults to highest frequency at power on and duty cycle goes from 0% (off) to 99.6% (almost always on) for better dimming control.

$$\frac{PWM_0}{256}$$

ON = LED ON
OFF = LED OFF

ON OFF ON OFF

$$\frac{PSC_0 + 1}{160}$$

$$\frac{PWM_1}{256}$$

ON OFF ON OFF ON

$$\frac{PSC_1 + 1}{160}$$

PWM0

PSC0

PWM1

PSC1

LED Selector

ON, OFF, BR1, BR2

PCA955x I^{2}C LED Blinkers

	0 (00$_H$)	255 (FF$_H$)
Frequency	**40 Hz**	**6.4 s**
Duty Cycle	**100 %**	**0.4 %**

$$\frac{256 - PWM0}{256}$$

ON = LED ON
OFF = LED OFF

ON   OFF   ON   OFF

$$\frac{PSC0 + 1}{40}$$

$$\frac{256 - PWM1}{256}$$

ON   OFF   ON   OFF   ON

$$\frac{PSC1 + 1}{40}$$

Input Register(s)

PWM0 (ON Time)

PSC0 (Frequency)

PWM1 (ON Time)

PSC1 (Frequency)
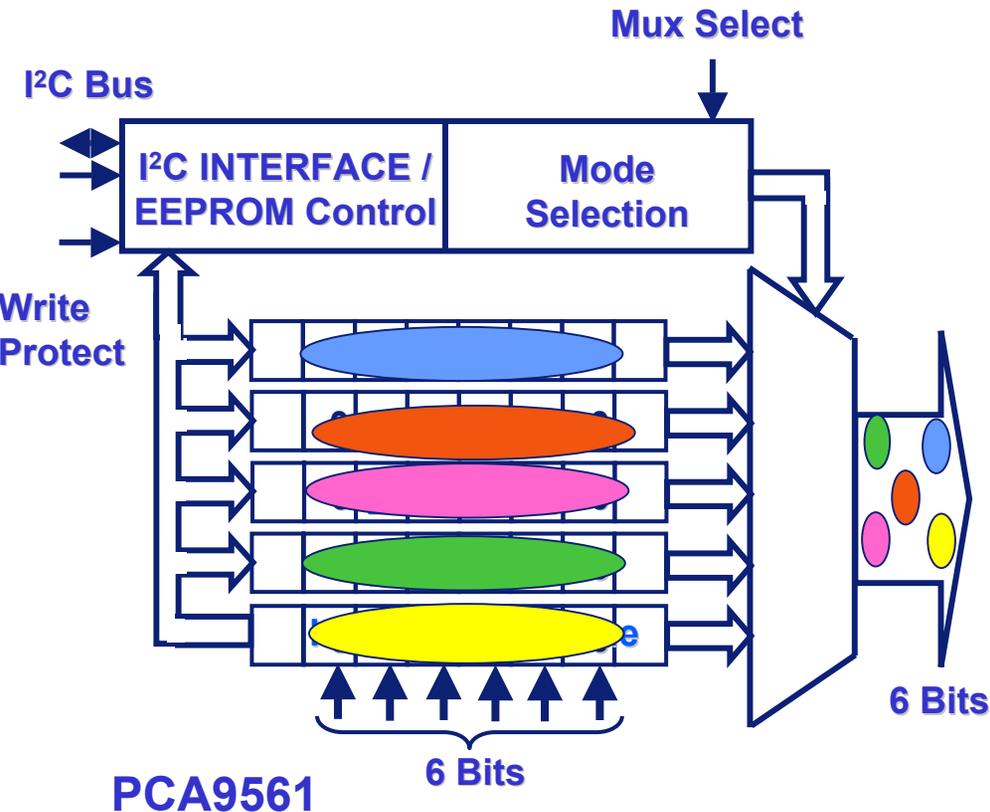
LED Selector

ON, OFF, BR1, BR2

LED Dimmers/Blinkers vs Micros

Difference between using a LED Blinker/Dimmer or a micro:

- Easier software generation to control LEDs
    - ➤ Don't have to use micro timer
    - ➤ Don't have to continually send on and off command to blink or dim LEDs
- Frequency fixed by device, not dependant on internal processor clock frequency
- I^2C devices have higher sink current capability per bit and larger sink current capability per device
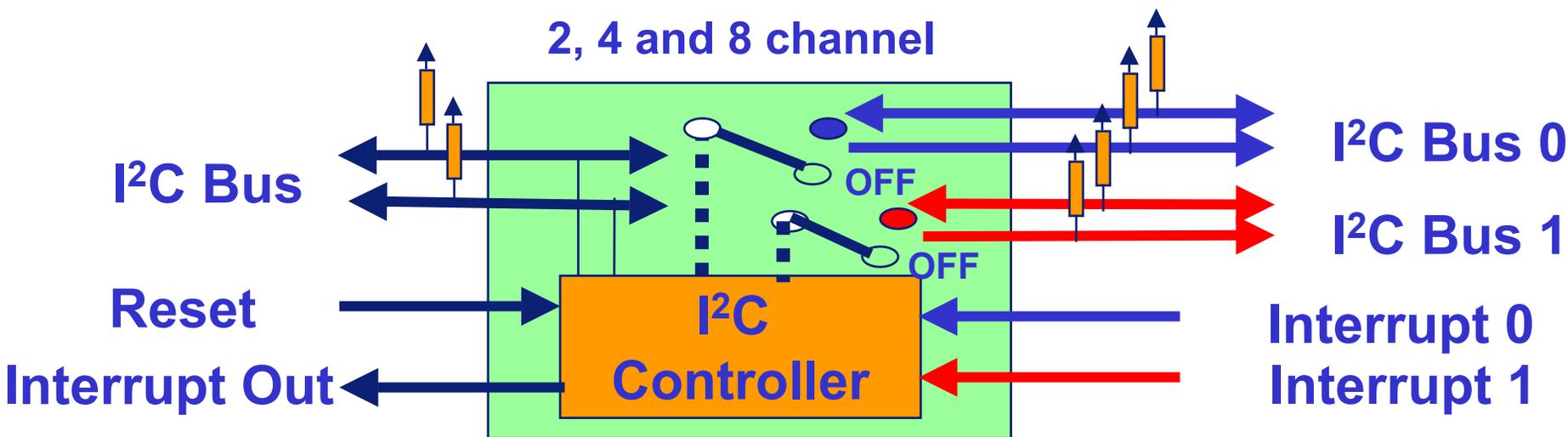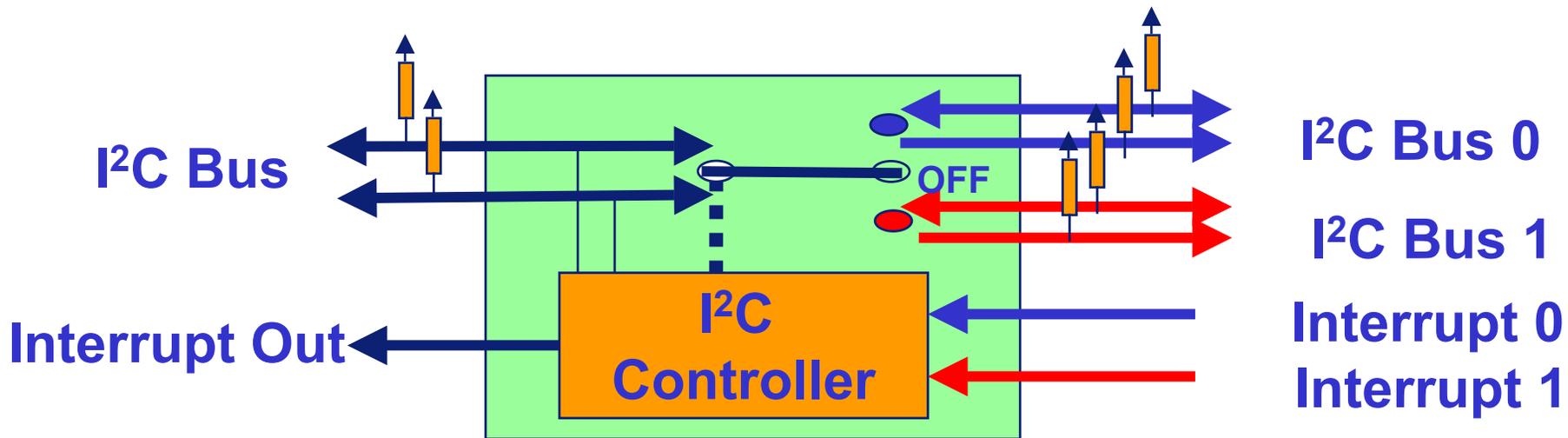
I^{2}C DIP Switches

Mux Select

I^{2}C Bus

| | I^{2}C INTERFACE / EEPROM Control | Mode Selection |

Write Protect

6 Bits

6 Bits

PCA9561

	# of Pins	# of Non Volatile Registers	# of Register Bits	# of Hardware Input Pins	# of Muxed Outputs	Non-Muxed Output
PCA8550	16	1	5	4	4	YES
PCA9558	28	1	6	5	5	YES
PCA9559	20	1	6	5	5	YES
PCA9560	20	2	6	5	5	YES
PCA9561	20	4	6	6	6	NO

Application Note AN250

6 bit output value is dependant on the mux select pin position or command from I^{2}C master
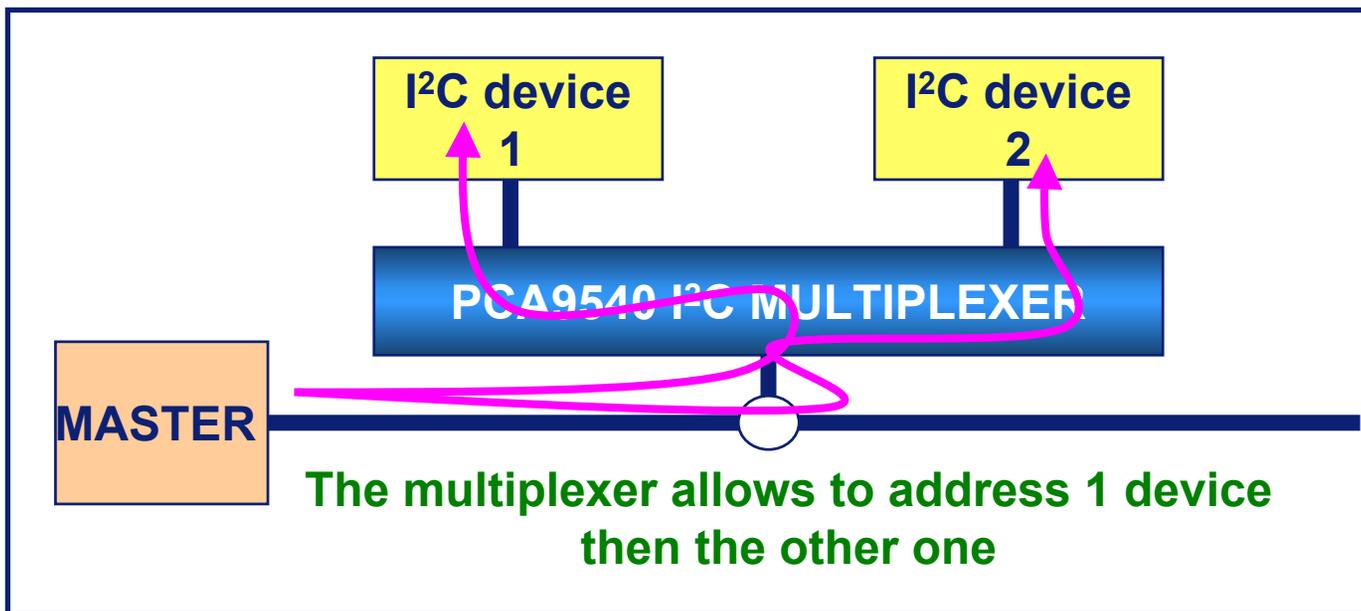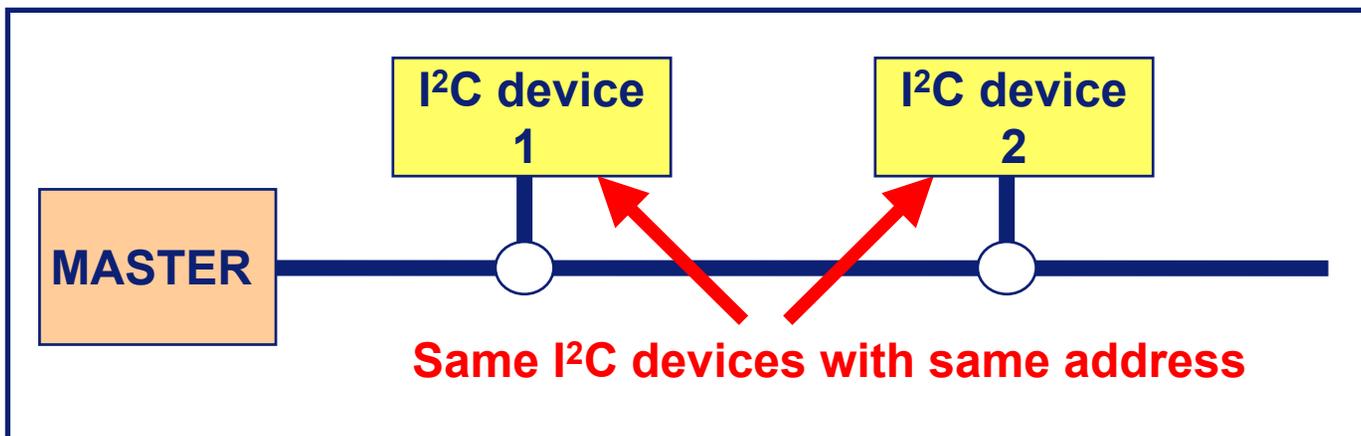
EEPROM 0 is default output
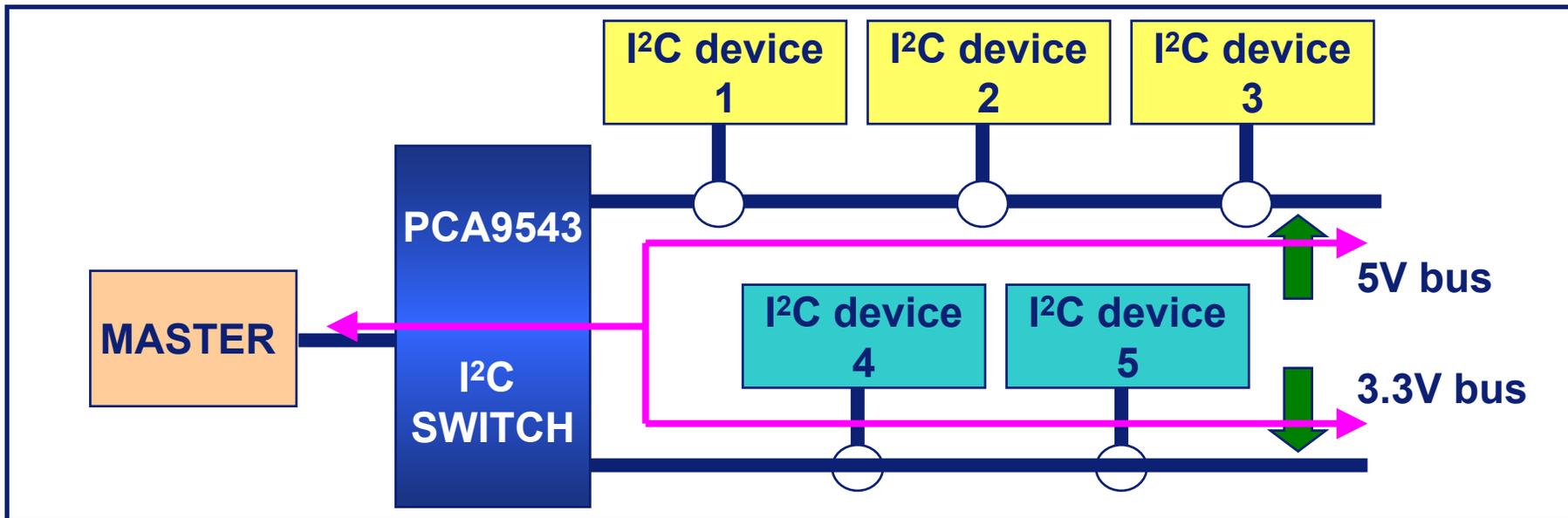
I^{2}C Multiplexers and Switches

I^{2}C Bus

Interrupt Out

I^{2}C Controller

I^{2}C Bus 0

I^{2}C Bus 1

OFF

Interrupt 0
Interrupt 1

2, 4 and 8 channel

I^{2}C Bus

Reset

Interrupt Out

I^{2}C Controller

I^{2}C Bus 0

OFF

I^{2}C Bus 1

OFF

Interrupt 0
Interrupt 1

Application Note AN262

I^{2}C Multiplexers: Address Deconflict

MASTER

I^{2}C device 1

I^{2}C device 2

Same I^{2}C devices with same address

MASTER

I^{2}C device 1

I^{2}C device 2

PCA9540 I^{2}C MULTIPLEXER

The multiplexer allows to address 1 device then the other one

I^{2}C Switches: Voltage Level Shifting
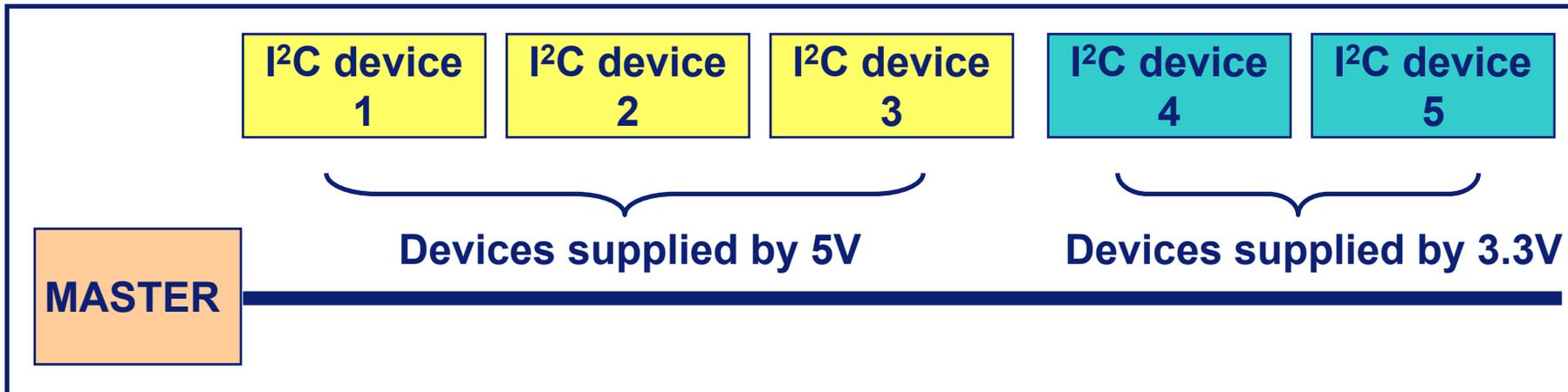
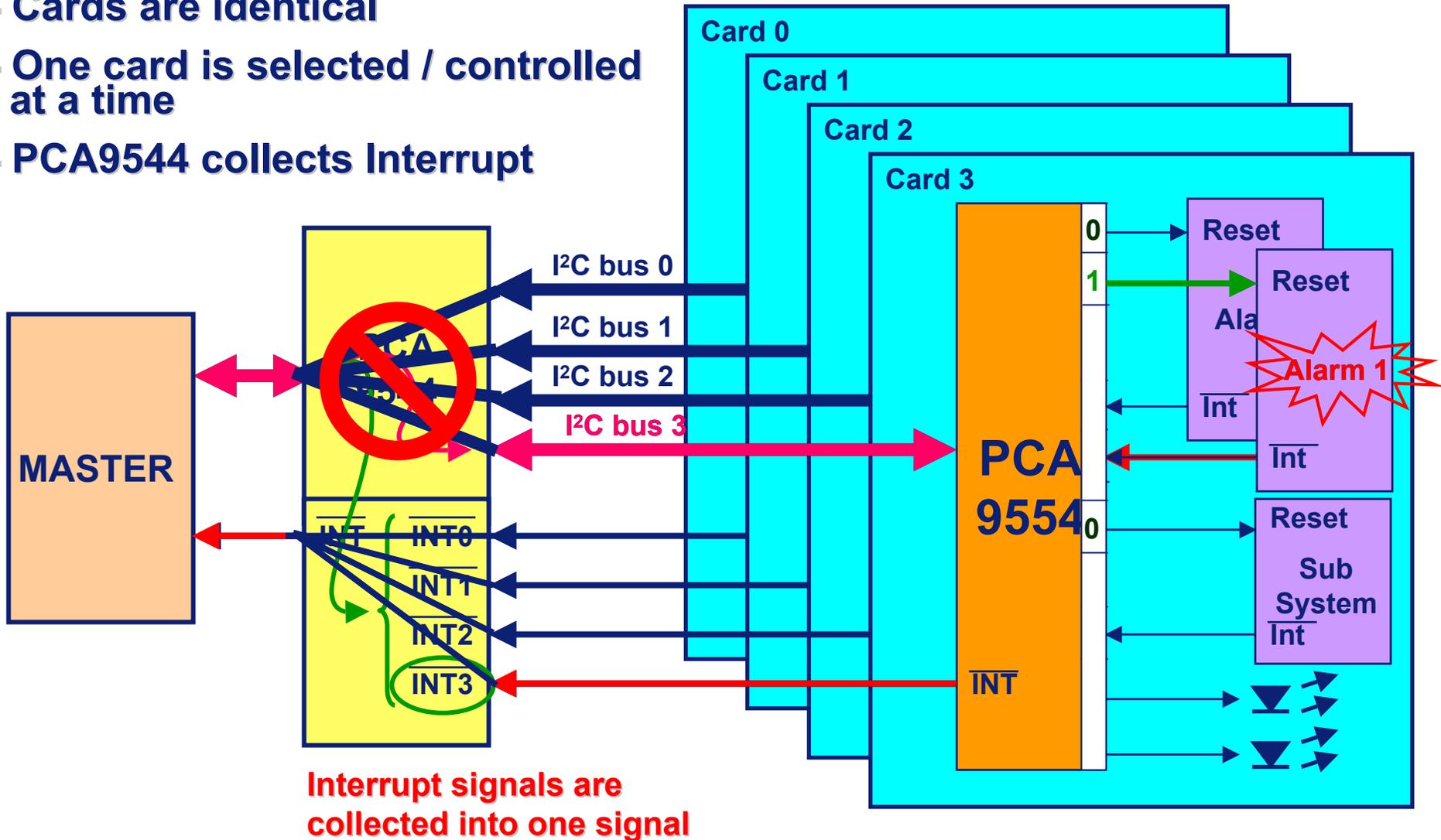# I^{2}C Switches: Branch isolation
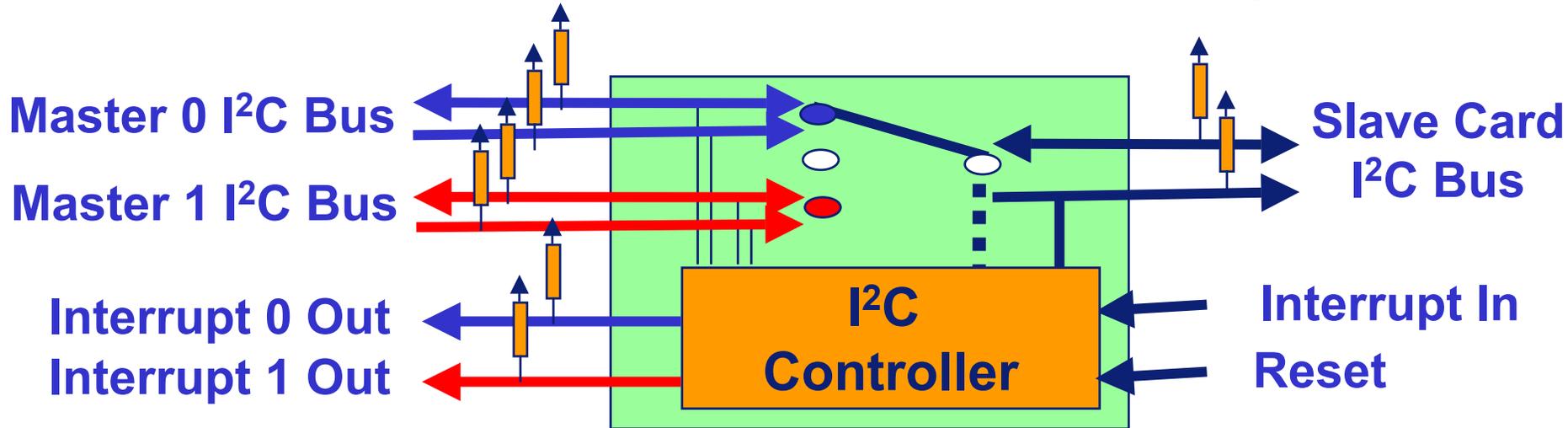

Separate devices 1, 2 and 3 from devices 4 and 5
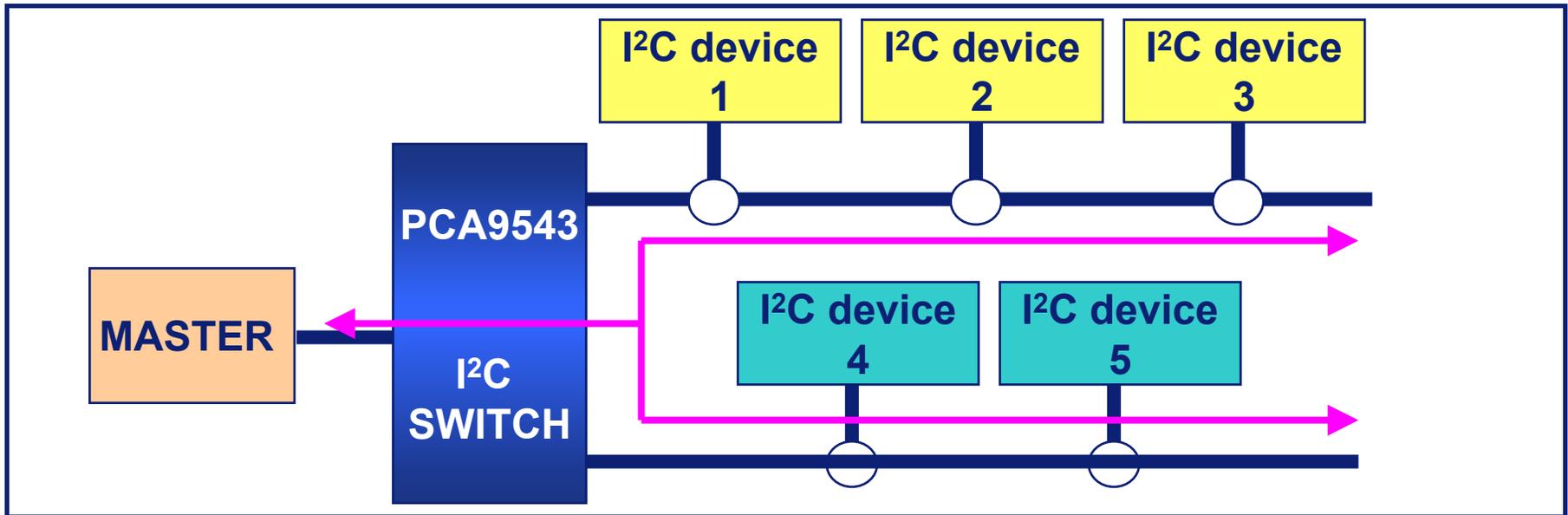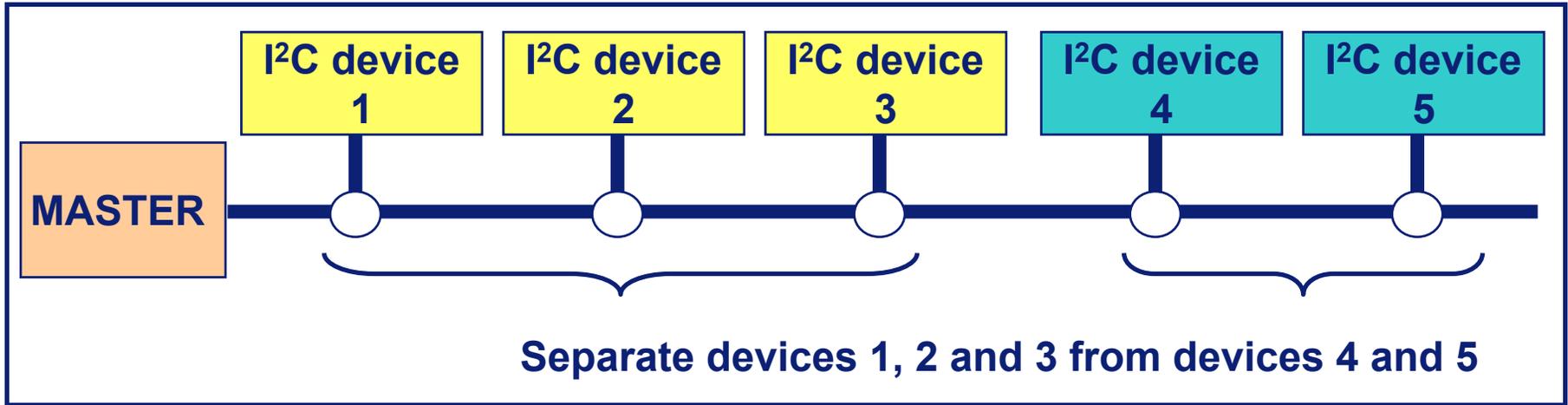
I^{2}C Multiplexers: Multi-card Application

- **Cards are identical**
- **One card is selected / controlled at a time**
- **PCA9544 collects Interrupt**

MASTER

Card 0
Card 1
Card 2
Card 3

I^{2}C bus 0
I^{2}C bus 1
I^{2}C bus 2
I^{2}C bus 3

PCA 9554

0
1

Reset
Reset
Ala
$\overline{\text{Int}}$

Alarm 1

$\overline{\text{Int}}$

0
Reset
Sub System
$\overline{\text{Int}}$

$\overline{\text{INT}}$
$\overline{\text{INT0}}$
$\overline{\text{INT1}}$
$\overline{\text{INT2}}$
$\overline{\text{INT3}}$

$\overline{\text{INT}}$

Interrupt signals are collected into one signal

2 to 1 I^{2}C Master Selector w/Interrupt Logic and Reset

Master 0 I^{2}C Bus

Master 1 I^{2}C Bus

Interrupt 0 Out
Interrupt 1 Out

I^{2}C Controller

Slave Card I^{2}C Bus

Interrupt In Reset

FEATURES
- Select one of two I^{2}C masters to a single channel
- I^{2}C/SMBus commands used to select channel
- Reset or Power On Reset (POR) resets state machine
- Interrupt outputs also report demultiplexer status
- Sends 9 clock pulses and stop condition to clear slave card prior to transferring master

KEY POINTS
- Allows primary and backup master to communicate to one downstream slave card.
- Arbitration circuit between bus masters
- Doesn't isolate bus capacitance
- Allows voltage translation between 1.8 V, 2.5 V, 3.3 V and 5 V
- Idle detect for live insertion protection

- **PCA9541/01 - defaults to channel 0 on start-up/reset**

- **PCA9541/02 - defaults to channel 0 on start-up/reset after stop condition**

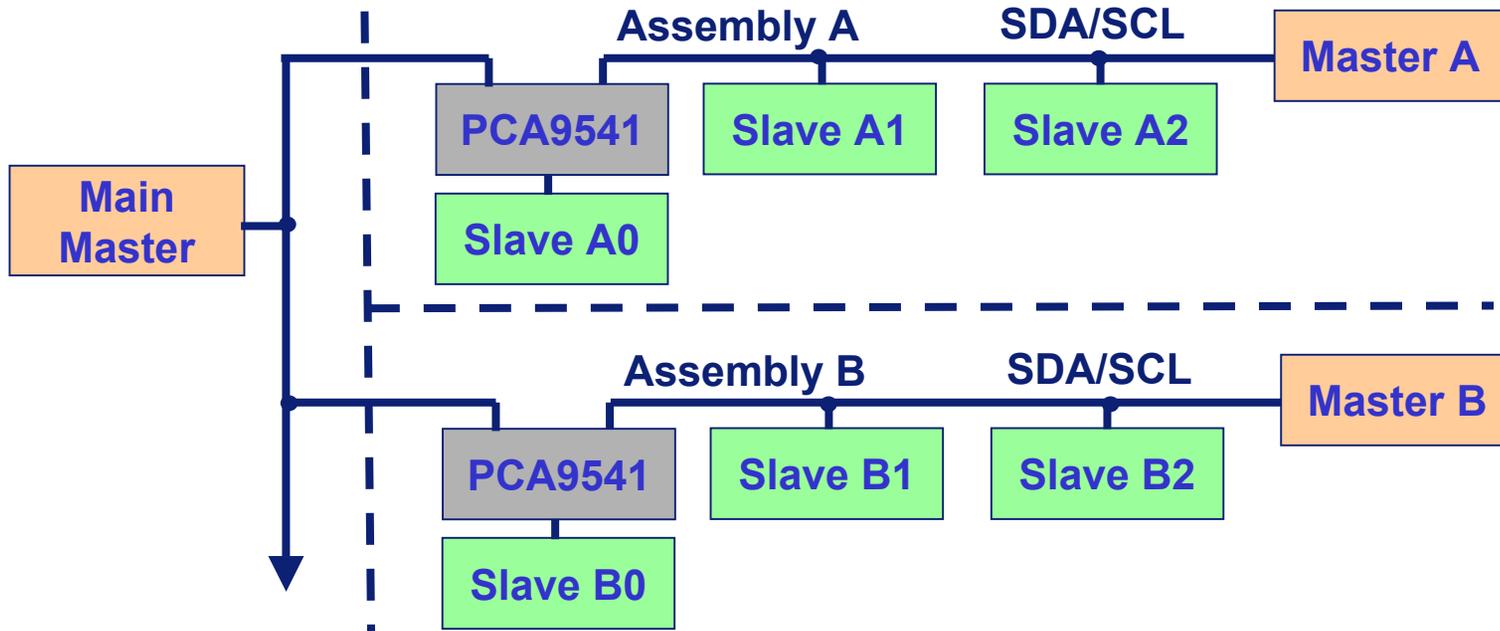- **PCA9541/03 – defaults to off on start-up/reset, master commands channel**

Semiconductors

PCA9541 - Multi-Point Application
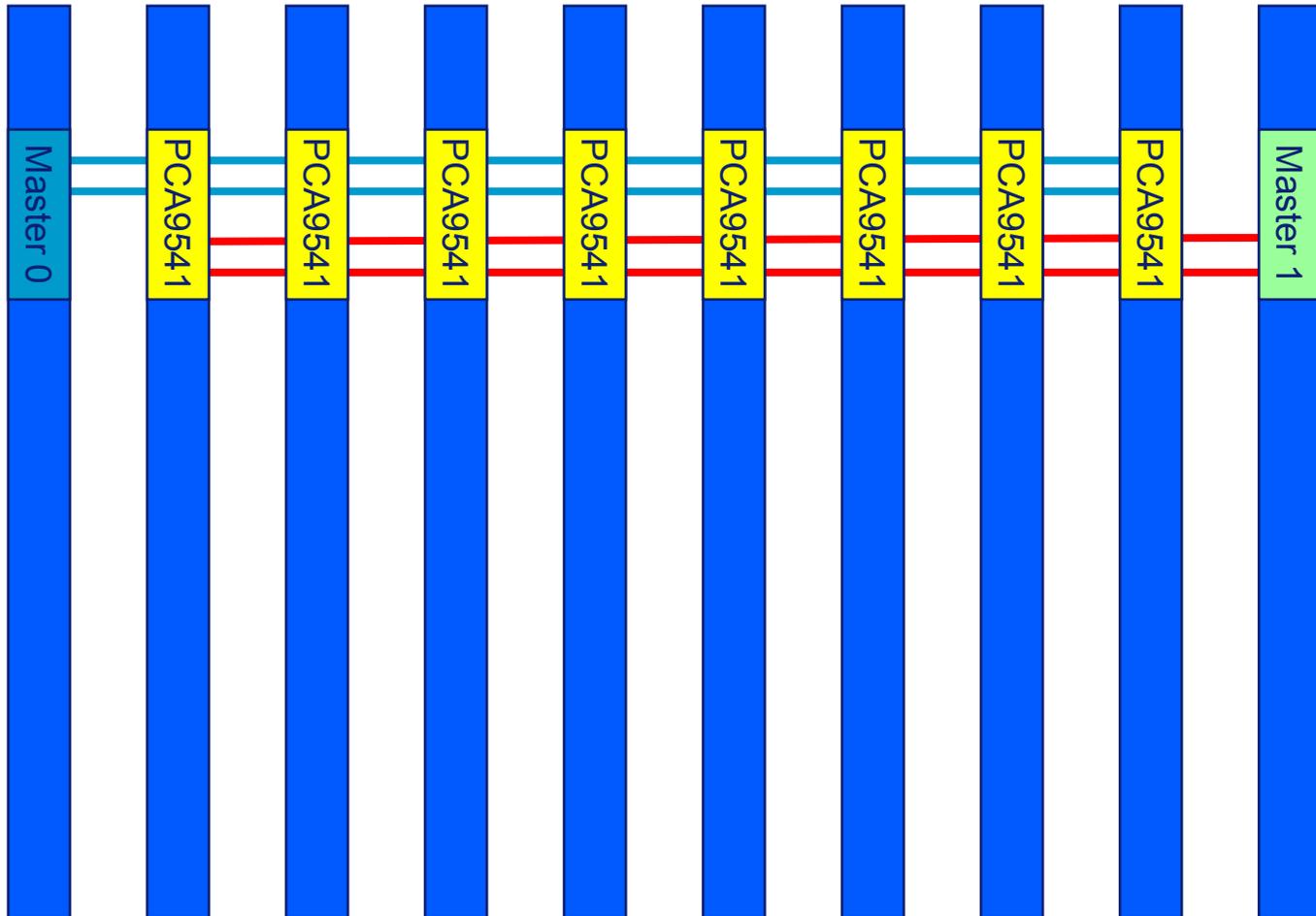
PCA9541 - Point-Point Application
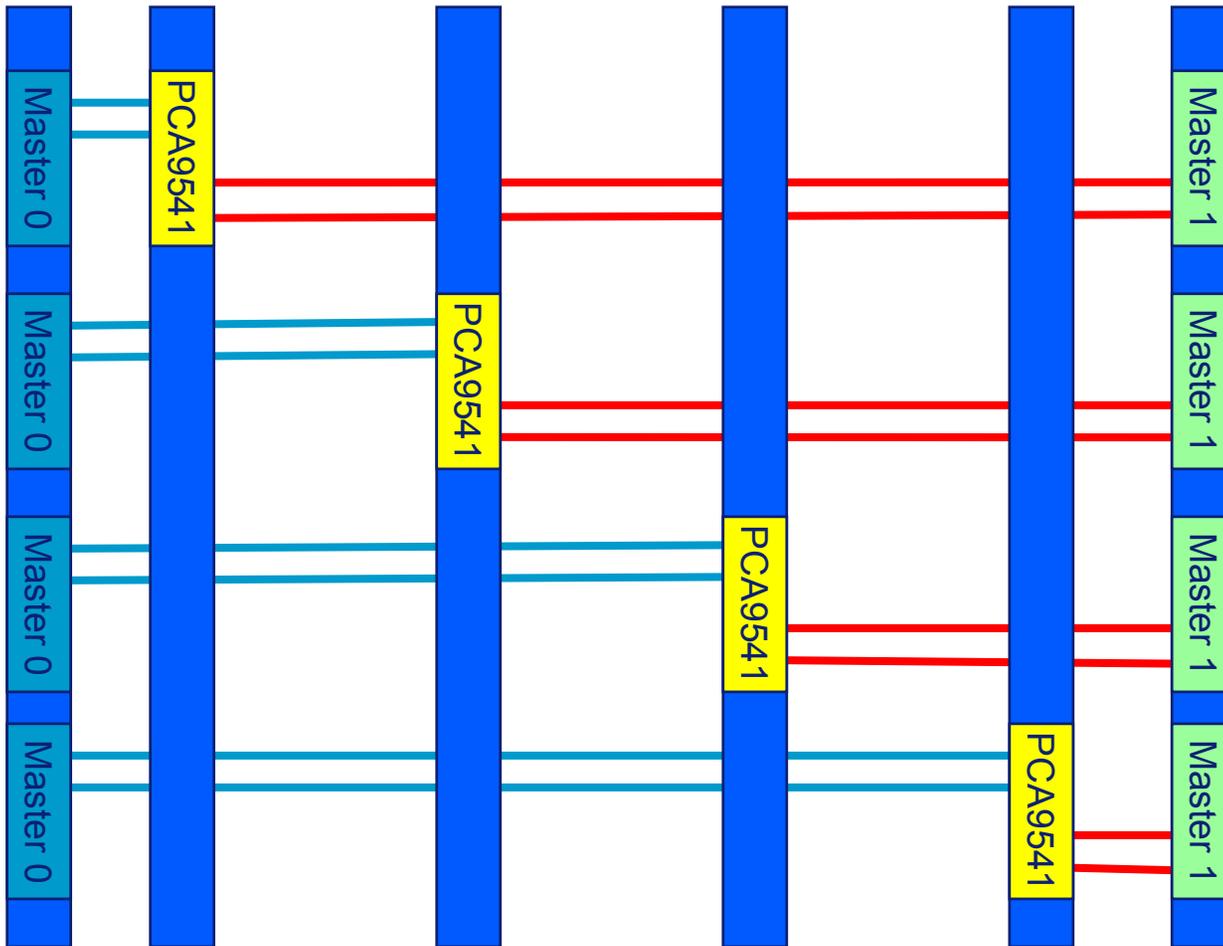
PCA9541 – Shared Resources

• Some masters may not be multi-master capable or some masters may not play well together and continually lock up the bus.

• The PCA9541 can be used to separate the masters but still allow shared access to slave devices, such as Field Replaceable Unit (FRU) EEPROMs or temperature sensors.

PCA9541 – Gatekeeper Multiplexer

• The PCA9541/03 acts as the gatekeeper to each card that have identically I2C addressed EEPROMs. The master turns each uniquely addressed PCA9541/03 on (master 0) and off, one at a time, to communicate with the EEPROMs.
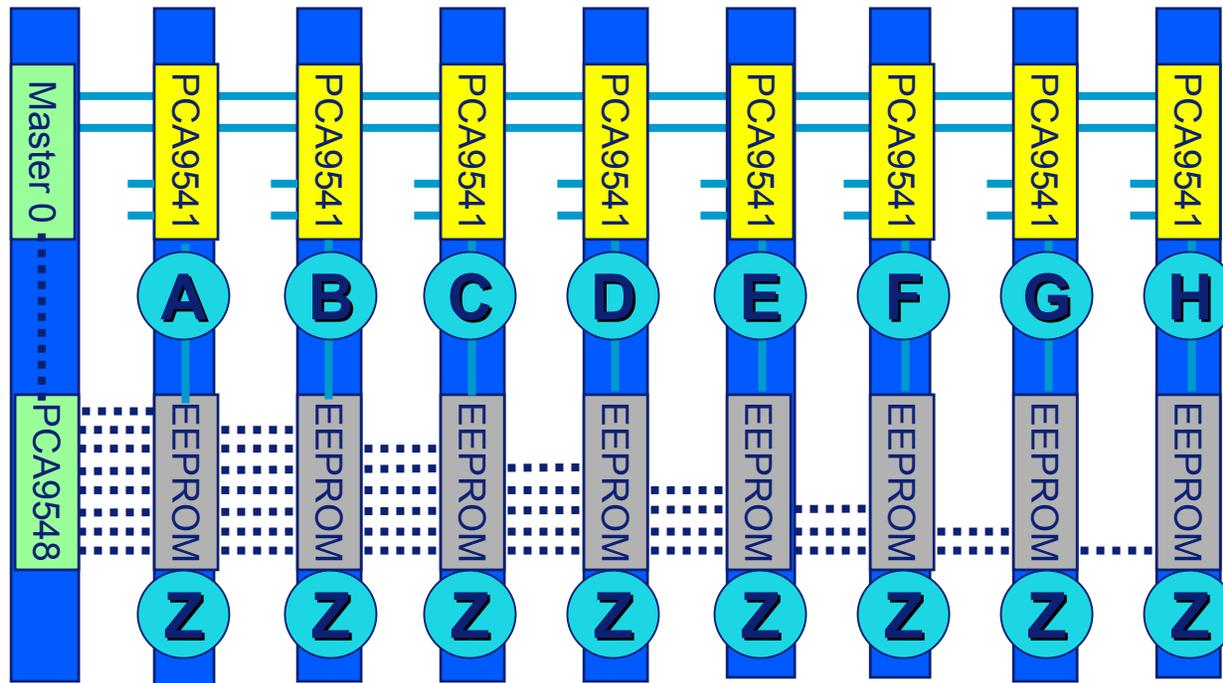
• The alternative is to use a PCA9548 to 1 to 8 multiplexer on the master card and then run 8 I2C buses, one to each EEPROM card. You use the same number of card pins but have 8 times the number of traces on the backplane.

PCA9541 – Bus Recovery
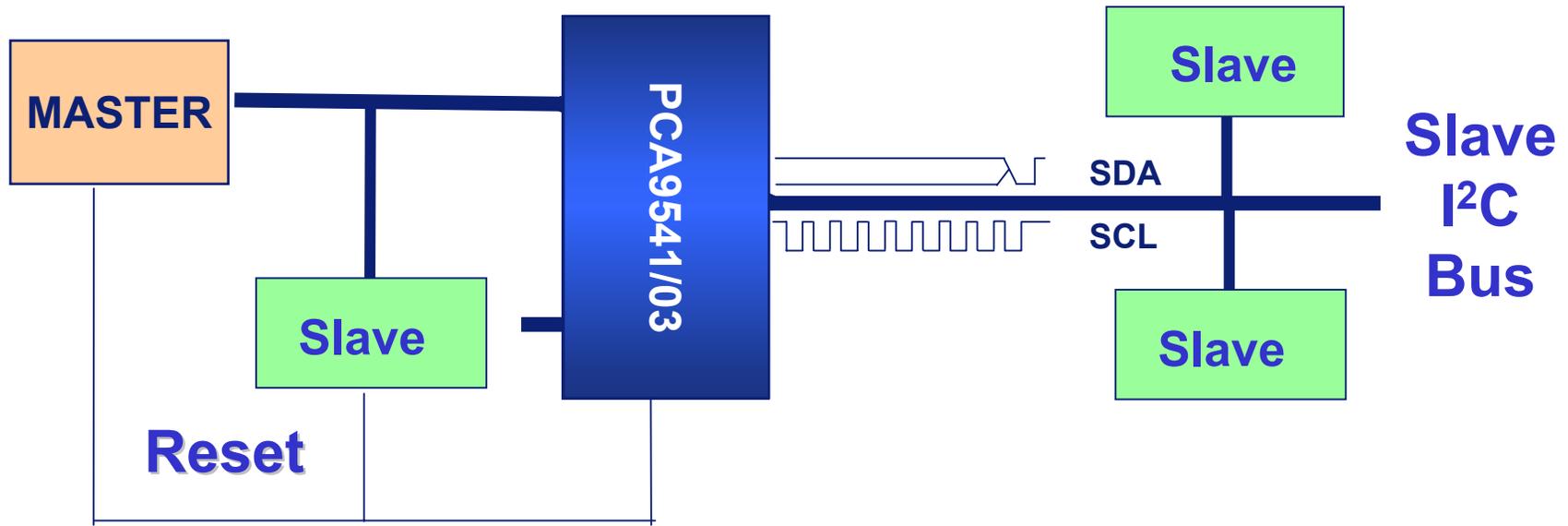
- If the I²C bus hangs up, the master will loose control of all slave devices.

- The PCA9541/03 can be used to isolate slave devices without a reset pin, allowing the master to initiate a reset on the upstream devices to regain control of the bus and then command the PCA9541/03 to send 9 clocks pulses and a stop condition to reset the state machine of the downstream slaves so that all devices are waiting for a START condition.

I²C Multiplexers and Switches

| Device | Multiplexer (In/Out) | Switch (In/Out) | Features | | | Packages | | | | |
			# of Addresses	Interrupt (In/Out)	Hardware RESET	Pin Count	SO (Narrow)	SO (Wide)	TSSOP	HVQFN
PCA9540	1-2		1			8	D		DP	
PCA9541	2-1		16	1-2	✔	16	D		PW	BS
PCA9542	1-2		8	2-1		14	D		PW	
PCA9543		1-2	4	2-1	✔	14	D		PW	
PCA9544	1-4		8	4-1		20		D	PW	BS
PCA9545		1-4	4	4-1	✔	20		D	PW	BS
PCA9546		1-4	8		✔	16	D		PW	BS
PCA9548		1-8	8		✔	24		D	PW	BS

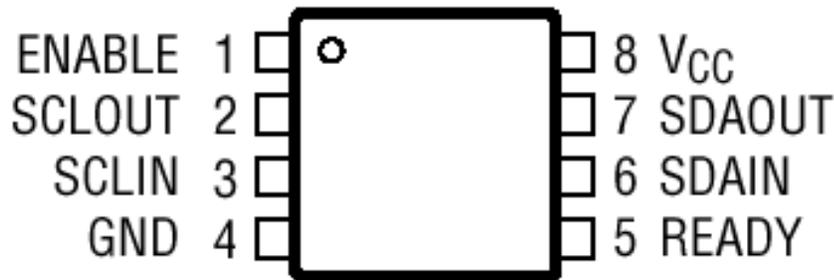# I²C Bus Bi-Directional Voltage Level Translation
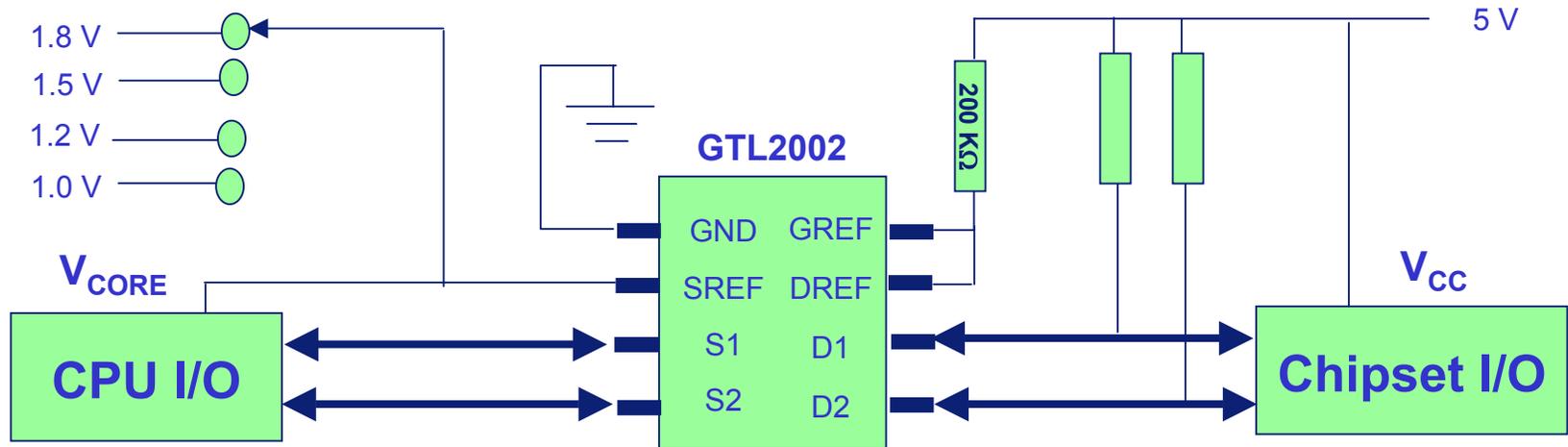
- Voltage translation between any voltage from 1.0 V to 5.0 V

- Bi-directional with no direction pin

- Reference voltage clamps the input voltage with low propagation delay

–**GTL2000 22-Bit**
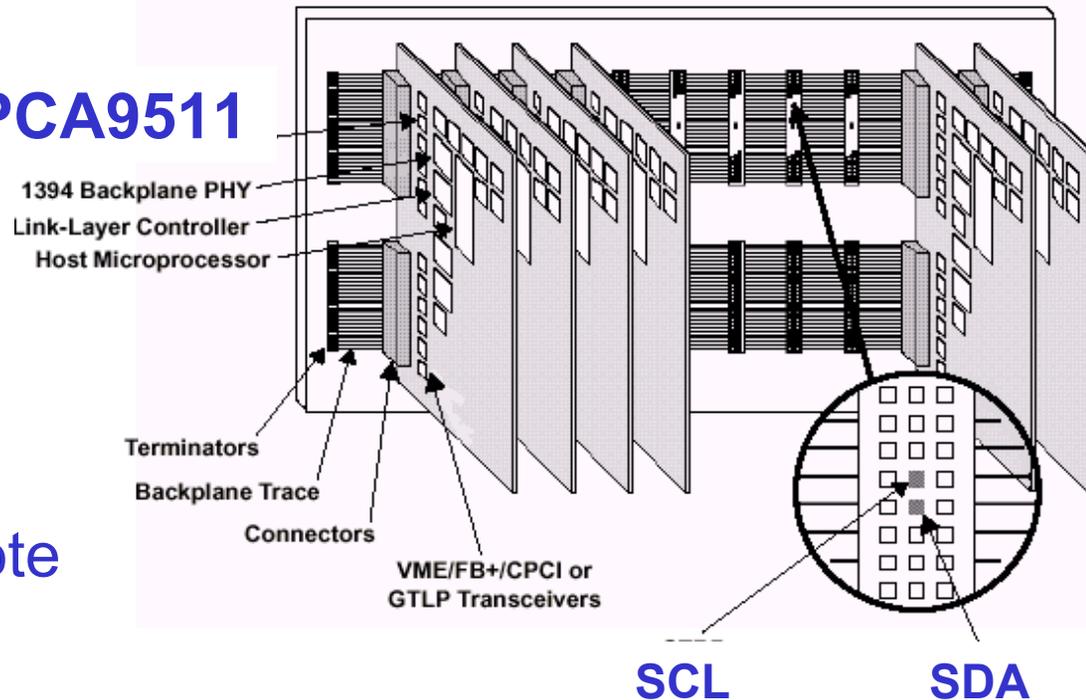
–**GTL2002 2-Bit**

–**GTL2010 10-Bit**

Application Note AN10145

I^{2}C Hot Swap Bus Buffer

```
ENABLE  1          8  V_CC
SCLOUT  2          7  SDAOUT
SCLIN   3          6  SDAIN
GND     4          5  READY
```

- **Isolate capacitance**
- **Stop and Idle detect**
- **SDA/SCL Precharge**
- **Rise Time Accelerators**

PCA9511

1394 Backplane PHY
Link-Layer Controller
Host Microprocessor

Terminators
Backplane Trace
Connectors

VME/FB+/CPCI or
GTLP Transceivers

SCL   **SDA**

Application Note
AN10160

Semiconductors

54

PHILIPS

I^{2}C Hot Swap Bus Buffer

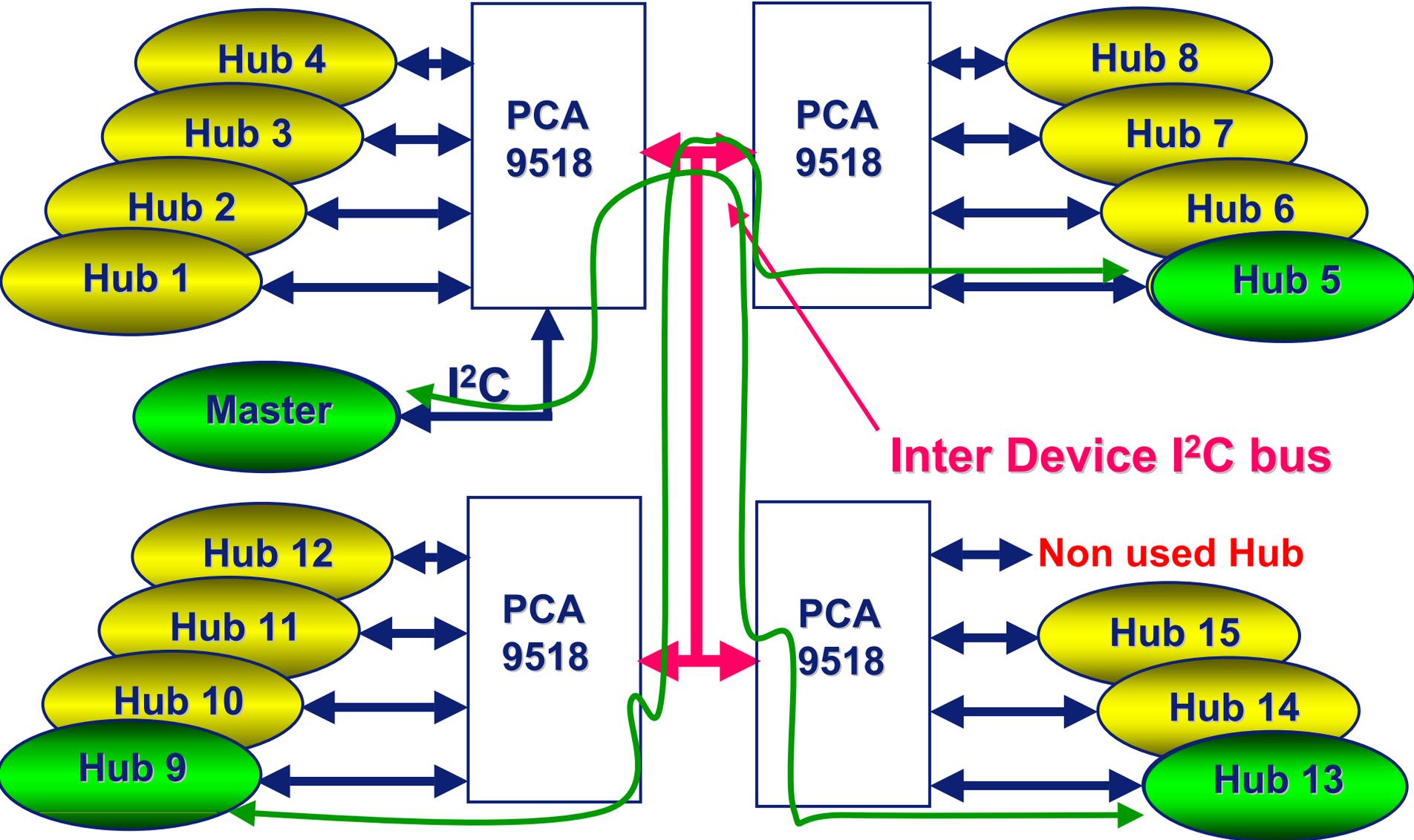| Feature	PCA9511	PCA9513	PCA9514		PCA9512
Alternate source to Linear Tech LTC4300-1ISM8	Yes	Similar	Similar		-
Alternate source to Linear Tech LTC4300-2ISM8	-	-	-		Yes
Idle Detect	Yes	Yes	Yes		Yes
High Impedance SDA, SCL pins for Vcc = 0V	Yes	Yes	Yes		Yes
Rise Time Accelerator Circuitry on all SDA and SCL lines	Yes	Yes	Yes		Yes
Rise Time Accelerator Circuitry Hardware Enable Pin	-	-	-		Yes
Rise Time Accelerator threshold 0.8 V vs 0.6 V improves noise margin	-	Yes	Yes		-
Low Icc chip disable < 1 uA	Yes	Yes	Yes		No
Ready Open Drain Output	Yes	Yes	Yes		No
Separate Vccs to support 5 V to 3.3 V level translation	-	-	-		
1V Precharge on all SDA and SCL Lines	Yes	No	No		Yes
92 uA Current Source on SCLIN and SDAIN for PICMG applications	-	Yes	-		-
Improve acknowledge and clock stretching behavior	Yes	Yes	Yes		Yes

Semiconductors

I^{2}C Bus repeater (PCA9515) and Hub (PCA9516)

Master

PCA 9515

PCA 9516

Hub 1

Hub 2

Hub 3

Hub 4

**Hub 5**
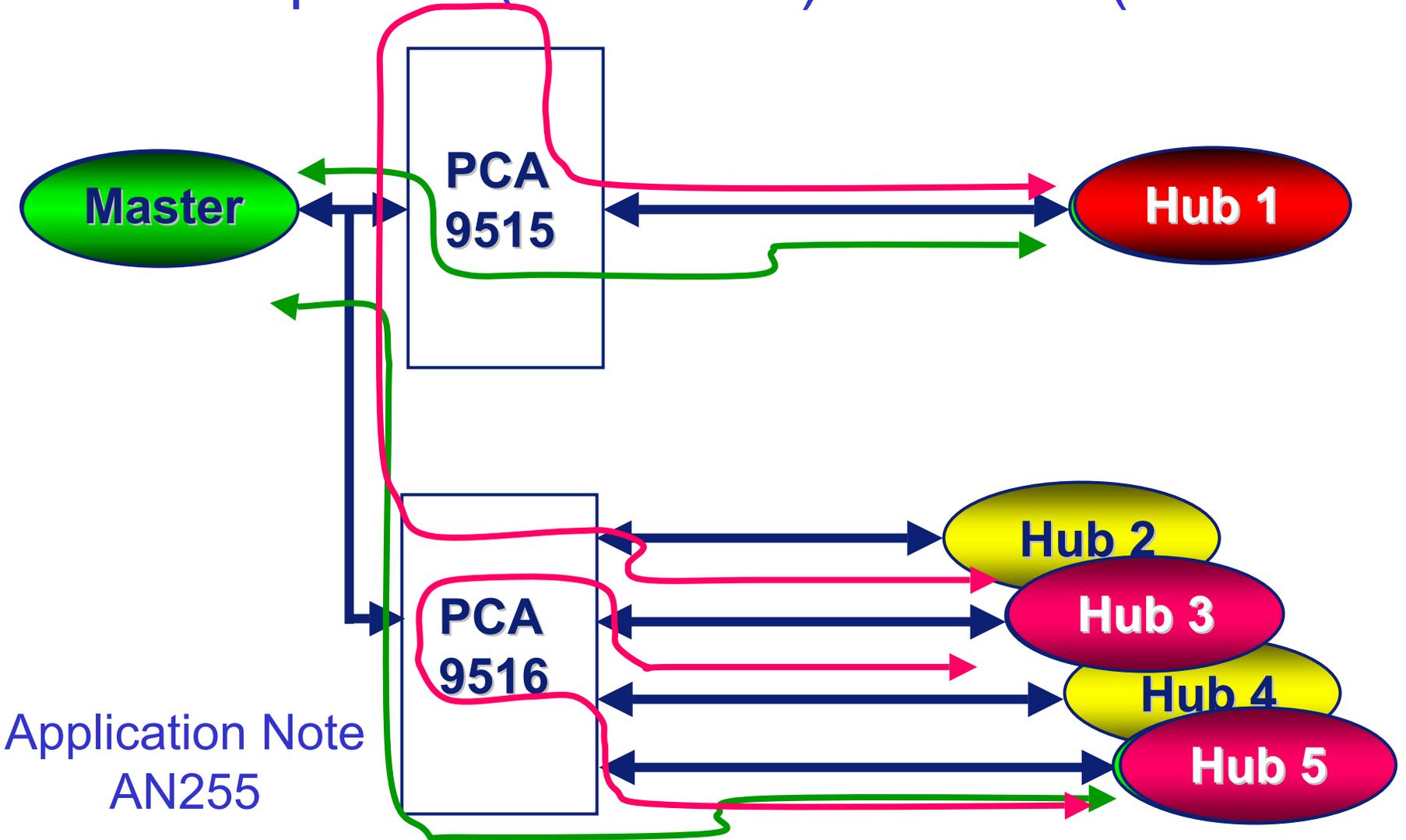
Application Note
AN255

PCA9515 and PCA9516 were designed to isolate up to 400 pF on each segment and uses an offset V$_{OL}$ to allow bi-directional signaling without use of a direction pin. They were not designed to operate on the same bus since a low signal is not passed through two devices.
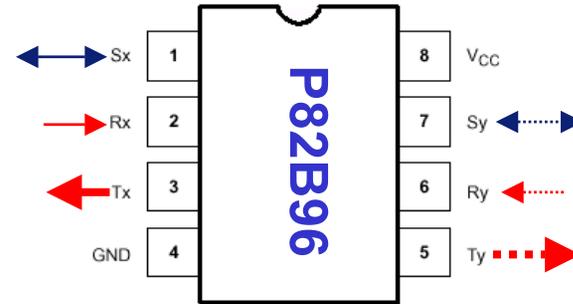
PCA9518 Applications

PHILIPS

Hub 4 — PCA 9518 — Hub 8
Hub 3 — Hub 7
Hub 2 — Hub 6
Hub 1 — PCA 9518 — Hub 5

I^2C

Master

Inter Device I^2C bus

Hub 12 — PCA 9518 — Non used Hub
Hub 11 — Hub 15
Hub 10 — PCA 9518 — Hub 14
Hub 9 — Hub 13

The PCA9518 was design to allow expansion to an unlimited number of segments of 400 pF each.

I²C Bus Extenders
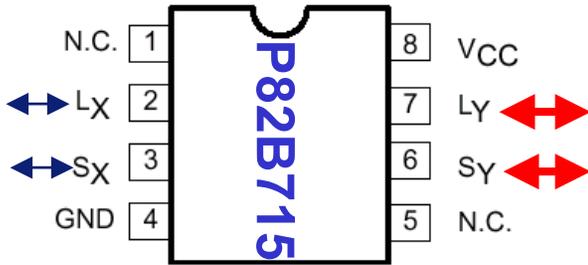
I²C Bus Extender

Dual Bi-Directional Bus Buffer

KEY POINTS
• High drive outputs are used to extend the reach of the I²C bus and exceed the 400 pF/system limit.
• Possible distances range from 50 meters at 85kHz to 1km at 31kHz over twisted-pair phone cable.
• P82B96 has split high drive outputs allowing differential transmission or Opto-isolation of the I²C Bus.
• See Application Note AN255 for more details.

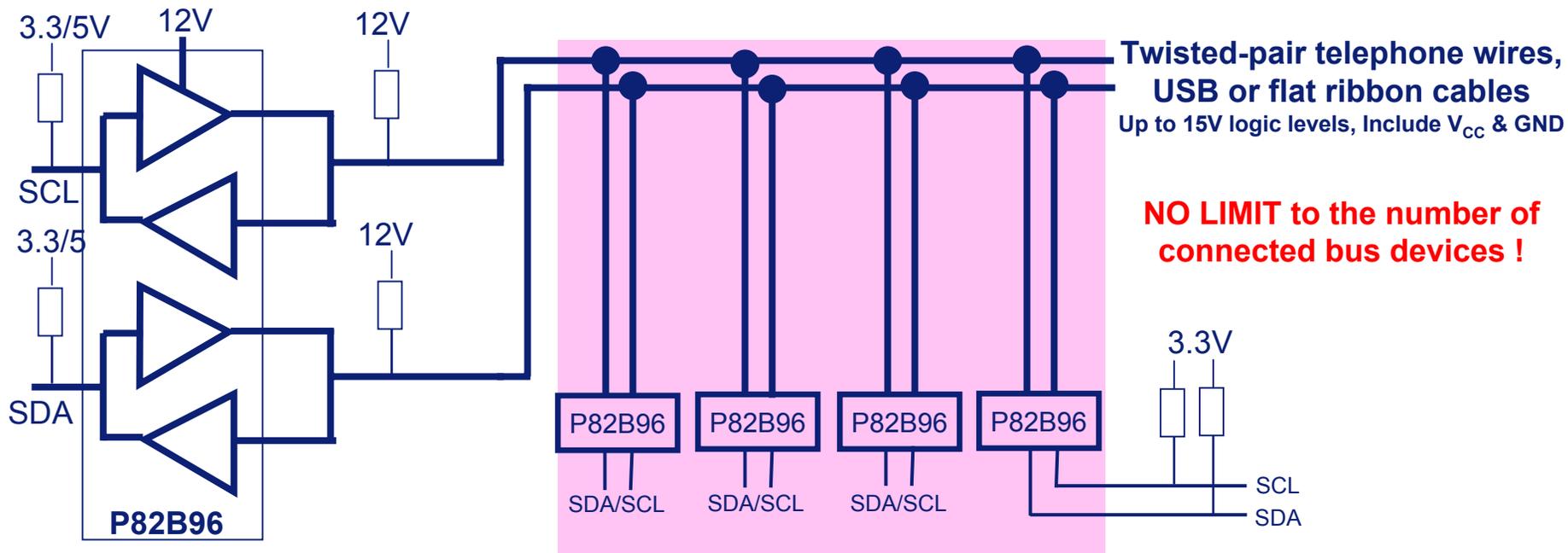# Driving I²C bus signals long distances
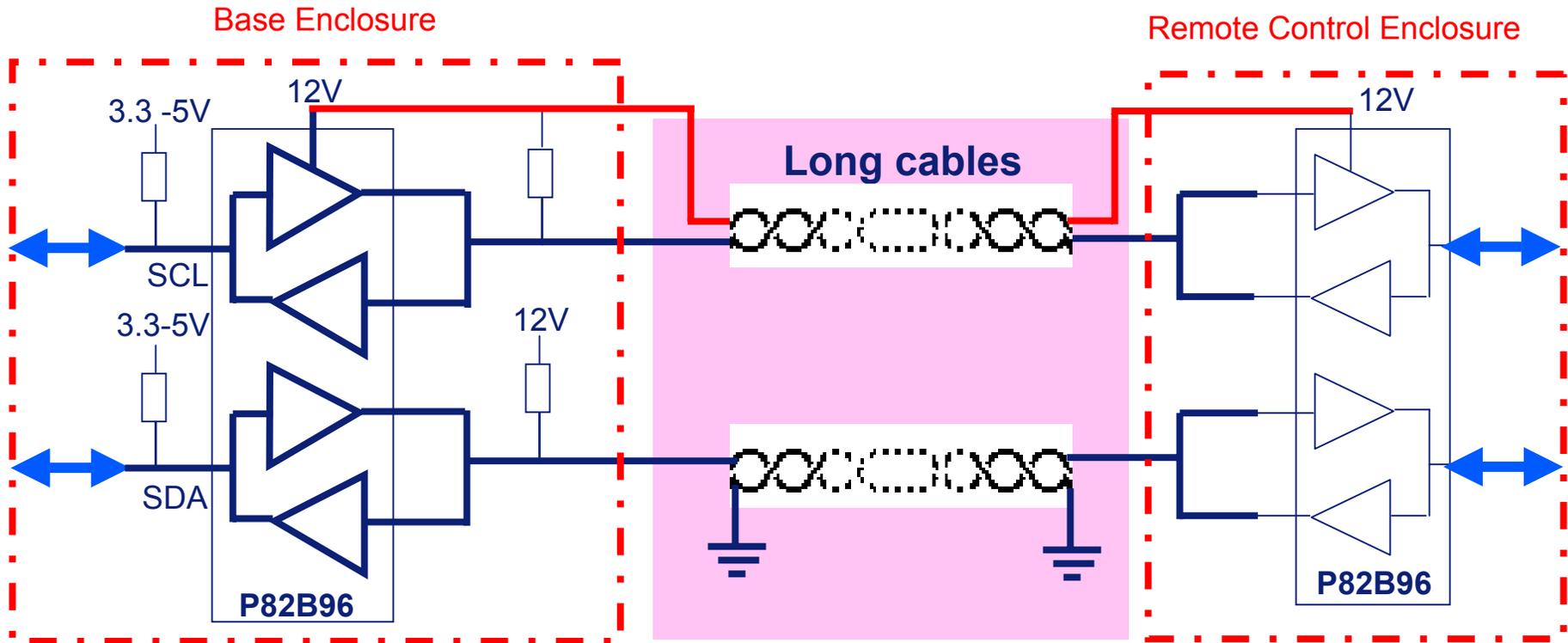
- Normal I²C logic levels (3.3 or 5 V)

- I²C currents (3mA)

- Conventional CMOS logic levels (2-15V)

- Higher current option, up to 30mA static sink

- Normal I²C logic levels (3.3 or 5 V)

- I²C currents (3mA)

Changing I^{2}C bus signals for multi-point applications!

3.3/5V 12V   12V

SCL

3.3/5   12V

SDA

P82B96

Twisted-pair telephone wires,
USB or flat ribbon cables
Up to 15V logic levels, Include V_{CC} & GND

**NO LIMIT to the number of
connected bus devices !**

| P82B96 | P82B96 | P82B96 | P82B96 |

3.3V

SDA/SCL   SDA/SCL   SDA/SCL

SCL
SDA

Link parking meters
and pay stations

Link vending machines
to save cell phone links

Warehouse
pick/pack
systems

- **Factory automation**

- **Access/alarm systems**

- **Video, LCD & LED display signs**

- **Hotel/motel management systems**

- **Monitor emergency lighting/exit signs**

Semiconductors

Changing I^{2}C bus signals for Opto-isolation

3.3/5V

SCL

3.3/5V

P82B96
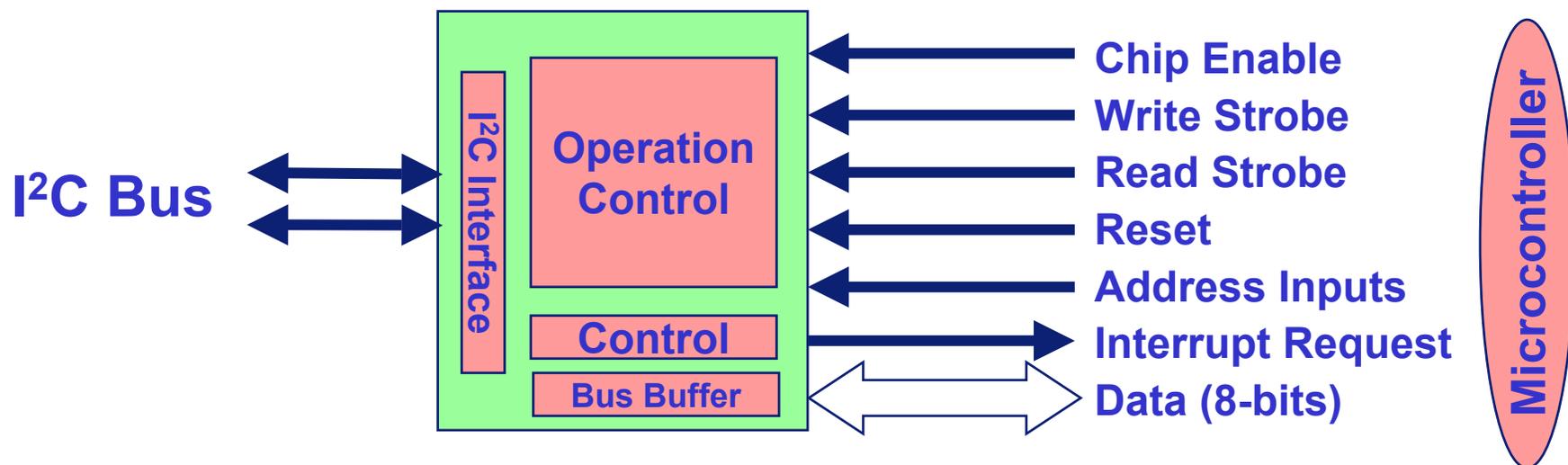
SDA

Vcc 1   Vcc 2

SCL

SDA
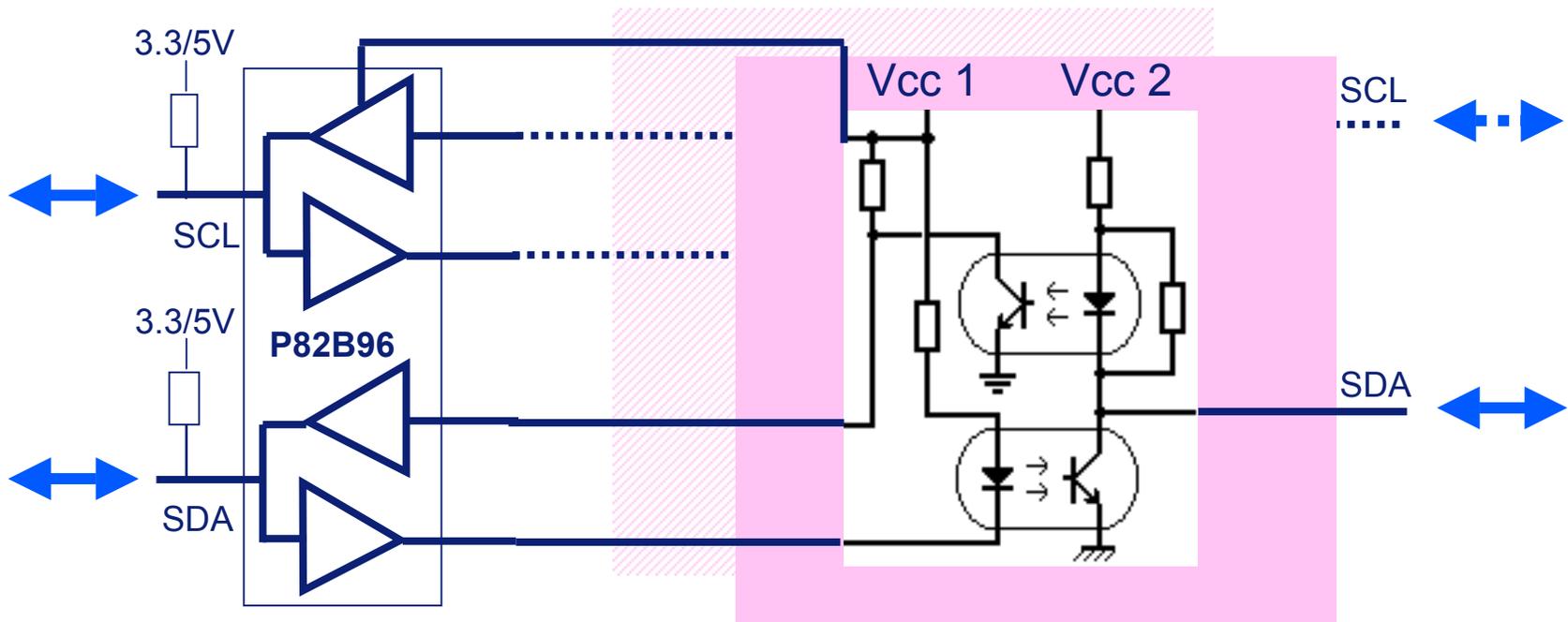
- **Low cost Optos can be directly driven (10-30mA)**

4N36 Optos for ~5kHz
6N137 for 100kHz
HCPL-060L for 400 kHz

- **Controlling equipment on phone lines**
- **AC Mains switches, lamp dimmers, power supplies**
- **Isolating medical or industrial equipment**

Parallel Bus to I^{2}C Bus Controller

I^{2}C Bus

I^{2}C Interface

Operation Control

Control

Bus Buffer

Chip Enable

Write Strobe

Read Strobe

Reset

Address Inputs

Interrupt Request

Data (8-bits)

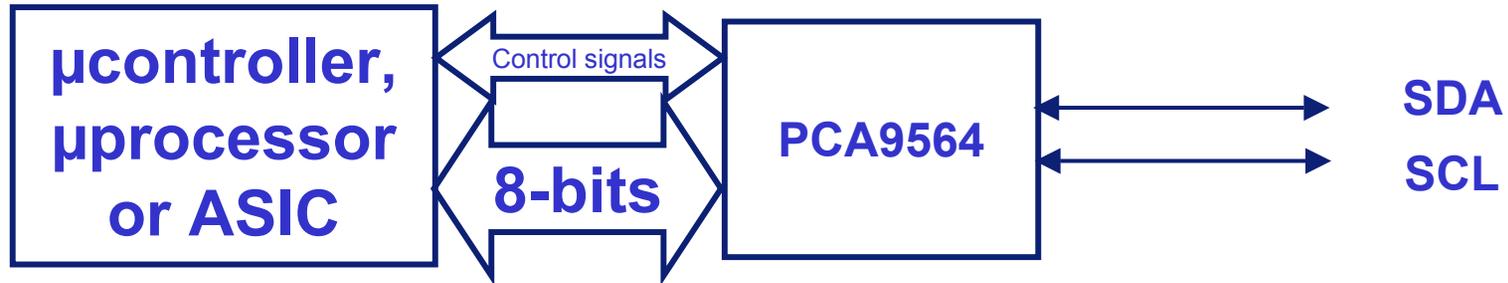**Microcontroller**

FEATURES

-Provides both master and slave functions.
-Controls all the I^{2}C bus specific sequences, protocol, arbitration and timing
-Internal oscillator (PCA9564 only)
-Hardware Reset pin and Power On Reset (POR)

KEY POINTS

-Serves as an interface between most standard parallel-bus microcontrollers/ microprocessors and the serial I^{2}C bus.
-Allows the parallel bus system to communicate with the I^{2}C bus

	Voltage range	Max I^{2}C freq	Clock source	Parallel interface
PCF8584	4.5 - 5.5V	90 kHz	External	3 MHz - Slow
PCA9564	2.3 - 3.6V w/5V tolerance	320 kHz	Internal	50 MHz - Fast

Semiconductors

Application Note AN10148

Application – Add I^{2}C Bus Port

μcontroller, μprocessor or ASIC

Control signals

8-bits

PCA9564

SDA
SCL

• **The PCA9564 converts 8-bit parellel data into a multiple master capable I^{2}C port for microcontrollers, microprocessors, custom ASICs, DSPs, etc.., that need to interface with I^{2}C or SMBus components.**

Bus Controller vs Bit-banging

Hardware I^{2}C

Disadvantages: additional cost

Advantages: frees up the micro to perform other tasks, multi-master capability, glitch filters, bus error detection and recovery, can easily be added to most microcontrollers, simple code (code for a hardware I^{2}C is relatively simple to write (to write a byte, just load the I2CDAT register with a byte and the hardware does the rest) but you may need to take into consideration all the different error conditions (such as lost arbitration, etc))

Bit-banging

Disadvantages: ties up the micro during the transmission and very difficult to use in a multi-master environment
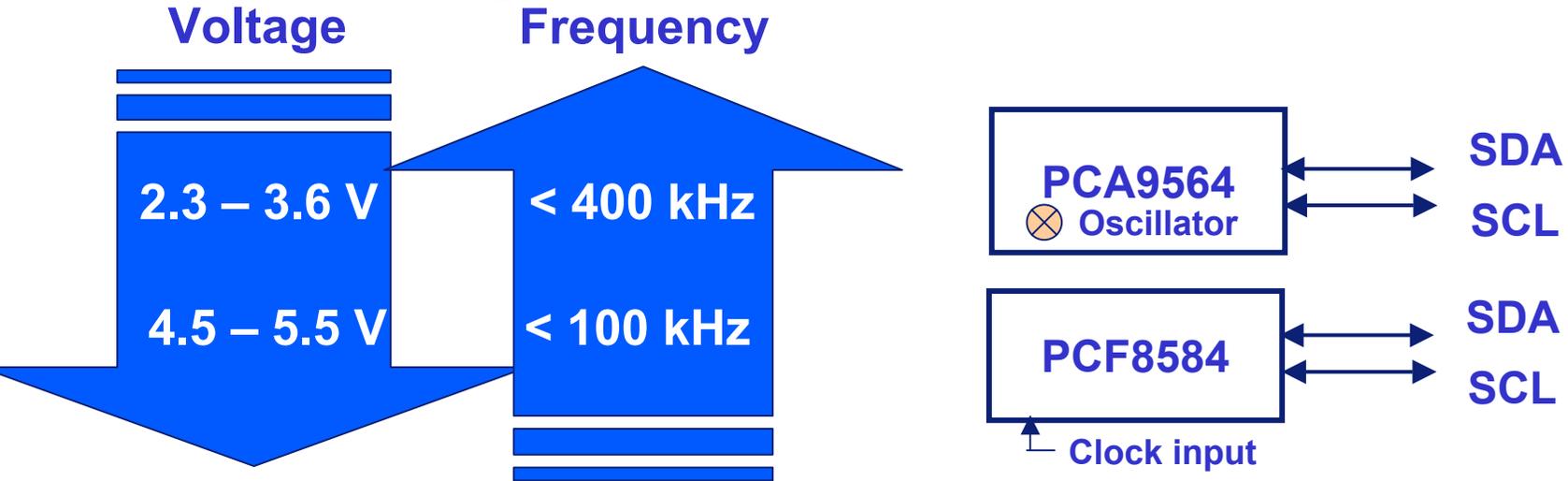
Advantages: inexpensive, can be incorporated into any micro and very little code required (code required for bit-banging an 80C51 micro is only about 50 bytes)

# Application – Add additional I^{2}C Bus Ports
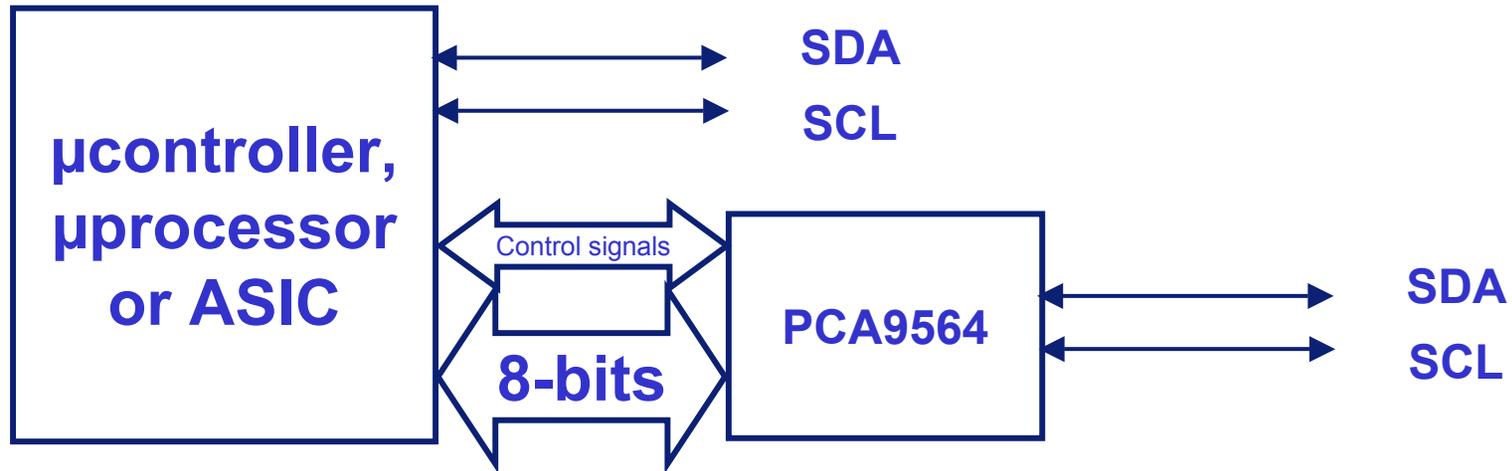
• **The PCA9564 can be used to convert 8-bit parallel data into additional multiple master capable I^{2}C port for microcontrollers, microprocessors, custom ASICs, DSPs, etc.., that already have an I^{2}C port but need one or more additional I^{2}C ports to interface with more I^{2}C or SMBus components or components that can't be located on the same bus (e.g., 100 kHz and 400 kHz slaves).**

Application – Lower Voltage & Higher Frequency Migration Path for PCF8584

Voltage

Frequency

2.3 – 3.6 V

< 400 kHz

4.5 – 5.5 V

< 100 kHz

PCA9564
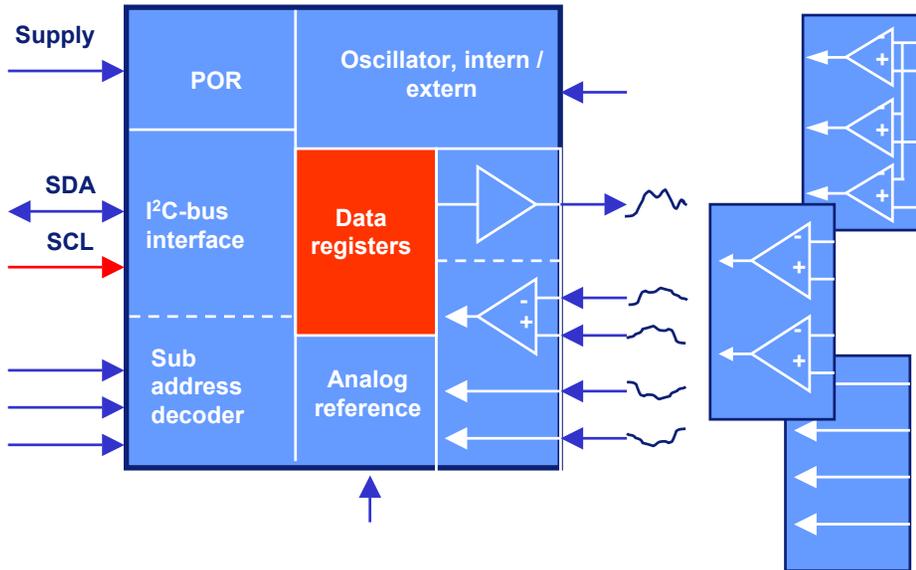Oscillator

SDA

SCL

PCF8584

SDA

SCL

Clock input

• **The PCA9564 does the same type of parallel to serial conversion as the PCF8584. Although not footprint compatible, the PCA9564 provides improvements such as:**

  • **Operating at 3.3 V and 2.5 V voltage nodes**

  • **Allows interface with I^{2}C or SMBus components at speeds up to 400 kHz.**

  • **The built-in oscillator provides a cost effective solution since the external clock input is no longer required.**

  • **Parallel data can be exchanged at speeds up to 50 MHz allowing the use of faster processors. The PCA9564 is optimized for the Intel 8051 architecture.**

Application – Convert 8 bits of parallel data into I^{2}C serial data stream

µprocessor	Control signals 8-bits **PCA9564**	SDA SCL **Master**
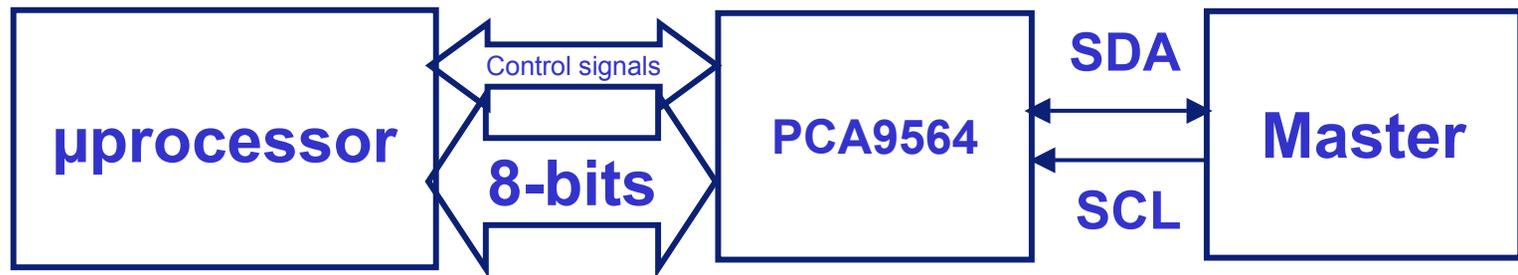
• **Functioning as a slave transmitter, the PCA9564 can convert 8-bit parallel data into a two wire I^{2}C data stream. This prevents having to run 8 traces across the entire width of the PC board.**

Analog to Digital Converter

KEY POINTS
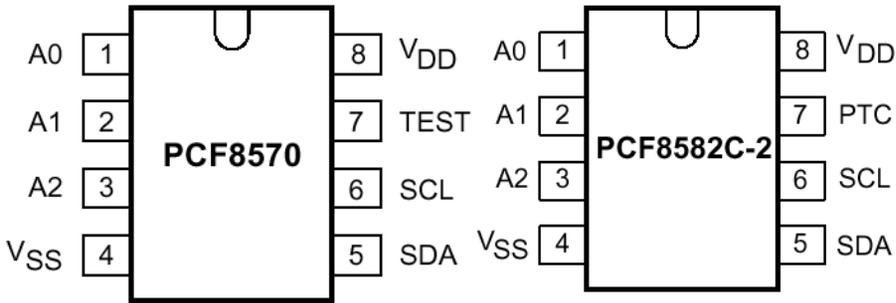-Converts signals from digital to analog and analog to digital

FEATURES
-4 channel A to D
-1 channel D to A
-Internal oscillator
-Power On Reset (POR)

	Voltage range	Max I^2C freq	Resolution
PCF8591	2.5 - 5.5V w/5V tolerance	100 kHz	8-bit

I²C Serial CMOS RAM/EEPROMs

256 x 8-bit RAM

256 x 8-byte (2 kbit)
Also PCF85102C-2 and PCF85103C-2

EEPROM

RAM
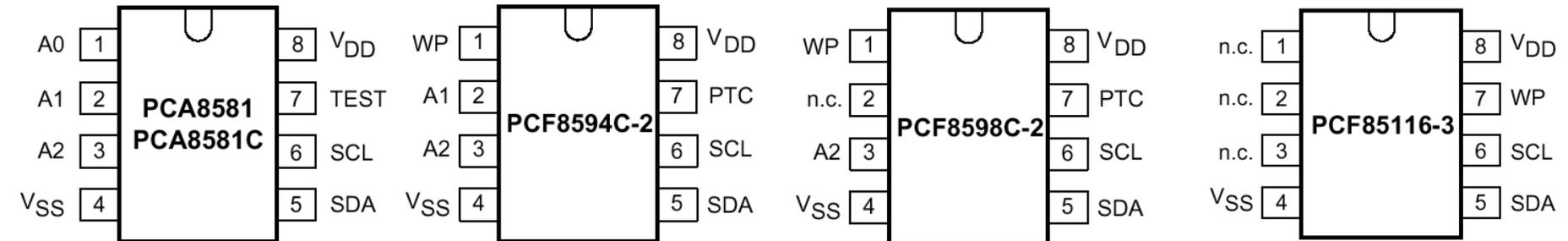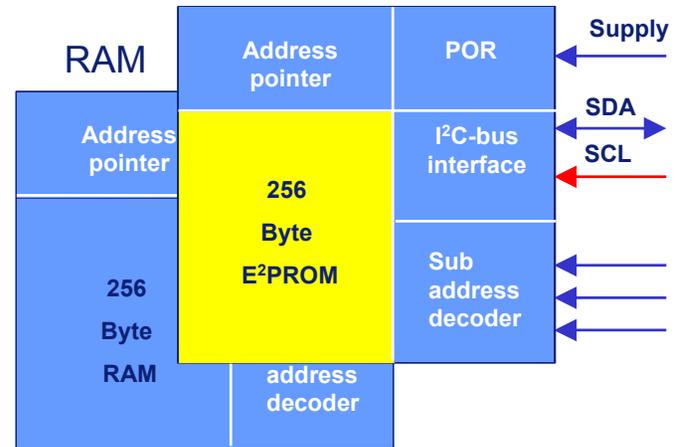
128 x 8-byte (1 kbit)

512 x 8-byte (4 kbit)

**1024 x 8-byte (8 kbit)**

2048 x 8-byte (16 kbit)

FEATURES
-Wide voltage range of 2.5 to 5.5V
-1,000,000 read and write cycles
-10 year data retention

KEY POINTS
-I²C bus is used to read and write information to and from the memory
-Wide voltage range minimizes the number of EEPROMs that need to be in inventory

Semiconductors

1024 X 8 CMOS Security EEPROM

NC 1   8 V$_{CC}$
NC 2   7 WP
$\overline{PROT}$ 3   6 SCL
GND 4   5 SDA

PCA24S08
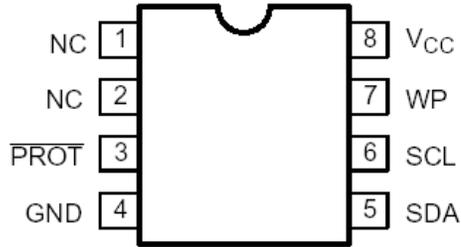
FEATURES

- Nonvolatile memory – I^{2}C serial interface
- Compatible with a Standard 24C08 Serial EEPROM
- Programmable access protection to limit reads or writes
- Lock/unlock function
- Highly-reliable EEPROM memory
- 8 k bits (1 k bytes), organized as 8 blocks of 128 bytes
- 16-byte page write, 5 ms write time
- 10 years retention, 100 k write cycle endurance
- Operating temperature range - 40 to +85 °C
- Operating power supply voltage range of 2.5 V to 3.6 V
- Packages offered: SO8 and TSSOP8
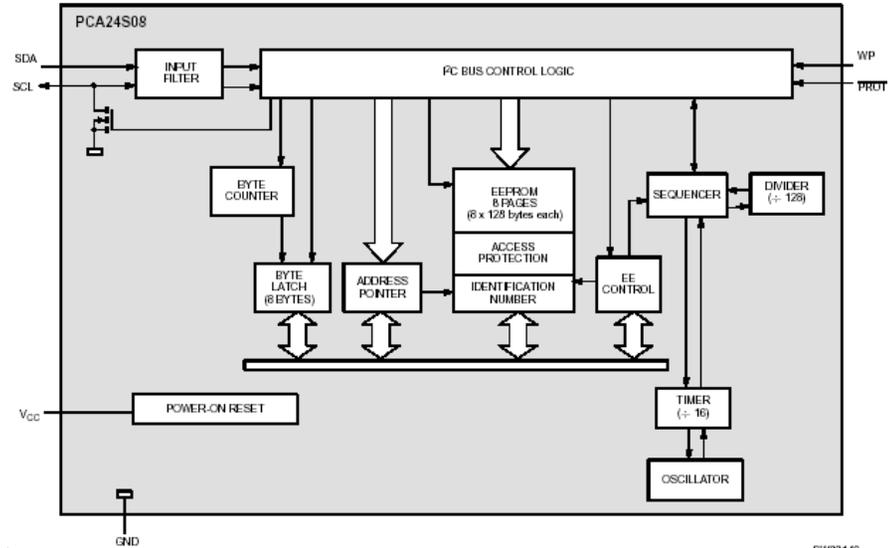
DESCRIPTION

The PCA24S08 functions as a dual access EEPROM with a wired serial port used to access the memory. Access permissions are set from the serial interface side to isolate blocks of memory from improper access.

10101B$_2$B$_1$.

Only 1 device allowed per bus
B$_2$B$_1$ are page access

PCA24S08 – 8 kbit EEPROM with access protection

Samples Sep 03 – Release Dec 03

New!

I²C Temperature Sensors

The human hand is capable of sensing temperature changes within 2°C

Our temperature sensors have a resolution up to 0.125°C

LM75A pinout:
- SDA 1
- SCL 2
- OS 3
- GND 4
- 8 V_CC
- 7 A0
- 6 A1
- 5 A2

Digital Temperature Sensor

and Thermal Watchdog™

SE95 / SE95A pinout:
- SDA 1
- SCL 2
- OS 3
- GND 4
- 8 V_CC
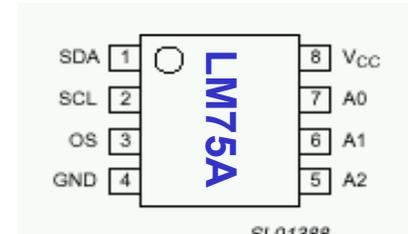- 7 A0
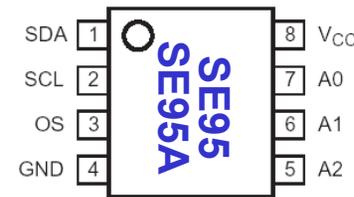- 6 A1
- 5 A2

New!

FEATURES
– Temperature range of – 55 to 125 °C
– Open drain interrupt output

KEY POINTS
– Sense temperature via I²C
– SE95 accurate to ± 1 °C from 0 to 100 °C
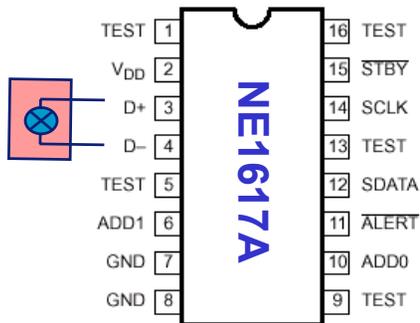– SE95A accurate to ± 0.5 °C from 0 to 100 °C

Ultra High Accuracy Digital

Temperature

Sensor and Thermal Watchdog™

Semiconductors

I²C Temperature Sensors
with Remote Sensor

NE1617A

TEST	1		16	TEST
V_DD	2		15	STBY
D+	3		14	SCLK
D–	4		13	TEST
TEST	5		12	SDATA
ADD1	6		11	ALERT
GND	7		10	ADD0
GND	8		9	TEST

I²C Temperature Monitor

NE1618

TEST1	1		16	TEST16
V_DD	2		15	STBY
D+	3		14	SCLK
D–	4		13	TEST13
TEST5	5		12	SDATA
ADD1	6		11	ALERT
GND	7		10	ADD0
GND	8		9	TEST9

Remote Sensor

Remote Sensor:

Ground

μP On-Board PNP Transistor

See Note 1

or Discrete NPN Transistor

0

High Accuracy Temp Monitor

SA56004-X

V_DD	1		8	SCLK
D+	2		7	SDATA
D–	3		6	ALERT
T_CRIT	4		5	GND

NE1619

SDA	1		16	A0/RESET/NTEST_OUT
SCL	2		15	V_CCPVIN
GND	3		14	2.5V_IN
V_DD/3.3VSB	4		13	3.3V_IN
VID0	5		12	5V_IN
VID1	6		11	12V_IN/VID4
VID2	7		10	D+
VID3	8		9	D–/NTEST_IN

New!

±1°C Accurate, Remote/Local Digital Temperature Sensor with Over Temperature Alarms
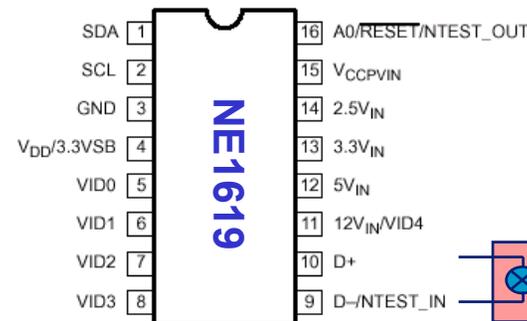
I²C Temperature and Voltage Monitor (Heceta4)

FEATURES
– High temperature accuracy
– SA56004 has eight address
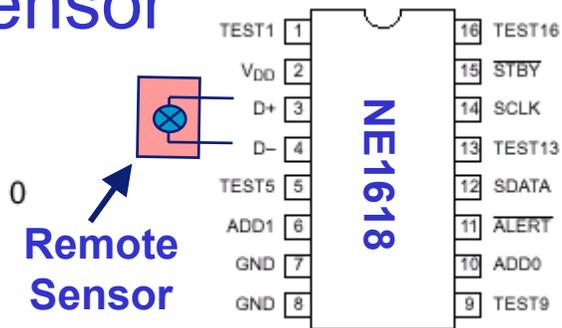
KEY POINTS
– Sense temperature and/or monitor voltage via I²C
– Remote sensor can be internal to microprocessor

SA56004 Applications

APPLICATIONS

• System thermal management in laptops, desktops, servers and workstations

• Computers and office electronic equipment

• Electronic test equipment & instrumentation

• HVAC

• Industrial controllers and embedded systems
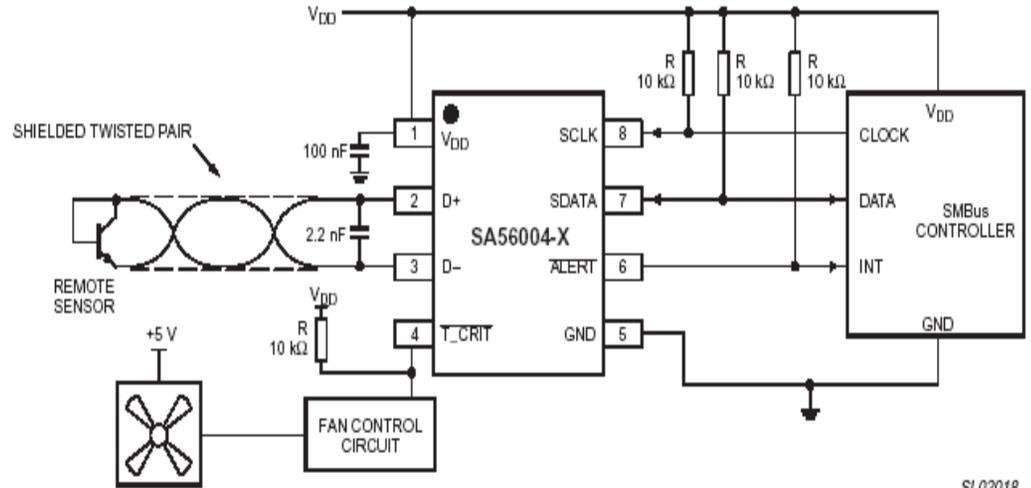
SL02018

FEATURES

• On-chip local and remote microprocessor thermal diodes or diode connected transistors temperature sensing within ±1 °C

• Offset registers available for adjusting the remote temperature accuracy

• Programmable under/over temperature alarms: ALERT and T_CRIT

• SMBus 2.0 compatible interface, supports TIMEOUT and 100/400 kHz I2C interface

• 11-bit, 0.125 °C resolution

• 8 different device addresses are available for server applications. The SA56004-ED/EDH with marking code ARW is address compatible with the National LM86, the MAX6657/8 and the ADM1032.

I²C Microcontroller
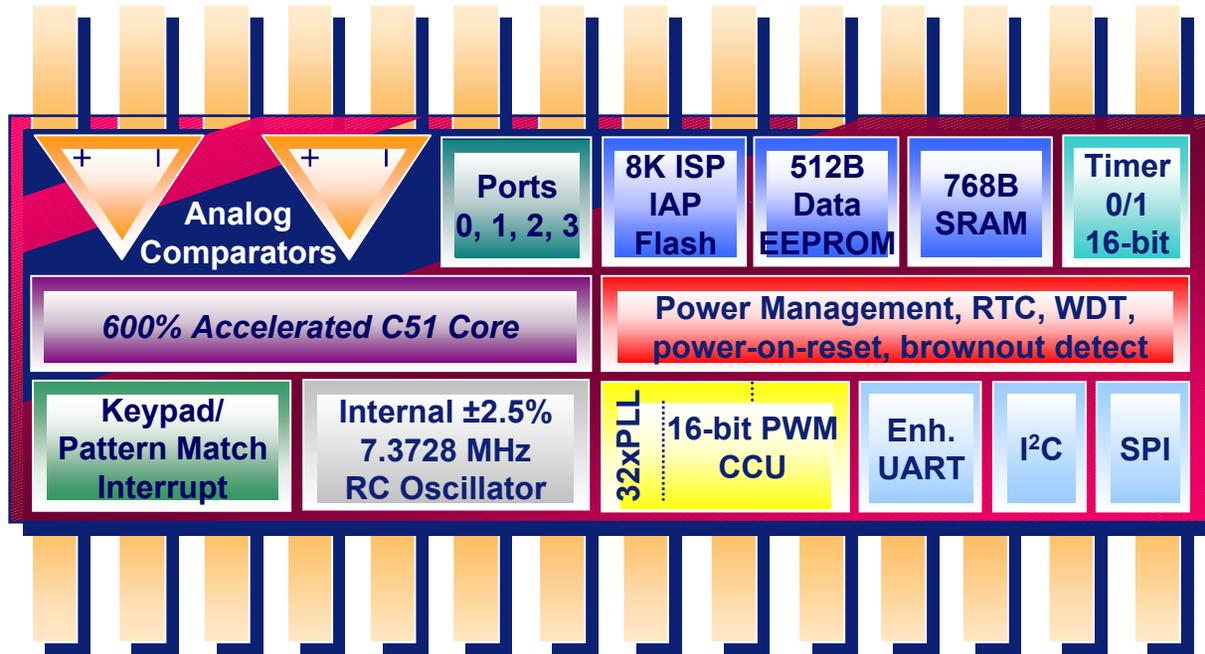
The μcontroller provides the brains behind the I²C bus operation and most feature at least one I²C port.

P87C55x	100 kHz I²C
P87C6xxX2	400 kHz I²C
P87LPC76x	100 kHz I²C
P89C66x	100 kHz I²C
P89LPC932	400 kHz I²C

I^{2}C Microcontroller

In December we've released a new P87C654X2 and with this family we also released our first microcontroller (P87C661) with two separate byte oriented I^{2}C interfaces.

The two I^{2}C blocks are useful for applications:
• Which need to support different transmission rates (e.g. 400 kHz and 100 kHz)
• With high amount of I^{2}C devices that physically can't be addressed all on one bus due to address conflicts
• Require gateway/re-route capability

I^{2}C Microcontroller - Bit Wise @ 100 kHz

P87LPC760   8-bit 80C51 (6 Clk) with 1 KB OTP, 128B RAM, IRC, UART, etc – 14 pin

P87LPC761   8-bit 80C51 (6 Clk) with 2 KB OTP, 128B RAM, IRC, UART, etc – 16 pin

P87LPC762   8-bit 80C51 (6 Clk) with 2 KB OTP, 128B RAM, IRC, UART, etc – 20 pin

P87LPC764   8-bit 80C51 (6 Clk) with 4 KB OTP, 128B RAM, IRC, UART, etc – 20 pin

P87LPC767   8-bit 80C51 (6 Clk) with 4 KB OTP, 128B RAM, 8-bit ADC, IRC, UART, etc – 20 pin

P87LPC768   8-bit 80C51 (6 Clk) with 4 KB OTP, 128B RAM, PWM, IRC, UART, etc – 20 pin

P87LPC769   8-bit 80C51 (6 Clk) with 4 KB OTP, 128B RAM, ADC/DAC, IRC, UART, etc–20 pin

I^{2}C Microcontroller - Byte Wise @ 100 kHz

P80C552   8-bit 80C51 ROMless with 256B RAM, 10-bit ADC, PWM, UART, etc – 68 pin

P80C554   8-bit 80C51 ROMless with 512B RAM, 10-bit ADC, PWM, UART, etc – 64 pin

P87C552   8-bit 80C51 with 8 KB OTP, 256B RAM, 10-bit ADC, PWM, UART, etc – 68 pin

P87C554   8-bit 80C51 with 16 KB OTP, 512B RAM, 10-bit ADC, PWM, UART, etc – 64/68 pin

P87C654X2   8-bit 80C51 (6 Clk) with 16 KB OTP, 256B RAM, UART, etc – 44 pin

P80C557E4   8-bit 80C51 ROMless with 1KB RAM, 10-bit ADC, UART, low EMI, etc – 80 pin

P87C557E8   8-bit 80C51 with 64 KB OTP, 2 KB RAM, 10-bit ADC, UART, low EMI etc – 80 pin

P87C591   8-bit 80C51 with 16 KB OTP, 512B RAM, 10-bit ADC, CAN2.0B, UART, etc – 44 pin

P89C660   8-bit 80C51 (6 Clk) with 16 KB Flash, 512B RAM, PCA, PWM, UART, etc – 44 pin

P89C662   8-bit 80C51 (6 Clk) with 32 KB Flash, 1 KB RAM, PCA, PWM, UART, etc – 44 pin

P89C664   8-bit 80C51 (6 Clk) with 64 KB Flash, 2 KB RAM, PCA, PWM, UART, etc – 44 pin

P89C668   8-bit 80C51 (6 Clk) with 64 KB Flash, 8 KB RAM, PCA, PWM, UART, etc – 44 pin

P89C669   8-bit 80C51 (6 Clk) with 96 KB Flash, 3 KB RAM, PCA, PWM, 2 UARTs, etc – 44 pin

Semiconductors

I^{2}C Microcontroller - Byte Wise @ 400 kHz

LPC2104   16/32-bit ARM7 with 128 KB Flash, 16 KB RAM, 2 UART, RTC, SPI, etc – 48 pin

LPC2105   16/32-bit ARM7 with 128 KB Flash, 32 KB RAM, 2 UART, RTC, SPI, etc – 48 pin

LPC2106   16/32-bit ARM7 with 128 KB Flash, 64 KB RAM, 2 UART, RTC, SPI, etc – 48 pin

LPC2114   16/32-bit ARM7 with 128 KB Flash, 16 KB RAM, 10b ADC, UARTs, SPIs, etc – 64 pin

LPC2124   16/32-bit ARM7 with 256 KB Flash, 16 KB RAM, 10b ADC, UARTs, SPIs, etc – 64 pin

P89LPC920   8-bit 80C51 (2 Clk) with 2 KB Flash, 256 B RAM, IRC, UART, RTC, etc – 20 pin

P89LPC921   8-bit 80C51 (2 Clk) with 4 KB Flash, 256 B RAM, IRC, UART, RTC, etc – 20 pin

P89LPC922   8-bit 80C51 (2 Clk) with 8 KB Flash, 256 B RAM, IRC, UART, RTC, etc – 20 pin

P89LPC930   8-bit 80C51 (2 Clk) with 4 KB Flash, 256 B RAM, IRC, UART, RTC, etc – 28 pin

P89LPC931   8-bit 80C51 (2 Clk) with 8 KB Flash, 256 B RAM, IRC, UART, RTC, etc – 28 pin

P89LPC932   8-bit 80C51 (2 Clk) with 8 KB Flash, 256 B RAM, 512 B EE, IRC, CCU, etc – 28 pin

PXAS30   16-bit ROMless with 1 KB RAM, 2 UARTs, PCA, PWM, 8-bit ADC, etc – 68/80 pin

PXAS37   16-bit with 32K OTP, 1 KB RAM, 2 UARTs, PCA, PWM, 8-bit ADC, etc – 68/80 pin

Semiconductors

I²C Signal Conversion

These microcontrollers have **I²C and UART (RS-232)** ports to allow conversion
- P87C6xxx2 family (661 has two byte oriented I²C interfaces)
- P87C55x
- P87LPC76x family
- P89C66x
- P89LPC932 and future LPC9xx products

These microcontrollers have **I²C and SPI** ports to allow conversion
- XA
- 87C51MX (future product)
- 89LPC9xx (future product)

These microcontrollers and USB devices allow a two device conversion between **I²C and USB**
- PDIUSBD12 + P89C66x -> 100 kHz I²C and USB1.1
- ISP1181 + P89C66x -> 100 kHz I²C and USB1.1
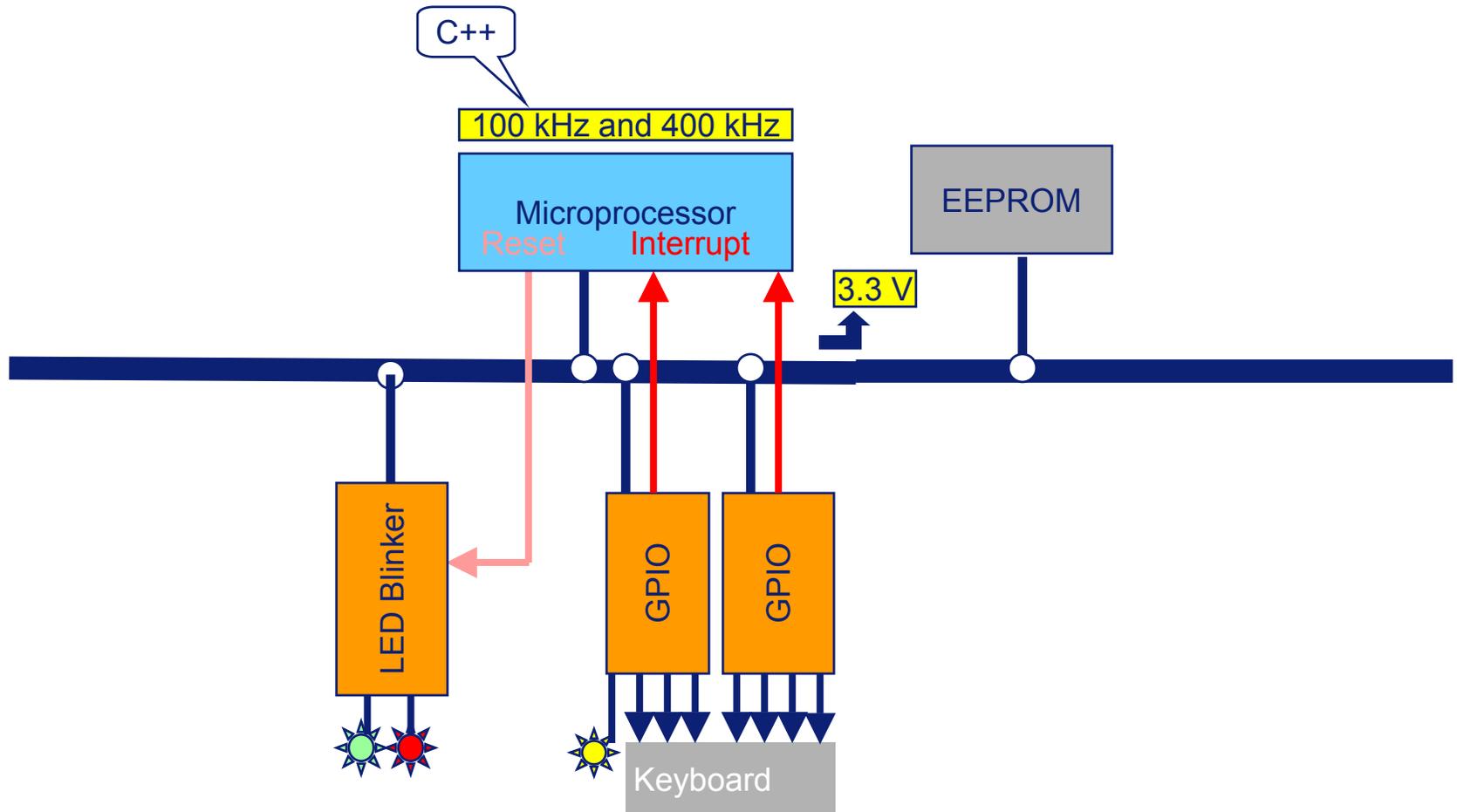- ISP1581 + P89LPC932 -> 400 kHz I²C and USB2.0

These ucontrollers have **I²C and CAN** ports to allow conversion
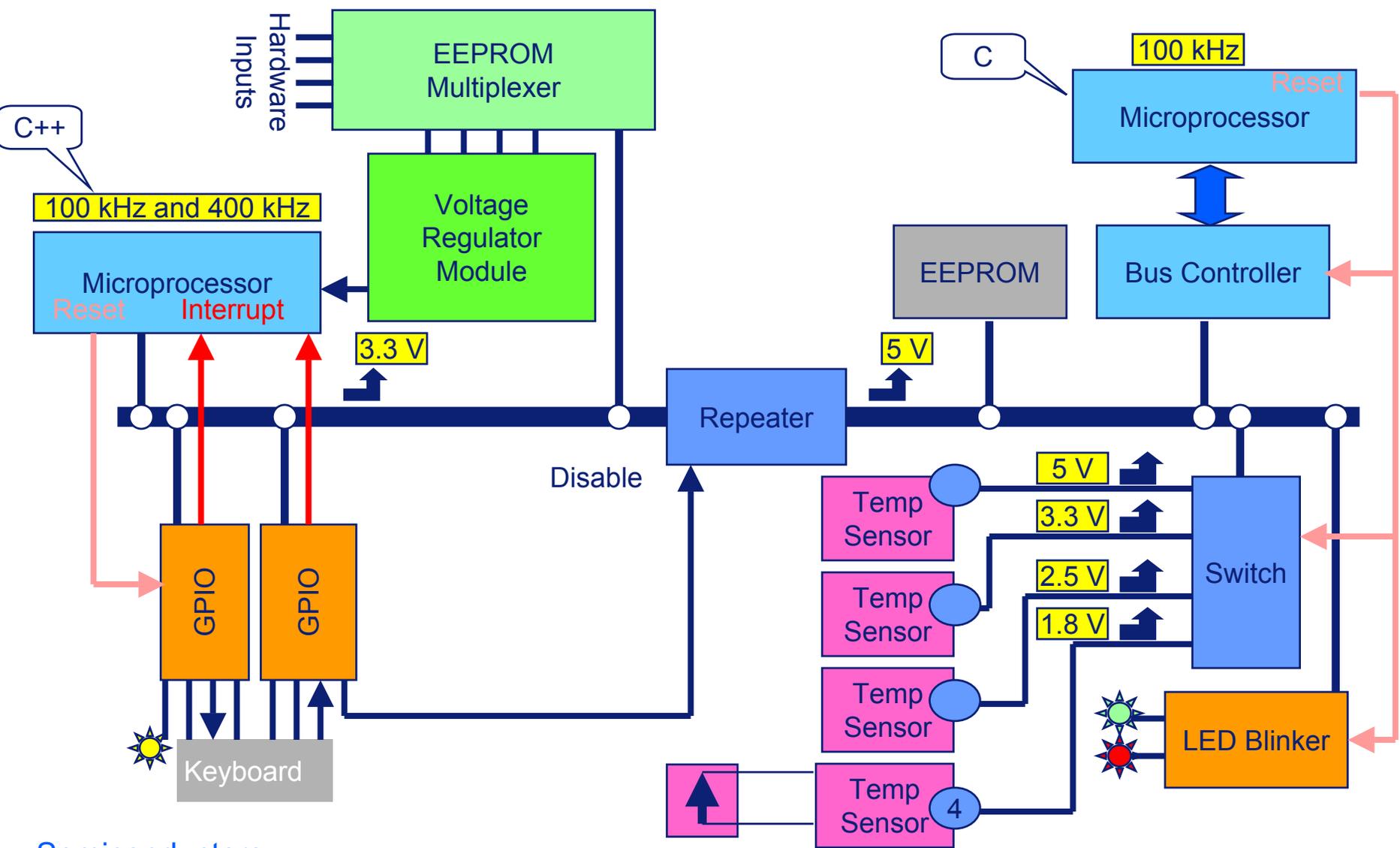- P87C591 - 8 bit solution
- PXA-C37 - 16 bit solution

Products from > www.semiconductors.philips.com/microcontrollers
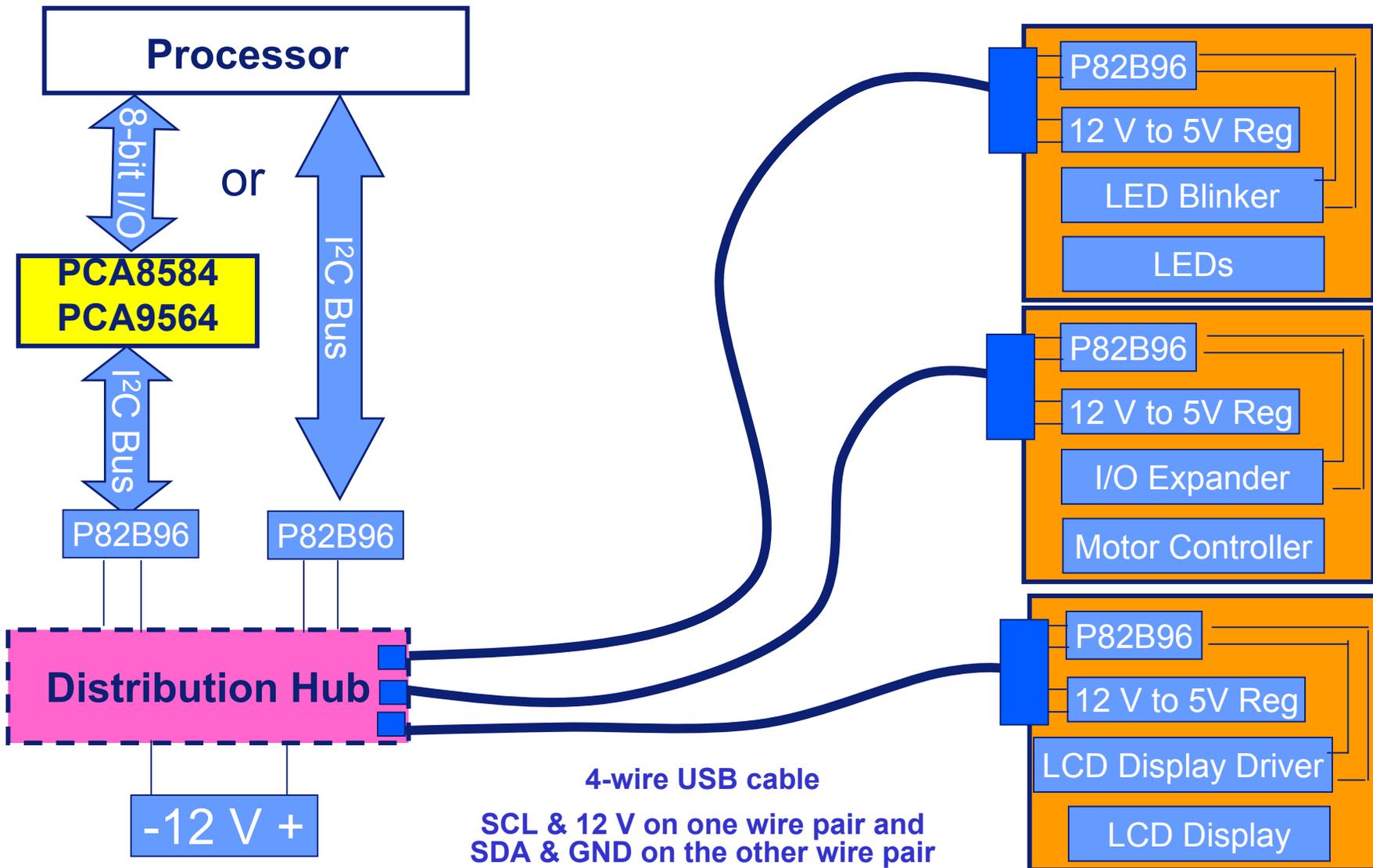**Support > www.PhilipsMCU.com/products/standard/microcontrollers/support/feedback/**

PHILIPS

Semiconductors
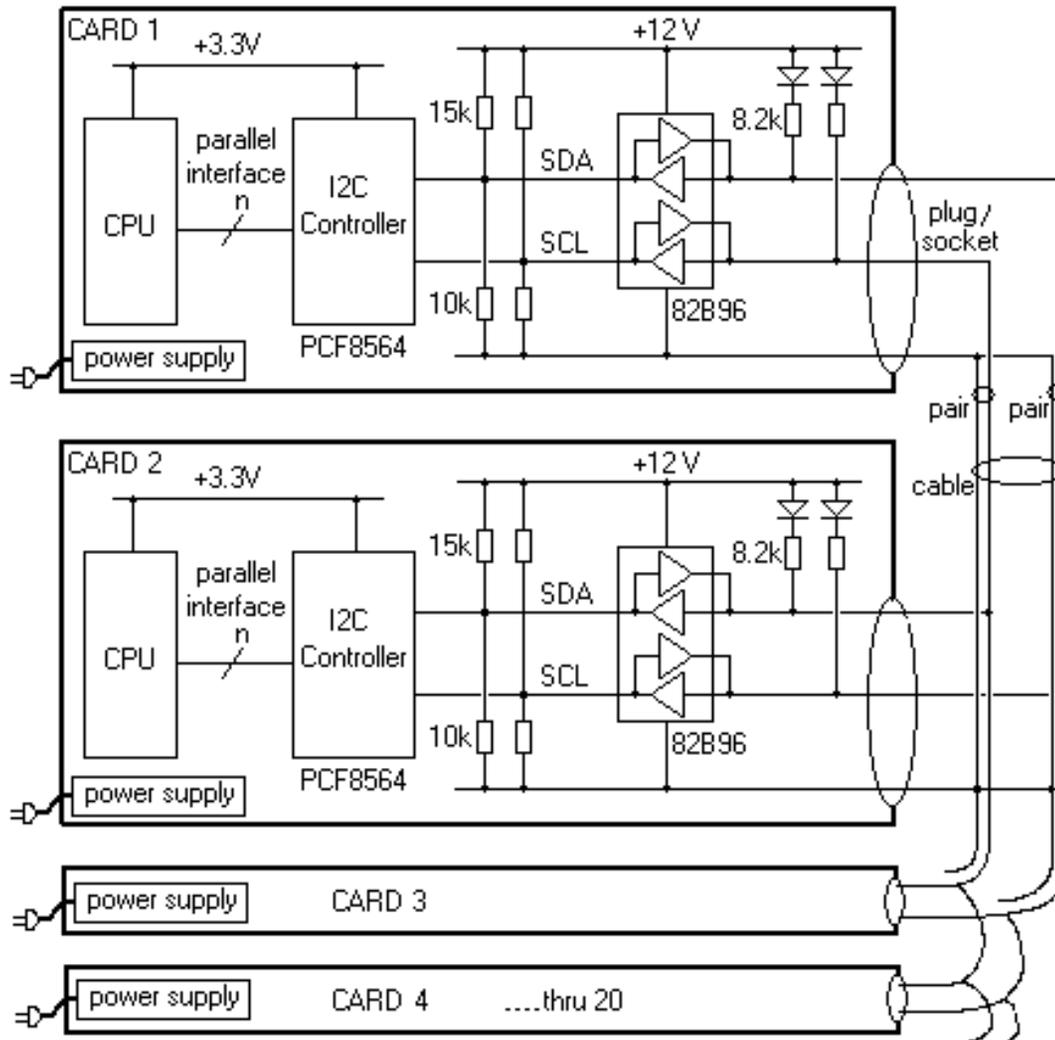
I^{2}C Bus Basics - Typical Bus Arrangement

I2C Bus Basics - Complex Bus Arrangement

Slot or Gaming Machine Setup

Processor

8-bit I/O

or

I²C Bus

PCA8584
PCA9564

I²C Bus

P82B96   P82B96

Distribution Hub

-12 V +

4-wire USB cable

SCL & 12 V on one wire pair and
SDA & GND on the other wire pair

P82B96
12 V to 5V Reg
LED Blinker
LEDs

P82B96
12 V to 5V Reg
I/O Expander
Motor Controller

P82B96
12 V to 5V Reg
LCD Display Driver
LCD Display

Changing I^{2}C bus signals for multi-point applications!

Twisted-pair telephone wires, USB or flat ribbon cables
Up to 15V logic levels, Include V$_{CC}$ & GND

NO LIMIT to the number of connected bus devices !

Connect servers together

Intelligent Platform Management Interface

- IPMI is **new Intel initiative** in conjunction with hp, NEC and Dell
- Consists of three specifications:
  - Intelligent Platform Management Interface (IPMI) for software extensions
  - Intelligent Platform Management Bus (IPMB) for intra-chassis (in side the box) extensions
  - Inter Chassis Management Bus (ICMB) for inter-chassis (outside of the box) extensions
- Needed since as the complexity of systems increase, MTBF decreases
- Defines a standardized, abstracted, message-based interface to intelligent platform management hardware.
- Defines standardized records for describing platform management devices and their characteristics.
- Provides a self monitoring capability increasing reliability of the systems

Intelligent Platform Management Bus

• Standardized bus and protocol for extending management control, monitoring, and event delivery **within** the chassis:

- I^2C based

- Multi-master

- Simple Request/Response Protocol

- Uses IPMI Command sets

- Supports non-IPMI devices

• Physically I^2C but write only (master capable devices), hot swap not required.

• Enables the Baseboard Management Controller (BMC) to accept IPMI request messages from other management controllers in the system.

• Allows non-intelligent devices as well as management controllers on the bus.

• BMC serves as a controller to give system software access to IPMB

IPMI Details

- Defines a standardized interface to intelligent platform management hardware
  - Prediction and early monitoring of hardware failures
  - Diagnosis of hardware problems
  - Automatic recovery and restoration measures after failure
  - Permanent availability management
  - Facilitate management and recovery
  - Autonomous Management Functions: Monitoring, Event Logging, Platform Inventory, Remote Recovery
  - Implemented using Autonomous Management Hardware: designed for Microcontrollers based implementations
- Hardware implementation is isolated from software implementation
- New sensors and events can then be added without any software changes

Overall IPMI Architecture
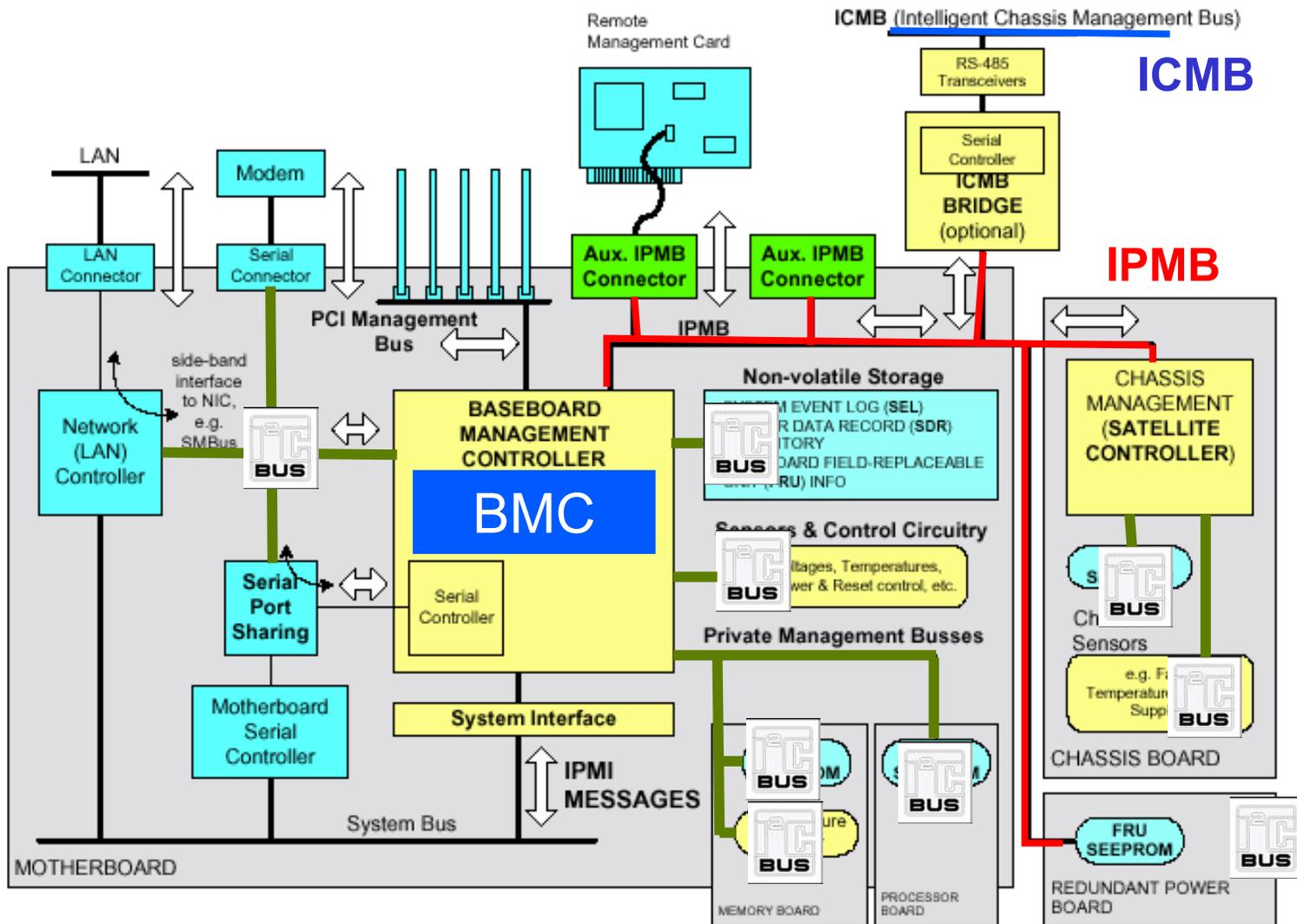
More information – www.intel.com/design/servers/ipmi/ipmi.htm

CompactPCI, AdvancedTCA and VME use IPMI

Known as	Specification	Based on	Comments
cPCI	PICMG 2.0	NA	No IPMB
cPCI	PICMG 2.9	IPMI 1.5	Single hot swap IPMB optional
AdvancedTCA	PICMG 3.x	IPMI 1.5	Dual redundant hot swap IPMB mandatory

- PICMG 2.0: CompactPCI Core
- PICMG 2.9: System Management
- PICMG 3.0: AdvancedTCA Core
    - 3.1 Ethernet Star (1000BX and XAUI)
    - 3.2 InfiniBand® Star & Mesh
    - 3.3 StarFabric
    - 3.4 PCI Express
- VME will use PICMG 2.9 specifications
- Backplanes lead AdvancedTCA push – excellent article >
http://newsletter.planetanalog.com/cgi-bin4/flo/y/eLZD0CePey0tJ0BwCW0Ay
- Page 32 of AN10216 I^{2}C Manual for additional information

These systems will use the PCA9511/12/13/14/15/16/18 or P82B715/96 to help buffer capacitance and provide hot swap protection.

Agenda

- **What is I^{2}C and why would you be interested in using the I^{2}C bus?**

- **What new I^{2}C devices are there and what are the typical applications?**

- **How are we going to help you design-in these devices?**

I2C 2002-1A Evaluation Board Kit

Provide easy to use, PC based system to play with the I2C devices and learn how they operate.

FEATURES

- Converts Personal Computer parallel port to I2C bus master
- Simple to use graphical interface for I2C commands
- Win-I2CNT software compatible with Windows 95, 98, ME, NT, XP and 2000
- Order kits at www.demoboard.com

PCA9551 LED Blinkers Win-I2CNT Interface Screen

Provide easy to use graphical interface that is device specific but also includes an universal mode.

Select LEDs mode
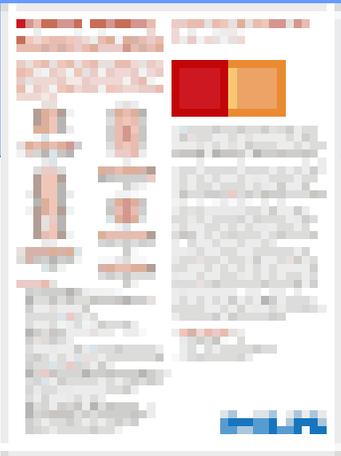
Device address CC for PCA9551

Write and Read Registers

Select blinking options

Register information

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I^{2}C Product Flyers and Selection Guides

|	
2003 I^{2}C Selection Guide	Order Number: 9397 750 10591
2003 CBT Selection Guide	Order Number: 9397 750 10336
LM75A	Order Number: None
NE1617A/18/19	Order Number: 9397 750 07609
PCA8550	Order Number: 9397 750 04323
PCA9500/01	Order Number: 9397 750 09897
PCA9504A	Order Number: 9397 750 08562
PCA9515/16	Order Number: 9397 750 08205
PCA9540/42/44	Order Number: 9397 750 06542
PCA954X	Order Number: 9397 750 09222
PCA9550/51/52	Order Number: 9397 750 09208
PCA9554/54A/55	Order Number: 9397 750 08924
PCA9556	Order Number: 9397 750 06812
PCA9558	Order Number: 9397 750 08211
PCA9559	Order Number: 9397 750 06813
PCA9560/61	Order Number: 9397 750 09206
PCF EEPROM	Order Number: 9397 750 09209
P82B96	Order Number: 9397 750 09084

Provide overview of all the devices to
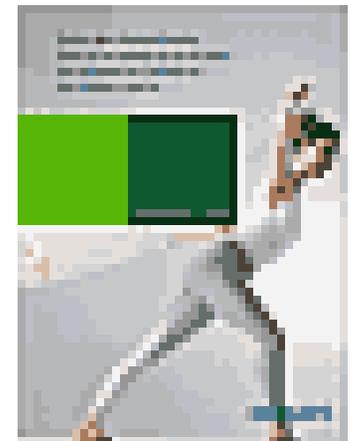
Download from > www.philipslogic.com/products/collateral

Semiconductors

Technical Support Information

Application Notes

AN250   PCA8550 4-Bit Multiplexed/1-Bit Latched 5-Bit I^{2}C E2PROM

AN255   I^{2}C and SMBus Hubs, Buffers, and Repeaters

AN444   P82B715 I^{2}C Bus Buffer

AN460   Introducing the P82B96 I^{2}C Bus Buffer

AN262   PCA954X Multiplexers and Switches

AN264   I^{2}C Devices for LED Display Control

AN469   I^{2}C I/O Port Selection

AN10145 Bi-Directional Voltage Translators

AN10146 I^{2}C 2002-1A Evaluation Board

AN10148 I^{2}C Bus Controller ** (July)

AN10149 PCA9564 Evaluation Board ** (Sep)

AN10160 I^{2}C Hot Swap Bus Buffers (preliminary)

AN10216 I^{2}C Manual
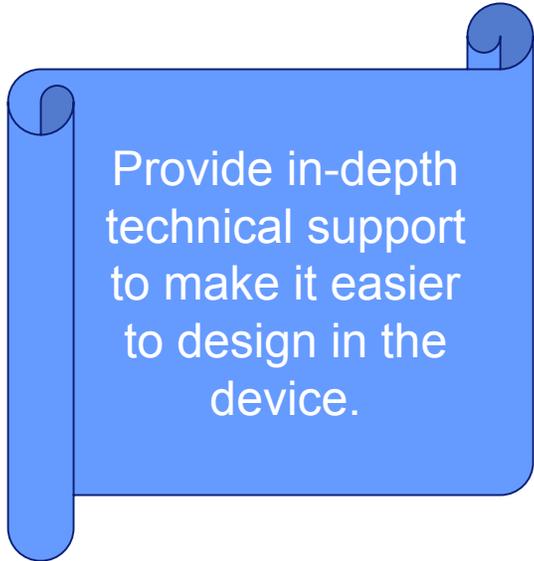
Provide in-depth technical support to make it easier to design in the device.

Download from > www.philipslogic.com/support/appnotes/

I^{2}C Sample Kit

The I^{2}C Sample Kit consists of eight different I^{2}C devices in tape inserted into the I^{2}C Sample Kit box with an informative insert.

Devices include three each of the GTL2010PW, P82B96TD, PCA9551D, PCA9545D, PCA9555D, PCA9557D, PCA9515D and PCA9501D

Provide small quantity of free samples to make it easy to assemble and test your system.

Request I^{2}C Sample Kit or individual samples from your Philips Sales Representative or directly from I2C.Support at philips.com

I^{2}C Device Data Sheets, IBIS models Application Notes and Other Information

Product family descriptions line cards cross reference data sheets

Link to app notes models user guides PLL design software datasheets

Provide easy to access to all the up to date data sheets, application notes and modeling tools.

www.philipslogic.com/i2c   or www.semiconductors.philips.com/i2c