Frequency-to-Voltage Converter uses Sample-and-Hold to Improve Response and Ripple

National Semiconductor
Linear Brief 45

Most frequency-to-voltage (F-to-V) converters suffer from the classical tradeoff of ripple versus speed of response. For example, the basic F-to-V converter shown below has 13 mVp-p of ripple, and a rather slow 0.6 second settling time, when C_{FILTER} is 1 μF. If you want less ripple than that, the response time will be even slower. If you want quicker response, it is easy to decrease C_{FILTER}, but the ripple will increase by the same factor.

The improved circuit in *Figure 2* makes an end-run around these compromises. A low-cost sample-and-hold circuit such as LF398 can sample the F-to-V's output at the peak of its ripple, and hold it until the next cycle. The LF398 has fairly low output ripple (rms) but it does have some short duration noise spikes and glitches which can be removed easily with a simple output filter. The ripple at the output of the active filter V6 is smaller than 1 mV peak, but the settling time for a step change of input frequency is only 60 ms, or ten times quicker than the "basic" FVC with C_{FILTER} = 1 μF.

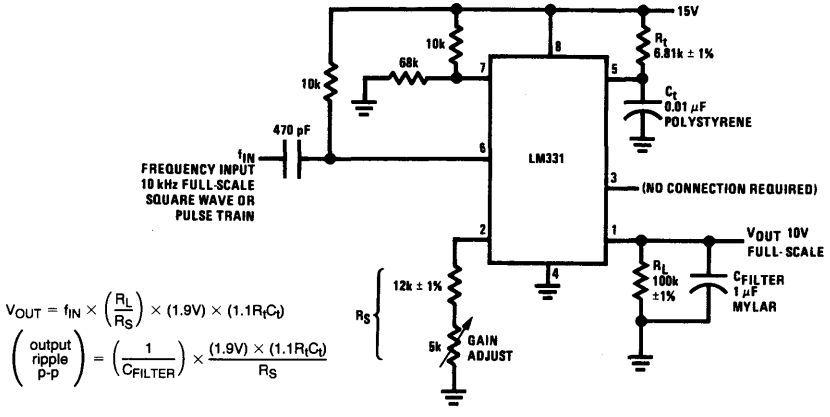

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FIGURE 1. Basic Frequency-to-Voltage Converter

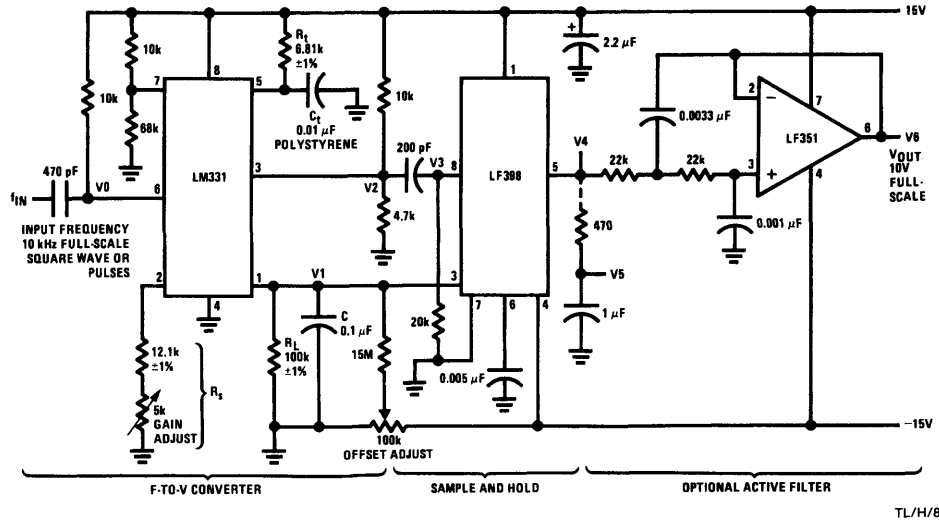

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FIGURE 2. Improved F-to-V Converter Using Sample-and-Hold

DETAILS OF OPERATION (Refer to *Figure 3*, Waveforms)

When the input frequency waveform has a negative-going transition, pin 6 of the LM331 is driven momentarily lower than the 13V threshold voltage at pin 7. This initiates a timing cycle controlled by the R_t and C_t at pin 5, and also causes a transition from +5V to 0V at pin 3, (the normal VFC logic output) which is usually left unused in F-to-V operation.

During the timing cycle ($t = 1.1 \times R_t \times C_t = 75\ \mu s$, for the example shown) a precision current source $i = 1.9\ V/R_S$ flows out of pin 1 of the LM331, and charges V1 up to a value slightly higher than the average DC value of V1. At the end of the timing cycle, V1 stops charging up, and also V2 rises. The 10 kΩ pull-up resistor is coupled (through the 200 pF capacitor) to V3, and causes the LF398 to *sample* for about 5 μs. Then the LF398 goes back into *hold*. This entire operation is repeated at the same frequency as f_{IN}. The average voltage at V1 will be the same 10V full scale, according to the same formula of *Figure 1*. And the peak-to-peak ripple can be computed as 65 mV peak, 130 mVp-p, using the appropriate formula.

Now, the input to the sample-and-hold at pin 3 may have a 10.000V average DC value, but the output will be at 10.065V, because the sample occurs at the peak value of V1. Thus, to get an output with low offset, a 15 MΩ resistor is used to offset the V1 signal to a lower level. Trim the offset adjust pot to get $V_{OUT} = 1V$ at 1 kHz, and trim the gain adjust pot to get $V_{OUT} = 10V$ at 10 kHz (the interaction is minor), as measured at V4, V5, or V6. The rms value of the ripple at V4 is rather small, but the peak-to-peak ripple (spikes and glitches) may be excessive. A simple R-C filter can provide a filtered output at V5; or a simple active filter using an inexpensive LF351, will give sub-millivolt (peak) ripple at V6, with improved settling time and low output impedance.

This F-to-V converter will have a good linearity, better than 0.1%, but only from 10 kHz down to 500 Hz. Between 200 Hz and 20 Hz, V_{OUT} is not very proportional to f_{IN}. And at 0 Hz, the output will be indeterminate, because the sample-and-hold will never sample! However, there are many F-to-V applications where a 20:1 frequency range is adequate.

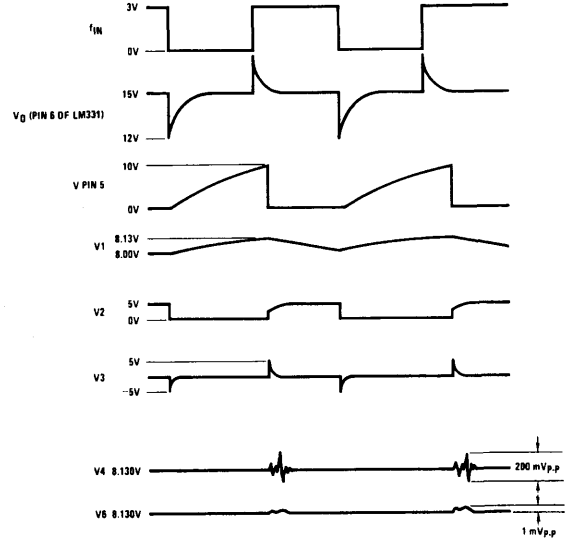

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FIGURE 3. Waveforms, Improved F-to-V Converter