Low-power data acquisition sub-system using the TI TLV1572

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With the entrance of the digital signal processor (DSP) into commercial electronic equipment in the late '80s, the number of analog applications turning into digital applications has increased significantly. Technical solutions, previously accomplished using analog circuitry, have been converted into data acquisition systems that translate analog input signals into digital information and process the binary data. In addition, the trend to portable equipment (i.e., PDAs, cellular phones, camcorders) requires electronic circuitry to be smaller and consume less power in order to extend battery life. This application note describes a low-power data acquisition system using the TI TLV1572 10-bit analog-to-digital converter (ADC) and the 16-bit, fixed-point TI TMS320C203 DSP. See Figure 1 for the system block diagram.

The power supply

The system power supply uses the TI TPS7101 adjustable low-voltage dropout regulator (LDO). The device regulates input voltages between 6 to 10 V down to the adjusted output level, providing a typical voltage drop of 32 mV per 100-mA load current. The output voltage is adjusted to 5 V via an external voltage divider consisting of 562-kΩ and 169-kΩ resistors. For an output voltage of 3 V, the 562-kΩ resistor is replaced by a 218-kΩ resistor. The following low-ESR (equivalent series resistance) 4.7-µF solid tantalum capacitor and the 100-nF high-frequency ceramic capacitor are sufficient to ensure stability, provided that the total ESR is maintained between 0.7 Ω and 2.5 Ω. For more information on the selection and type of low-ESR capacitors, refer to the TPS7101 Data Sheet, literature number SLVS092F.

The analog input buffer

The analog input signal is buffered by the TI TLV2772, a fast, low-voltage, low-noise CMOS operational amplifier (op amp). This device operates from 2.2 V to 5.5 V with a typical slew rate of 10.5 V/µs and a typical noise density of 17 nV/√Hz @ 1 kHz. In the configuration shown in Figure 1, the op amp works as a non-inverting amplifier with a gain of two. Before it is amplified, the analog input signal in the range of 0 V to $V_{CC}/2$ is band-limited by the 75-Ω/2.2-nF input low-pass filter. The 100-Ω/3.3-nF low-pass filter at the output reduces the output noise significantly and ensures a signal-to-noise ratio greater than 90 dB at the ADC input.

The analog-to-digital converter

The TLV1572 is a 10-bit, successive approximation ADC operating within a supply voltage range of 2.7 V to 5.5 V. The typical conversion time is ten SCLK cycles with the specified maximum of SCLK = 20 MHz at 4.5-V supply and 10 MHz at 3-V supply. The TLV1572 interfaces easily to DSPs and microcontrollers via a 4-wire serial interface.

Figure 1. Data acquisition sub-system

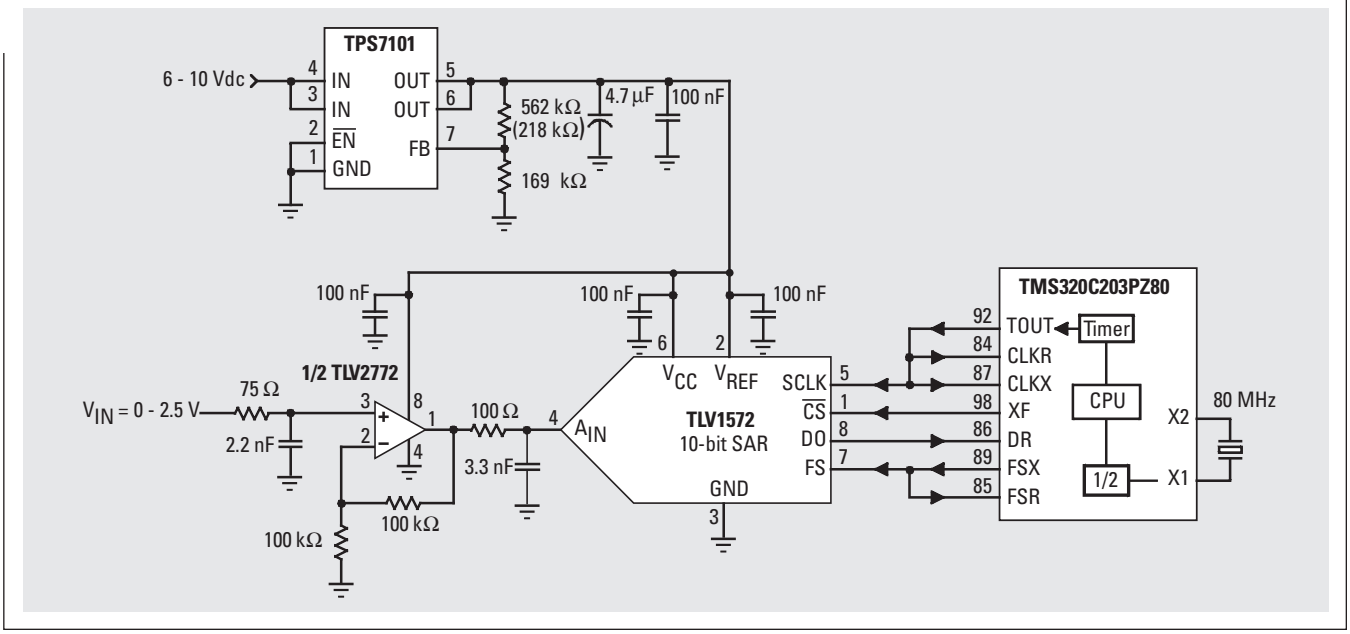
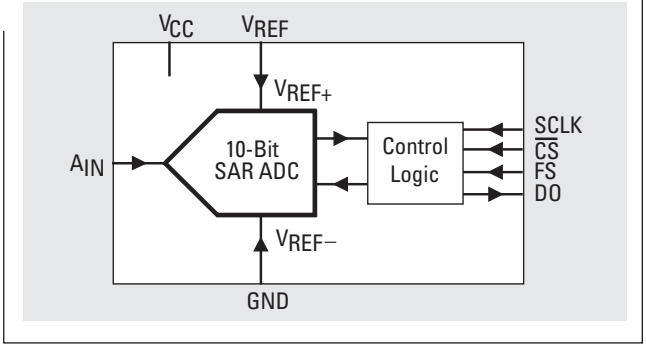


Figure 2. TLV1572 block diagram



The device features an auto-power-down mode that becomes active whenever a conversion is not performed, thus reducing the current consumption to 10 µA.

Figure 2 shows the block diagram of the device. The actual converter employs switched-capacitor architecture to perform successive approximations through charge redistribution. The internal control logic synchronizes the serial interface timing with the sampling and conversion process.

Serial interface timing

Figure 3 shows the interface timing between ADC and DSP. The ADC distinguishes between the µC and DSP modes by checking the frame sync (FS) input level at the falling edge of chip select. If FS is low, DSP mode is set, otherwise the µC mode is set.

With the rising edge of FS, the ADC starts transferring data to the DSP. Six zeros precede the 10-bit result to comply with the 16-bit data format of the DSP. Sampling occurs from the first falling edge of SCLK after FS goes low until the rising edge of SCLK when the sixth zero bit is sent out. Thereafter, decisions are made on the rising edges and data is sent out on the rising edges delayed by 1 bit. The DSP samples on the falling edge of SCLK.

DO goes into 3-state on the 17th rising edge and comes out on a FS rising edge. The device goes into auto-power-down on the 17th falling edge of SCLK. A rising edge of FS pulls it out of power-down and the next data transfer begins.

Interface program

The C-callable assembler routine, which ensures the timely sequence of the interface signals, is shown in Figure 4.

TLV1572START (start assembler routine)

The main program (in C language) starts the assembler routine via a call instruction. All pointers and registers previously used in the C-program are saved and the DSP and its serial port are initialized.

Any user-defined values such as memory start address, number of samples and the used supply voltage are copied from the C-program into the assembler program. The DSP on-chip timer, used as the interface-clock generator, assumes a default value of 10 MHz if a 3-V supply is used. If a 5-V supply is chosen, the timer value is overwritten for 20-MHz operation. Before the actual data transfer starts, the DSP internal receive interrupt flag, RINT, is enabled. The program status flag, END-BIT, which signalizes the exit of the assembler routine, is set to 1. Then the ADC is enabled via its chip-select input. The DSP initiates a data transfer by sending an FS pulse to the ADC, then resides in idle mode and waits for a RINT to occur.

RINT (receive interrupt routine)

On the 16th clock cycle of SCLK, a RINT is generated that forces the CPU to execute the RINT service routine (RINT-ISR). At the beginning of the RINT routine the receive data is stored in the data memory and the memory address is increased by one. The following decision-box decrements the number of samples and checks whether all samples have been received. If all samples were received, the ADC is disabled and the END_BIT is set to zero. Then the timer is stopped and RINT is disabled. The program leaves the RINT-ISR via the EXIT-routine and returns to the C-program. If more samples need to be acquired, the program clears the RINT flag and returns to the Idle-mode where it sends the FS-pulse and stays idle until the next RINT occurs.

Exit 1572 program

As long as END-BIT is set to one, the CPU diverts to the Start-Data-Transfer box to continue acquiring data. Once END_BIT has been set to zero, all previously saved registers in the Save-Context box are restored. The CPU now exits the interface routine and returns to the C-program.

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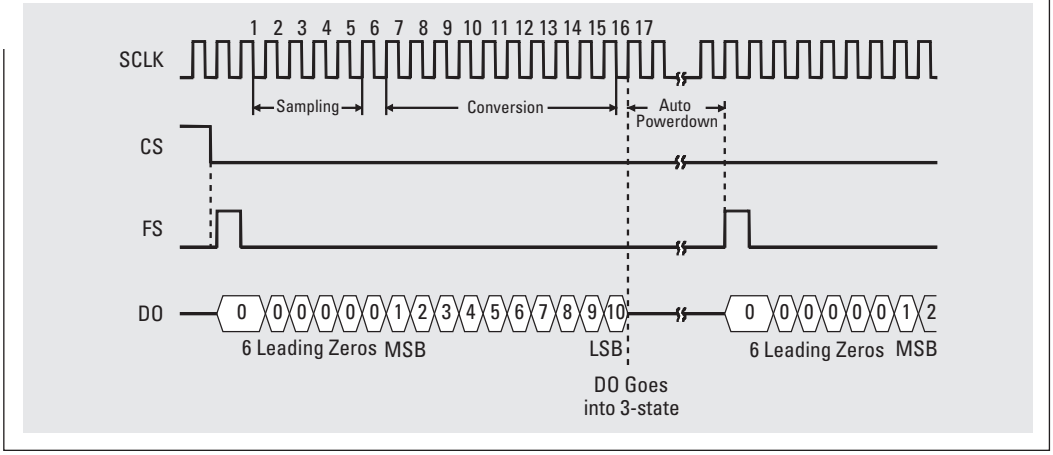
Figure 3. ADC/DSP interface timing



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References

For additional information and references, see the following related documents:

1. TMS320C2xx User's Guide, literature number SPRU127B.
2. TMS320C2xx Data Sheet, literature number SPRS025B.
3. TLV1572 Data Sheet, literature number SLAS171A.
4. TLV1572 EVM Manual, literature number SLAU018.
5. Interfacing the TLV1572 ADC to the TMS320C203 DSP Application Report, literature number SLAA026B.
6. TPS7101 Data Sheet, literature number SLVS092F.
7. Switched-Capacitor Analog Input Calculations Application Report, literature number SLAA036.

Figure 4. Flowchart of the interface program