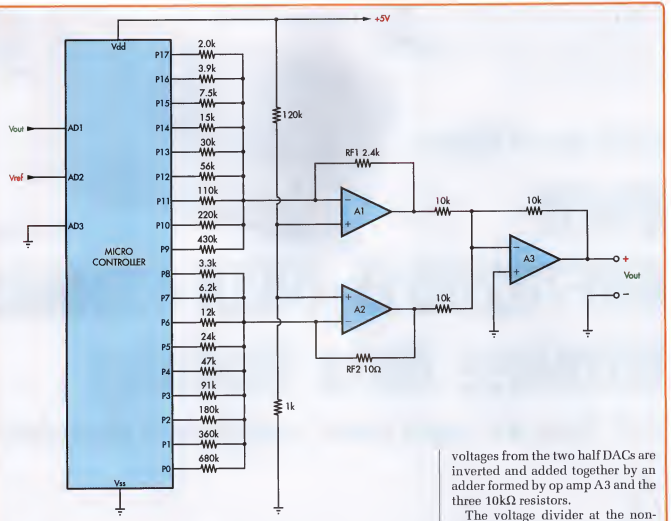

Wide current-mode 18-bit DAC

Current-mode DACs have the useful property that each bit-weighting resistor independently determines the voltage contributed by that bit to the total output voltage. This makes possible DAC schemes that measure the individual voltage contribution of each bit and calculate the appropriate digital value to present to the DAC to obtain a desired output voltage.

A downside of current-mode DACs is that their current requirements double with each added bit of width. A wide current-mode DAC will therefore suffer by either having such a low current in the lowest-order bit-weighting resistor that it will be swamped by noise, or the highest-order bit-weighting resistor will have such a high current in it that it will heat up, affecting its value (not to mention that the total current drain of the DAC may also be prohibitive).

The circuit shows a solution to this problem using an 18-bit DAC with non-precision weighting resistors as an example. The solution is to split the 18-bit DAC into two 9-bit DACs, each with its own I-V (current-to-voltage) converter. A 9-bit DAC is not so wide that it suffers from the above problems: if the current contributed by the bit 0 weighting resistor is around 10µA the current in the bit 8 weighting resistor will be around 2.5mA.

The I-V converter for the upper nine bits is formed around op amp A1 and has a 2.4kΩ feedback resistor, while the I-V converter for the lower nine bits is formed around op amp A2 and has a 10-ohm feedback resistor. The result is that while the currents in the two half DACs are roughly similar, the output step voltage of the upper half DAC is about 240 times that of the lower one. The voltages from the two half DACs are inverted and added together by an adder formed by op amp A3 and the three 10kΩ resistors.

The voltage divider at the non-inverting inputs of A1 and A2 holds those inputs at 41mV. This is intended to be slightly more than the sum of the maximum input offset voltages of A1, A2 and A3. This guarantees that Vout will be slightly negative when the digital input is 0 and enables the output range to include 0V to within half the output step voltage of the DAC.

The resulting DAC has an output range of 0-12.16V with a maximum output step voltage of 76.3µV. As far as the microcontroller is concerned the two DAC halves behave as a single DAC with the appropriate bit weights.

The microcontroller can calibrate the DAC by turning on each output in turn and measuring the output step with reference to Vref. For best accuracy, use a micro with a high-resolution internal analog-to-digital converter (ADC) or with an internal programmable-gain amplifier (PGA).

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