Bryan Lizon86 *Jul 21, 2015*

Other Parts Discussed in Post: ADS1262

Consider the following scenario.

You've just opened the box with your brand-new evaluation module (EVM) inside, and you're eager to start taking data. You think, "I'll start off nice and slow with a single-ended measurement at a gain of 1V/V using the internal 2.5V reference." Simple and quick, right? What could go wrong?

You hook up your supplies, program your registers, apply your input signal – and get an error (Figure 1).

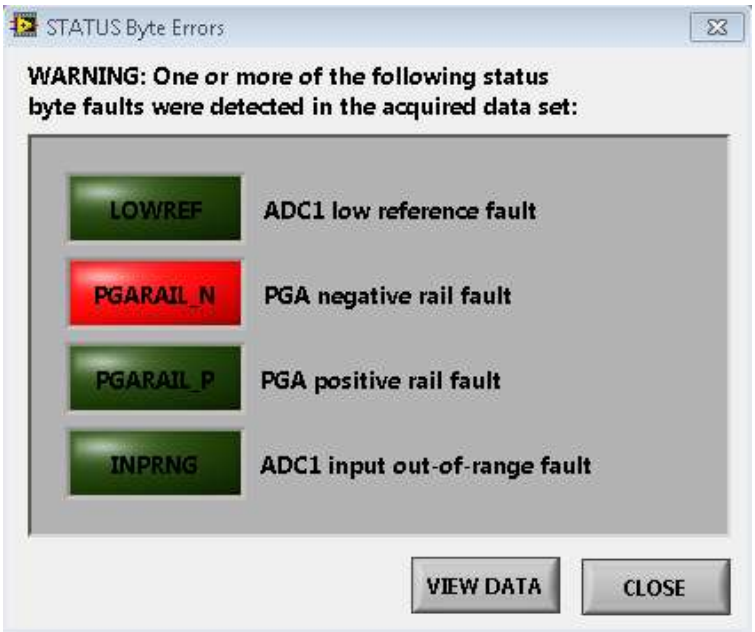

Figure 1: An error is detected by the ADS1262 software

What happened? The source of this error is due to a violation of the integrated programmable gain amplifier's (PGA) input range requirements. To illustrate what causes this issue and how to fix it, I'll use the 32-bit ADS1262 analog-to-digital converter (ADC) as an example, although this information also applies to many other delta-sigma ADCs with integrated programmable gain amplifiers (PGAs), like the 24-bit ADS1220 and ADS1248.

First things first

Before diving right into the fault, let's look at the ADC inputs to make sure you haven't violated any additional operating conditions. Consider the hierarchal diagram shown in Figure 2.

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	V_{AVDD} to V_{AVSS}	4.75	5	5.25	V
		V_{AVSS} to V_{DGND}	–2.6		0	V
	Digital power supply	V_{DVDD} to V_{DGND}	2.7		5.25	V
ANALOG INPUTS ADC1						
FSR	Full-scale differential input voltage range(1)		$-V_{REF}$ / Gain		$+V_{REF}$ / Gain	V
V_{INP},V_{INN}	Absolute input voltage (2)	PGA mode	See Equation 11			V
		PGA bypass	V_{AVSS} - 0.1		V_{AVDD} + 0.1	V
VOLTAGE REFERENCE INPUTS						
V_{REF}	Differential reference voltage	$V_{REF} = V_{REFP} - V_{REFN}$	0.9		$V_{AVDD} - V_{AVSS}$ + 0.2	V
V_{REFN}	Negative reference voltage		V_{AVSS} – 0.1		V_{REFP} - 0.9	V
V_{REFP}	Positive reference voltage		V_{REFN} + 0.9		V_{AVDD} + 0.1	V

Figure 2: ADC input diagram and corresponding data sheet limits

The flow chart in Figure 2 illustrates how each input or setting affects the others:

- The power-supply voltages determine the acceptable ranges for the reference voltages and the PGA output-voltage limits.
- Both of these limits, in conjunction with the PGA gain, set the differential and absolute input-voltage limits.
- The input signal must agree with both the differential and absolute requirements (discussed in more detail later).

The key takeaway: **you need to consider all of these requirements and how they relate to one another.** This is especially important because one value may actually tighten the restriction on another, as is the case with the reference voltage and PGA gain limiting the differential input voltage (Figure 2). While this may seem obvious, many designers overlook these simple details, resulting in unnecessary headaches.

Identifying the issue

Now that I've covered the data sheet's input-signal requirements, let's identify the fault in my original example. If you're using the ADS1262EVM's software, it's easy to determine which error occurred (Figure 1). However, if you're integrating the ADS1262 into your own system, it can be beneficial to enable the STATUS byte (the ADS1262EVM software always reads this byte to display the correct error message).

Let's get familiar with the alarm flags provided in the STATUS byte – for the ADS1262, you'll want to check bits 1 through 4 (Figure 3). These bits report reference and PGA differential voltage faults, as well as PGA negative and positive rail faults, which may be some of the only ways to detect these conditions when not otherwise obvious from the ADC's output code.

7	6	5	4	3	2	1	0
ADC2	ADC1	EXTCLK	REF_ALM	PGAL_ALM	PGAH_ALM	PGAD_ALM	RESET
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Figure 3: The ADS1262's STATUS byte register map

In my example, the PGAL_ALM bit is high; therefore, I drove the PGA output too close to the negative rail. Let's use Equation 1 for the PGA input range requirements to analytically confirm if this is what happened:

$$V_{AVSS} + 0.3 + |V_{IN}| * \frac{Gain-1}{2} < V_{INP} \text{ and } V_{INN} < V_{AVDD} - 0.3 - |V_{IN}| * \frac{Gain-1}{2} \quad (1)$$

Using Equation 1 with AVDD at 5V, AVSS at 0V, and a gain of 1V/V, the absolute input voltages on AINN and AINP can range from 0.3V to 4.7V. As with many single-ended measurements that use the PGA, if you try to connect AINN to AVSS, you'll violate these input-voltage requirements and get an invalid conversion result. Using the ADS1262EVM, this will result in a "PGA negative rail fault" warning.

Why does this happen?

As a result of its topology – non rail-to-rail output (RRO) – the PGA begins to enter its nonlinear region of operation within 300mV of the supply rails (the gray region in Figure 4). To avoid this region entirely and ensure predictable device operation, designers include that 300mV cushion in the PGA's input range requirement equation. To learn more about this phenomenon, watch this training video (myTI login required).

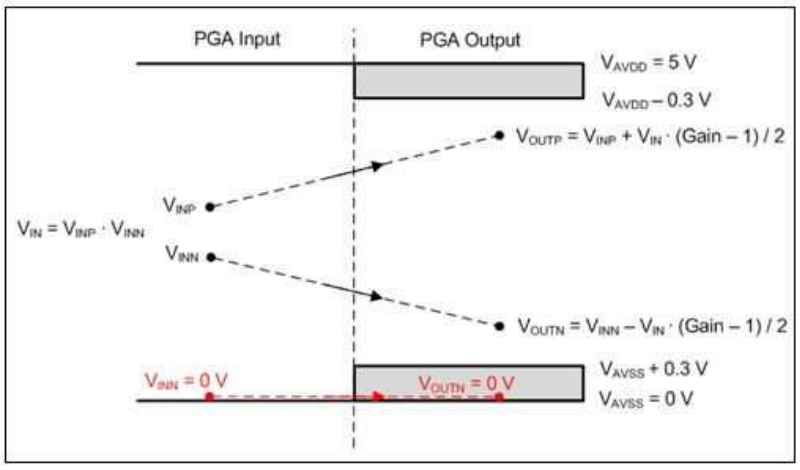

Figure 4: PGA input-to-output voltage translation diagram

How do you correct this issue?

- There are a few actions you can take to make sure that you don't violate the PGA's input range requirements:

1. Level shifting

Shifting the entire input signal by at least 300mV ensures compliance with the PGA voltage requirements, assuming a gain of 1V/V and a valid differential input voltage. To make things easier, the ADS1262 has an internal level-shifter on the AINCOM pin that outputs the mid-supply voltage; for example, 2.5V given AVDD = 5V and AVSS = 0V (Figure 5).

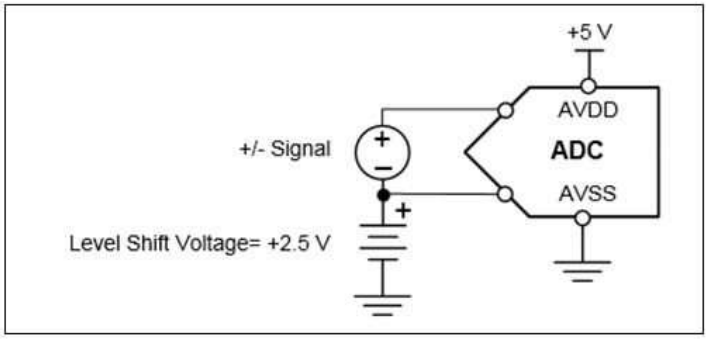

Figure 5: Using a level-shifted voltage to avoid saturating the PGA

2. Bipolar supplies

If you absolutely need to keep your negative rail at GND, you can apply bipolar supplies (e.g. ±2.5V) to AVDD and AVSS. This changes your allowable input range to ±2.2V, assuming a gain of 1V/V, and allows AINN to be 0V.

3. Bypass the PGA

If you don't require gain, you can always bypass the PGA by setting the BYPASS bit in the MODE2 register to 1. This increases your allowable input range to a maximum of AVDD+0.1V and a minimum of AVDD-0.1V. However, in this scenario, you should confirm that you have very stable power supplies, as approximately 100mV of drift on AVSS can cause this input to move outside of its recommended operating range. Also, the signal source requires a low output impedance, as the PGA no longer buffers the input signal.

Tools to help

- While this is a fairly straightforward idea, it's not always easy to understand how combinations of different input voltages will impact the PGA's output. To simplify things, TI developed an Excel tool for the ADS1262 that performs this calculation for you, given the gain, input, supply and reference voltages (Figure 6). The tool also calculates cyclic redundancy check (CRC)/checksum values, provides sinc filter-response information and includes a register map.

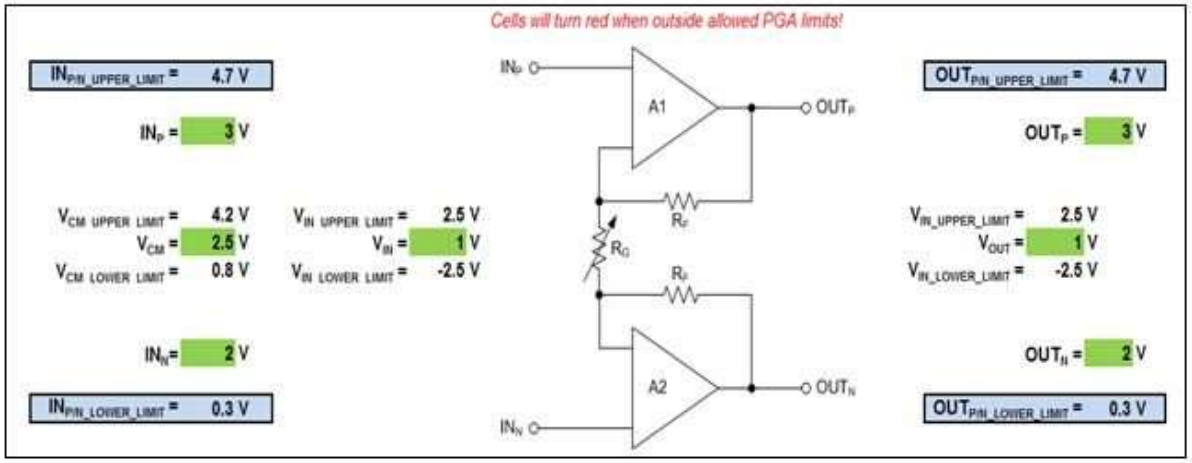

Figure 6: PGA allowable input range calculator from the ADS1262 tool

Now you know what to do if you get an error message using the ADS1262EVM, or a flag in the STATUS byte when using any ADC with this error-detection capability: stay clear of the rails and enjoy your new device.

Additional resources

- Learn more about the ADS1262.
- Download the ADS1262 Excel calculator tool.
- Learn more about the ADS1263.
- Download our white paper to learn how to improve system reliability with the ADS1262.
- Find how-to design resources organized by topic in our new Data Converter Learning Center.