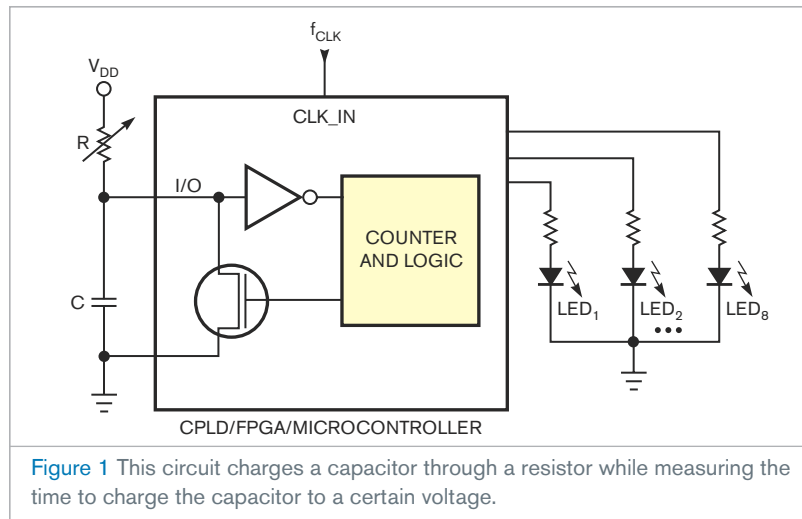


ADC for programmable logic uses one capacitor

Jef Thoné and Robert Puers,
Katholieke Universiteit Leuven, Leuven, Belgium



Many electronic devices require user input for setting the application properties. Typical input devices include pushbuttons, potentiometers, and touchscreens. To minimize overall project cost, you may have to select low-range microcontrollers, FPGAs (field-programmable gate arrays), or PLDs (programmable-logic devices). These devices don't provide a wide range of peripherals and often lack analog-to-digital-conversion capability, which can prove annoying when trying to acquire user input. This Design Idea describes a method for adding a low-end ADC to a single programmable-logic I/O pin. The circuit charges a capacitor through a resistor while measuring the time to charge the capacitor to a certain voltage.

Before each measurement, the capacitor discharges to 0V. A single I/O pin can perform both the dis-

charging and the timing. For an FPGA or a PLD, you can perform a discharge by setting the I/O as an output pin and forcing a zero at that pin. You can charge the capacitor by setting the I/O as an input pin, which gives it a high impedance. The capacitor charges through the potentiometer (**Figure 1**). Meanwhile, a counter starts, and the CPLD monitors the input voltage. As soon as the capacitor voltage reaches the threshold, the counter stops at a value that is a measure of the charging time. The charging time or counter value relates to the clock frequency, the value of the resistor, the value of the capacitor, and the input threshold voltage:

$$V_{TH} = V_{DD} \times \left(1 - e^{-\frac{t}{R \times C}} \right)$$

$$T = \frac{\text{COUNTERVALUE}}{f_{CLK}}$$

$$\text{COUNTERVALUE} = -f_{CLK} \times R \times C \times \ln \left(1 - \frac{V_{TH}}{V_{DD}} \right)$$

If you assume that the capacitor value, the input threshold voltage, and the clock frequency remain fairly constant over the operating range, the charging time is linearly dependent on the value of the resistor. If you replace the resistor with a potentiometer, a counter value depends on the potentiometer position. The application uses a Xilinx (www.xilinx.com) XC9500 XL CPLD (**Figure 2**). The I/O, which VHDL (very-high-speed-IC hardware-description language) declares as a tristate buffer, first shorts the capacitor. Hardware limits the output short-circuit current of the I/O pins to ± 10 mA, so the capacitor's shorting should last long enough to guarantee a full discharge. You can calculate the minimum shorting time using the capacitor value, short-circuit current, and discharge voltage, assuming that the threshold voltage must discharge from the capacitor:

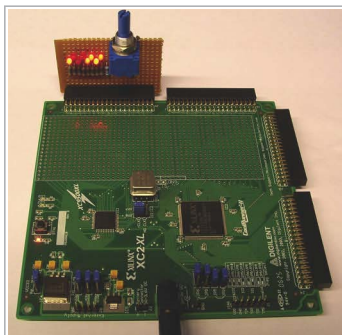


Figure 2 The application uses a Xilinx XC9500 XL CPLD.

$$t_{DISCMIN} = V_{THRESHOLD} \times \frac{C}{I_{SHORT}}$$

The discharge delay can be realized with a small counter. After the discharge time, the I/O pin acts as an input, which causes the capacitor to charge through a pullup potentiometer. Meanwhile, the internal counter starts. When the capacitor voltage reaches the input threshold voltage, the counter stops. Eight LEDs show the 8-bit value. In this application, a 10-k Ω potentiometer in series with a 1-k Ω resistor charges a 22-nF capacitor. The input clock of the PLD is 1.8432 MHz. The input threshold is 1.5V at a supply of 3.3V. This arrangement allows a measurement range between a counter value of 25 and 270, equivalent to a resolution of almost 8 bits. **Figure 3** shows the capacitor charging/discharging waveform.

Every IC's I/O pin has a certain bias sink or source current, causing a voltage drop over the charging resistor. This situation limits the charge voltage to $V_{DD} - R_{CHARGE} \times I_{BIAS}$. In other words, if the charging resistance is too large, the capacitor doesn't charge above the input-pin threshold voltage, stopping the circuit's operation. Similar applications for microcontrollers or PLDs (**references 1 through 5**) include adding multiple inputs to a single I/O pin and using a different pullup-resistor value for each input. By discriminating the charging times for each resistor, the PLD can decide which resistor or combination of resistors the user has actuated.

Another application for microcon-

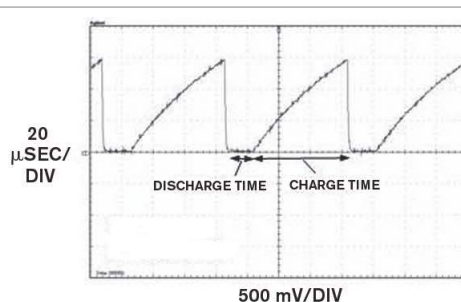


Figure 3 In this application, a 10-k Ω potentiometer in series with a 1-k Ω resistor charges a 22-nF capacitor.

trollers is temperature measurement. By replacing the pullup resistor with a PTC (positive-temperature-coefficient) or an NTC (negative-temperature-coefficient) resistor, you can derive the temperature from the charging time after calibration. You can also use these devices to make true analog-to-digital measurements. By replacing the pullup resistor with a voltage-controlled current source, an input-voltage change causes a linear change in the charging time, providing a real analog-to-digital conversion.**EDN**

REFERENCES

- 1 Eggers, Torsten, and Thomas Schmidt, "AN10187 Low-cost A/D Conversion with Philips LPC Microcontrollers," Philips Semiconductors, Oct 4, 2002, www.nxp.com/acrobat_download/applicationnotes/AN10187_1.pdf.
- 2 "Using an I/O Port Pin as an A/D Converter Input," Holtek, www.holtek.com.tw/english/tech/appnote/uc/pdf/ha0128e.pdf.
- 3 "AVR400: Low Cost A/D Converter," Atmel, www.atmel.com/dyn/resources/prod_documents/doc0942.pdf.
- 4 Quiring, Keith, "Implementing An Ultralow-Power Thermostat With Slope A/D Conversion," Texas Instruments, Jan 2006, <http://focus.ti.com/lit/an/slaa129b/slaa129b.pdf>.
- 5 "CoolRunner-II Low Cost, Low Power Thermometer for Embedded Designs," Xilinx, Nov 29, 2004, www.xilinx.com/support/documentation/application_notes/xapp438.pdf.