A/D CONVERSION SERIES – Part IV

HIGH SPEED DIGITAL-TO-ANALOG AND ANALOG-TO-DIGITAL TECHNIQUES

A brief overview of some of the more popular techniques for accomplishing D/A and A/D techniques. In particular those techniques which lead themselves to high speed conversion.

HIGH SPEED DIGITAL-TO-ANALOG AND ANALOG-TO-DIGITAL TECHNIQUES

INTRODUCTION

The world in which we live is truly an analog world. Data taken from anything that is tested or measured will usually appear in analog form and is difficult to handle, process, or store for later use without introducing considerable error. If data is taken frequently from a large number of sources, it will accumulate at such a rate that it becomes a burden and a major problem to the laboratory running the test. A digital computer has the capability of processing such data at rates comparable to those at which it was produced; however, the data must first be converted into a form usable by the digital computer. Then after the digital processing is complete, the digits must be reconverted to analog form to interface with the real world.

Although a pure analog system is capable of better accuracy than an analog-digital system, its accuracy is rarely completely usable because it is presented in a form that cannot be easily read, recorded, or interpreted with high accuracy. Digital data, however, is readily presented in numerical form regardless of the number of bits, and is just as easily manipulated, processed, and stored. Once data is converted into digital form it may be processed mathematically, sorted, analyzed, and used for control much more accurately and rapidly than with the analog data. If data must be "handled" much after it is acquired, it is safer to digitize it because there is little chance of error accumulation in successive manipulation. Further, digital data can be stored in many non-volatile types of memory devices.

The applications of A/D and D/A converters are almost unlimited. As the state-of-the-art of semiconductor technology advances, the cost of these conversion systems will continue to drop, and more system designers will be able to use A/Ds and D/As, which were before economically or physically impractical. A few current uses include: space telemetry systems, all digital voltmeters, voice security systems, closed loop process control systems (i.e., chemical plants, steel mills, etc.), in-flight checkout systems (to code the output of sensors so that a small computer on board can process the information), and hybrid computers use both A/D and D/A converters as a means of interfacing analog and digital computers to solve large system simulation problems. The listed applications indicate the versatility and represents only a small portion of the actual uses.

It should be obvious that the A/D converter that controls the ambient temperature of a large supermarket cannot encode the video information from an optical scanner; obviously, the system requirements are as different as night and day. There are many ways of performing A/D and D/A conversion, from very slow, inexpensive techniques to ultra-fast expensive ones. For the rest of this note, only the latter category will be discussed.

Appendix A is a glossary of terms pertaining to the subject of A/D and D/A conversion, and may benefit the reader in understanding the author's interpretation of some key terms.

Appendix B discusses several of the more common digital codes used with A/D and D/A conversion.

HIGH SPEED D/A CONVERTERS

Digital-to-Analog conversion can be accomplished by quite a number of methods. It is not the purpose of this discussion to give an exhaustive description of each type, but merely to mention a few of the more popular techniques and point out where they fit into the more specialized category of high speed D/A converters.

Voltage Output D/As

The output of a D/A converter can be an analog voltage or current. The voltage output types will be discussed first, since they are used most commonly and are easiest to understand.

Figure 1 shows the block diagram of a 3-bit voltage output D/A using weighted resistors and a summing amplifier. The summing resistors of an operational amplifier are weighted in binary fashion and are connected via an electronic switch to the reference or to ground, depending upon the state of each individual digital input. A digital "1" connects the resistor to the reference, and thus adds in its respective binary weighted increment. Although double-throw switches are shown, conceptually it is unnecessary to switch the resistor to ground when not connected to the reference. However, when single pole switches are utilized, the gain of the amplifier varies with the digital input and this affects bandwidth, dc offset, and drift. This variation is eliminated by the more expensive double throw switch.

A significant disadvantage of the simple weighted resistor approach of Figure 1 is that the accuracy and

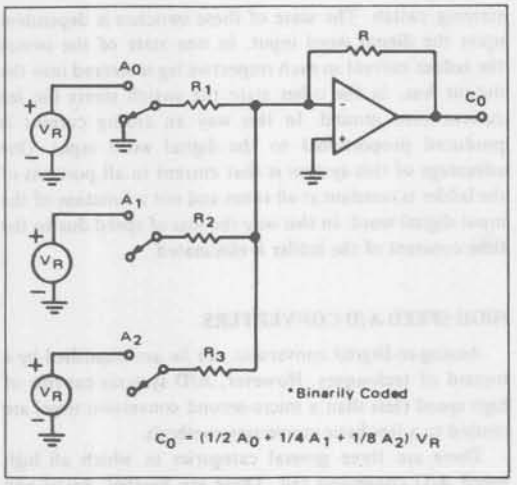


FIGURE 1 – Voltage Output Weighted Resistor Summing D/A

stability of this type of DAC is dependent upon the absolute accuracy of the resistors and their ability to track each other versus temperature. Since the input resistors all have different values, it is difficult to obtain identical tracking characteristics. Furthermore, since each input resistor's value is twice the preceding one, the absolute values become quite large. For higher resolution DACs it is also difficult, or at least expensive to get good stable resistors at such values. The high impedances, as well as the speed limitations of voltage switches and operation amplifiers, result in the voltage output DAC being relatively slow.

To overcome the problems relating primarily to the resistors, an alternate technique utilizing an R-2R resistive "ladder" network, shown in Figure 2, is generally used. Note, that if one leg of the ladder is connected to the reference by the electronic switch and the remaining are all grounded, a current is produced in the leg which "travels" through the ladder and gets divided by a factor of two at each junction. Thus, the contribution of current from that leg (e.g., bit) at the summing junction is binarily weighted in accordance with the number of junctions through which it has passed. The LSB (least significant bit) is therefore on the left in Figure 2.

One of the most significant advantages of the R-2R ladder approach is that the impedance as seen from the input to the op-amp is constant (equal to R). Hence, bandwidth, etc., do not change with digital setting. Of more significance, however, is the fact that all the resistors are either R or 2R. Note that the accuracy is *not* dependent upon the absolute value of all the Rs, but rather only their differences. Similarly, temperature effects are only significant with respect to how well all the Rs and 2Rs *track* each other, respectively. Since the value of R can be any convenient value (0.1 k to 50 k), ladder networks are a natural for monolithic diffusion or deposition, which further improve their tracking capability. Also, the impedance levels can be kept sufficiently low to minimize bandwidth limitations due to stray capacitance.

Another type of R-2R ladder, voltage output D/A, is shown in Figure 3. This circuit is very similar to the one just described, except equal value current sources are switched into the nodes of the ladder rather than switching the "legs" of the ladder between voltages. Simply network theory will show that the effect of each current, at e_0, is the same as in the previous circuit, hence they are binarily weighted.

For several reasons, currents may be switched much more rapidly than voltages. This gives the current source D/A an increase in speed by at least one order of magnitude. Because of this switched current-source R-2R ladder D/A is one of the types most often used in high speed voltage-output D/As. This technique, because of the R-2R ladder and current switching, lends itself to monolithic fabrication.

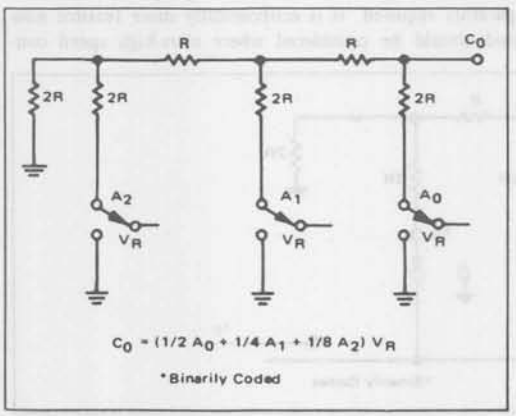


FIGURE 2 – Switched Voltage Source R-2R Ladder D/A

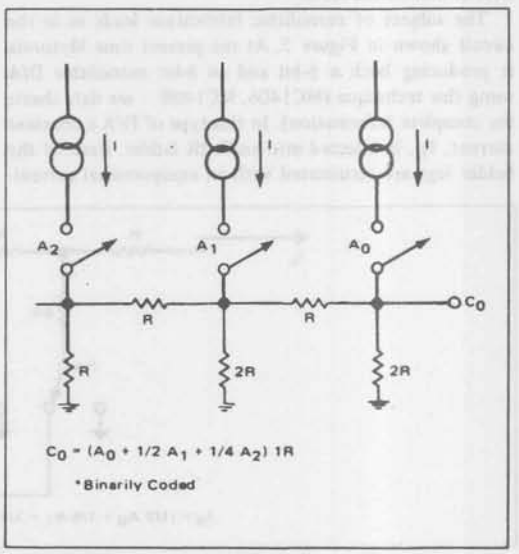


FIGURE 3 – Switched Current Source R-2R Ladder

3

Current Output D/As

This type of D/A can be implemented by generating binarily-weighted currents, preferably from active sources, and summing these on a common bus. Figure 4 shows a block diagram of a D/A using this principle.

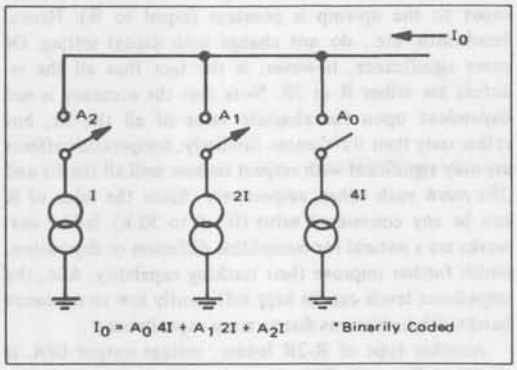


FIGURE 4 – Current Output D/A Using Weighted Current Sources

In an actual circuit the switches controlled by the digital word input, would simply be current steering circuits, not on-off switches as shown. Current from a current source would either be steered into the output bus or into another node of the circuit. This type of switching is the fastest method of current switching available; switching speeds of less than a nanosecond are possible with emitter coupled logic (MECL).

The weighted current source D/A technique is also a method that can easily be implemented in monolithic form. It is the opinion of this author that this system offers the best possibility of producing a truly high-speed D/A in monolithic form.

The subject of monolithic fabrication leads us to the circuit shown in Figure 5. At the present time Motorola is producing both a 6-bit and an 8-bit monolithic D/A using this technique (MC1406, MC1408 – see data sheets for complete information). In this type of D/A a constant current, I_L, is injected into an R-2R ladder. Each of the ladder legs are terminated with an equipotential current-steering switch. The state of these switches is dependent upon the digital word input. In one state of the switch the ladder current in each respective leg is steered into the output bus, in the other state the switch steers the leg current into ground. In this way an analog current is produced proportional to the digital word input. One advantage of this system is that current in all portions of the ladder is constant at all times and not a function of the input digital word. In this way the loss of speed due to the time constant of the ladder is eliminated.

HIGH SPEED A/D CONVERTERS

Analog-to-Digital conversion can be accomplished by a myraid of techniques. However, A/D systems capable of high speed (less than a micro-second conversion time) are limited to a few basic conversion methods.

There are three general categories in which all high speed A/D converters fall. These are Parallel, Serial and Combination. In a parallel conversion technique, all of the bits are converted simultaneously by many circuits in parallel. In a serial type of A/D each bit is converted sequentially one at a time. The third category, combination, is simply a combination of the previous two.

In general the parallel systems are faster and more complex than the serial types. The combination types are simply a compromise between speed and complexity.

The Parallel A/D (Flash)

In the parallel method, all bits of the digital representation are determined simultaneously. It is called the parallel method because of the configuration; a bank of voltage comparators, each responding to a different level of input voltage. This method is also called "Flash" encoding. Figure 6 shows the block diagram.

Characteristic of this configuration, it can be shown that for n-bits of binary information the system requires 2^n-1 comparators, and each comparator determines one LSB level. Unitl recent advances in the state-of-the-art of integrated circuits, this method was prohibitive if "n" were very large because of the large quantity of comparators required. It is economically more feasible now and should be considered where ultra-high speed con-

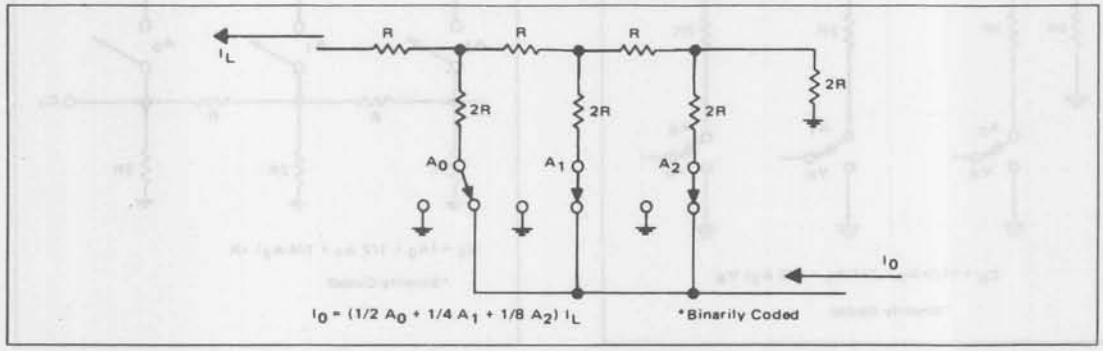


FIGURE 5 – Current Output R-2R Ladder D/A

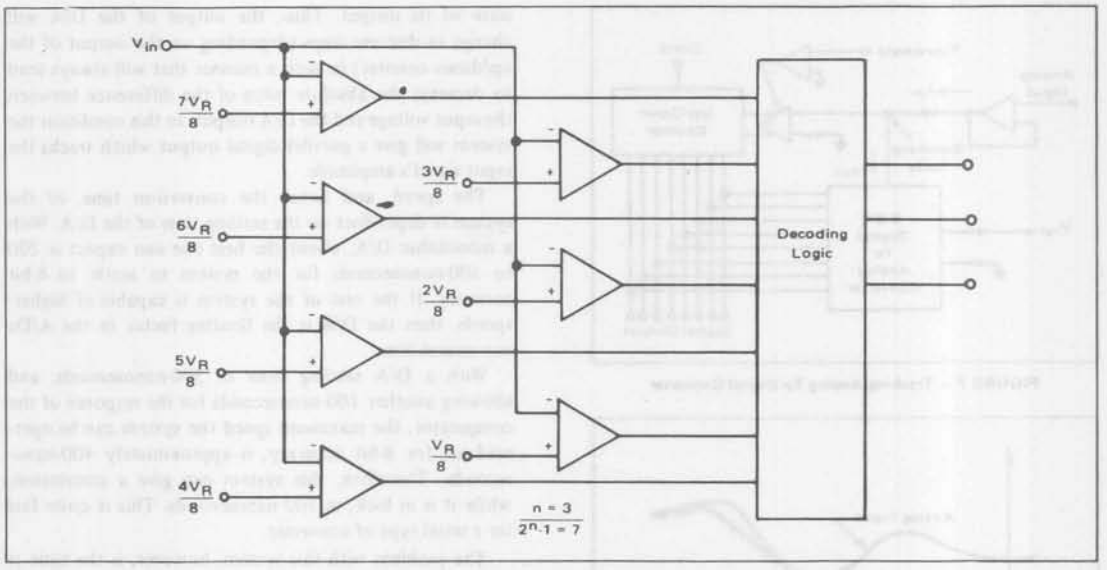


FIGURE 6 – Parallel A/D Block Diagram (Flash)

version is required. As MSI and LSI circuits become more and more common, it is very likely that a semiconductor manufacturer could produce a one chip A/D of 4-6 bits on one monolithic IC. It is the opinion of this author that this is an interim solution at best because the performance of such a device could not match those of the discrete circuits. And there are other techniques, some of which will be discussed later, that suggest more attractive performance specifications per nano-acre than that of the Flash system at lower cost.

One disadvantage of this system is that the output of the comparator bank is not directly usable information. These 2^n-1 outputs must be converted to binary information in some sort of binary code. (For more information on coding, see Appendix B.) For large values of n, the massiveness of the conversion logic not only increases cost and complexity, but requires more successive stages, thus increasing the conversion time.

The parallel converter is essentially asynchronous by the nature of its construction, and can be used effectively in both multiplexing or continuous tracking mode. It should be noted that often times a set of latches and a clock are added to this system to store and up-date the output in a clocked manner. This is done because the output of the Flash system can give erroneous glitches during a change from one value to another.

Specific requirements of the complete system determine the type of comparator needed. With this system since 2^n-1 comparators are used, the total input bias current of the system is one of the comparator's input bias currents multiplied by 2^n-1. This figure can be quite high if "n" is on the order of 6 to 8 bits.

Most comparators and digital logic circuits have a relatively fixed propagation delay. If parts are selected with this feature, the system can be preloaded. This means that a new signal can be injected to the system before the system has had time to completely convert the previous signal. While one signal is propagating through the digital logic a new signal is applied to the comparators. The digital logic operates on this signal while the comparators convert a new signal. This procedure will, in effect, decrease the total conversion time. However, it must be attempted with great care, since timing problems can arise in this sort of configuration.

Tracking Type of A/D

The Tracking A/D derives its name from the fact that the digital output continuously "tracks" the analog input voltage. This type of A/D is usually used in communications systems or some other application where the input is a continuously varying signal.

The Tracking type of A/D is one of several systems that use a Digital-to-Analog converter (D/A) in a feedback path to make an A/D. With this type of converter the accuracy can be no better than the D/A being used, (usually 6-10 bits).

Figure 7 shows the block diagram of the Tracking type A/D. There are two operating modes of the Tracking A/D. The first of these is when the A/D is "locked" on the signal and is "tracking" with it. The system will stay "locked" onto the signal as long as the signal does not increase or decrease in amplitude faster than the A/D system can "track" with it. The other mode of operation occurs when the system is just turned on or the signal has changed amplitude faster than the A/D could follow. When this occurs the system is "out of lock" and the A/D generates a staircase, in the direction of the input siganl change, until it again reaches the input voltage and acquires "lock" again. Figure 8 shows the waveform generated by

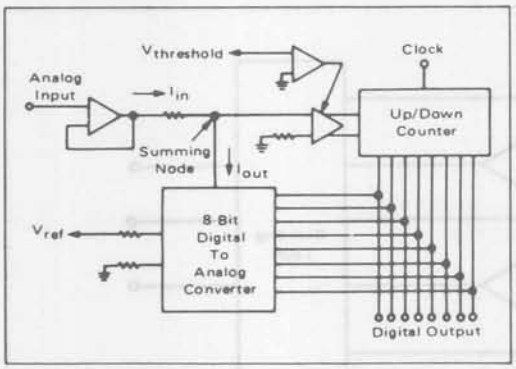


FIGURE 7 – Tracking Analog To Digital Converter

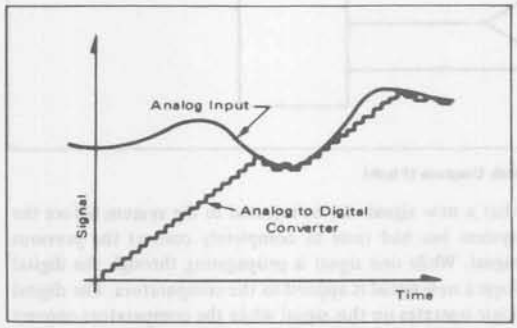


FIGURE 8 – Tracking Analog To Digital Converter Waveforms

the output of the D/A and the input signal plotted on the same set of axes. This figure shows both the "locked" and "out of lock" conditions.

Conversion time, for this type of A/D is a very nebulous thing. As long as the A/D is "locked" onto the signal, the conversion time is now the time required for the system to acquire lock again. This time will vary, depending on the absolute value difference between the output voltage of the D/A and the input signal. One can see from this that this system would be good if the requirement is to continuously monitor a slowly changing signal. If, however, the input signal varies in steps, as the case of several different signals being multiplexed, this particular system would not be a proper choice.

In operation the D/A generates a voltage output with a possible 2^n discrete step, the value of this voltage being directly proportional to the digital "word" that is on the digital inputs of the D/A. A comparator in the system compares the output of the D/A to the input voltage and gives an output signifying whether the input is above or below the D/A voltage.

Also included in the system is an n-bit up/down counter and a free-running oscillator or clock. The "n" outputs of the up/down counter are connected to the input of the D/A, thus determining its output voltage. The "n" outputs of the counters are also the digital output of the A/D.

The output of the comparator causes the up/down counter to count either up or down, depending on the state of its output. Thus, the output of the D/A will change in discrete steps (depending on the output of the up/down counter) in such a manner that will always tend to decrease the absolute value of the difference between the input voltage and the D/A output. In this condition the system will give a parallel digital output which tracks the input signal's amplitude.

The speed, and hence the conversion time, of the system is dependnet on the settling time of the D/A. With a monolithic D/A, about the best one can expect is 200 to 300-nonoseconds for the system to settle to 8-bit accuracy. If the rest of the system is capable of higher-speeds, then the D/A is the limiting factor in the A/Ds conversion time.

With a D/A settling time of 300-nanoseconds, and allowing another 100-nanoseconds for the response of the comparator, the maximum speed the system can be operated at, for 8-bit accuracy, is approximately 400-nanoseconds. Therefore, this system can give a conversion, while it is in lock, in 500 nanoseconds. This is quite fast for a serial type of converter.

The problem with this system, however, is the time it takes the A/D to reacquire lock once the signal is lost. In the absolute worst case, it could take 2^n clock pulses! This is very poor indeed. In order to prevent this condition in operation, the slew rate of the input signal must be limited.

In most applications, the operational characteristics of the Tracking A/D are undesirable. However, there are applications where its "unique" features are not detrimental and in these cases the Tracking type of A/D can be a very powerful, economical system.

Motorola will soon offer a new IC which is useful in implementing the Tracking A/D converter technique. The type MC1507L contains a high-speed op amp and a dual threshold comparator with separate UP and DOWN outputs. Both thresholds may be adjusted simultaneously by varying a reference voltage input.

Combining the MC1507 with either a MC1506L or MC1508L-8 D/A Converter and a pair of UP/DOWN counters produces a relatively inexpensive tracking converter. The MC1507 data sheet also shows a method of speeding up the clock to hasten the conversion time under the conditions when the system gets out of lock. This option requires use of a second MC1507 function block.

Successive Approximation A/D

The Successive Approximation (S/A) type of A/D is a serial system which uses a D/A in a feedback loop. It is relatively slow compared to other types of high-speed A/Ds, but its low cost, ease of construction, and system operational features more than make up for its lack of speed in many applications. It is by far the most widely used A/D system in use today.

Figure 9 shows the block diagram of the system. In operation, the system enables the bits of the D/A one at a time, starting with the most significant bit (MSB). As each bit is enabled, the comparator gives an output

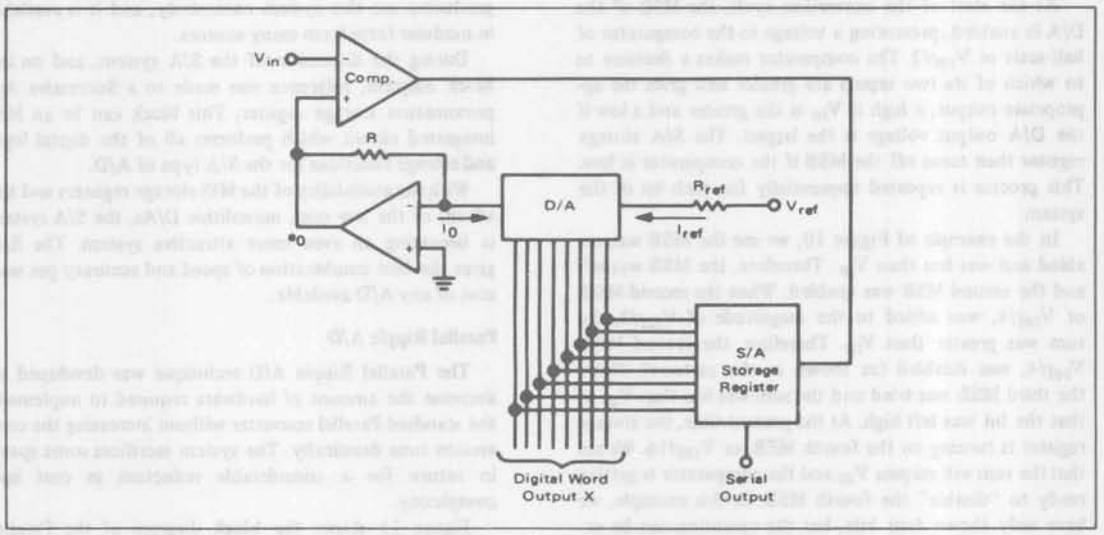


FIGURE 9 – Successive Approximation Block Diagram

signifying that the input signal is greater or less in amplitude than the output of the D/A. If the D/A output is greater than the input signal, the bit is "reset" or turned off. The system does this with the MSB first, then the next most significant bit, then the next, etc. After all the bits of the D/A have been tried, the conversion cycle is complete. At this time, another conversion cycle is started. The operation of the system can easily be understood by referring to Figure 10. This cartoon shows the system in actual operation.

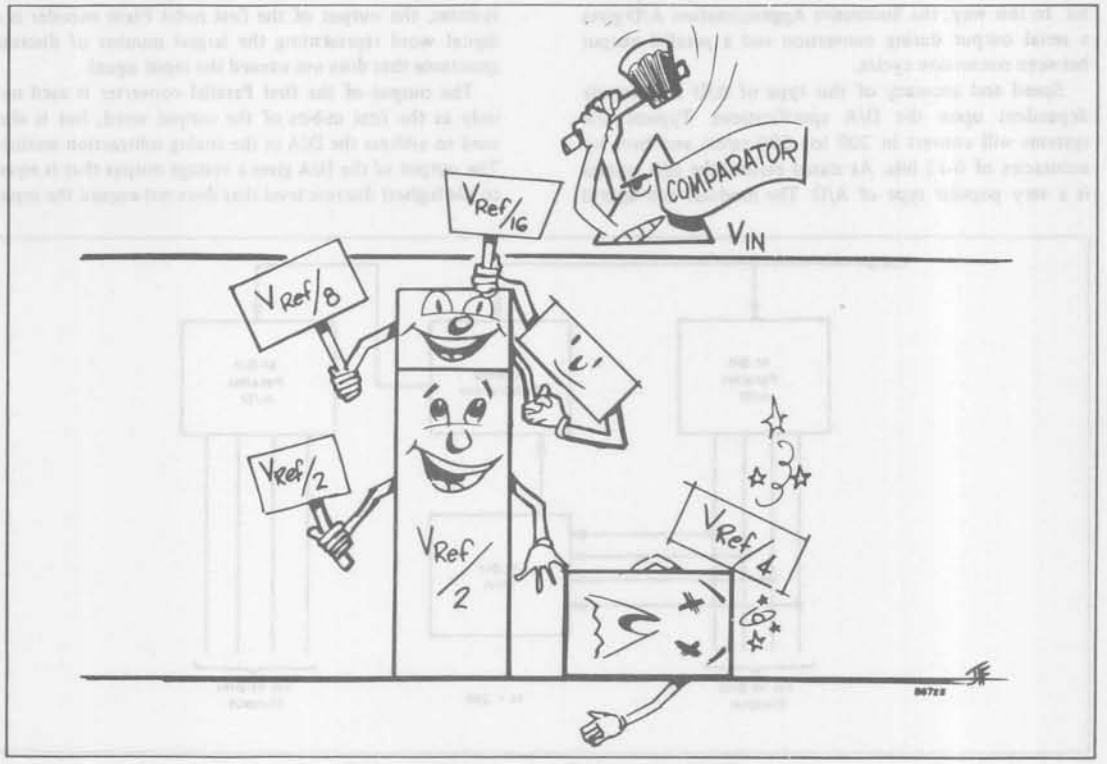


FIGURE 10 – Successive Approximation

At the start of the conversion cycle, the MSB of the D/A is enabled, presenting a voltage to the comparator of half-scale or $V_{ref}/2$. The comparator makes a decision as to which of its two inputs are greater and gives the appropriate output, a high if V_{in} is the greater and a low if the D/A output voltage is the largest. The S/A storage register then turns off the MSB if the comparator is low. This process is repeated sequentially for each bit of the system.

In the example of Figure 10, we see the MSB was enabled and was less than V_{in}. Therefore, the MSB was left and the second MSB was enabled. When the second MSB, or $V_{ref}/4$, was added to the magnitude of $V_{ref}/2$, the sum was greater than V_{in}. Therefore, the second MSB, $V_{ref}/4$, was disabled (as shown in the cartoon). Next, the third MSB was tried and the sum was less than V_{in} so that the bit was left high. At the present time, the storage register is turning on the fourth MSB, or $V_{ref}/16$. We see that the sum will surpass V_{in} and the comparator is getting ready to "disable" the fourth MSB. In this example, we have only shown four bits, but the operation can be extended to as many as desired. After the conversion cycle has completed the address of the D/A is the parallel binary word output of the A/D.

The serial output of the system is taken from the output of the comparator. While the system is in the conversion cycle, the comparator output will be either low or high, corresponding to the digital state of the respective bit. In this way, the Successive Approximation A/D gives a serial output during conversion and a parallel output between conversion cycles.

Speed and accuracy of this type of A/D are directly dependent upon the D/A specifications. Typical S/A systems will convert in 200 to -500-ns/bit and have bit accuracies of 6-12 bits. As stated earlier, the S/A system is a very popular type of A/D. The modular and hybrid producers use this system extensively, and it is available in modular form from many sources.

During the discussion of the S/A system, and on the block diagram, reference was made to a Successive Approximation storage register. This block can be an MSI integrated circuit which performs all of the digital logic and storage functions for the S/A type of A/D.

With the availability of the MIS storage registers and the advent of the low cost, monolithic D/As, the S/A system is becoming an even more attractive system. The S/A gives the best combination of speed and accuracy per unit cost of any A/D available.

Parallel Ripple A/D

The Parallel Ripple A/D technique was developed to decrease the amount of hardware required to implement the standard Parallel converter without increasing the conversion time drastically. The system sacrifices some speed in return for a considerable reduction in cost and complexity.

Figure 11 shows the block diagram of the Parallel Ripple type of A/D. Basically, the system consists of two each, m-bit Parallel converters, and an m-bit D/A. The total system has an n-bit output, where n = 2m. In this system both the parallel converters and the D/A-subtraction circuits must be n-bit accurate!.

In operation, the A/D converts the first m-bits of the output by the standard flash technique. As in most A/D systems, the output of the first m-bit Flash encoder is a digital word representing the largest number of discrete quantums that does not exceed the input signal.

The output of the first Parallel converter is used not only as the first m-bits of the output word, but is also used to address the D/A in the analog subtraction section. The output of the D/A gives a voltage output that is equal to the highest discrete level that does not exceed the input

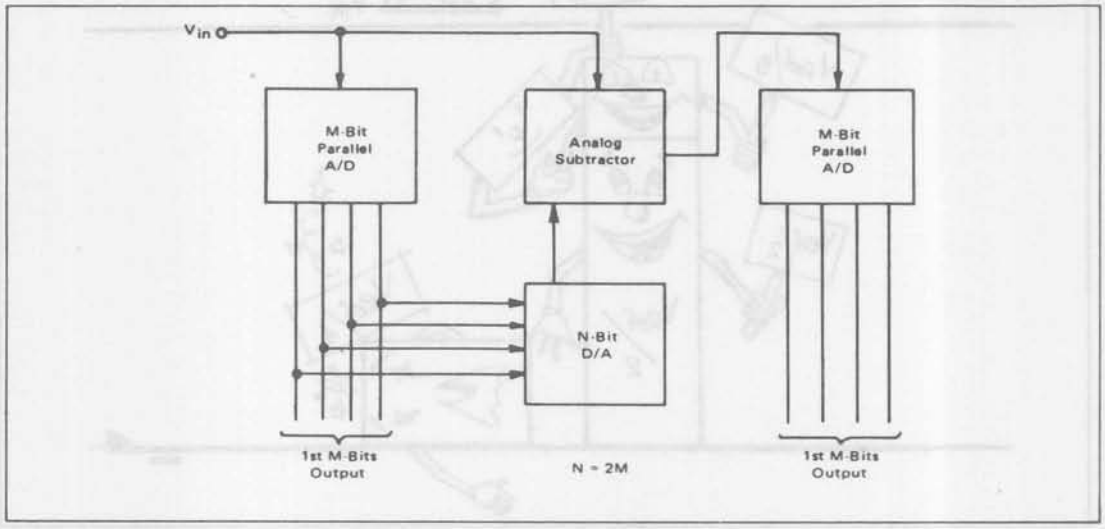


FIGURE 11 – Block Diagram of Parallel Ripple A/D

signal. This voltage is subtracted, by analog means, from the input signal. The remainder is then fed to another m-bit Flash encoder which converts the remaining m-bits of the system. In an actual system, either the thresholds of the second set of 2^m-1 comparators must be scaled down by a factor of 2^m, or the remainder signal must be amplified by 2^m.

As can easily be seen, the time required to complete a conversion is the sum of:

1. Time required for first m-bit conversion
2. Time for D/A to settle to required accuracy
3. Time to complete analog subtraction
4. Time required for second m-bit conversion

Since the first m-bits arrive at the output ahead of the second, and the system uses the Parallel technique, the name of Parallel Ripple was coined.

As stated earlier, at the present time no one is producing a monolithic A/D of any type. However, this scheme, and the other types of A/Ds about to be described, offer the possibility of monolithic fabrication of an A/D system. With present technology the system would probably have to be divided into several parts, each of which could be integrated. As the capabilities of the manufacturers continue to increase, a one chip, high speed A/D becomes more and more feasible.

VTF A/D System

The Variable Threshold Flash A/D converter is a clockless, non-synchronous type of A/D which gives a binary output, requires only one comparator per bit, and needs no decoding of the comparator outputs.

Primarily, the advantage of the VTF system over other types of A/Ds is the capability of high speed conversion coupled with low parts count and low cost. Also, the unique method that the system uses for conversion gives it added versatility. More will be said about this later. In addition to the above, the VTF type of A/D lends itself to monolithic fabrication.

Basically the VTF system is a "flash" approach with the addition of feedback. The addition of the feedback reduces the number of comparators required for an n-bit system from 2^n-1 to n. Like the flash method, n comparators have their thresholds initially set at the binary weightings of the reference voltage. That is, the threshold of the MSB is set at $V_{ref}/2$; the threshold of the second MSB is set at $V_{ref}/4$, etc.* (See AN-471).

In VTF operation, however, the comparator threshold voltages are changed at appropriate times and in such manner that their outputs are made to count in the proper code. Note that the VTF system may be set up to count standard "binary", Grey code, BCD or several other codings.

Figure 12 shows a block diagram of a 3-bit A/D using the VTF principle. Operation of the system may be easily understood if we look at each of the threshold determining circuits as a D/A converter. Note that only a one-bit D/A is needed for the MSB, a two-bit D/A is required for the second MSB, a three-bit for the third MSB, etc. The reason for this is shown in Figures 13(a) and 13(b). Figure 13(a)

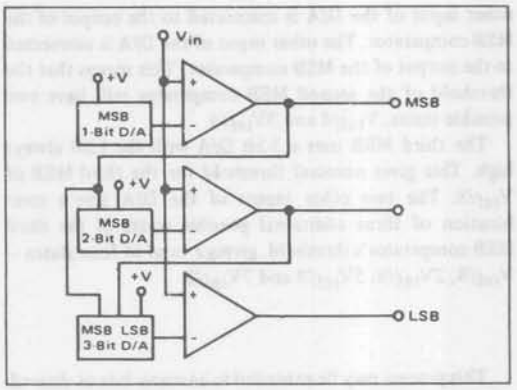
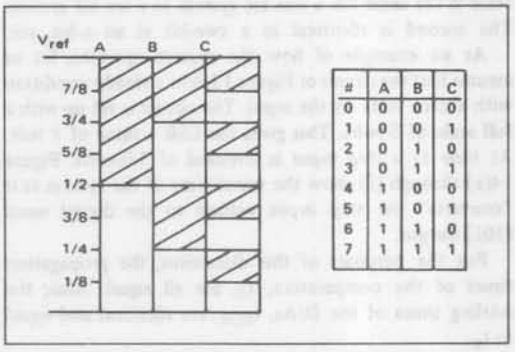


FIGURE 12 – Block Diagram of Variable Threshold Flash



#	A	B	C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

FIGURE 13 – VTF Threshold Levels

lists all of the possible states of a three-bit binary code. Figure 13(b) shows the level where each respective bit is high; the shaded areas representing the input voltage range for which the bit is high and the non-shaded areas the range of a low state.

It can be seen that there are 2^n separate areas for each bit, counting both shaded and non-shaded areas, where "n" is the bit number starting with the MSB as 1. An n bit D/A has 2^n possible output levels. Therefore, the system requires an n-bit D/A for bit number "n". This can be generalized to any number of bits.

Figure 13(b) shows that the first (lowest) transition of bit number n, occurs at the level of $V_{ref}/2^n$. Therefore, the lowest value of the comparator threshold for the bit is $V_{ref}/2^n$. This corresponds to the level out of the D/A with the least significant bit energized. For this reason the LSB of each D/A is always left on.

Using the above rules, the MSB uses a 1-bit D/A which is always on. This gives, in effect, a constant voltage equal to $V_{ref}/2$ as the threshold voltage of the MSB comparator. As can be seen in Figures 12 and 13, the threshold of the MSB does not change.

The second most significant bit uses a 2-bit D/A, (no pun intended). The LSB of this D/A is always on, giving a threshold of $V_{ref}/4$ to the second MSB comparator. The

other input of the D/A is connected to the output of the MSB comparator. The other input of the D/A is connected to the output of the MSB comparator. This means that the threshold of the second MSB comparator will have two possible states, $V_{ref}/4$ and $3V_{ref}/4$.

The third MSB uses a 3-bit D/A with the LSB always high. This gives nominal threshold for the third MSB of $V_{ref}/8$. The two other inputs of the D/A give a combination of three additional possible states of the third MSB comparator's threshold, giving a total of four states – $V_{ref}/8$, $2V_{ref}/8$, $5V_{ref}/8$ and $7V_{ref}/8$.

This process may be extended to as many bits as desired. Note that the addition of more bits to the system increases the compleixty of the additional bits only. The MSB is the same for a one-bit system as a ten-bit system. The second is identical in a two-bit as an n-bit, etc.

As an example of how the system operates, let us assume that the circuit of Figure 12 is in a steady condition with a zero volts on the input. The circuit is set up with a full scale of 8-volts. This gives the LSB a value of 1 volt. At time t_1 a step input is initiated of 5.0-volts. Figure 14(a) through (f) show the waveforms of the system as it "converts" the step input voltage to the digital word (101) output.

For the purposes of this discussion, the propagation times of the comparators, t_c, are all equal. Also, the settling times of the D/As, $t_{d/A}$, are identical and equal to t_c.

Figure 14(a) shows the threshold of the MSB comparator and the input voltage, V_{in}. The output of the MSB is shown in Figure 14(b). Figures 14(c) and (d) and 14(e) and (f) show the same points for each of the other two bits respectively.

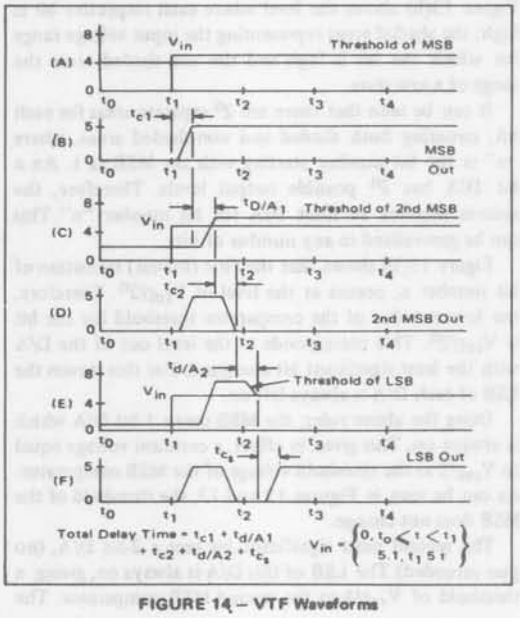


FIGURE 14 – VTF Waveforms

From time t_0 to t_1 the input voltage to the system V_{in} is zero volts. The threshold of the comparators are at their lowest states, namely, 4, 2, and 1-volt respectively. As the input voltage is below all of the thresholds the outputs of the comparators are all low.

At time, t_1, the input voltage is stepped to 5.0-volts. The input being greater than each of the respective threshold voltages, causes all of the outputs to go high. Therefore at time, $t_1 + t_{c1}$, all of the bits are high. The output of the MSB is one input to each of the D/As on the two least significant bits. Also, the output of the second MSB is one input of the LSB's D/A. These voltages on the D/A inputs cause the threshold of the second MSB to go to six volts and the LSB threshold to go to seven volts. At time, $t_1 + t_c + t_{d/A}$, the thresholds of the two least significant bits are at 6 and 7-volts respectively.

Since at this time the input voltage is less than the 2nd MSB's comparator and LSB's thresholds, both of the two least significant bits of the A/D go to a low. Because the output of the second MSB is an input to the LSB's D/A, the threshold of the LSB again changes. At time, $t_1 + t_{c1} + t_{d/A1} + t_{c2} + t_{d/A2}$ the threshold of the LSB is at 5.0-volts. As 5.0 is less than the 5.1-volts input, the output of the LSB goes high. The conversion is complete at time $t_1 + t_{c1} + t_{d/A1} + t_{c2} + t_{d/A2} + t_{c3}$. Thus, at this time, the data on the outputs of the comparators is the digital representation of the input voltage.

The data at the output of the MSB is valid one comparator delay after the input has been applied. The reason for this is the fact that the threshold of the MBS never changes.

The threshold of the second MSB is dependent on the state of the MSB. Therefore, the threshold voltage of the second MSB cannot be assumed to be accurate until one D/A settling time after the MSB reaches its final state. The output of the second MSB requires one comparator delay in addition to this. Because of this, the output of the second MSB cannot be guaranteed to be valid until two comparator delays and one D/A settling time after the input has been applied.

This process can be repeated through all of the stages of an n-bit system, giving a time necessary to guarantee the accuracy of a given bit. It is, however, easy to generalize the process by the formula:

$$t = nt_c + (n-1)\, t_{d/A} \qquad (1)$$

where n is the bit number, t_c is the propagation delay time of a comparator and $t_{d/A}$ is the settling time of a D/A.

Because of the above phenomenon, in operation the VTF A/D system converts the most significant bit first, then the second, etc. This means that if the output were taken before the A/D had completely converted the answer, the error would be in the least significant bits only. This appears as error and rolls off the amplitude of the signal output so that it appears as though the system were bandwidth limited. This means that the converter can give useful information before the A/D system has had

time to guarantee a complete conversion. Most A/D converters of this speed capability will give a completely unpredictable answer if the output is taken before the system has completely converted.

It should be noted here that the VTF A/D does not always require the time given by equation (1). The system can give the correct answer in as little as one comparator delay. The time required to give the complete conversion is a function of the amount of change of V_{in} since the last conversion. For example, if V_{in} only changes 1 LSB, the worst-case conversion time is two comparator delays and one D/A settling time.

The system as described here is a clockless, non-synchronous type of A/D. In this type of system, the converter output follows the input and the output can go through false states during the conversion. If desired, the VTF A/D system could be made into a completely synchronous, clocked type of system by adding digital delay circuits plus an analog delay time.

Synchronous VTF A/D System

Figure 15 shows the VTF system in a clock synchronous configuration. This circuit is identical to the one described earlier and shown in Figure 12, except for the addition of the D-type flip-flops and the analog delay lines. The advantages of this system is that after an initial n-clock period propagation delay, the output of the A/D gives a complete conversion every clock pulse thereafter. The only requirements being that the delay of the analog delay line must be equal to the clock period, and that period must be greater than the sum of one comparator delay and one D/A settling time.

The purpose of the analog and digital delay circuits is to allow the more significant bits to make another comparison before the least significant bits have completely converted. For example, let us assume the circuit is setting at zero and a signal input is applied as a step function. The value of the step input changes every clock period to a new value. This waveform is shown in Figure 16(b).

As described in the non-synchronous system, the MSB comparator output is valid after one comparator delay. This output is fed to all of the successive stages to change the other bit's respective thresholds. In the non-synchronous system the input signal must remain constant until the system has had time to complete the conversion. However, in the synchronous system the output is stored in a flip-flop and the output of the flip-flop is fed to the successive stages. This allows the MSB to give a new output without waiting for the rest of the system to complete the conversion.

This process is repeated through all of the stages of the A/D. In this manner the A/D can, after an initial n-clock period delay, give a complete conversion every clock period.

Figures (a) through (n) show waveforms of the system in operation. The delays are shown and one can see how the system gives a complete conversion every clock period.

As can be seen from the block diagrams of the systems and the above discussion, the VTF technique gives the simplest, lowest cost, and lowest parts count, high speed A/D that can be built with today's technology. Also, the

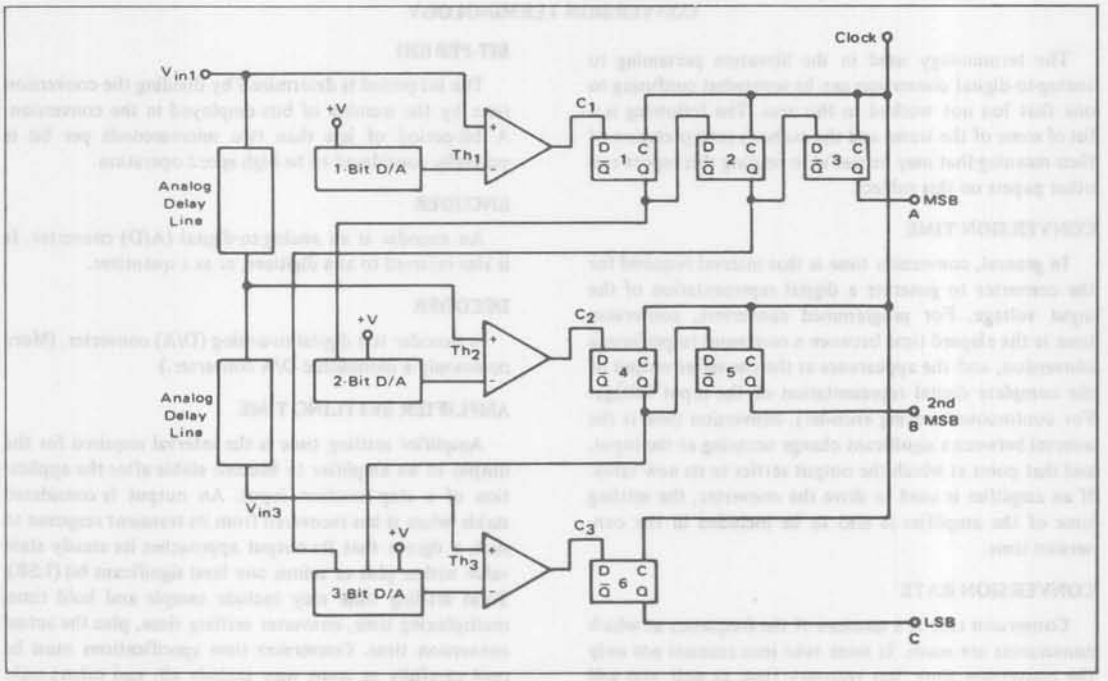


FIGURE 15 – Block Diagram of Synchronous VTF

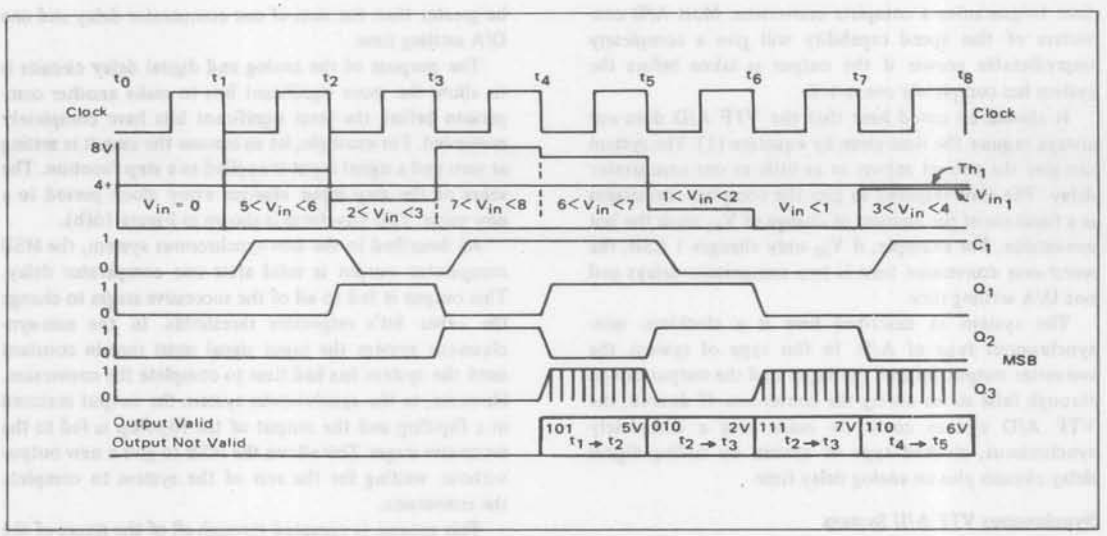


FIGURE 16 – MSB Waveforms For Synchronous VTF

fact that the VTF A/D can be built in monolithic form could give the system an added benefit to the user who desired to fabricate a high-speed A/D.

A 6-bit A/D using the non-synchronous system has been constructed at Motorola's Application Facility. Using MECL III Comparators and discrete part D/As, a worst-case conversion time of 60 nanoseconds was achieved. It is not unreasonable to expect the synchronous system to give an 8-bit conversion in 15 ns, at a cost of less than $250!

APPENDIX A
GLOSSARY OF ANALOG-TO-DIGITAL CONVERSION TERMINOLOGY

The terminology used in the literature pertaining to analog-to-digital conversion can be somewhat confusing to one that has not worked in this area. The following is a list of some of the terms and the author's interpretation of their meaning that may be useful in reading this report and other papers on this subject.

CONVERSION TIME

In general, conversion time is that interval required for the converter to generate a digital representation of the input voltage. For programmed converters, conversion time is the elapsed time between a command to perform a conversion, and the appearance at the converter output of the complete digital representation of the input voltage. For continuous tracking encoders, conversion time is the interval between a significant change occuring at the input, and that point at which the output settles to its new value. If an amplifier is used to drive the converter, the settling time of the amplifier is also to be included in the conversion time.

CONVERSION RATE

Conversion rate is a measure of the frequency at which conversions are made. It must take into account not only the conversion time, but recovery time as well, and will usually be less than the reciprocal of conversion time.

BIT-PERIOD

The bit-period is determined by dividing the conversion time by the number of bits employed in the conversion. A bit-period of less than two microseconds per bit is generally considered to be high speed operation.

ENCODER

An encoder is an analog-to-digital (A/D) converter. It is also referred to as a digitizer, or as a quantizer.

DECODER

A decoder is a digital-to-analog (D/A) converter. (More commonly a monolithic D/A converter.)

AMPLIFIER SETTLING TIME

Amplifier settling time is the interval required for the output of an amplifier to become stable after the application of a step-function input. An output is considered stable when it has recovered from its transient response to such a dgreee that its output approaches its steady state value within plus or minus one least significant bit (LSB). Total settling time may include sample and hold time, multiplexing time, converter settling time, plus the actual conversion time. Conversion time specifications must be read carefully as some may include all, and others only part of the above mentioned.

Note that in a 15-bit system, the RC time constants must be multiplied by at least 12 before the settling time error can be ignored. With each time constant period, the error decreases about 36%. After ten time constants, an exponential voltage is 0.005% away from the full value.

APERTURE

Aperture is the amount of uncertainty about the exact time when the encoder input was at the value represented by a given output code. In general, the aperture is equal to the conversion time. However, with the use of a sample-and-hold circuit as an input network, the aperture can be reduced, since more information is known about when the input sample was obtained relative to the timing of the output result.

QUANTUM LEVEL

In an n-bit encoder there are exactly 2^n different states. If the analog reference voltage is divided into 2^n parts then one part represents a quantum of voltage. The reference voltage is quantized into 2^n quantum levels where each quantum level is represented by one of the 2^n binary states in an n-bit quantizer.

The error of quantization is a function of the number of bits in the converter. An A/D converter is normally adjusted for the center of each of the binary weighted steps; hence, the error of quantization is at most one-half of a significant bit (1/2 LSB).

RESOLUTION

Resolution is the ability of the converter to distinguish between adjacent values of the quantity being measured. Normally the resolution would be considered to be limited only by the number of bits carried. In practice, however, the ultimate resolution of a given design is limited by the noise in the various analog and switching circuits, and by the linearity and monotonicity of the converter. Specifications for the resolution of a converter should be compatible with the number of bits and vice-versa, otherwise the specification would imply that the readings convey a higher degree of resolution than could actually exist.

ACCURACY

Accuracy must include all of the sources of errors (quantization, non-linearily, noise, and short term drift). Relative accuracy is often defined as the deviation from a straight line passing through zero and the nominal full scale value (very similar to linearity). A typical accuracy specification might be 0.05% ± 1/2 LSB at +25°C.

Long term stability, not included in the accuracy specification, defines the additional error introduced because of component aging. It is measured over a period of time (generally one to three months) at a fixed ambient temperature. A typical long term stability specification might be ±0.005%/90 days at +25°C.

PRECISION

Precision relates to the repeatability of successive measurements. Precision is limited in practice by noise and a small but finite quantization error that always exists in some "dead band" at each successive numerical value. When the unknown analog voltage lies within any of the dead bands around each of the possible values, the repeatability can never be greater than plus or minus one least-significant-bit. One measure of the quality of the high speed analog-to-digital converter is the ratio of the dead band to the full quantization level for each value across the entire range.

MONOTONICITY

Monotonicity relates to an increasing output for every increasing value of input voltage. Another way of saying this is that the derivative of the output with respect to the input is always positive. A converter must be capable of producing every coded value within the input range defined. The accuracy of the various resistors in the digital-to-analog converter ladder network and the offser voltage in the switching electronics must be minimized, so that the sum of the errors for any given number of successive lesser significant bits is less than the error produced by the next most significant bit; otherwise, it would be possible to force non-uniform spacing of the quantum levels and miss some of the output codes altogether. Absolute requirements for monotonicity are that all codes are obtainable and that the quantization level of each code be within one-half of one least-significant-bit of the ideal, linear-related quantization level.

LINEARITY

Linearity is a measure of the deviation from a straight line of a plot of the input-output radio of an analog-to-digital converter over its operating range and is usually expressed in a percent of full scale.

STABILITY

The factor of stability simply relates to the ability of the converter to maintain the characteristics (relative accuracy, resolution, precision, etc.) over a defined operating interval. Lack of stability occurs primarily for two reasons: drift in the voltage reference and the resistors, and drift in the conversion switching networks.

CONVERSION ERROR

The discrepancy between the actual output of an analog-to-digital converter and the exact digital representation of the quantity being measured at the instant of measurement is conversion error. It is generally one-half of the value represented by the least-significant-bit.

INPUT IMPEDANCE

The input impedance of the converter system is the amount of load that the ADC represents to its source, the quantity being measured. A typical comparator with a 50 MΩ input resistance will load a source resistance of 1 kΩ sufficiently to introduce an error of 0.002%.

SYSTEM TEMPERATURE COEFFICIENT

The system temperature coefficient in the worst case is the sum of the contributions of each of the component temperature coefficients. One must be careful in reading A/D converter specifications to avoid being misled by the "RMS-trick". RMS calculations are good when a large number of terms are included, but are not valid when only a few elements are present. Consider the following as an example of this mis-specification:

Voltage Reference TC = 0.0006%/°C
Voltage Comparator TC = 0.0005%/°C
Ladder Resistor TC = 0.0003%/°C

Algebraic Total = 0.0014%/°C
$(\text{rms total})^2 = (0.006)^2 + (0.005)^2 + (0.003)^2$
$= 0.00000070$
rms total 0.0008%/°C

The RMS total is obviously a misleading specification when the algebraic total could quite possibly occur since the probability that a few things could occur simultaneously is not too small.

APPENDIX B
CODES AND NUMBERING SYSTEMS USED IN A/D AND D/A CONVERSION

Several computational codes or number systems are used in data handling machines, the majority of which may be categorized as positional notations. Positional notation means that any integar may be represented by the sum of a number of digits, weighted in value according to their position in the notation.

Using this notation, it is possible to express any integer (A) as

$$A = a_n B^n + a_{n-1} Bn-1 + \ldots + a_0 B^0 \quad (1)$$

where B is the base or radix of the number system, and a_n is an integer number. A fractional number may likewise be expressed in the form of equation 1 by using negative exponential powers. The three commonly used bases are 10 (decimal system), 8 (octal system), and 2 (binary system).

One of the basic requirements of all positional notations is that the base of the code equal the total number of digit symbols, all possible values of a_n, used to represent the coded numbers, a_n is a digit between 0 and (B-1), where again B is the radix of the number system.

Decimal

The decimal system uses 10 symbols (0, 1, 2, 3, ..., 8, 9); therefore, from our previous discussion the base of the decimal system is 10, and any integer (A) can be represented as

$$A = a_n 10^n + a_{n-1} 10^{n-1} + a_{n-2} 10^{n-2} + \ldots + a_0 10^0 \quad (2)$$

Where a_i is an integer between and including 0 and 9. As an example, the number 15 to the base 10, which symbolically is $(15)_{10}$, is represented as shown below.

$$(15)_{10} = 1 \times 10^1 + 5 \times 10^0 \quad (3)$$

Because of its early development and its natural association to man (i.e., 10 fingers, 10 toes), the decimal system is universally used for human computation. However, when the decimal system is used for notational purposes in high speed data systems, it becomes clumsy, inconvenient, and very inefficient.

Using the decimal system, electronic circuitry would be required to accurately represent ten different states corresponding to the ten digit symbols. Circuitry of this type is currently unavailable. However, many methods now exist for representing two independent states electrically.

Binary

The binary number system was developed to take advantage of the convenience of the 2-state concept which was just discussed. This system uses the number base 2 which means that only two digits (0 and 1) can be used to represent all coded numbers (a_i's). As an example, the number $(15)_{10}$ represented in base-2 notation is:

$$(15)_{10} = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = (1111)_2 \quad (4)$$

This illustrates that the binary code sacrifices length of notation for simplicity of digital symbolism.

When the machine language is completely binary, communication between man and machine is frequently impossible and at very best, messy. To overcome this problem a coding system is needed which combines the ease of machine computation of the binary system with the familiarity of the decimal system. A coding technique that combines these features into one code is the binary-coded decimal (BCD) system which uses an arbitrary four-digit binary code to represent each of the decimal digits (0 through 9).

Binary-Coded Decimal

One specific binary-coded decimal code is formed by using the binary representations of the decimal numbers 0 through 9. This is commonly called the 8-4-2-1 code. The first 16 decimal numbers and their representations in the binary and binary-coded decimal system are shown in columns one through three in Table I, included at the end of this appendix. Using the binary-coded decimal code, the decimal number 715 is written as

7	1	5	
0111	0001	0101	(5)

or

$$(715)_{10} = (011100010101)_{BCD} \quad (6)$$

To convert from binary-coded decimal (BCD) to decimal numbers, one has only to make the coded number into four digit sections, starting with the least significant digit and proceeding to the left, and then apply the definition of the binary numbers 0 through 9 to each section.

Gray

One binary-coded decimal code which finds wide application in analog-to-digital converters is the unit-distance code (also called the Gray Code, after its inventor, and also commonly called the "cyclic" or the "Reflected Binary Code".

The Gray Code has the unique property that its states are a unit-distance apart. That is in going from any decimal number (i.e., 11) to any adjacent decimal number (10 or 12) only one binary digit will change value. The fourth column of Table I illustrates the Gray code representations for the decimal number 0 through 15.

As a matter of general information, the generating equation for the magnitude of each one (1) in the Gray code is

$$\sum_{j=0}^{j=n} 2^j \qquad (7)$$

where n represents the digit column in which the one (1) appears. The most significant one (1) has a positive sign and each of the succeeding ones (1's) to the right will have an alternate sign. As an illustration, consider the Gray-coded number 1110.

$$(1110)_G = \sum_{j=0}^{3} 2^j - \sum_{j=0}^{2} 2^j + \sum_{j=0}^{1} 2^j$$

$$= 2^0 + 2^1 + 2^2 + 2^3 - 2^0 - 2^1 - 2^2 + 2^0 + 2^1$$

$$= 2^3 + 2^0 + 2^1 = (11)_{10} \qquad (8)$$

TABLE I

The Binary, Binary-Coded Decimal, and Gray Code Equivalents of the First 16 Decimal Numbers

Decimal	Binary	Binary Coded Decimal	Gray Code
0	0000	0000 0000	0000
1	0001	0000 0001	0001
2	0010	0000 0010	0011
3	0011	0000 0011	0010
4	0100	0000 0100	0110
5	0101	0000 0101	0111
6	0110	0000 0110	0101
7	0111	0000 0111	0100
8	1000	0000 1000	1100
9	1001	0000 1001	1101
10	1010	0001 0000	1111
11	1011	0001 0001	1110
12	1100	0001 0010	1010
13	1101	0001 0011	1011
14	1110	0001 0100	1001
15	1111	0001 0101	1000

Hence, the Gray code for the decimal 11 is 1110. The Gray code for the decimal 12 is 1010. Only the second most significant digit (bit) changes between the successive numbers (11 and 12) allowing no ambiguity to exist in the digital readout. The point is of reasonable significance when decoding is required and erroneous spikes cannot be tolerated.

REFERENCES:

1. Susskind, A.K., Notes on Analog-Digital Conversion Techniques (John Wiley Book Company, New York, 1957).
2. Freeman, J., "Ladder Networks Are Easy to Design," Electronic Design (July 5, 1967).
3. Renschler, E., "Design of An Integrated Circuit Analog-to-Digital Conversion System," Dept. of Electrical Engineering, Arizona State University, and Motorola Semiconductor Products Division, Phoenix, Arizona, April 1, 1968.
4. Schmid, H., "D/A Conversion", Electronic Design (October 24, 1968).
5. Digital Logic Handbook, Digital Equipment Corporation, Maynard, Massachusetts, Part 5, Chapters 1 thru 6 (1967).