Notes on Converter System Component Selection

by Cy Brown, Marketing Manager — ADI Converter Products

LET THERE BE LIGHT!

The applications for digital data-handling equipment, and for its rapidly-growing handmaidens, the products of the conversion-and-data-acquisition industry, have spawned a terrifying multiplicity and diversity of companies, product lines, and products. We find it sobering (though not a little gratifying!) to discover that, as a major manufacturer, with a reasonably-complete line, we can deliver some 250 distinct D/A converter types, and that that line alone is growing by 75 types per year.

Thus, the very large number of converter products available in the marketplace, even from a single manufacturer, can overwhelm even the most informed engineer, when faced with the problem of selecting a device, or a group of devices, for a given application.

Interpretation of the specifications adds another dimension to the task, which is further complicated by the virtual absence of standardized definitions of specifications among the manufacturers. To remedy this situation, and attempt to make the system-designer's job a little easier, we list here some of the steps a user can take to help him "home in" on a near-optimum selection. On the opposite page, we show how one engineer made a choice and confirmed its efficacy. (Ed.)*

TWO BASIC FACTORS

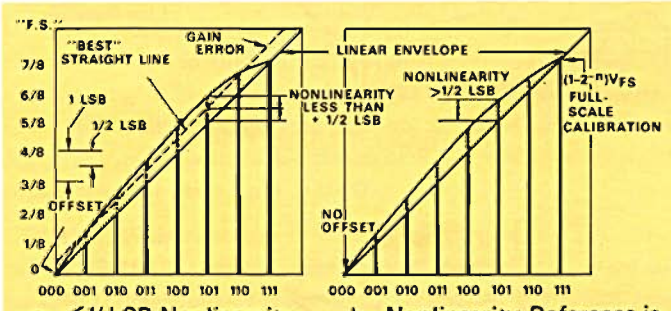
The two key factors in choosing the right device are:

- **Completely define the design objectives.** Consider all known objectives and try to anticipate the unknowns that will pop up later. Include such factors as signal and noise levels, required accuracy, throughput rate, characteristics of the signal and control interface, environmental conditions and space factors, anticipated budgetary limitations that may force performance compromises.

- **Understand what the specs mean.** It is essential to have a firm understanding of what the manufacturer means by his set of specifications. It should not be assumed that any two manufacturers mean the same thing when they publish identical numbers defining a given parameter. In most cases, the manufacturer has honestly attempted to provide accurate information about his product. This information must be interpreted, however, in terms meaningful to the user's requirements, which requires a knowledge of how the terms are defined. For example:

D/A Converter Linearity. The conventional definition of nonlinearity of a device is deviation from a "best straight line." To determine whether a device meets the stated linearity specification, the shape of the nonlinearity and its amplitude have to be known so that the end points (e.g., the zero and full-scale points for a unipolar device) can be offset by a "best" amount to minimize linearity error. As Figure 1a shows, by the use of this criterion, a bowed nonlinearity may be specified as ½ the worst case deviation from the straight line obtained by calibrating the end points. This is fine if you're a vendor and want to prove that the device meets its specs, but it's of little help to the user, who needs the specified linearity for a unit that has been calibrated for zero and scale factor.

For this reason, even though it makes our design and Q.C. jobs twice as hard, Analog Devices specifies nonlinearity of converters as the *maximum* deviation, at any point, from the calibrated linear relationship (Figure 1b). The user now needs only to set the two end points, according to the standard calibration procedure. The normal limit used is ±½LSB (least significant bit). This then means that the sum of positive errors or the sum of the negative errors of the individual bits must not exceed ½LSB, which means, further, that the errors of the bits themselves must be considerably less than ½LSB.



a. <½LSB Nonlinearity Achieved by Arbitrary Location of "Best Straight Line"

b. Nonlinearity Reference is Straight Line Through End Points. Nonlinearity >½LSB for Curve of Fig. 1a

Figure 1. Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points is Easier to Measure, Gives More-Conservative Specification

APPLICATION CHECKLISTS

General Considerations

A. Accurate description of input and output
   1. Analog signal range, source or load impedance
   2. Digital code needed: Binary, 2's Complement, BCD, etc.
   3. Logic-level compatibility: TTL, CMOS, etc., logic polarity

B. Data throughput rate

C. Control interface details

D. What does the system error budget allow for each block?

E. What are the environmental conditions: temperature range, supply voltage, recalibration interval, etc., over which the converter should operate to the desired accuracy?

Besides these general considerations, there are specific items to consider when choosing each block in a system.

Considerations for D/A Converters

A. What resolution is needed? How many bits (e.g., 8, 10, 12, etc.) of the incoming data word must be converted. To what degree of accuracy, linearity, etc.?

B. What logic levels and codes can be provided to the DAC? The most popular logic system is TTL, and the most-frequently-used codes are binary, 2's complement, offset binary, BCD, and their complements.

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*This article is based on material in the Converter-Product Selection Guide, to be found in the 1972 full-line catalog from Analog Devices, available in March. If you are on the mailing list for *Analog Dialogue*, your copy has either arrived or is about to arrive. Otherwise, Circle F4

SELECTING COMPONENTS FOR A SYSTEM — A BRIEF EXAMPLE*

THE PROBLEM

A computer data-acquisition system is to be assembled to process data from a number of strain gages. Signal-conditioning hardware, to be purchased with the gages, delivers ±10V full-scale signals with 10-ohm source impedance. The signal channels must be sequentially scanned in no more than 50 microseconds per channel. Maximum allowable error of the system is about 0.1% of full scale. System logic is to be TTL, and hardware may work in either binary or 2's complement code. Parallel data readout will be used.

Probable temperature range in the equipment cabinets (including equipment temperature rise) is +25°C to +55°C. Sufficient power at both ±15V and +5V is available, but the regulation of the ±15V supply is 150mV.

The objective: Specify a set of conversion components having appropriate accuracy and speed.

FIRST APPROXIMATION

A useful rule of thumb that usually provides satisfactory results is this: For the critical specs of a multi-component system, choose each component to perform roughly 10 times better than the overall desired performance. Thus, for a system that needs 0.1%-grade performance, use a 0.01% converter (12 bits) with compatible multiplexer and sample-hold.

Reviewing the available A/D converters, we find the ADC-12Q and ADC-12QM to be possible choices. If the entire system is to be built on a single card, the ADC-12QM, a 2" x 4" x 0.4" encapsulated module would be a convenient choice.

The ADC-12QM completes a conversion in 25μs. For sample-hold, the compatible SHA-1A is chosen, adding 5μs of settling time. Thus, the combination appears to be amply capable of meeting the 50μs/channel scanning requirement. Since the multiplexer will scan sequentially, its settling time is inconsequential. The multiplexer can be switched to the next address as soon as the SHA goes into *hold* on data from the current address. Thus it has at least 25μs to settle before a measurement is called for. For convenience, one may use the MPX-8A; the small 2" x 2" x 0.4" module fits into the packaging concept, and the built-in complete binary-address decoding makes it easy to work with.

ERROR ANALYSIS

It's clear that the MPX-8A, the SHA-1A, and the ADC-12QM generally meet the problem's requirements for speed and resolution. Now we must look further into the details of errors, to determine if the worst-case situation is within the allowable 0.1% system error.

Multiplexer (MPX–8A)†

The switches of the MPX-8A, being MOSFET's with variable-resistance channels, are not subject to voltage offset errors. Errors here will be due to two factors:

1. Leakage current into the *on* channel from the *off* channels develops an offset voltage across the source impedance.
   Leakage current @ 25°C 10nA
   Source impedance 10Ω
   Error voltage = $10 \times 10 \times 10^{-9} = 10^{-7}$ V (negligible)
2. Transfer error due to voltage division across the MOSFET *on* resistance and input impedance of the SHA-1A:
   ON resistance 1000Ω maximum
   SHA-1A R_{in} $10^{12}\Omega$
   Divider ratio attenuation error: 10^{-9} (negligible)

Sample-Hold (SHA-1A)†

1. Nonlinearity is 2mV over the 20V range, or 0.01%
2. Gain error of 0.05% maximum (and other similarly small initial gain errors in the system) may be compensated for overall when calibrating the system by setting the scale constant of the ADC. Gain T.C. of a follower-type Sample-Hold, as used in this example, is insignificant.
3. Input bias current of 10nA (max) causes an offset error voltage in the source resistance.
   Source resistance = $10\Omega_{(source)} + 1k\Omega$ (MPX switch)
   Offset error = $10^{3} \times 10^{-8} = 10\mu V$ (negligible)
4. Offset vs temperature = 25μV/°C

Since the temperature inside the housing may change by as much as 30°C, the total change over the range will be
25 x 30 = 750μV, or 7.5ppm of ±10V

An offset adjustment is provided for initial trimming.

5. Offset vs power supply = $100\mu V/\%\Delta V_S$

Since the supply may vary by 150mV, or 1% of 15V, the error contribution is 100μV, or 0.01% of full scale.

By an analysis comparable to the above, we would normally also prepare a system timing diagram, and assign operate- and settling-time allowances. However, the components selected for this example have better-than-adequate settling time, even for 0.01% operation; consequently, we can overlook the need for a formal timing analysis to determine whether settling times are adequate.

Converter (ADC-12QM)†

1. Specified linearity error (relative accuracy) ½LSB, or 0.0125%.
2. Quantizing uncertainty: ½LSB, or 0.0125%. This is a resolution limitation, not normally considered in the error budget.
3. Temperature errors
   a. Gain temperature coefficient: 5ppm/°C for 30°C
      5 x 30 = 150ppm, or 0.015%
   b. Zero temperature coefficient: 5ppm/°C for 30°C
      5 x 30 = 150ppm, or 0.015%
4. Power supply sensitivity error: $0.002\%/\%\Delta V_S$
5. Differential nonlinearity temperature coefficient, 3ppm/°C. For 30°C temperature change, error is 90ppm, less than ½LSB. Therefore, 12-bit monotonicity can be maintained, with no missing codes.

CONCLUSION

The worst-case arithmetic sum of these errors is 0.07%, and the rms sum is 0.03%. Since these values are reasonably conservative for a system with specified error of 0.1%, the designer may either rest with these choices and go on to the more-difficult hardware, software, interface, and wiring problems, or — if absolute-minimum cost of conversion hardware is an important objective — seek to reduce cost by considering a more marginal design.

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*For maximum tutorial benefit, to avoid clutter, and to fit the available space, some of the less-salient sources of error have been intentionally omitted. If there are any that you're concerned about for your application but don't see here, we invite you to communicate with the author.

†For technical data on these 3 products, use reply card. Circle F5

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C. What kind of output signal is needed: a current or a voltage? What is the desired full-scale range? (Most DAC's are available with either current output – at very high speed – or voltage output, with the added delay of an internal operational amplifier. Voltage-output DAC's are the more convenient to use and, with the exception of those designed specifically for high speed, will serve in all but those applications calling for μs and sub-μs settling times. Current-output DAC's are used in applications where high speed is more essential than stiff voltage output, such as circuits with comparators, e.g., A/D converters, or where fast amplification is to be provided externally, e.g., via CRT deflection amplifiers.)

D. What are the speed requirements? What is likely to be the shortest time between data changes? After a change in the digital input data, how long can the system wait for the output signal of the DAC to settle to the desired accuracy . . . for a full-scale change? For a 1-bit change at the major carry? Are switching transients of any consequence? Can they be filtered? Must they be suppressed within the DAC?

E. Over how wide a temperature range (at the module – i.e., ambient plus temperature rise) must the converter operate? Over how much of this range must the converter perform essentially within its specifications without readjustment?

F. How stable are the terminal voltages of the power supplies that will power the DAC? Is the power-supply sensitivity specification adequate to hold errors from this source within reasonable limits?

Considerations for A/D Converters

The process of selecting an A/D converter is similar to that involved in the selection of D/A converters. The following considerations are typical:

A. What is the analog input range, and to what resolution must the signal be measured?

B. What is the requirement for linearity error, relative accuracy, stability of calibration, etc.?

C. To what extent must the various sources of error be minimized as environmental temperature changes? Are missed codes tolerable under any conditions?

D. How much time is allowed for each complete conversion?

E. How stable is the system power supply? How much error due to power-supply variation is tolerable in the conversion system?

F. What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter. (A/D converters are designed according to several different circuit philosophies: e.g., successive approximation, dual-slope integration, counter-and-comparator, etc. As a rule, integrating types are best for converting noisy input signals at relatively-slow rates, while successive-approximation is best suited to converting sampled or filtered inputs at rates up to 1MHz. Counter-comparator types provide lowest cost, but may be both slow and noise-susceptible.)

Considerations for Multiplexers and Sample-Holds

When a sampled-data system is to be assembled, in which one A/D converter is time-shared among many input channels by using a multiplexer and a sample-hold, the contribution of these accessory devices to system performance errors must be taken into account.

Multiplexers

A. How many input channels are needed? Single-ended or differential? High-level or low-level? What dynamic range?

B. What kind of addressing scheme is to be used?

C. How much time is needed for settling to desired accuracy when switching from one channel to another? Maximum switching rate?

D. How much ac crosstalk error between channels is allowable? At what frequencies?

E. What error is produced by the leakage current flowing through the source resistance?

F. What will be the multiplexer "transfer" error, produced by the voltage divider formed by the *On* resistance of the multiplexer and the input resistance of the sample-hold. Is multiplexer active or passive? (Does it have an output amplifier?)

G. Is the channel-switching rate to be fixed or flexible? Continuous or interruptible? Should it be capable of stopping on one channel for test and calibration purposes?

H. Is there danger of damage to active signal sources when the power is turned off? MOSFET multiplexers are inherently "safe," since the switches open when power is removed. JFET multiplexer switches usually close when power is removed, making it possible to interconnect, and therefore damage active signal sources. (MOSFET's are used as switches in *all* ADI multiplexers.)

Sample-Holds

A. What is the input signal range?

B. Considering the slewing rate of the signal and the multiplexer's channel-switching rate, what is the sample-hold's allowable acquisition time to within the desired error band?

C. What accuracy is needed (gain, linearity, and offset errors)?

D. What aperture delay and jitter are allowable, going into *Hold?* The delay component of aperture time is considered to be correctible, since the switching operation can be advanced to compensate. The uncertainty (jitter) cannot be compensated, and a random jitter of 5ns applied to a signal slewing at, say, 1V/μs produces an uncertainty of 5mV. In sampled-data systems, operating at a constant sampling rate, with data that is not correlated to the sampling rate, delay is of no importance, but jitter modulates the sampling rate.

E. How much "droop" in *hold* is allowable?

F. What are the effects of temperature, time, and power supply variation?

G. What offset error is caused by the flow of the sample-hold's input bias current through the series resistance of the multiplex switch and the signal source?

SYSTEM-COMPONENT SELECTION PROCESS

The most natural process for selection of appropriate off-the-shelf components to meet a system requirement involves a method of successive approximations: Choose the least costly device that meets the most significant requirements, and perform an error analysis to check its adequacy. If its performance seems far in excess of that needed (at possibly excessive cost), or inadequate in some respects, inspect the discrepancies for possible design tradeoffs, make a new choice (if necessary) and repeat the analysis. Remember that in a maturing industry, costs can be expected to decline. *It is often less costly in the long run to go for better performance rather than lowest possible cost in the initial stages of design.*