CHAPTER 6: CONVERTERS

SECTION 6.6: DATA CONVERTER AC ERRORS (cont.)

BASIC LINEAR DESIGN

CHAPTER 6: CONVERTERS

Introduction

There are two basic type of converters, digital-to-analog (DACs or D/As) and analog-to-digital (ADCs or A/Ds). Their purpose is fairly straightforward. In the case of DACs, they output an analog voltage that is a proportion of a reference voltage, the proportion based on the digital word applied. In the case of the ADC, a digital representation of the analog voltage that is applied to the ADCs input is outputted, the representation proportional to a reference voltage.

In both cases the digital word is almost always based on a binarily weighted proportion. The digital input or output is arranged in words of varying widths, referred to as bits, typically anywhere from 6 bits to 24 bits. In a binarily weighted system each bit is worth half of the bit to its left and twice the bit to its right. The greater the number of bits in the digital word, the finer the resolution. These bits are typically arranged in groups of four, called bytes, for convenience.

For a better understanding of the relationship between the digital domain and the analog domain please refer to the section on sampling theory.

As stated earlier, we shall look at the operation of converters primarily from a “black box” view. We will concern ourselves less with the internal construction of the converter and more with its operation. We cannot, however, completely ignore the internal architecture because in many cases it is relevant to operational advantages or limitations. There are a number of works that cover the internal workings of the converters in much more detail (see References).

Another point that should be kept in mind is the difference between accuracy and resolution. The resolution of a converter is the number of bits in its digital word. The accuracy is the number of those bits that meet the specifications. For instance, a DAC might have 16 bits of resolution, but might only be monotonic to 14 bits. This means that the assured accuracy of the DAC will be no better than 14 bits. Also, an audio ADC might have a digital word width of 16 bits, but the SNR may be only 70 dB. This means that the accuracy will only be at the 12-bit level. This is not to say that the other bits are irrelevant. With further processing, typically filtering, often the accuracy can be improved. While these terms are similar and sometimes used interchangeably, the distinction between the two should be remembered.

We shall examine the DAC first.

SECTION 6.1: DIGITAL-TO-ANALOG CONVERTER ARCHITECTURES

Digital-to-Analog Converters (DACs or D/As) Introduction

What we commonly refer to as a DAC today is typically quite a bit more. The DAC will typically have the converter itself and a collection of support circuitry built into the chip.

The first DACs were board level designs, built from discrete components, including vacuum tubes as the switching elements. Monolithic DACs began to appear in the early ’70s. These early examples were actually sub-blocks of the DAC. An example of this would be the AD550, which was a 4 bit binarily weighted current source. This current source block would be mated to a separate part, such as the AD850, which contained a resistor array and CMOS switches. Together these would form the basic DAC. As we moved on in time these functions were integrated on the same die, additional digital circuitry, specifically latches to store the digital input, were added. Then a second rank of latches was often added. The purpose of the second rank was to allow the microprocessor or microcontroller to write to many DACs in a system and the updated them all at the same time. The input rank of latches could also be a shift register, which would allow a serial interface.

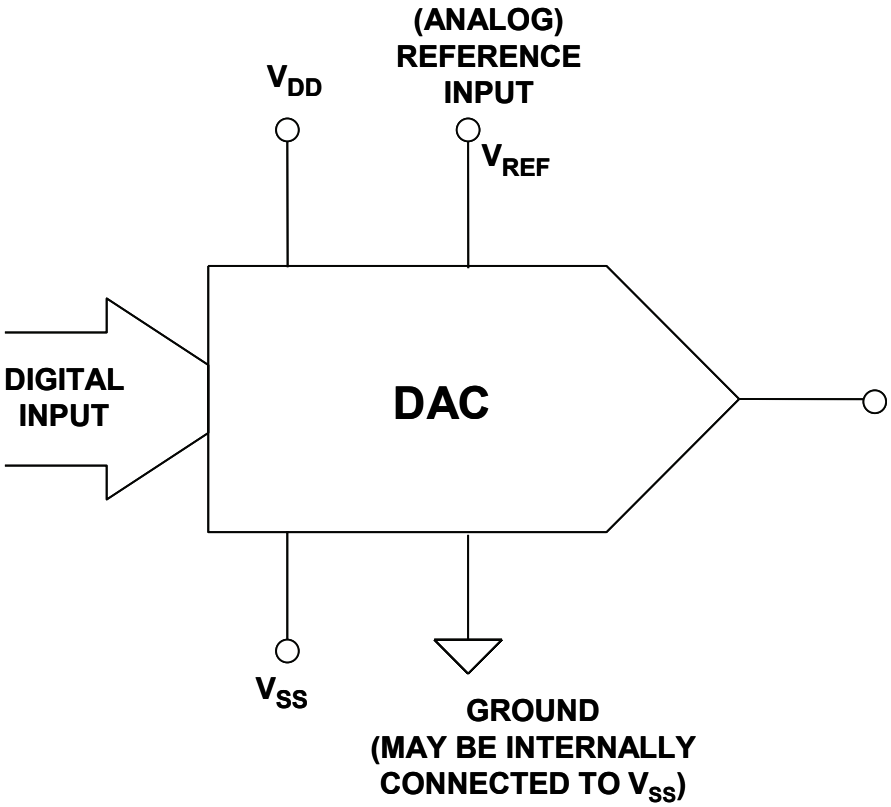


Figure 6.1: *The Basic DAC*

On the back end, since the output of the DAC is often a current, an op amp is often added to perform the current-to-voltage (I/V) conversion. On the front end a voltage reference is often added.

Process limitations did not allow the integration of all these sub-blocks to occur at once. Initially, the processes used to make the various sub-blocks were not compatible. The process that made the best switches was typically not the best for the amplifier and the reference. As the processes became more advanced these limitations became less. Today CMOS can make acceptable amplifiers and processes combining bipolar and CMOS together exist.

There are several advantages to including all this additional circuitry in one package. The first is the obvious advantage of reducing the chip count. This reduces the size of the circuitry and increases the reliability. Probably more important is that the circuit designer now doesn't have to concern himself with the accuracy of several parts in a system. The system is now one part and tested by the manufacturer as a unit.

Next we will look at the various DAC architectures. When we refer to DACs here we are referring to the basic converter rather than the complete system.

Kelvin Divider (String DAC)

The simplest structure of all is the Kelvin divider or string DAC as shown in Figure 6.2. An N-bit version of this DAC simply consists of 2^N equal resistors in series and 2^N switches (usually CMOS), one between each node of the chain and the output. The output is taken from the appropriate tap by closing just one of the switches (there is some slight digital complexity involved in decoding to 1 of 2^N switches from N-bit data).

This architecture is simple, has a voltage output and is inherently monotonic—even if a resistor is accidentally short-circuited, output n cannot exceed output n + 1. It is linear if all the resistors are equal, but may be made deliberately nonlinear if a nonlinear DAC is required. The output is a voltage, but it has the disadvantage of having a relatively large output impedance. This output impedance is also code dependant (the impedance changes with changes to the digital input). In many cases it will be beneficial to follow the output of the DAC with an op amp to buffer this output impedance and present a low impedance source to the following circuitry.

Since only two switches operate during a transition it is a low glitch architecture (the concept of glitch will be examined in a following section). Also, the switching glitch is not code-dependent, making it ideal for low distortion applications. Because the glitch is constant regardless of the code transition, the frequency content of the glitch is at the DAC update rate and its harmonics—not at the harmonics of the DAC output signal frequency. The major drawback of the Kelvin DAC is the large number of resistors and switches required for high resolution. There are 2^N resistors required, so a 10 bit DAC would require 1024 switches and resistors, and as a result it was not commonly used as a simple DAC architecture until the recent advent of very small IC feature sizes made it very practical for low and medium resolution (typically up to 10 bits) DACs.

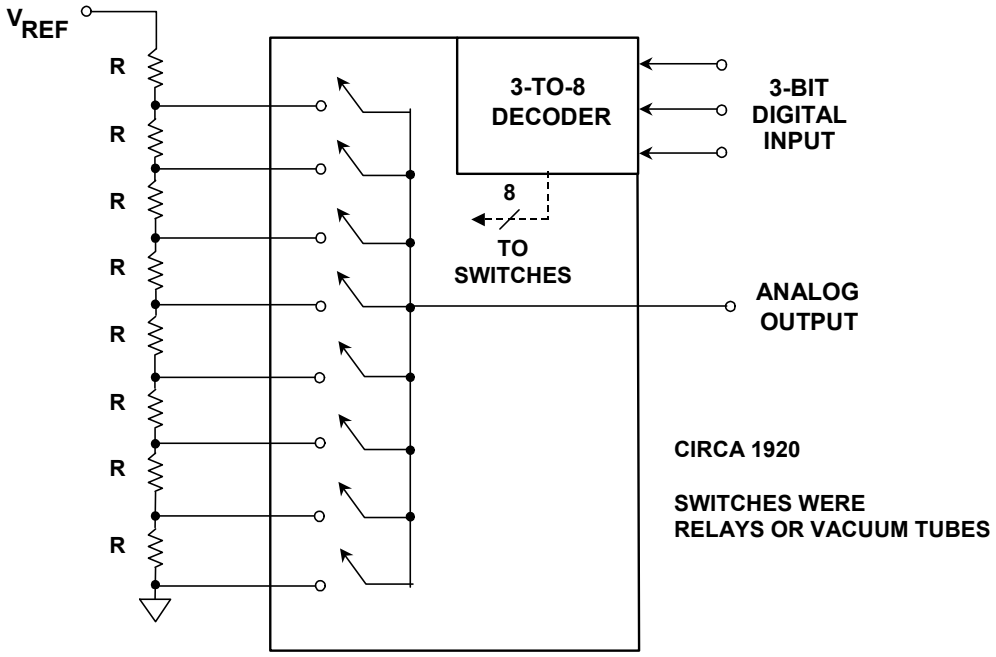


Figure 6.2: *Simplest Voltage-Output Thermometer DAC: The Kelvin Divider*

As we mentioned in the section on sampling theory, the output of a DAC for an all 1s code is 1 LSB below the reference, so a Kelvin divider DAC intended for use as a general-purpose DAC has a resistor between the reference terminal and the first switch as shown in Figure 6.2.

Segmented String DACs

A variation of the Kelvin divider is the segmented string DAC. Here we reduce the number of resistors required by segmenting. Figure 6.3 shows two varieties of segmented voltage-output DAC. The architecture in Figure 6.3A is sometimes called a Kelvin-Varley Divider. Since there are buffers between the first and second stages, the second string DAC does not load the first, and the resistors in the second string do not need to have the same value as the resistors in the first. All the resistors in each string, however, do need to be equal to each other or the DAC will not be linear. The examples shown have 3-bit first and second stages but for the sake of generality, let us refer to the first (MSB) stage resolution as M-bits and the second (LSB) as K-bits for a total of $N = M + K$ bits. The MSB DAC has a string of 2^M equal resistors and a string of 2^K equal resistors in the LSB DAC. As an example, if we make a 10-bit string DAC out of two 5-bit sections, each segment would have 2^5 or 32 resistors, for a total of 64, as opposed to the 1024 required for a standard Kelvin divider. This is an obvious advantage.

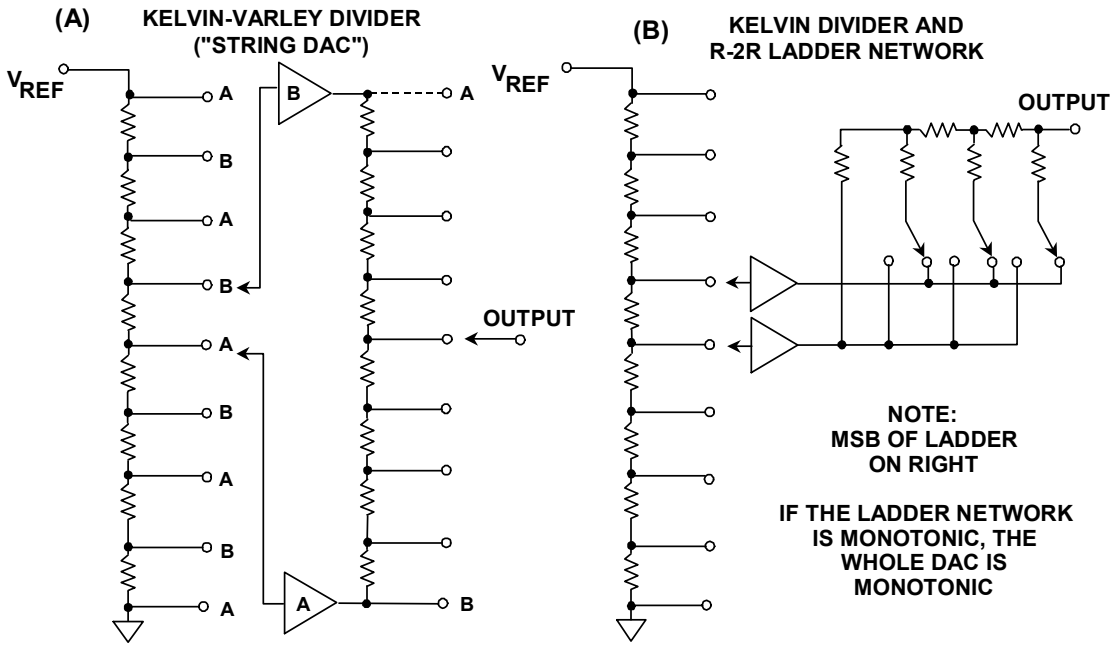


Figure 6.3: *Segmented Voltage-Output DACs*

Buffer amplifiers can have offset, of course, and this can cause nonmonotonicity in a buffered segmented string DAC.

In the simpler configuration of a buffered Kelvin-Varley divider buffer (Figure 6.3A), buffer A is always "below" (at a lower potential than) buffer B, and the extra tap labeled "A" on the LSB string DAC is not necessary. The data decoding is just two priority encoders.

But if the decoding of the MSB string DAC is made more complex so that buffer A can only be connected to the taps labeled "A" in the MSB string DAC, and buffer B to the taps labeled "B," then it is not possible for buffer offsets to cause nonmonotonicity. Of course, the LSB string DAC decoding must change direction each time one buffer "leapfrogs" the other, and taps A and B on the LSB string DAC are alternately not used—but this involves a fairly trivial increase in logic complexity and is justified by the increased performance.

Rather than using a second string of resistors, a binary R-2R DAC can be used to generate the three LSBs as shown in Figure 6.3B. This voltage-output DAC (Figure 6.3B) consists of a 3-bit string DAC followed by a 3-bit buffered voltage-mode ladder network. Again the number of resistors require for the DAC is reduced.

An unbuffered version of the segmented string DAC is shown in Figure 6.4. This version is more clever in concept. Here, the resistors in the two strings must be equal, except that the top resistor in the MSB string must be smaller—$1/2^K$ of the value of the others—and the LSB string has $2^K - 1$ resistors rather than 2^K. Because there are no buffers, the LSB string appears in parallel with the resistor in the MSB string that it is switched across and loads it. This drops the voltage across that MSB resistor by 1 LSB of the LSB DAC—which is exactly what is required. The output impedance of this DAC, being unbuffered,

varies with changing digital code. This circuit is intrinsically monotonic since it is unbuffered (and, of course, can be manufactured on CMOS processes which make resistors and switches but not high precision amplifiers, so it may be cheaper as well).

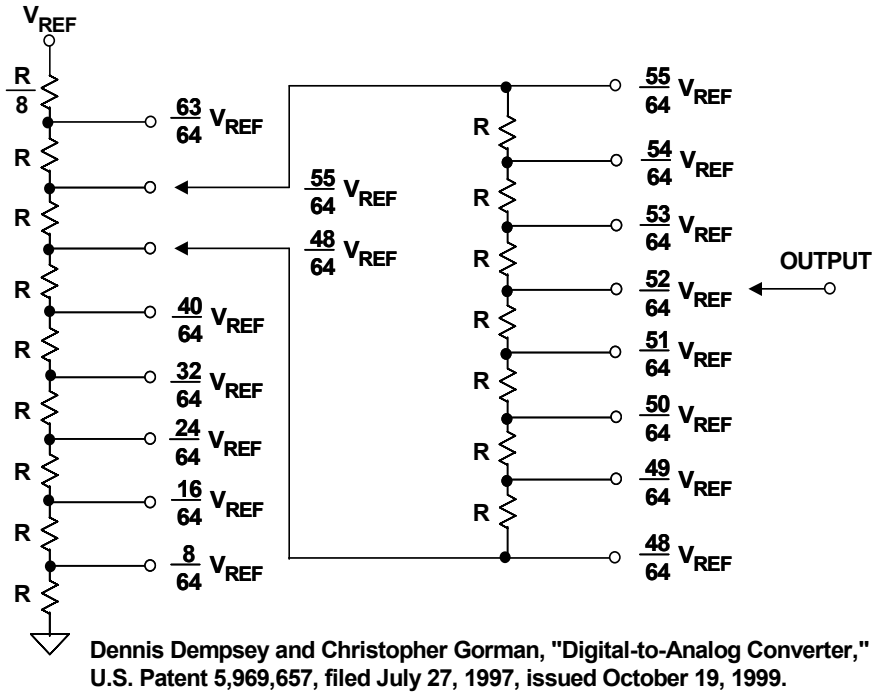


Figure 6.4: *Segmented Unbuffered String DACs Use Patented Architecture*

In order to understand this clever concept better, the actual voltages at each of the taps has been worked out and labeled for the 6-bit segmented DAC composed of two 3-bit string DACs shown in Figure 6.4. The reader is urged to go through this simple analysis with the second string DAC connected across any other resistor in the first string DAC and verify the numbers. A detailed mathematical analysis of the unbuffered segmented string DAC can be found in the relevant patent filed by Dennis Dempsey and Christopher Gorman of Analog Devices in 1997 (Reference 14).

Digital Potentiometers

Another variation of the string DAC is the digital potentiometer. A simple digital potentiometer is shown in Figure 6.5.

The major difference is that the lower arm of the potentiometer (terminal B) is not connected to ground, but is instead left floating. The absolute values of the resistors in a Kelvin DAC typically are not critical. They are limited by the available material. They must, of course, be the same as each other. In a digital potentiometer the end-to-end resistance is specified. The accuracy of the end to end resistance is on the order of a

mechanical potentiometer. Digital potentiometers are typically available in end-to-end resistance values from 10 kΩ to 1 MΩ. Lower values of end-to-end resistance are difficult since the on resistance of the CMOS switches is on the order of the resistor segment, so the linearity of the pot suffers at the low end.

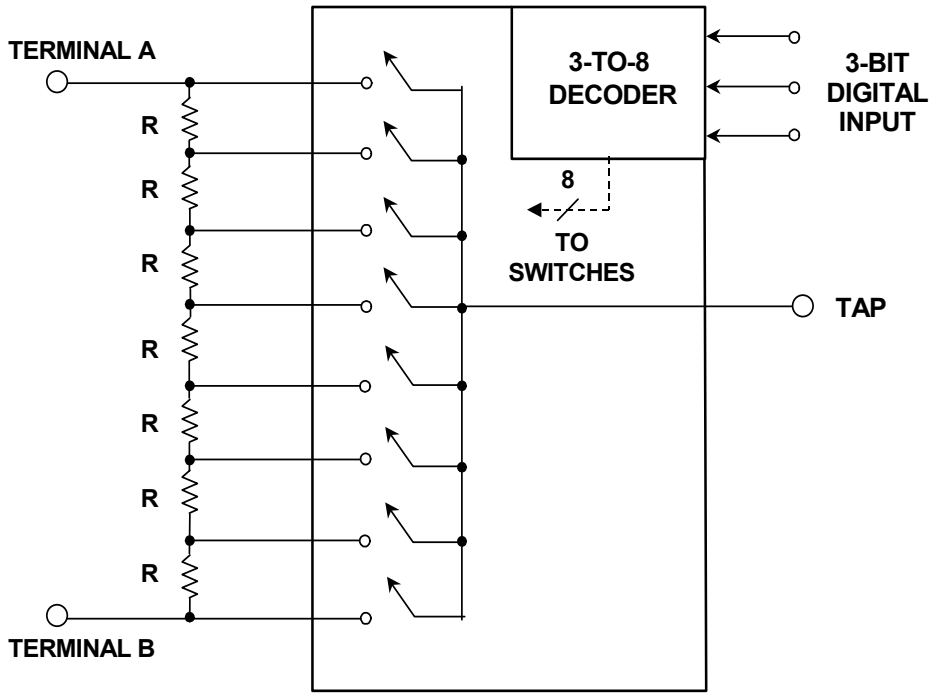


Figure 6.5: *A Slight Modification to a Kelvin DAC Yields a "Digital Potentiometer"*

The advantages to digital potentiometers are many. Even the lowest resolution digital potentiometers have better setability than their mechanical counterparts. Also, they are immune to mechanical vibration and oxidation of the wiper contact. Obviously, adjustments can be made without human intervention.

In most digital potentiometers the voltage on the input pins can not exceed the supplies (typically 3 V or 5 V) due to the CMOS switches used in their construction, but certain models are designed for ±15 V operation.

Another design feature on many of the digital potentiometers is that on power up (sometimes from an internal timer, sometimes controlled by an external pin) the wiper is shorted to one of the terminals. This is useful since output on power up is undefined until it is written to. Since it might take a while (relatively) for the micro-controller to initialize itself and then get around to initializing the rest of the system, having the digital potentiometer in a known state can be useful. Some digital potentiometers incorporate nonvolatile logic so that their settings are retained when they are turned off.

One time programmable (OTP) versions of digital potentiometers have become available. Here the digital code is locked into the potentiometer once the setting had been determined. The technology used is fuseable links. A variation on this theme is the two

times programeable (TTP) digital potentiometer. This allows the nonvolatile settings to be modified one time. The block diagram of a TTP digital potentiometer is shown in Figure 6.6.

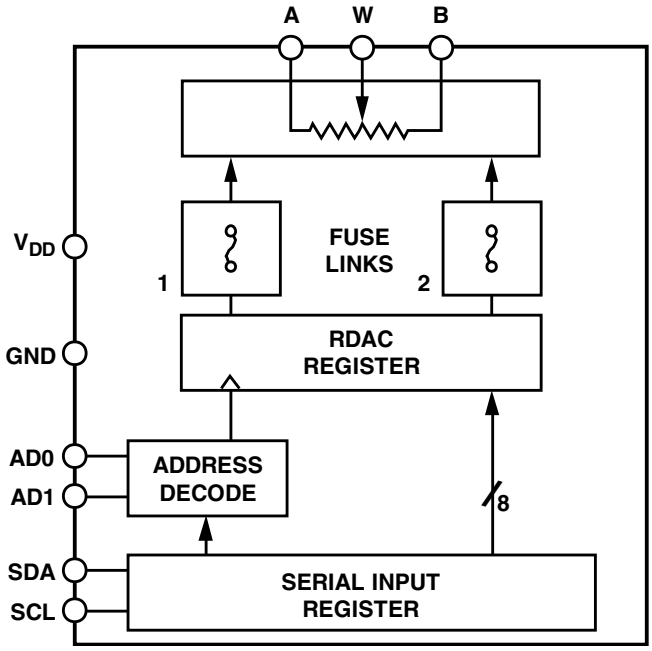


Figure 6.6: *Two Times Programmable (TTP) Digital Potentiometer Block Diagram*

Thermometer (Fully Decoded) DACs

There is a current-output DAC architecture analogous to a string DAC which consists of $2^N - 1$ switchable current sources (which may be resistors and a voltage reference or may be active current sources) connected to an output terminal. This output must be at, or close to, ground. Figure 6.7 shows a thermometer DAC which use resistors connected to a reference voltage to generate the currents.

If active current sources are used as shown in Figure 6.8, the output may have more compliance (the allowable voltage on the output pin which still guarantees performance), and a resistive load is typically used to develop an output voltage. The load resistor must be chosen so that at maximum output current the output terminal remains within its rated compliance voltage

Once a current in a thermometer DAC is switched into the circuit by increasing the digital code, any further increases do not switch it out again. The structure is thus inherently monotonic, irrespective of inaccuracies in the currents. Again, like the Kelvin divider, only the advent of high density IC processes has made this architecture practical for general purpose medium resolution DACs, although a slightly more complex version—shown in the next diagram—is quite widely used in high speed applications. Unlike the Kelvin divider, this type of current-mode DAC does not have a unique name, although both types may be referred to as *fully decoded* DACs or *thermometer* DACs.

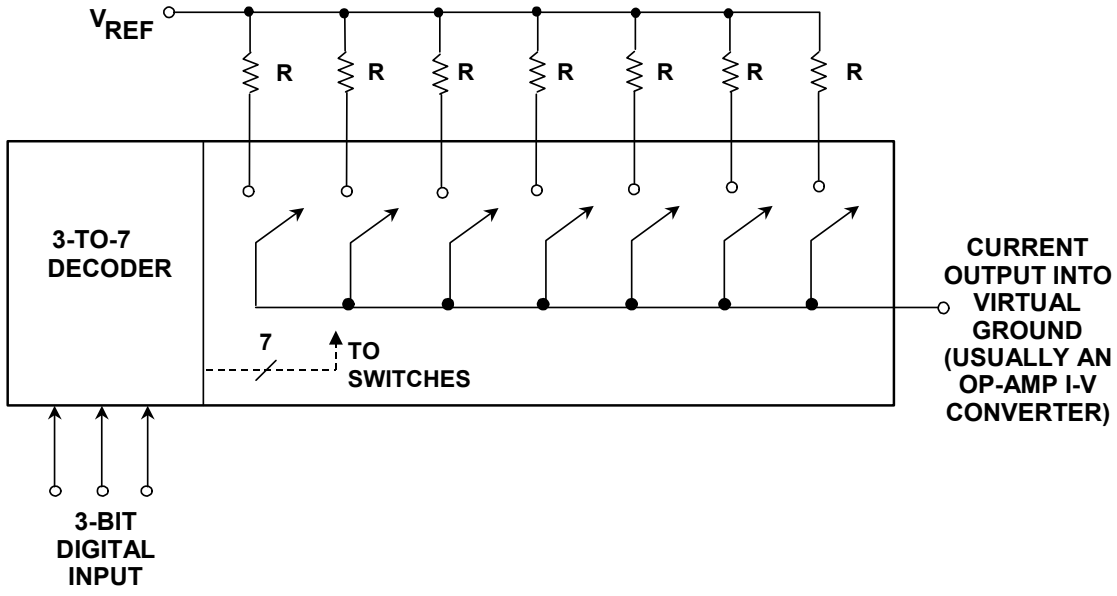


Figure 6.7: *The Simplest Current-Output Thermometer (Fully Decoded) DAC*

A DAC where the currents are switched between two output lines—one of which is often grounded, but may, in the more general case, be used as the inverted output—is more suitable for high speed applications because switching a current between two outputs is far less disruptive, and so causes a far lower glitch than simply switching a current on and off. This architecture is shown in Figure 6.9.

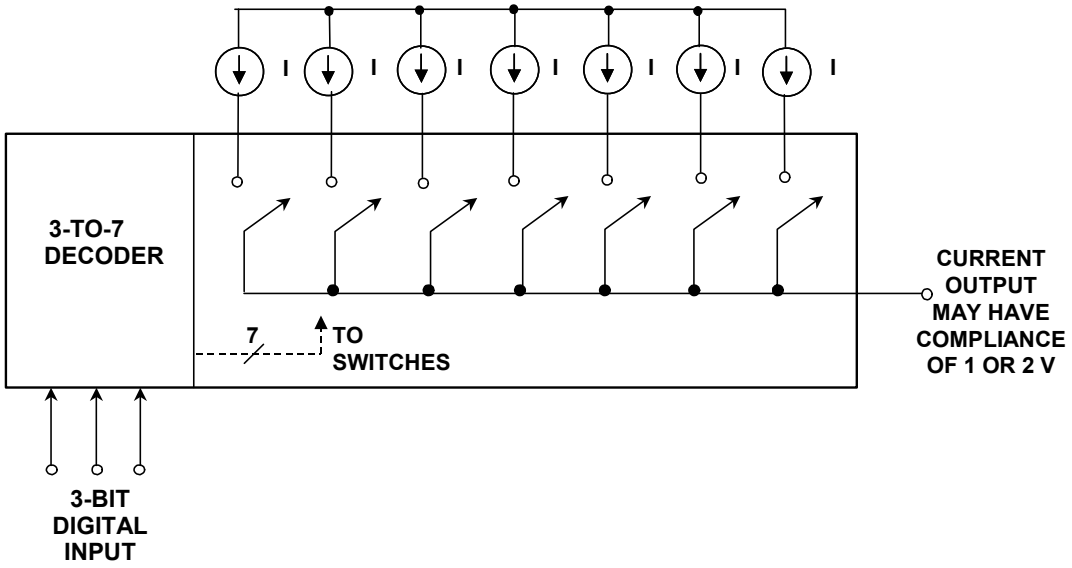


Figure 6.8: *Current Sources Improve the Basic Current-Output Thermometer DAC*

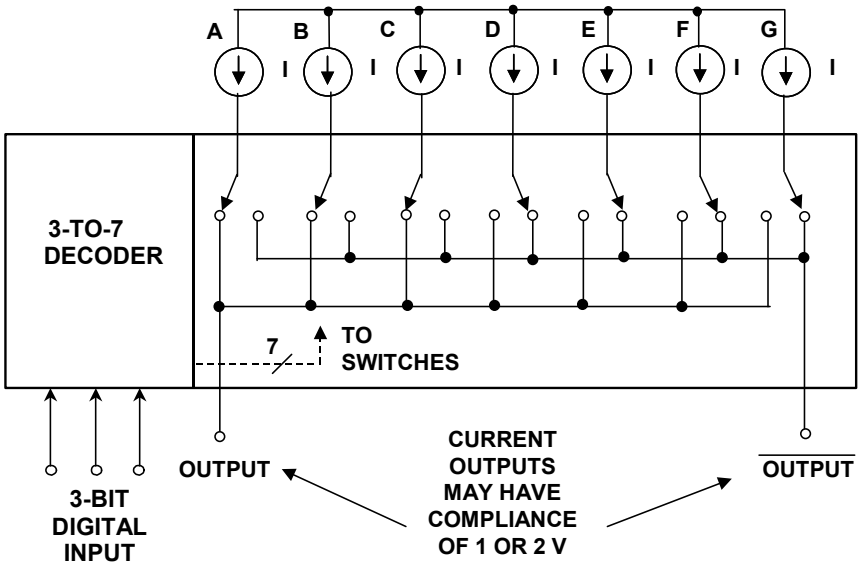


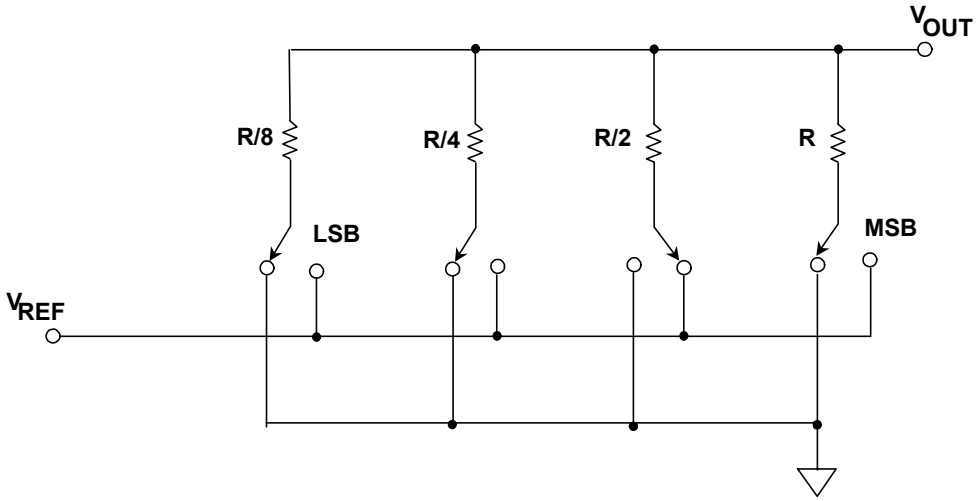
Figure 6.9: *High Speed Thermometer DAC with Complementary Current Outputs*

But the settling time of this DAC still varies with initial and final code, giving rise to *intersymbol distortion* (ISI). This can be addressed with even more complex switching where the output current is returned to zero before going to its next value. Note that although the current in the output is returned to zero it is not "turned off"—the current is dumped to ground when it is not being used, rather than being switched on and off. The techniques involved are too complex to discuss in detail here but can be found in the references.

In the normal (linear) version of this DAC, all the currents are nominally equal. Where it is used for high speed reconstruction, its linearity can also be improved by dynamically changing the order in which the currents are switched by ascending code. Instead of code 001 always turning on current A; code 010 always turning on currents A and B, code 011 always turning on currents A, B, and C; etc. the order of turn-on relative to ascending code changes for each new data point. This can be done quite easily with a little extra logic in the decoder. The simplest way of achieving it is with a counter which increments with each clock cycle so that the order advances: ABCDEFG, BCDEFGA, CDEFGAB, etc., but this algorithm may give rise to spurious tones in the DAC output. A better approach is to set a new pseudo-random order on each clock cycle—this requires a little more logic, but even complex logic is now very cheap and easily implemented on CMOS processes. There are other, even more complex, techniques which involve using the data itself to select bits and thus turn current mismatch into shaped noise. Again they are too complex for a book of this sort. (See references for a more detailed discussion).

Binary Weighted Current Source

The voltage-mode binary-weighted resistor DAC shown in Figure 6.10 is usually the simplest textbook example of a DAC. However, this DAC is not inherently monotonic and is actually quite hard to manufacture successfully at high resolutions due to the large spread in component (resistor) values. In addition, the output impedance of the voltage-mode binary DAC changes with the input code.



Adapted from: B. D. Smith, "Coding by Feedback Methods," Proceedings of the I. R. E., Vol. 41, August 1953, pp. 1053-1058

Figure 6.10: *Voltage-Mode Binary-Weighted Resistor DAC*

Current-mode binary weighted DACs are shown in Figure 6.11A (resistor-based), and Figure 6.11B (current-source based). An N-bit DAC of this type consists of N weighted current sources (which may simply be resistors and a voltage reference) in the ratio 1:2:4:8:....:2^{N-1}. The LSB switches the 2^{N-1} current, the MSB the 1 current, etc. The theory is simple but the practical problems of manufacturing an IC of an economical size with current or resistor ratios of even 128:1 for an 8-bit DAC are enormous, especially as they must have matched temperature coefficients. This architecture is virtually never used on its own in integrated circuit DACs, although, again, 3-bit or 4-bit versions have been used as components in more complex structures. For example, the AD550 mentioned at the beginning of this section is an example of a binary-weighted DAC.

If the MSB current is slightly low in value, it will be less than the sum of all the other bit currents, and the DAC will not be monotonic (the differential nonlinearity of most types of DAC is worst at major bit transitions).

However, there is another binary-weighted DAC structure which has recently become widely used. This uses binary-weighted capacitors as shown in Figure 6.12. The problem with a DAC using capacitors is that leakage causes it to lose its accuracy within a few milliseconds of being set. This may make capacitive DACs unsuitable for general-purpose DAC applications, but it is not a problem in successive approximation ADCs,

since the conversion is complete in a few μs or less—long before leakage has any appreciable effect.

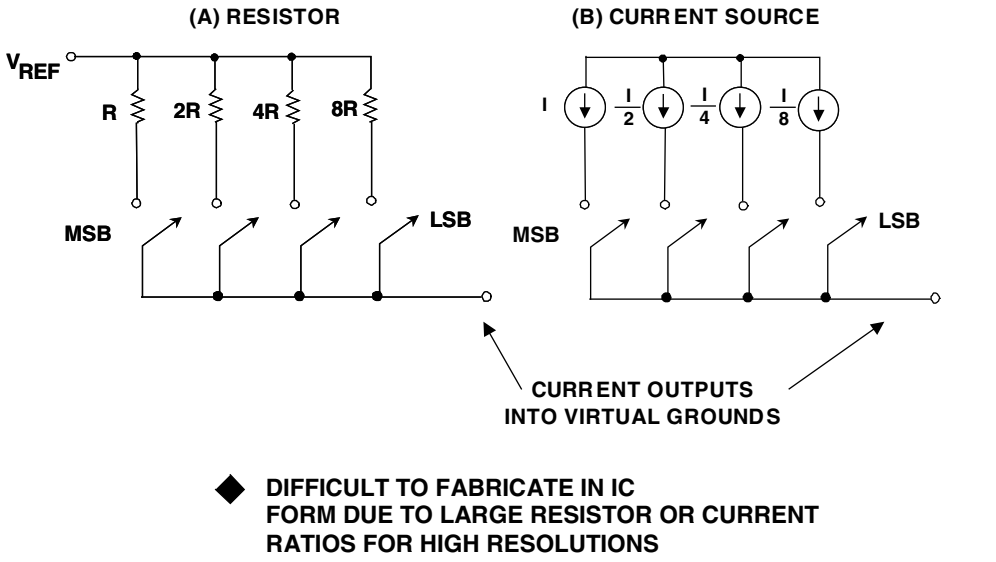


Figure 6.11: *Current-Mode Binary-Weighted DACs*

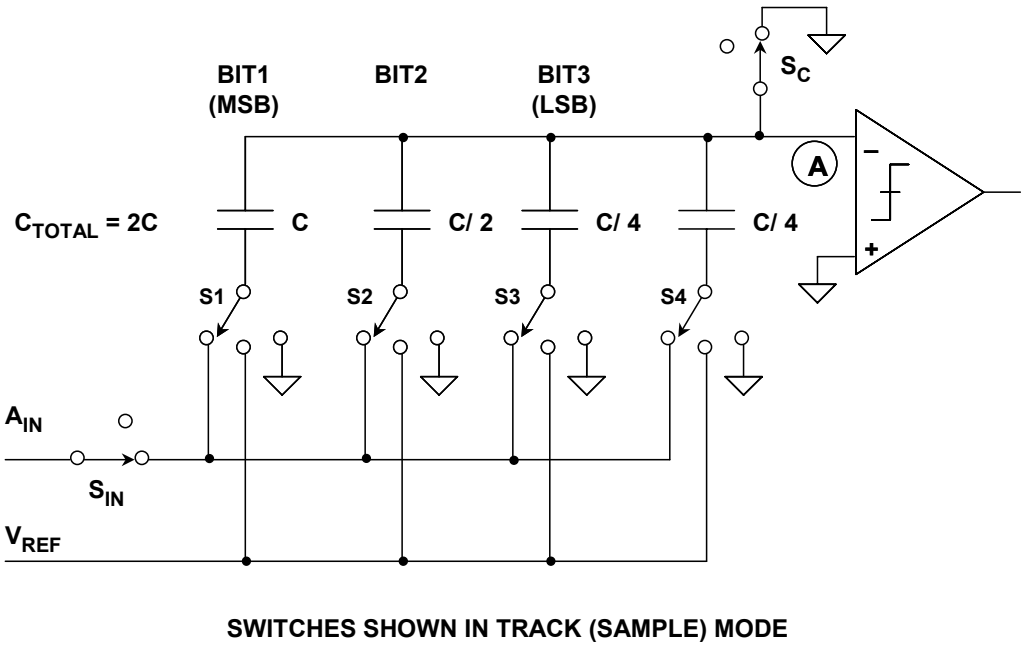


Figure 6.12: *Capacitive Binary-Weighted DAC in Successive Approximation ADC*

The use of capacitive charge redistribution DACs offers another advantage as well—the DAC itself behaves as a sample-and-hold circuit (SHA), so not only is an external SHA

unnecessary with these ADCs, there is no need to allocate separate chip area for a separate integral SHA.

R-2R Ladder

One of the most common DAC building-block structures is the R-2R resistor ladder network shown in Figure 3.15. It uses resistors of only two different values, and their ratio is 2:1. An N-bit DAC requires 2N resistors, and they are quite easily trimmed. There are also relatively few resistors to trim.

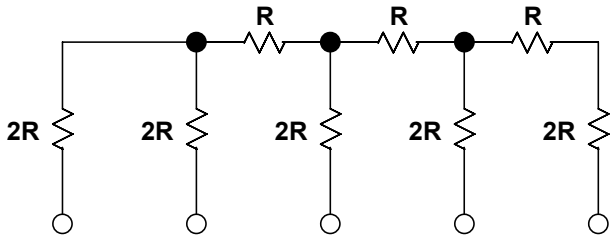


Figure 6.13: *4-Bit R-2R Ladder Network*

This structure is the basis of a large family of DACs. Figure 6.14 is the block diagram of the AD7524, which is typical of a basic current output CMOS DAC. The diagram shows the structure of the DAC.

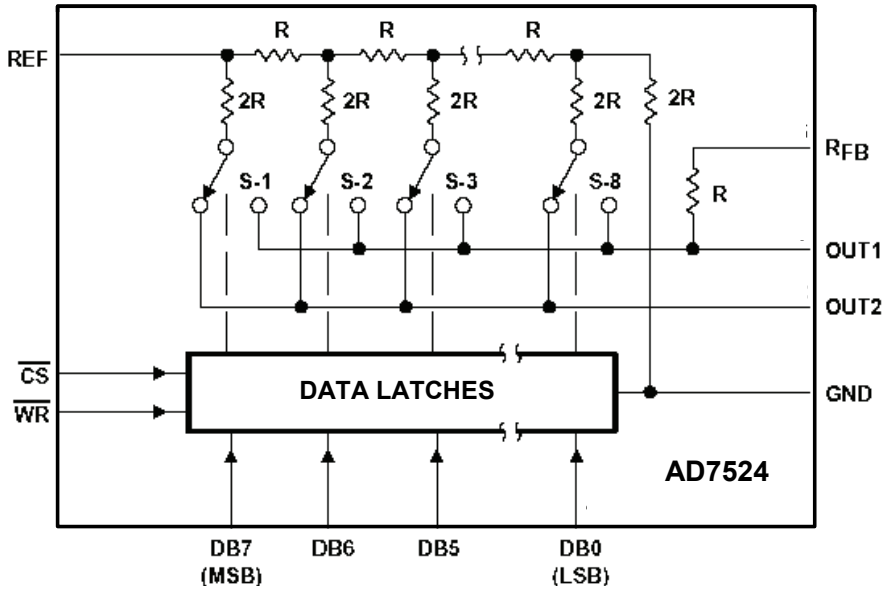


Figure 6.14: *AD7524 CMOS DAC Block Diagram*

The input impedance (basically the value of the resistors) is not a closely specified parameter. The specified range is 4:1 (5 kΩ min, 20 kΩ max, although it is typically closer than that). It is the relative accuracy, not the absolute accuracy of the resistors that is of interest. In most applications the absolute value is not important. Certain applications exist where the value does matter. In these instances, the parts must be selected at test.

Note the extra resistor added at the $R_{FEEDBACK}$ pin. This is designed to be the feedback resistor for the I/V op amp. This resistor is trimmed along with the rest of the resistors so it tracks. Also, since it is made of the same material as the rest of the resistors, therefore having the same temperature coefficient, and is on the same substrate, hence at the same temperature, it will track over temperature.

Figure 6.15 shows a more modern example of a CMOS DAC, the AD7394. Several trends are obvious here. First off, the output is voltage, not current. Advancements in process technology have allowed reasonable quality CMOS op amps to be created. Also note the two ranks of latches. The purpose of these latches is to allow the micro-controller to write to all converters in a system and then update them all at the same time. This will be covered on more detail in a later section. Note also the power on reset circuit. Since the wake up state of a CMOS DAC is undefined and not repeatable, many modern DACs include a circuit to force the output to either half scale of minimum scale, depending on whether the intended application is unipolar or bipolar. Probably the most obvious difference is that this is a multiple DAC package. Shrinking device geometries have allowed more circuitry to be included, even with the smaller packages in use today.

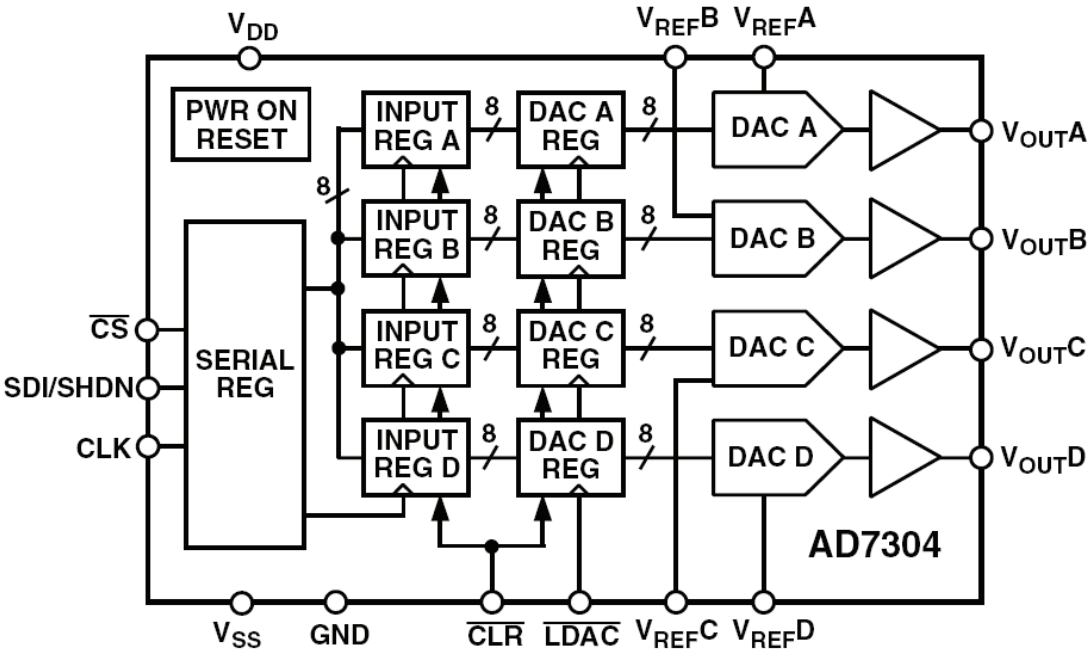


Figure 6.15: *AD7394 Quad CMOS DAC Block Diagram*

The previous examples were CMOS devices, that is to say, that the switches were implemented with CMOS switches. The switches could also be implemented with bipolar transistors (BJT). An example of this is the classic DAC-08. Its block diagram is shown in Figure 6.16. One major difference in the BJT implementation is that the switch allows current in one direction, versus the CMOS switch, which can allow bidirectional current. This limits the BJT DAC to 2-quadrant operation while the CMOS version can be 4-quadrant. Supplies tend to be different as well.

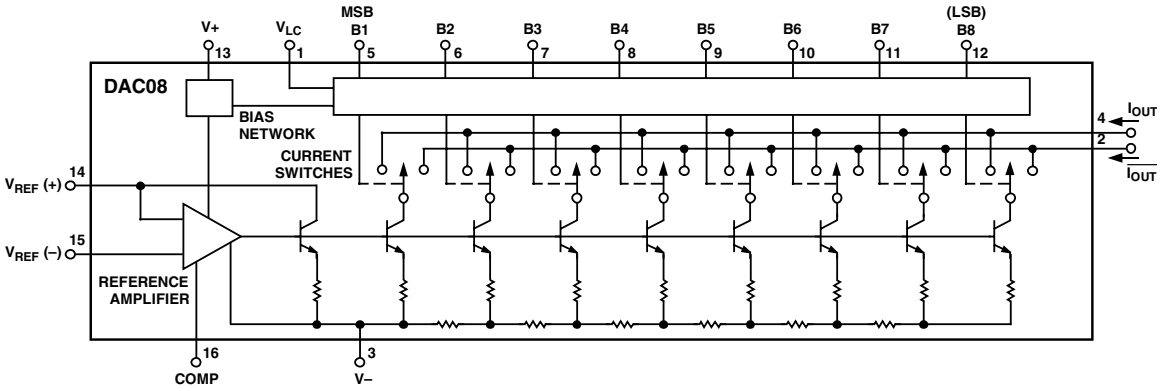


Figure 6.16: *DAC-08 Block Diagram*

There are two ways in which the R-2R ladder network may be used as a DAC—known respectively as the *voltage mode* and the *current mode* (they are sometimes called "normal" mode and "inverted" mode, but as there is no consensus on whether the voltage mode or the current mode is the "normal" mode for a ladder network this nomenclature can be misleading, although in most cases the current mode would be considered the "normal" mode). Each mode has its advantages and disadvantages.

In the current-mode R-2R ladder DAC shown in Figure 6.17, the gain of the DAC may be adjusted with a series resistor at the V_{REF} terminal, since in the current mode, the end of the ladder, with its code-independent impedance, is used as the V_{REF} terminal; and the ends of the arms are switched between ground and an output line which must be held at ground potential. The normal connection of a current-mode ladder network output is to an op amp's inverting input (virtual ground), but stabilization of this op amp is complicated by the DAC output impedance variation with digital code.

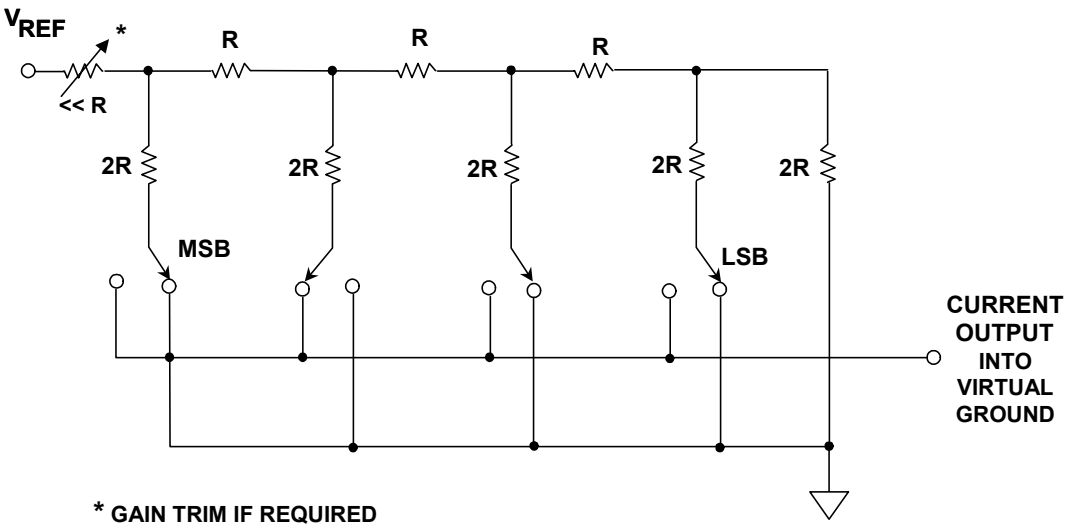


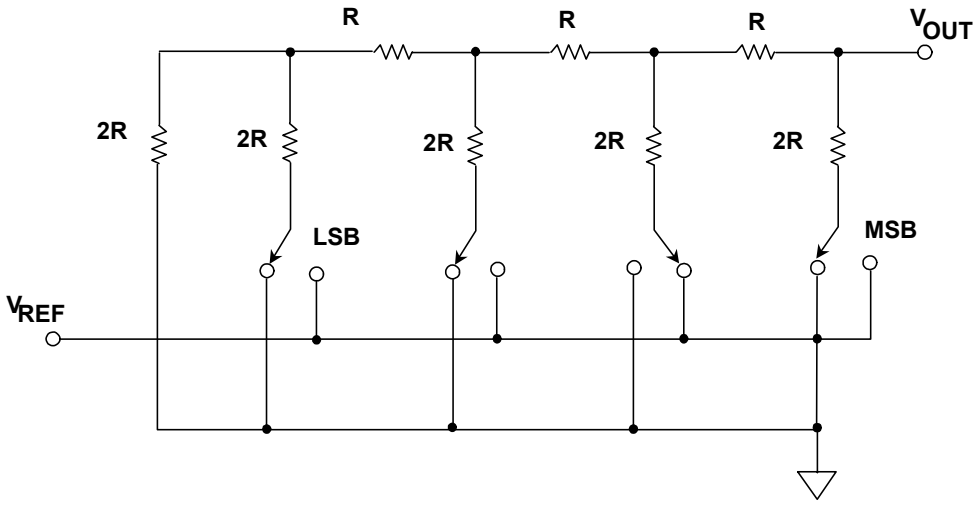
Figure 6.17: *Current-Mode R-2R Ladder Network DAC*

Current-mode operation has a larger switching glitch than voltage mode since the switches connect directly to the output line(s). However, since the switches of a current-mode ladder network are always at ground potential, their design is less demanding and, in particular, their voltage rating does not affect the reference voltage rating. If switches capable of carrying current in either direction (such as CMOS devices) are used, the reference voltage may have either polarity, or may even be ac. Such a structure is one of the most common types used as a multiplying DAC (MDAC) which will be discussed later in this section.

Since the switches are always at, or very close to, ground potential, the maximum reference voltage may greatly exceed the logic voltage, provided the switches are make-before-break—which they are in this type of DAC. It is not unknown for a CMOS MDAC to accept a ±30 V reference (or even a 60-V peak-to-peak ac reference) while working from a single 5 V supply.

In the voltage mode R-2R ladder DAC shown in Figure 6.18, the "rungs" or arms of the ladder are switched between V_{REF} and ground, and the output is taken from the end of the ladder. The output may be taken as a voltage, but the output impedance is independent of code, so it may equally well be taken as a current into a virtual ground.

The voltage output is an advantage of this mode, as is the constant output impedance, which eases the stabilization of any amplifier connected to the output node. Additionally, the switches switch the arms of the ladder between a low impedance V_{REF} connection and ground, which is also, of course, low impedance, so capacitive glitch currents tend not to flow in the load. On the other hand, the switches must operate over a wide voltage range (V_{REF} to ground), which is difficult from a design and manufacturing viewpoint, and the reference input impedance varies widely with code, so that the reference input must be driven from a very low impedance. In addition, the gain of the DAC cannot be adjusted by means of a resistor in series with the V_{REF} terminal.



Adapted from: B. D. Smith, "Coding by Feedback Methods," Proceedings of the I. R. E., Vol. 41, August 1953, pp. 1053-1058

Figure 6.18: *Voltage-Mode R-2R Ladder Network DAC*

Probably the most important advantage to the voltage mode is that it allows single-supply operation. This is because the op amp that is commonly used as I/V converter in the current mode converter is in the inverting configuration so would require a negative output for a positive input, assuming ground reference. Of course you could bias everything up to a rail-splitter ground, but that introduces other issues into the system.

Multiplying DACs (MDACs)

In most cases the reference to a DAC is a highly stable dc voltage. In some instances, however, it is useful to have a variable reference. The R-2R ladder structure using CMOS switches can easily handle a bipolar signal on its input. Having the ability to have bipolar (positive and negative) signals on the input allows construction of 2-quadrant and 4-quadrant Multiplying DACs. Figure 6.19 shows the schematic and Table I outlines the operation of a 2-quadrant MDAC and Figure 6.20 shows the schematic and Table II outlines the operation of a 4-quadrant MDAC for an 8-bit DAC.

DACs utilizing bipolar transistors as switches, such as the DAC-08 above, cannot accommodate bipolar signals on the reference. Therefore they can only implement 2-quadrant MDACs. In addition, the reference voltage can not go all the way to 0 V. The maximum allowable range is typically from 10% to 100% of the allowable reference voltage range.

One of the main applications of the MDAC is as a variable gain amplifier, where the gain is controlled by the digital word applied to the MDAC.

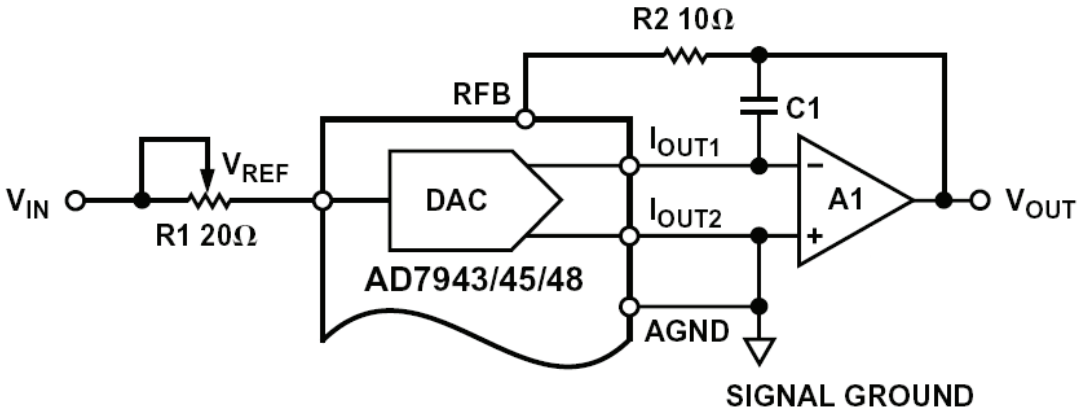


Figure 6.19: *2-Quadrant Multiplying DAC*

Table I. Unipolar Binary Code Table

Digital Input MSB LSB	Analog Output
1111 1111	$-V_{REF}$ (255/256)
1000 0001	$-V_{REF}$ (129/256)
1000 0000	$-V_{REF}$ (128/256) = $-V_{REF}/2$
0111 1111	$-V_{REF}$ (127/256)
0000 0001	$-V_{REF}$ (1/256)
0000 0000	$-V_{REF}$ (0/256) = 0

Note: 1 LSB = $(2^{-8})(V_{REF})$ = 1/256 (V_{REF})

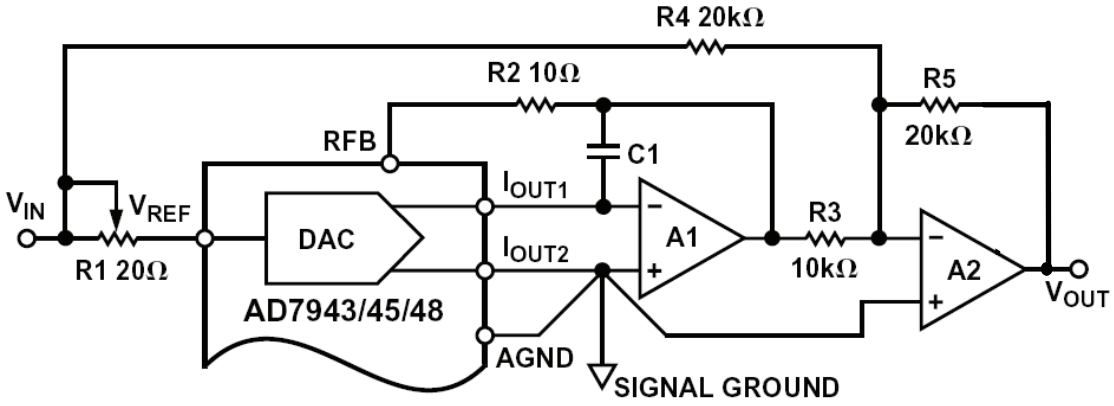


Figure 6.20: *4-Quadrant Multiplying DAC*

Table II. Bipolar (Offset Binary) Code Table

Digital Input MSB LSB	Analog Output
1111 1111	$+V_{REF}$ (127/128)
1000 0001	$+V_{REF}$ (1/128)
1000 0000	0
0111 1111	$-V_{REF}$ (1/128)
0000 0001	$-V_{REF}$ (127/128)
0000 0000	$-V_{REF}$ (128/128)

Note: 1 LSB = $(2^{-7})(V_{REF})$ = 1/128 (V_{REF})

The frequency response of the MDAC is limited by the parasitic capacitance across the switches in the off condition. As the frequency goes up the impedance of the capacitors goes down, effectively bypassing the switch. This reduces the off isolation at higher frequencies. Typically the frequency response of an MDAC will be on the order of 1 MHz.

Segmented DACs

So far we have considered mostly basic DAC architectures. When we are required to design a DAC with a specific performance, it may well be that no single architecture is ideal. In such cases, two or more DACs may be combined in a single higher resolution DAC to give the required performance. These DACs may be of the same type or of different types and need not each have the same resolution. For example, the segmented string DAC is a segmented DAC where 2 Kelvin DACs are cascaded.

Typically, one DAC handles the MSBs, another handles the LSBs, and their outputs are added in some way. The process is known as "segmentation," and these more complex structures are called "segmented DACs." There are many different types of segmented DACs and some, but by no means all, will be illustrated in the next few diagrams. It is sometimes not obvious from looking at the data sheet that a particular DAC is segmented.

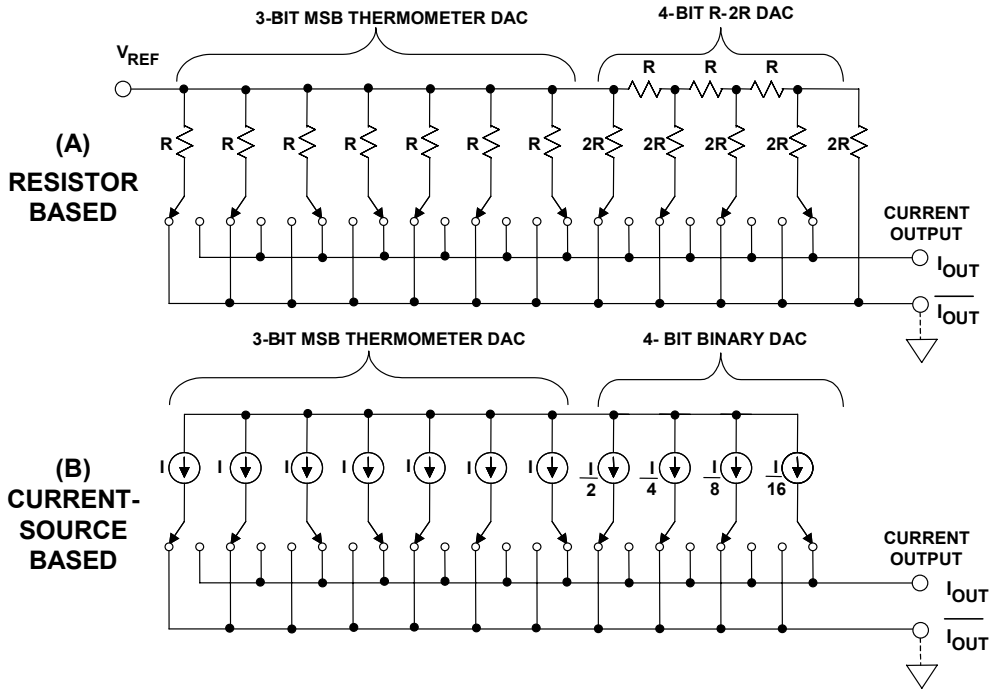


Figure 6.21: *Segmented Current-Output DACs: (A) Resistor-Based, (B) Current-Source Based*

Very high speed DACs for video, communications, and other HF reconstruction applications are often built with arrays of fully decoded current sources. The two or three

LSBs may use binary-weighted current sources. It is extremely important that such DACs have low distortion at high frequency, and there are several important issues to be considered in their design.

Two examples of segmented current-output DAC structures are shown in Figure 6.21. Figure 6.21A shows a resistor-based approach for the 7-bit DAC where the 3 MSBs are fully decoded, and the 4 LSBs are derived from an R-2R network. Figure 6.21B shows a similar implementation using current sources. The current source implementation is by far the most popular for today's high-speed reconstruction DACs.

It is also often desirable to utilize more than one fully decoded thermometer section to make up the total DAC. Figure 6.22 shows a 6-bit DAC constructed from two fully decoded 3-bit DACs. As previously discussed, these current switches must be driven simultaneously from parallel latches in order to minimize the output glitch.

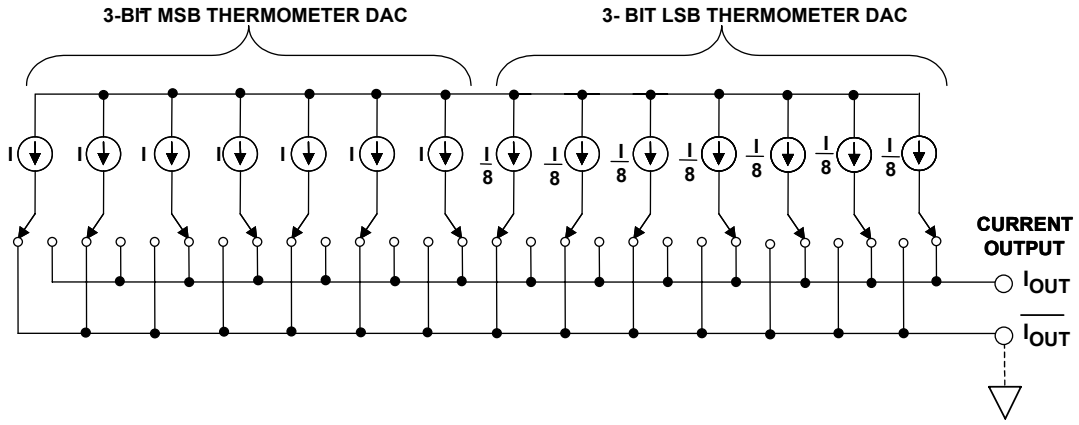


Figure 6.22: *6-Bit Current-Output Segmented DAC Based on Two 3-Bit Thermometer DACs*

The AD9775 14-bit, 160-MSPS (input)/400-MSPS (output) TxDAC™ uses three sections of segmentation as shown in Figure 6.23. Other members of the AD977x-family and the AD985x-family also use this same basic core.

The first 5 bits (MSBs) are fully decoded and drive 31 equally weighted current switches, each supplying 512 LSBs of current. The next 4 bits are decoded into 15 lines which drive 15 current switches, each supplying 32 LSBs of current. The 5 LSBs are latched and drive a traditional binary-weighted DAC which supplies 1 LSB per output level. A total of 51 current switches and latches are required to implement this ultra low glitch architecture.

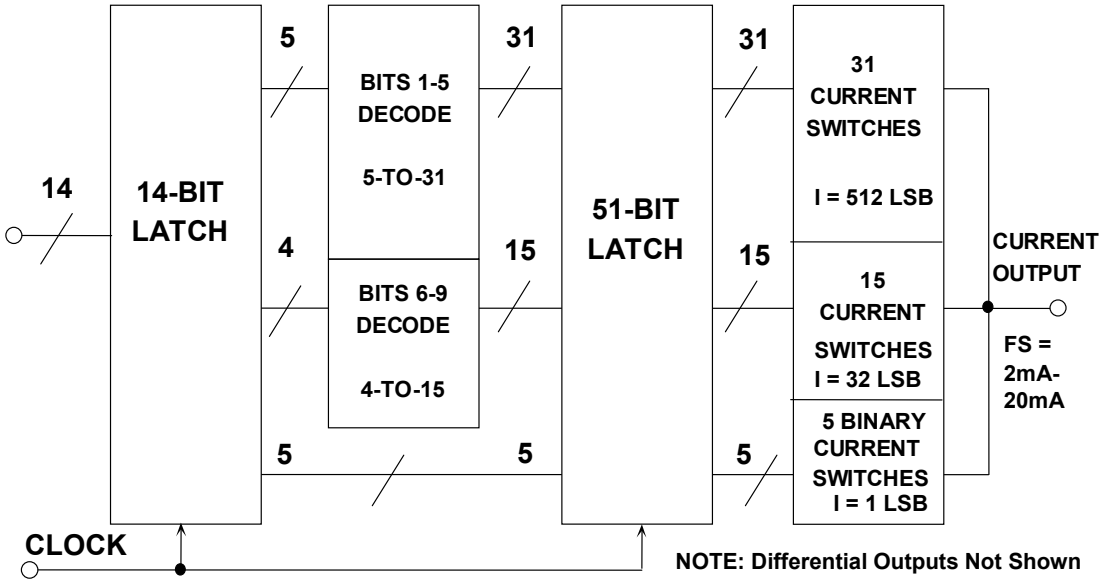


Figure 6.23: *AD9775 TxDAC 14-Bit CMOS DAC Core*

Decoding must be done before the new data is applied to the DAC so that all the data is ready and can be applied simultaneously to all the switches in the DAC. This is generally implemented by using a separate parallel latch for the individual switches in fully decoded array. If all switches were to change state instantaneously and simultaneously there would be no skew glitch—by very careful design of propagation delays around the chip and time constants of switch resistance and stray capacitance the update synchronization can be made very good, and hence the glitch-related distortion is very small.

Sigma-Delta DACs

Sigma-Delta DACs will be discussed in detail in the Sigma-Delta section.

I/V Converters

Modern IC DACs provide either voltage or current outputs. Figure 6.24 below shows three fundamental configurations, all with the objective of using an op amp for a buffered output voltage.

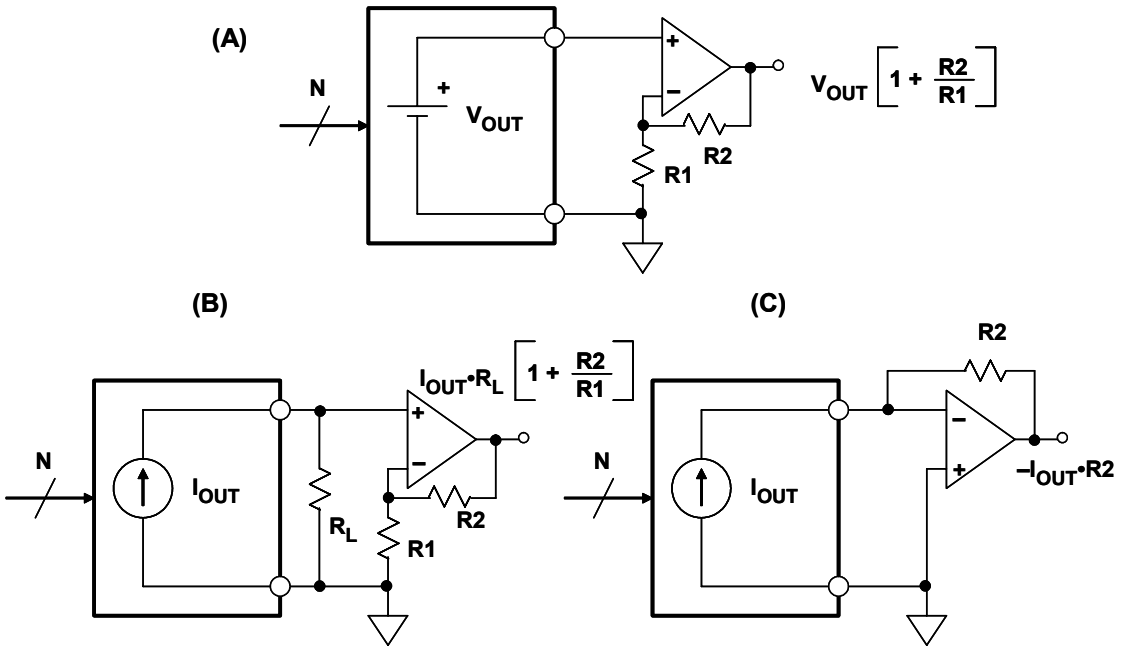


Figure 6.24: *Buffering DAC Outputs with Op Amps*

Figure 6.24A shows a buffered voltage output DAC. In many cases, the DAC output can be used directly, without additional buffering. If an additional op amp is needed, it is usually configured in a noninverting mode, with gain determined by R1 and R2.

There are two basic methods for dealing with a current output DAC.

A direct method to convert the output current into a voltage is shown in Figure 6.24C. This circuit is usually called a current-to-voltage converter, or I/V. In this circuit, the DAC output drives the inverting input of an op amp, with the output voltage developed across the R2 feedback resistor. In this approach the DAC output always operates at virtual ground (which may give a linearity improvement vis-à-vis Fig. 6.24B).

In Figure 6.24B, a voltage is simply developed across external load resistor, RL. This is typically done with high speed op amps. An external op amp can be used to buffer and/or amplify this voltage if required. The output current is dumped into a resistor instead of into an op amp directly since the fast edges may exceed the slew rate of the amplifier and cause distortion. Many DACs supply full-scale currents of 20 mA or more, thereby allowing reasonable voltages to be developed across fairly low value load resistors. For instance, fast settling video DACs typically supply nearly 30 mA full-scale current,

allowing 1 V to be developed across a source and load terminated 75 Ω coaxial cable (representing a dc load of 37.5 Ω to the DAC output).

The general selection process for an op amp used as a DAC buffer is that the performance of the op amp should not compromise the performance of the DAC. The basic specifications of interest are DC accuracy, noise, settling time, bandwidth, distortion, etc.

Differential to Single-Ended Conversion Techniques

A general model of a modern current output DAC is shown in Figure 6.25. This model is typical of the AD976X and AD977X TxDAC series (see Reference 1).

Current output is more popular than voltage output, especially at audio frequencies and above. If the DAC is fabricated on a bipolar or BiCMOS process, it is likely that the output will sink current, and that the output impedance will be less than 500 Ω (due to the internal R/2R resistive ladder network). On the other hand, a CMOS DAC is more likely to source output current and have a high output impedance, typically greater than 100 kΩ.

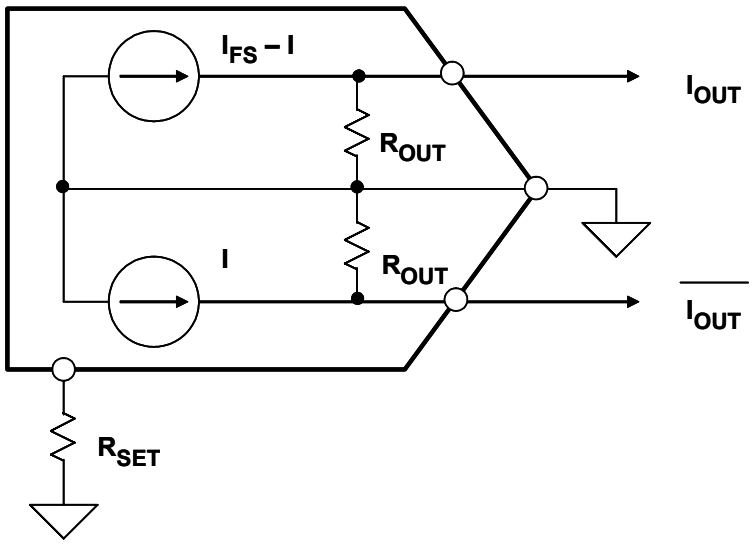


Figure 6.25: *Model of High Speed DAC Output*

Another consideration is the output *compliance voltage*—the maximum voltage swing allowed at the output in order for the DAC to maintain its linearity. This voltage is typically 1 V to 1.5 V, but will vary depending upon the DAC. Best DAC linearity is generally achieved when driving a virtual ground, such as an op amp I/V converter. Modern current output DACs usually have differential outputs, to achieve high CM rejection and reduce the even-order distortion products. Full-scale output currents in the range of 2 to 20 mA are common.

In most applications, it is desirable to convert the differential output of the DAC into a single-ended signal, suitable for driving a coax line. This can be readily achieved with an

RF transformer, provided low frequency response is not required. Figure 6.26 shows a typical example of this approach. The high impedance current output of the DAC is terminated differentially with 50 Ω, which defines the source impedance to the transformer as 50 Ω.

The resulting differential voltage drives the primary of a 1:1 RF transformer, to develop a single-ended voltage at the output of the secondary winding. The output of the 50 Ω LC filter is matched with the 50 Ω load resistor RL, and a final output voltage of 1 V p-p is developed.

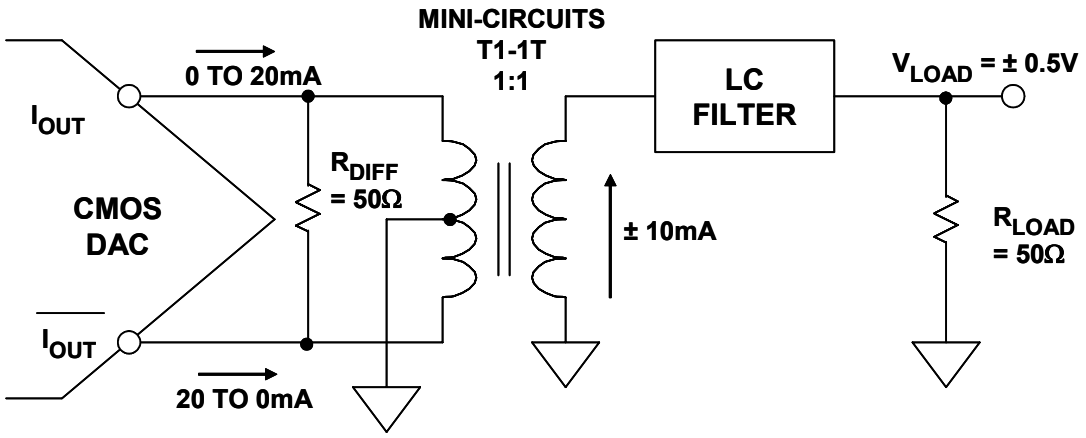


Figure 6.26: *Differential Transformer Coupling*

The transformer not only serves to convert the differential output into a single-ended signal, but it also isolates the output of the DAC from the reactive load presented by the LC filter, thereby improving overall distortion performance.

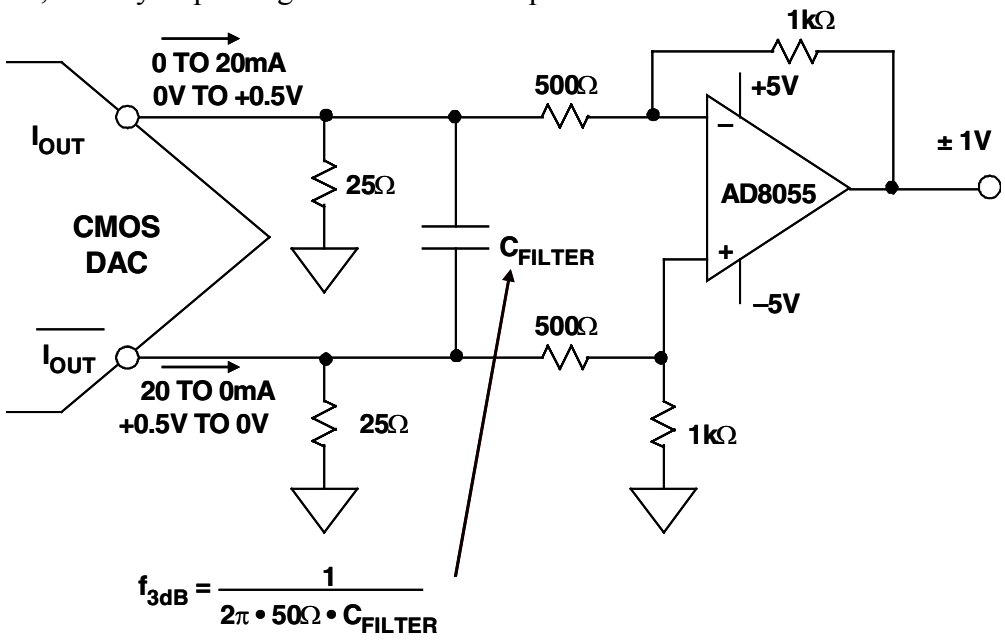


Figure 6.27: *Differential DC Coupled Output Using a Dual Supply Op Amp*

An op amp connected as a differential to single-ended converter can be used to obtain a single-ended output when frequency response to DC is required. In Figure 6.28 the AD8055 op amp is used to achieve high bandwidth and low distortion (see Reference 2). The current output DAC drives balanced 25 Ω resistive loads, thereby developing an out-of-phase voltage of 0 V to +0.5 V at each output. The AD8055 is configured for a gain of 8, to develop a final single-ended ground-referenced output voltage of 2 V p-p. Note that because the output signal swings above and below ground, a dual-supply op amp is required.

The C_{FILTER} capacitor forms a differential filter with the equivalent 50 Ω differential output impedance. This filter reduces any slew induced distortion of the op amp, and the optimum cutoff frequency of the filter is determined empirically to give the best overall distortion performance.

A modified form of the Figure 6.26 circuit can also be operated on a single supply, provided the CM voltage of the op amp is set to mid-supply (+2.5 V). This is shown in Figure 6.28. The output voltage is 2 V p-p centered around a CM voltage of +2.5 V. This CM voltage can be either developed from the +5 V supply using a resistor divider, or directly from a +2.5 V voltage reference. If the +5 V supply is used as the CM voltage, it must be heavily decoupled to prevent supply noise from being amplified.

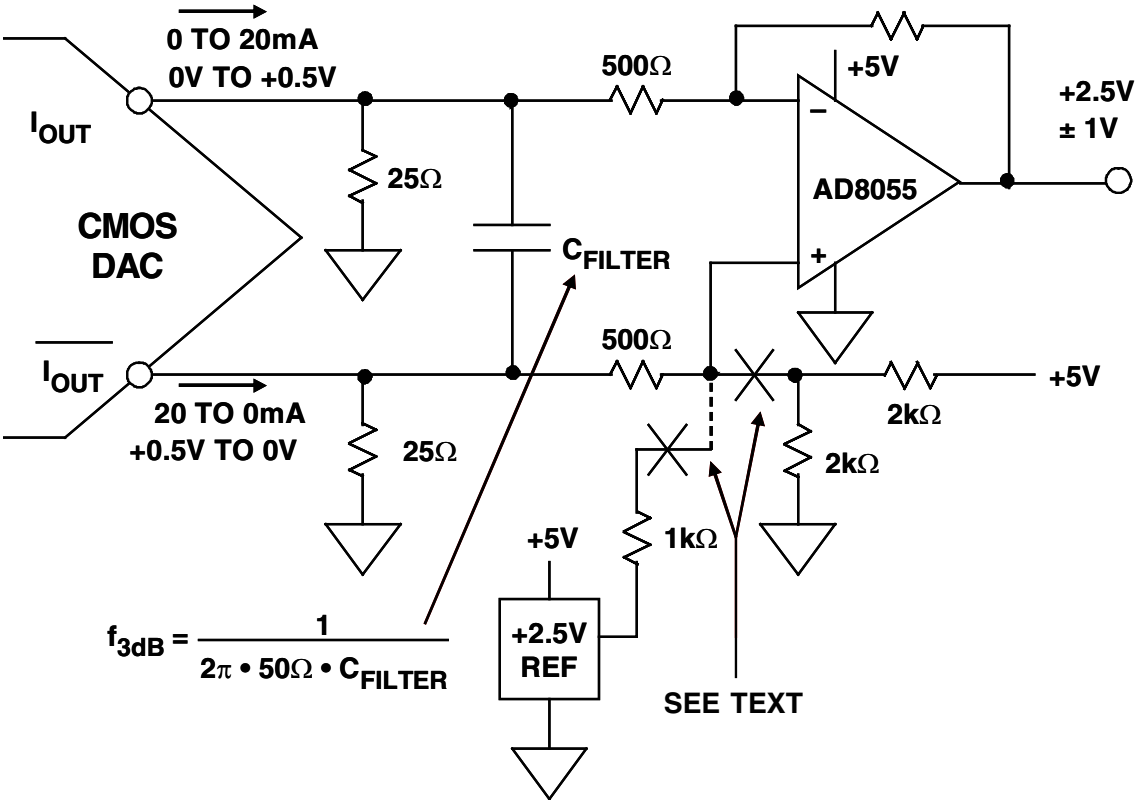


Figure 6.28: *Differential DC Coupled Output Using a Single-Supply Op Amp*

Single-Ended Current-to-Voltage Conversion

Single-ended current-to-voltage conversion is easily performed using a single op amp as an I/V converter, as shown in Figure 6.29. The 10 mA full-scale DAC current from the AD768 (see Reference 3) develops a 0 V to +2 V output voltage across the 200 Ω R_F.

Driving the virtual ground of the AD8055 op amp minimizes any distortion due to nonlinearity in the DAC output impedance. In fact, most high resolution DACs of this type are factory trimmed using an I/V converter.

It should be recalled, however, that using the single-ended output of the DAC in this manner will cause degradation in the CM rejection and increased second-order distortion products, compared to a differential operating mode.

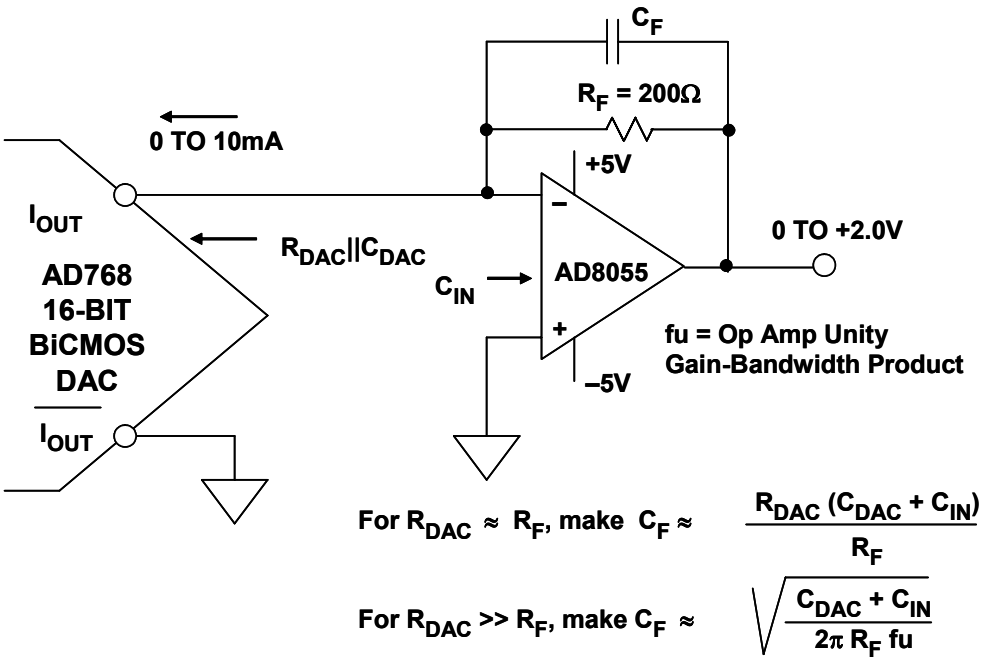


Figure 6.29: *Single-Ended I/V Op Amp Interface for Precision 16-bit AD768 DAC*

The C_F feedback capacitor should be optimized for best pulse response in the circuit. The equations given in the diagram should only be used as guidelines. A more detailed analysis of this circuit is given in the References.

Differential Current-to-Differential Voltage Conversion

If a buffered differential voltage output is required from a current output DAC, the AD813X-series of differential amplifiers can be used as shown in Figure 6.30.

The DAC output current is first converted into a voltage that is developed across the 25 Ω resistors. The voltage is amplified by a factor of 5 using the AD813X. This technique is used in lieu of a direct I/V conversion to prevent fast slewing DAC currents from overloading the amplifier and introducing distortion. Care must be taken so that the DAC output voltage is within its compliance rating.

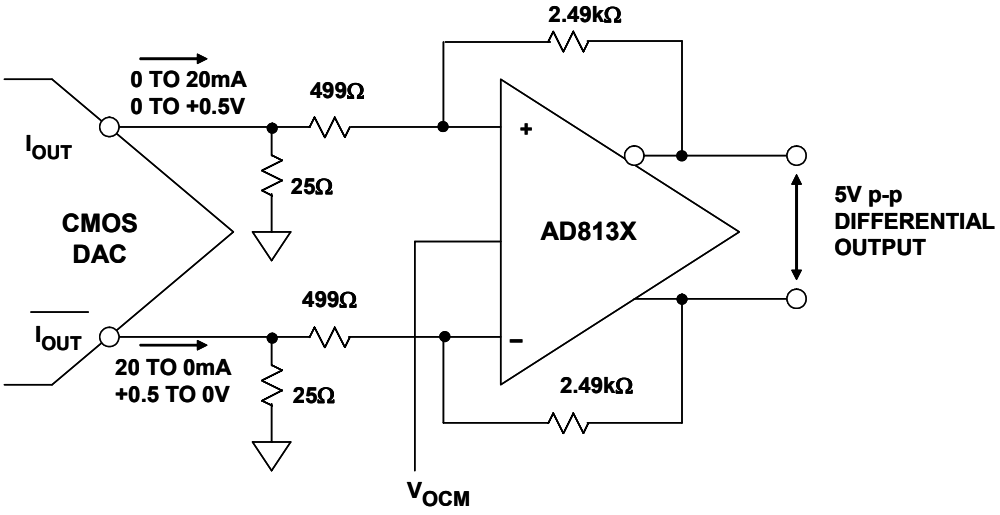


Figure 6.30: *Buffering High Speed DACs using AD813X Differential Amplifier*

The V_{OCM} input on the AD813X can be used to set a final output CM voltage within the range of the AD813X. If transmission lines are to be driven at the output, adding a pair of 75 Ω resistors will allow this.

Digital Interfaces

The earliest monolithic DACs contained little, if any, logic circuitry, and parallel data had to be maintained on the digital input to maintain the digital output. Today almost all DACs are latched and data need only be written to them, not maintained. Some even have nonvolatile latches and remember settings while turned off.

There are innumerable variations of DAC digital input structure, which will not be discussed here, but the nearly all are described as "double-buffered." A double-buffered DAC has two sets of latches. Data is initially latched in the first rank and subsequently transferred to the second as shown in Figure 6.31. There are two reasons why this arrangement is useful.

The first is that it allows data to enter the DAC in many different ways. A DAC without a latch, or with a single latch, must be loaded in parallel with all bits at once, since otherwise its output during loading may be totally different from what it was or what it is to become. A double-buffered DAC, on the other hand, may be loaded with parallel data, or with serial data, or with 4-bit or 8-bit words, or whatever, and the output will be

unaffected until the new data is completely loaded and the DAC receives its update instruction.

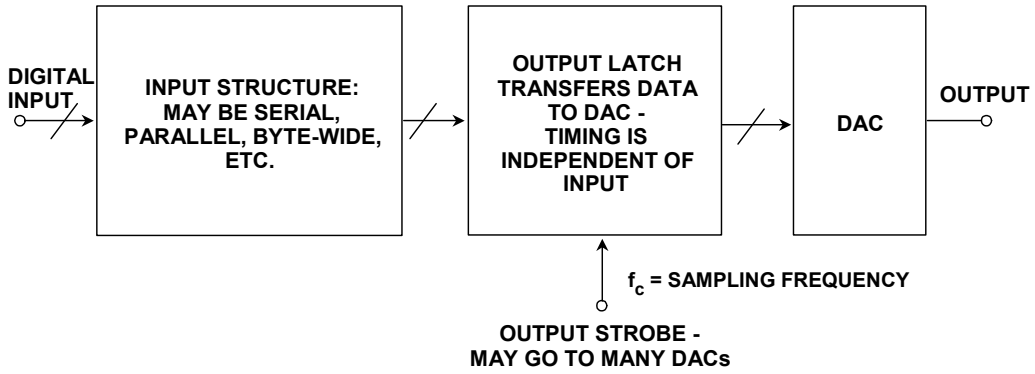


Figure 6.31: *Double-Buffered DAC Permits Complex Input Structures and Simultaneous Update*

The other convenience of the double-buffered structure is that many DACs may be updated simultaneously: data is loaded into the first rank of each DAC in turn, and when all is ready, the output buffers of all the DACs are updated at once. There are many DAC applications where the output of a number of DACs must change simultaneously, and the double-buffered structure allows this to be done very easily.

Most early monolithic high resolution DACs had parallel or byte-wide data ports and tended to be connected to parallel data buses and address decoders and addressed by microprocessors as if they were very small write-only memories. (Some parallel DACs are not write-only, but can have their contents read as well—this is convenient for some applications, but is not very common.) A DAC connected to a data bus is vulnerable to capacitive coupling of logic noise from the bus to the analog output Serial interfaces are less vulnerable to such noise (since fewer noisy pins are involved), use fewer pins, and therefore take less board space, and are frequently more convenient for use with modern microprocessors, most of which have serial data ports. Some, but not all, of such serial DACs have data outputs as well as data inputs so that several DACs may be connected in series and data clocked to them all from a single serial port. This arrangement is often referred to as "daisy-chaining."

Of course, serial DACs cannot be used where high update rates are involved, since the clock rate of the serial data would be too high. Some very high speed DACs actually have two parallel data ports and use them alternately in a multiplexed fashion (sometimes this is called a “ping-pong” input) to reduce the data rate on each port as shown in Figure 6.32. The alternate loading (ping-pong) DAC in the diagram loads from port A and port B alternately on the rising and falling edges of the clock, which must have a mark-space ratio close to 50:50. The internal clock multiplier ensures that the DAC itself is updated with data A and data B alternately at exactly 50:50 time ratio, even if the external clock is not so precise.

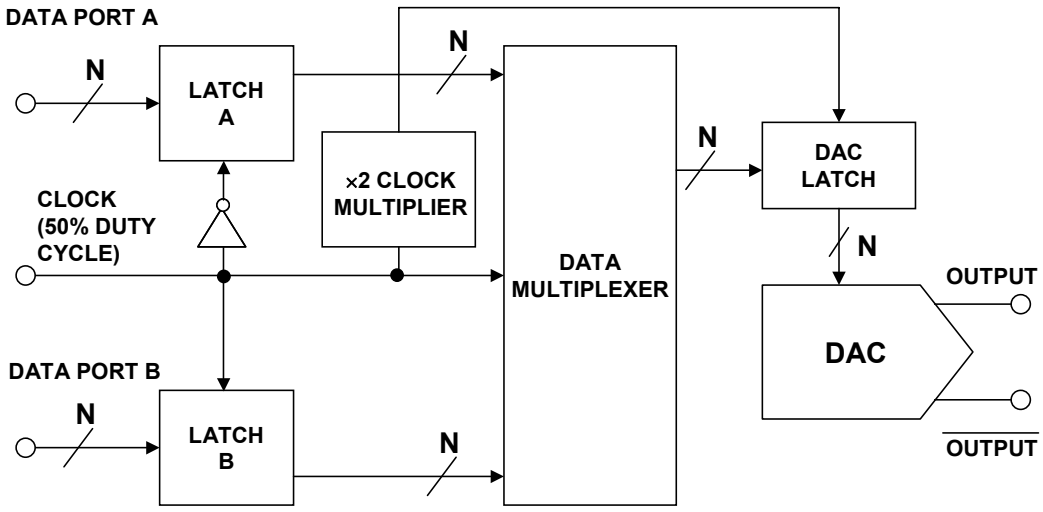


Figure 6.32: *Alternate Loading (Ping-Pong) High Speed DAC*

Historically integrated circuit logic circuitry (with the exception of emitter coupled logic or ECL) operated from 5 V supplies and had compatible logic levels—with a few exceptions 5 V logic would interface with other 5 V logic. Today, with the advent of low voltage logic operating with supplies of 3.3 V, 2.7 V, or even less, it is important to ensure that logic interfaces are compatible. There are several issues which must be considered—absolute maximum ratings, worst case logic levels, and timing. The logic inputs of integrated circuits generally have absolute maximum ratings, as do most other inputs, of 300 mV outside the power supply. Note that these are instantaneous ratings. If an IC has such a rating and is currently operating from a +5 V supply then the logic inputs may be between –0.3 V and +5.3 V—but if the supply is not present then that input must be between +0.3 V and –0.3 V, not the –0.3 V to +5.3 V which are the limits once the power is applied—ICs cannot predict the future.

The reason for the rating of 0.3 V is to ensure that no parasitic diode inside the IC is ever turned on by a voltage outside the IC's absolute maximum rating. It is quite common to protect an input from such over-voltage with a Schottky diode clamp. At low temperatures the clamp voltage of a Schottky diode may be a little more than 0.3 V, and so the IC may see voltages just outside its absolute maximum rating. Although, strictly speaking, this subjects the IC to stresses outside its absolute maximum ratings and so is forbidden, this is an acceptable exception to the general rule provided the Schottky diode is at a similar temperature to the IC that it is protecting (say within ±10°C).

Some low voltage devices, however, have inputs with absolute maximum ratings which are substantially greater than their supply voltage. This allows such circuits to be driven by higher voltage logic without additional interface or clamp circuitry. But it is important to read the data sheets and ensure that both logic levels and absolute maximum voltages are compatible for all combinations of high and low supplies.

This is the general rule when interfacing different low-voltage logic circuitry—it is always necessary to check both that at the lowest value of its power supply the logic 1

output from the driving circuit applied to its worst-case load is greater than the specified minimum logic 1 input for the receiving circuit, and that, again with its lowest value of power supply and with its output sinking maximum allowed current, the logic 0 output is less than the specified logic 0 input of the receiver. If the logic specifications of your chosen devices do not meet these criteria it will be necessary to select different devices, use different power supplies, or use additional interface circuitry to ensure that the required levels are available. Note that additional interface circuitry will introduce extra delays in timing.

It is not sufficient to build an experimental set-up and test it. In general, logic thresholds are generously specified and usually logic circuits will work correctly well outside their specified limits—but it is not possible to rely on this in a production design. At some point a batch of devices near the limit on low output swing will be required to drive some devices needing slightly more drive than usual—and will be unable to do so.

One of the latest developments in high speed logic interface is LVDS. Low voltage differential signaling (LVDS) presents a solution to the high speed converter interface problem by mitigating the effects of CMOS single-ended interfaces and accommodating higher data rates. The LVDS standard specifies a p-p voltage swing of 350 mV around a common-mode voltage of 1.2 V, which facilitates transmission of high-speed differential digital signals with balanced current, thereby reducing the slew rate requirement. Reducing the slew rate eliminates the gradients that result in noise from ground bounce that are present in conventional CMOS drivers. Ground-bounce noise can couple back into sensitive analog circuits and degrade the converter's dynamic range. Parallel LVDS interfaces enable much higher data rates and optimum dynamic performance, in high-speed data converters.

LVDS also offers some benefit in reduced EMI. The EMI fields generated by the opposing currents will tend to cancel each other (for matched edge rates). Trace length, skew, and discontinuities will reduce this benefit and should be avoided.

LVDS also offers simpler timing constraints compared to a demuxed CMOS solution at similar data rates. A demuxed databus requires a synchronization signal that is not required in LVDS. In demuxed CMOS buses, a clock equal to one-half the ADC sample rate is needed, adding cost and complexity, that is not required in LVDS. In general, the LVDS is more forgiving and can lead to a simpler, cleaner design.

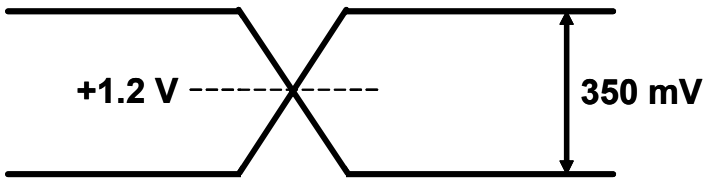


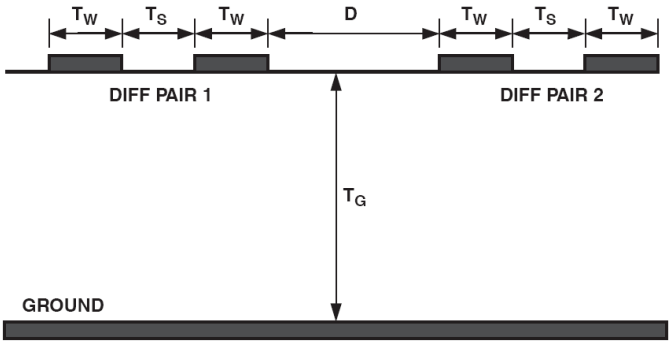
Figure 6.33: *LVDS Output Levels*

The LVDS specification (IEEE Standard 1596.3) was developed as an extension to the 1992 SCI protocol (IEEE Standard 1596-1992). The original SCI protocol was suitable for high speed packet transmissions in high end computing and used ECL levels.

However, for low end and power sensitive applications, a new standard was needed. LVDS signals were chosen because the voltage swing is smaller than that of ECL outputs, allowing for lower power supplies in power sensitive designs.

Unlike CMOS, which is typically a voltage output, LVDS is a current output technology. LVDS outputs for high performance converters should be treated differently than standard LVDS outputs used in digital logic. While standard LVDS can drive 1 m to 10 m in high speed digital applications (dependent on data rate), it is not recommended to let a high performance converters drive that distance. It is recommended to keep the output trace lengths short (<2 in.), minimizing the opportunity for any noise coupling onto the outputs from the adjacent circuitry, which may get back to the analog outputs. The differential output traces should be routed close together, maximizing common-mode rejection with the 100 Ω termination resistor close to the receiver. Users should pay attention to PCB trace lengths to minimize any delay skew.

A typical differential microstrip PCB trace cross section is shown in Figure 6.34.



Layout Guidelines

Keep T_W, T_S, and D constant over the trace length
Keep T_S ~ < 2 T_W
Avoid use of vias where possible
Keep D > 2 T_S
Avoid 90° bends if possible
Design T_W and T_G for ~50 Ω

Figure 6.34: *PCB Trace Spacing*

Power supply decoupling is very important with these fast (<0.5 ns) edge rates. A low inductance, surface-mount capacitor should be placed at every power supply and ground pin as close to the converter as possible. Placing the decoupling caps on the other side of the PCB is not recommended, since the via inductance will reduce the effective decoupling. The differential Z_O will tend to be slightly lower than twice the single-ended Z_O of each conductor due to proximity effects—the Z_O of each line should be designed to be slightly higher than 50 Ω. Simulation can be used in critical applications to verify impedance matching. In short runs, this should not be critical.

Data Converter Logic: Timing and other Issues

It is not the purpose of this brief section to discuss logic architectures, so we shall not define the many different data converter logic interface operations and their timing specifications except to note that data converter logic interfaces may be more complex than you expect—do not expect that because there is a pin with the same name on memory and interface chips it will behave in exactly the same way in a data converter. Unfortunately, there is not a standard nomenclature for pin functionality, even for the same manufacturer. The data sheet should always be consulted to determine the operation of all control pins. Also some data converters reset to a known state on power-up but many more do not.

But it is very necessary to consider general timing issues. The new low voltage processes which are used for many modern data converters have a number of desirable features. One which is often overlooked by users (but not by converter designers!) is their higher logic speed. DACs built on older processes frequently had logic which was orders of magnitude slower than the microprocessors that they interfaced with and it was sometimes necessary to use separate buffers, or multiple WAIT instructions, to make the two compatible. Today it is much more common for the write times of DACs to be compatible with those of the fast logic with which they interface.

Nevertheless not all DACs are speed compatible with all logic interfaces and it is still important to ensure that minimum data set-up times and write pulse widths are observed. Again, experiments will often show that devices work with faster signals than their specification requires—but at the limits of temperature or supply voltage some may not and interfaces should be designed on the basis of specified rather than measured timing.

Interpolating DACs (Interpolating TxDACs)

The concept of oversampling, to be discussed in another section (on sampling theory), can be applied high speed DACs typically used in communications applications. Oversampling relaxes the requirements on the output filter as well as increasing the SNR due to process gain.

Assume a traditional DAC is driven at an input word rate of 30 MSPS (see Figure 6.35A). Assume the DAC output frequency is 10 MHz. The image frequency component at 30 MHz – 10 MHz = 20 MHz must be attenuated by the analog reconstruction filter, and the transition band of the filter is therefore 10 MHz to 20 MHz. Assume that the image frequency must be attenuated by 60 dB. The filter must therefore go from a passband of 10 MHz to 60 dB stopband attenuation over the transition band lying between 10 MHz and 20 MHz (one octave). Filter gives 6 dB attenuation per octave for each pole. Therefore, a minimum of 10 poles is required to provide the desired attenuation. This is a fairly aggressive filter and would involve high Q sections which would be difficult to align and manufacture. Filters become even more complex as the transition band becomes narrower.

Assume that we increase the DAC update rate to 60 MSPS and insert a "zero" between each original data sample. The parallel data stream is now 60 MSPS, but we must now determine the value of the zero-value data points. This is done by passing the 60 MSPS data stream with the added zeros through a digital interpolation filter which computes the additional data points. The response of the digital filter relative to the 2-times oversampling frequency is shown in Figure 6.35B. The analog antialiasing filter transition zone is now 10 MHz to 50 MHz (the first image occurs at $2f_c - f_o = 60 - 10 = 50$ MHz). This transition zone is a little greater than 2 octaves, implying that a 5-pole or 6-pole Butterworth filter is sufficient.

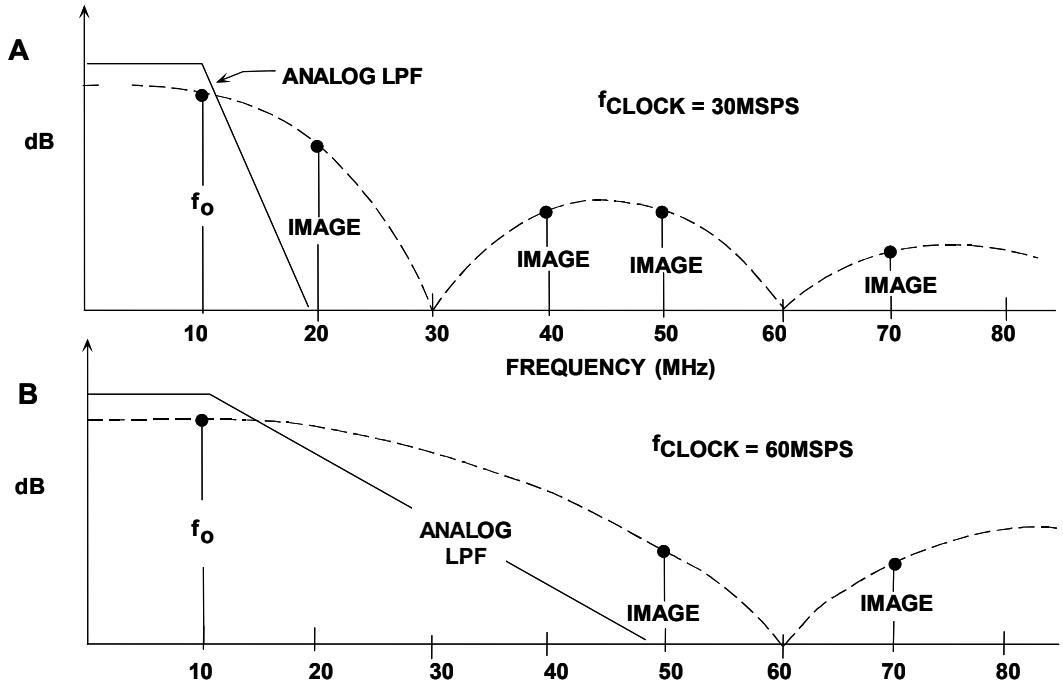


Figure 6.35: *Analog Filter Requirements for f_o = 10 MHz: (A) f_c = 30 MSPS, and (B) f_c = 60 MSPS*

The AD9773/AD9775/AD9777 (12-/14-/16-bit) series of Transmit DACs (TxDAC) are selectable 2×, 4×, or 8× oversampling interpolating dual DACs, and a simplified block diagram is shown in Figure 6.36. These devices are designed to handle 12-/14-/16-bit input word rates up to 160 MSPS. The output word rate is 400 MSPS maximum. For an output frequency of 50 MHz, an input update rate of 160 MHz, and an oversampling ratio of 2×, the image frequency occurs at 320 MHz – 50 MHz = 270 MHz. The transition band for the analog filter is therefore 50 MHz to 270 MHz. Without 2× oversampling, the image frequency occurs at 160 MHz – 50 MHz = 110 MHz, and the filter transition band is 60 MHz to 110 MHz.

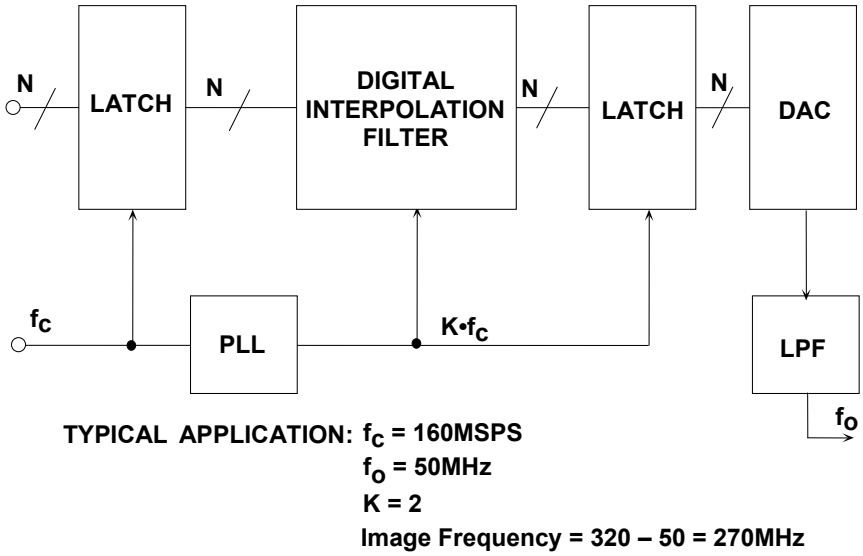


Figure 6.36: *Oversampling Interpolating TxDAC Simplified Block Diagram*

Reconstruction Filters

The output of a DAC is not a continuously varying waveform, but instead a series of dc levels. This output must be passed through a filter to remove the high frequency components and smooth waveform into a more truly analog waveform.

The concept of filtering is discussed in more detail in Chapter 8.

In general, to preserve spectral purity, the images of the DAC output must be attenuated below the resolution of DAC. To use the example sited above, we assume that the DAC output pass-band is 10 MHz. The sample rate is 30 MHz. Therefore the image of the pass-band that must be attenuated is 30 MHz – 10 MHz = 20 MHz. This is the sample rate minus the pass-band frequency. The DAC in this example is a 10-bit device, which would indicate a distortion level of −60 dB. So a reconstruction filter should reduce the image by 60 dB while not attenuating the fundamental at all. Since a filter attenuates at 6 dB/pole, this would indicate that a 10^{th} order filter would be required.

There are several other considerations that must be taken into account.

First is that most filter cutoffs are measured at the −3 dB point. Therefore, if we do not want the fundamental attenuated, some margin in the filter is required. The graphs in the filter section will help illustrate this point. This will cause the transition band to become narrower and thus the order of the filter to increase.

Secondly, there is a phenomenon called “sinc.”

Sin(x)/(x) (sinc)

The output of a D/A converter is not a continually varying wave form bit instead a series of DC levels. The DAC puts out a dc level until it is told to put out a new level. This is illustrated in Figure 6.37.

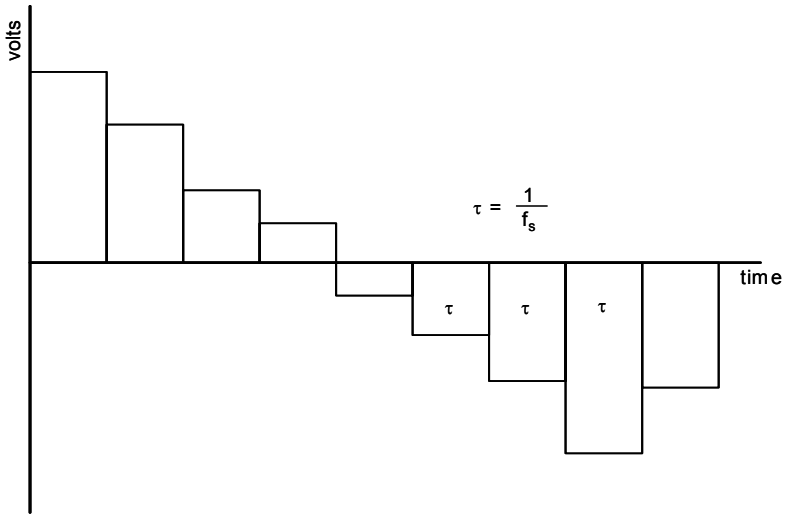


Figure 6.37: *Output of a DAC*

The width of the pulses is $1/F_S$. The spectrum of each pulse is the sin (x)/x curve. This is also known as the sinc curve. This response is added to the response of the reconstruction filter to provide the overall response of the converter. This will cause an amplitude error as the output frequency approaches the Nyquist frequency ($F_S/2$). The value of the sinc function is shown in Figure 6.38. Some high speed DACs incorporate an inverse filter (in the digital domain) to compensate for this rolloff.

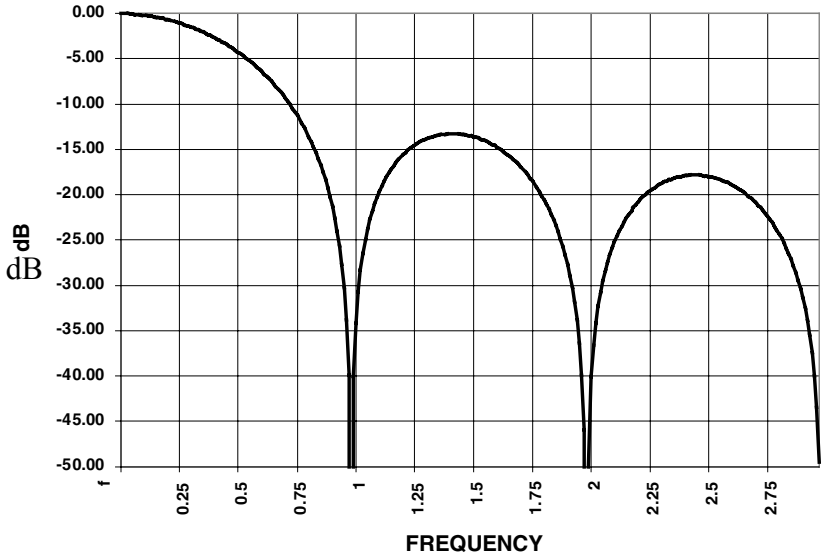


Figure 6.38: *Sinc (sin x/x) Curve (Normalized to F_S)*

Intentionally Nonlinear DACs

Thus far, we have emphasized the importance of maintaining good differential and integral linearity. However, there are situations where ADCs and DACs which have been made intentionally nonlinear (but maintaining good differential linearity) are useful, especially when processing signals having a wide dynamic range. One of the earliest uses of nonlinear data converters was in the digitization of voice-band signals for pulse code modulation (PCM) systems. Major contributions were made at Bell Labs during the development of the T1 carrier system. The motive for the nonlinear ADCs and DACs was to reduce the total number of bits (and therefore the serial transmission rate) required to digitize voice channels. Straight linear encoding of a voice channel required 11-bits or 12-bits at an 8 kSPS per channel sampling rate. In the 1960s Bell Labs determined that 7-bit nonlinear encoding was sufficient, and later in the 1970s went to 8-bit nonlinear encoding for better performance.

The nonlinear transfer function allocates more quantization levels out of the total range for small signals and fewer for large amplitude signals. In effect, this reduces the quantization noise associated with small signals (where it is most noticeable) and increases the quantization noise for larger signals (where it is less noticeable). The term *companding* is generally used to describe this form of encoding.

The logarithmic transfer function chosen is referred to as the "Bell μ-255" standard, or simply "μ-law." A similar standard developed in Europe is referred to as "A-law." The Bell μ-law allows a dynamic range of about 4000:1 using 8 bits, whereas an 8-bit linear data converter provides a range of only 256:1.

The first generation channel bank (D1) used temperature controlled resistor-diode networks for "compressors" ahead of a 7-bit linear ADC in the transmitter to generate the logarithmic transfer function. Corresponding resistor-diode "expandors" having an inverse transfer function followed the 7-bit linear DAC in the receiver. The next generation D2 channel banks used nonlinear ADCs and DACs to accomplish the compression/expansion functions in a much more reliable and cost-effective manner and eliminated the need for the temperature-controlled diode networks.

In his 1953 classic paper, B. D. Smith proposed that the transfer function of a successive approximation ADC utilizing a nonlinear internal DAC in the feedback path would be the inverse transfer function of the DAC (Reference 8). The same basic DAC could therefore be used in the ADC and also for the reconstruction DAC. Later in the 1960s and early 1970s, nonlinear ADC and DAC technology using piecewise linear approximations of the desired transfer function allowed low cost, high volume implementations (References 18-23). These nonlinear 8-bit, 8-kSPS data converters became popular telecommunications building blocks.

The nonlinear transfer function of the 8-bit DAC is first divided into 16 segments (chords) of different slopes—the slopes are determined by the desired nonlinear transfer function. The 4 MSBs determine the segment containing the desired data point, and the individual segment is further subdivided into 16 equal quantization levels by the 4 LSBs of the 8-bit word. This is shown in Figure 6.39 for a 6-bit DAC, where the first three bits identify one of the eight possible chords, and each chord is further subdivided into eight

equal levels defined by the 3 LSBs. The 3 MSBs are generated using a nonlinear string DAC, and the 3 LSBs are generated using a 3-bit binary R-2R DAC.

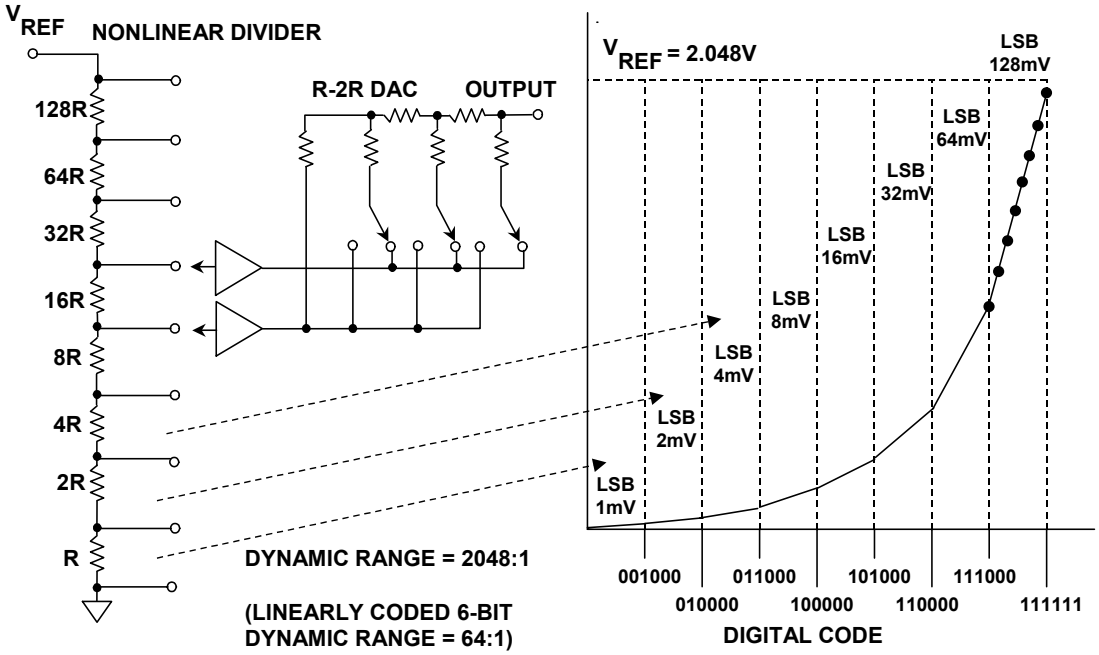


Figure 6.39: *Nonlinear 6-Bit Segmented DAC*

In 1982, Analog Devices introduced the LOGDAC™ AD7111 monolithic multiplying DAC featuring wide dynamic range using a logarithmic transfer function. The basic DAC in the LOGDAC is a linear 17-bit voltage-mode R-2R DAC preceded by an 8-bit input decoder (A functional diagram of the LOGDAC is shown in Figure 6.40). The LOGDAC can attenuate an analog input signal, V_{IN}, over the range 0 dB to 88.5 dB in 0.375 dB steps. The degree of attenuation across the DAC is determined by a nonlinear-coded 8-bit word applied to the onboard decode logic. This 8-bit word is mapped into the appropriate 17-bit word which is then applied to a 17-bit, R-2R ladder. In addition to providing the logarithmic transfer function, the LOGDAC also acts as a full four-quadrant multiplying DAC.

With the introduction of high resolution linear ADCs and DACs, the method used in the LOGDAC is widely used today to implement various nonlinear transfer functions such as the μ-law and A-law companding functions required for telecommunications and other applications. Figure 6.41 shows a general block diagram of the modern approach. The μ-law or A-law companded input data is mapped into data points on the transfer function of a high resolution DAC. This mapping can be easily accomplished by a simple lookup table in either hardware, software, or firmware. A similar nonlinear ADC can be constructed by digitizing the analog input signal using a high resolution ADC and mapping the data points into a shorter word using the appropriate transfer function. A big advantage of this method is that the transfer curve does not have to be approximated with straight line segments as in the earlier method, thereby providing more accuracy.

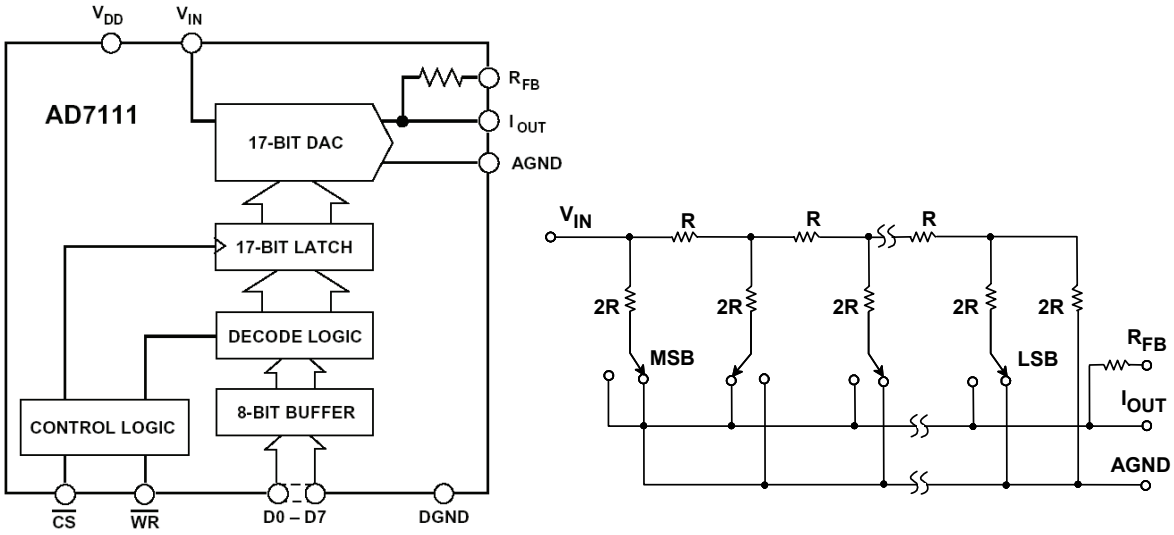


Figure 6.40: *AD7111 LOGDAC (Released 1982)*

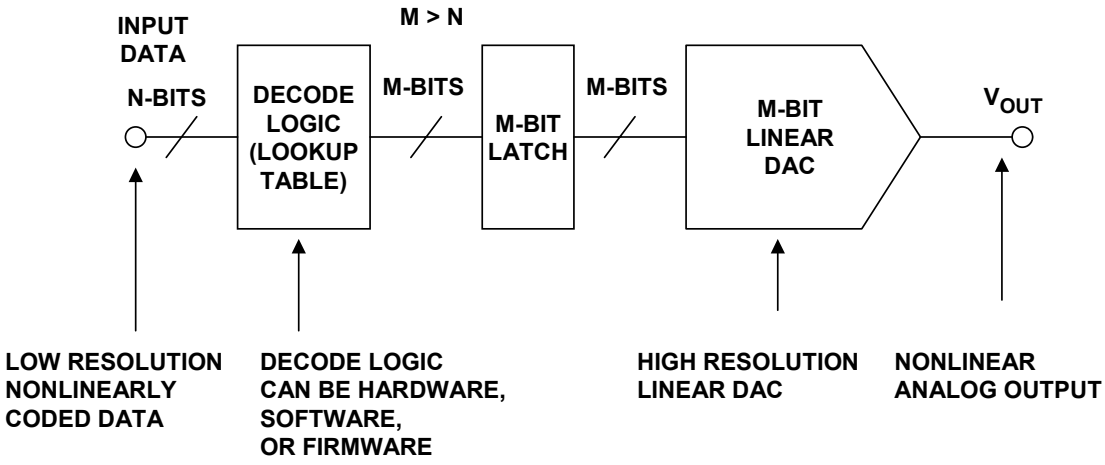


Figure 6.41: *General Nonlinear DAC*

SECTION 6.2: ANALOG-TO-DIGITAL CONVERTER ARCHITECTURES

The basic ADC function is shown in Figure 6.42. This could also be referred to as a quantizer. Most ADC chips also include some of the support circuitry, such as clock oscillator for the sampling clock, reference (REF), the sample and hold function, and output data latches. In addition to these basic functions, some ADCs have additional circuitry built in. These functions could include multiplexers, sequencers, auto-calibration circuits, programmable gain amplifiers (PGAs), etc.

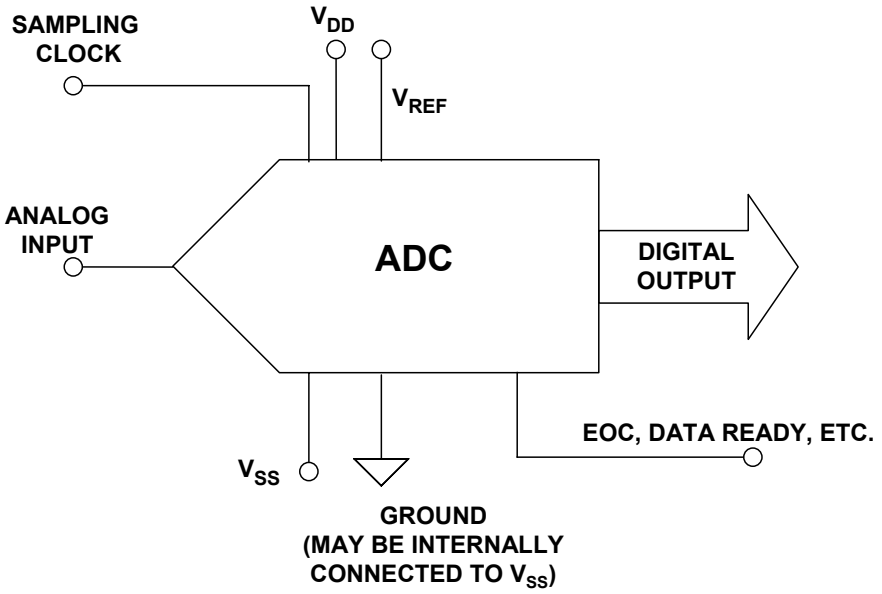


Figure 6.42: *Basic ADC Function*

Similar to DACs, some ADCs use external references and have a reference input terminal, while others have an output from an internal reference. In some instances, the ADC may have an internal reference that is pinned out through a resistor. This connection allows the reference to be filtered (using the internal R and an external C) or by allowing the internal reference to be overdriven by an external reference. The AD789X family of parts is an example of ADC that use this type of connection. The simplest ADCs, of course, have neither—the reference is on the ADC chip and has no external connections.

If an ADC has an internal reference, its overall accuracy is specified when using that reference. If such an ADC is used with a perfectly accurate external reference, its absolute accuracy may actually be worse than when it is operated with its own internal reference. This is because it is trimmed for absolute accuracy when working with its own actual reference voltage, not with the nominal value. Twenty years ago it was common for converter references to have accuracies as poor as ±5% since these references were trimmed for low temperature coefficient rather than absolute accuracy, and the inaccuracy of the reference was compensated in the gain trim of the ADC itself. Today the problem is much less severe, but it is still important to check for possible loss of

absolute accuracy when using an external reference with an ADC which has a built-in one.

ADCs which have reference terminals must, of course, specify their behavior and parameters. If there is a reference input the first specification will be the reference input voltage—and of course this has two values, the absolute maximum rating, and the range of voltages over which the ADC performs correctly.

Most ADCs require that their reference voltage is within quite a narrow range whose maximum value is less than or equal to the ADC's V_{DD}.

The reference input terminal of an ADC may be buffered as shown in Figure 6.43, in which case it has input impedance (usually high) and bias current (usually low) specifications, or it may connect directly to the ADC. In either case, the transient currents developed on the reference input due to the internal conversion process need good decoupling with external low inductance capacitors. Good ADC data sheets recommend appropriate decoupling networks.

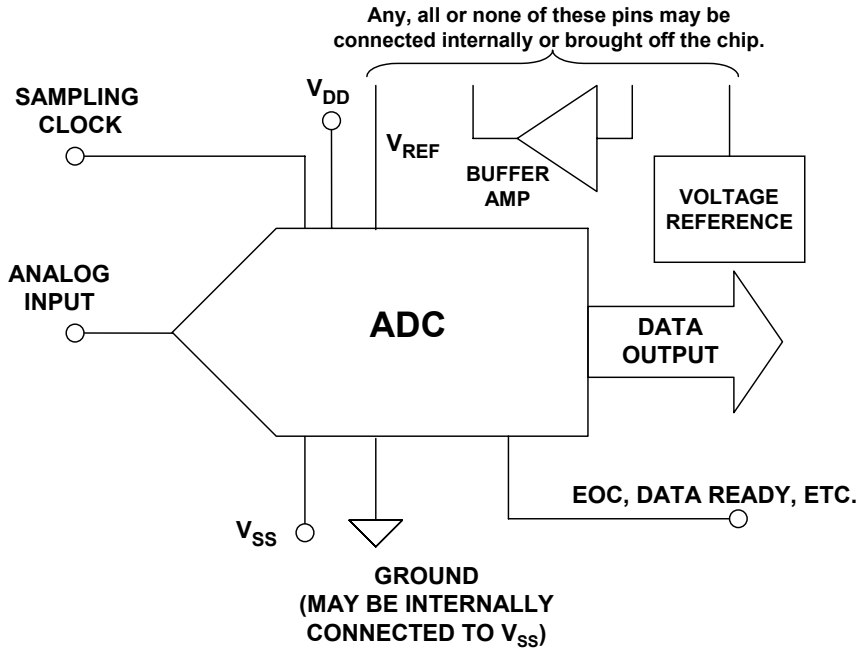


Figure 6.43: *ADC with Reference and Buffer*

The reference output may be buffered or unbuffered. If it is buffered, the maximum output current will probably be specified. In general such a buffer will have a unidirectional output stage which sources current but does not allow current to flow into the output terminal. If the buffer does have a push-pull output stage (not as common), the output current will probably be defined as ±(SOME VALUE) mA. If the reference output is unbuffered, the output impedance may be specified, or the data sheet may simply advise the use of a high input impedance external buffer.
There are some instances where the power supply is the reference. In these cases it is imperative to make sure the power supply is clean.

The *sampling clock* input is a critical function in an ADC and a source of some confusion. It could truly be the sampling clock. This frequency would typically be several times higher than the sampling rate of the converter. It could also be a convert start (or encode) command which would happen once per conversion. Pipeline architecture devices and sigma delta (Σ-Δ) converters are continuously converting and have no convert start command.

Regardless of the ADC, it is extremely important to read the data sheet and determine exactly what the external clock requirements are, because they can vary widely from one ADC to another.

At some point after the assertion of the sampling clock, the output data is valid. This data may be in parallel or serial format depending upon the ADC. Early successive approximation ADCs such as the AD574 simply provided a STATUS output (STS) which went high during the conversion, and returned to the low state when the output data was valid. In other ADCs, this line is variously called *busy*, *end-of-conversion (EOC), data ready,* etc. Regardless of the ADC, there must be some method of knowing when the output data is valid—and again, the data sheet is where this information can always be found.

Another detail which can cause trouble is the difference between EOC and DRDY (data ready). EOC indicates that conversion has finished, DRDY that data is available at the output. In some ADCs, EOC functions as DRDY—in others, data is not valid until several tens of nanoseconds *after* the EOC has become valid, and if EOC is used as a data strobe, the results will be unreliable.

There are one or two other practical points which are worth remembering about the logic of ADCs. On power-up, many ADCs do not have logic reset circuitry and may enter an anomalous logical state. Several conversions may be necessary to restore their logic to proper operation so: (a) the first few conversions after power-up should never be trusted, and (b) control outputs (EOC, data ready, etc.) may behave in unexpected ways at this time (and not necessarily in the same way at each power-up), and (c) care should be taken to ensure that such anomalous behavior cannot cause system latch-up. For example, EOC (end-of-conversion) should not be used to initiate conversion if there is any possibility that EOC will not occur until the first conversion has taken place, as otherwise initiation will never occur.

Some low-power ADCs now have power-saving modes of operation variously called *standby*, *power-down*, *sleep*, etc. When an ADC comes out of one of these low-power modes, there is a certain recovery time required before the ADC can operate at its full specified performance. The data sheet should therefore be carefully studied when using these modes of operation.

As a final example, some ADCs use CS (Chip Select) edges to reset internal logic, and it may not be possible to perform another conversion without asserting or reasserting CS (or it may not be possible to read the same data twice, or both).
For more detail, it is important to read the whole data sheet before using an ADC since there are innumerable small logic variations from type to type. Unfortunately, many data

sheets are not as clear as one might wish, so it is also important to understand the general principles of ADCs in order to interpret data sheets correctly. That is one of the purposes of this section.

There are a couple of general trend in ADCs that should be addressed. The first is the general trend toward lower supply voltages. This is partially due to the processes, particularly CMOS, which are used to manufacture the chips. Increasing demand for speed has driven the feature size of the processes down. This typically results in lower breakdown voltages for the transistors. This, in turn, requires lower supply voltages. Very few new parts are developed with the legacy ±15 V supplies and ±10 V input range.

Since the input signal range of the ADCs is shrinking, there is also a trend towards differential inputs. This helps improve the dynamic range of a converter, typically by 6 dB. There could be even further improvement since the common-mode ground referenced noise is rejected. In many cases the differential input can be driven single endedly (with the resultant reduction of SNR). Occasionally the REF input might also be differential.

The Comparator: A 1-Bit ADC

A comparator is a 1-bit ADC (see Figure 6.44). If the input is above a threshold, the output has one logic value, below it has another. There is no ADC architecture which does not use at least one comparator of some sort. So while a 1 bit ADC is of very limited usefulness it is a building block for other architectures.

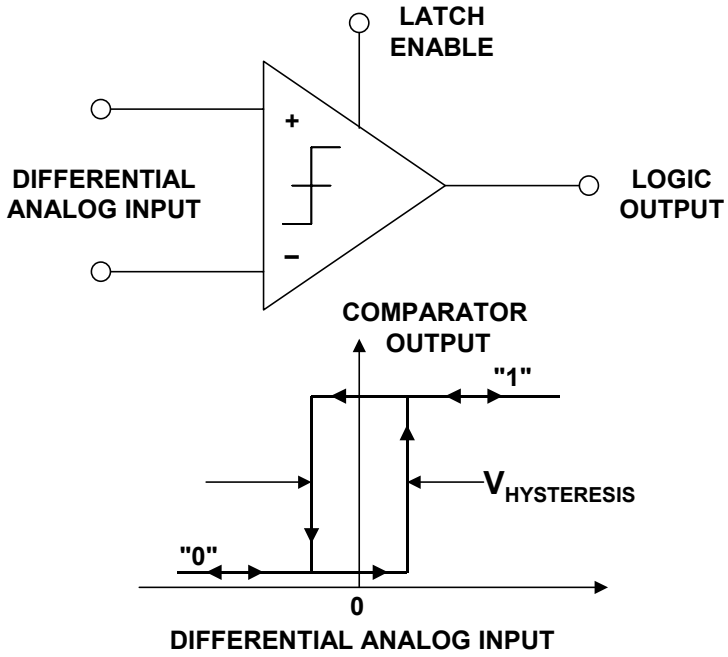


Figure 6.44: *The Comparator: A 1-Bit ADC*

Comparators used as building blocks in ADCs need good resolution which implies high gain. This can lead to uncontrolled oscillation when the differential input approaches zero. In order to prevent this, *hysteresis* is often added to comparators using a small amount of positive feedback. Figure 6.44 shows the effects of hysteresis on the overall transfer function. Many comparators have a millivolt or two of hysteresis to encourage "snap" action and to prevent local feedback from causing instability in the transition region. Note that the resolution of the comparator can be no less than the hysteresis, so large values of hysteresis are generally not useful.

Successive Approximation ADCs

The successive approximation ADC has been the mainstay of data acquisition for many years. Recent design improvements have extended the sampling frequency of these ADCs into the megahertz region.

The basic successive approximation ADC is shown in Figure 6.45. It performs conversions on command. On the assertion of the CONVERT START command, the sample-and-hold (SHA) is placed in the *hold* mode, and all the bits of the successive approximation register (SAR) are reset to "0" except the MSB which is set to "1." The SAR output drives the internal DAC. If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The next most significant bit is then set to "1." If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The process is repeated with each bit in turn. When all the bits have been set, tested, and reset or not as appropriate, the contents of the SAR correspond to the value of the analog input, and the conversion is complete. These bit "tests" can form the basis of a serial output version SAR-based ADC.

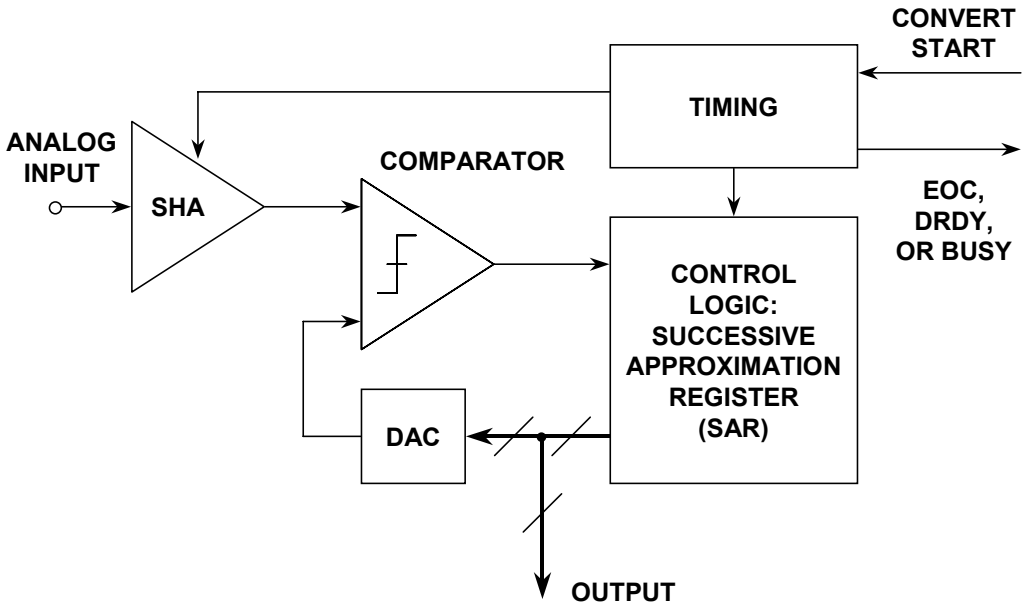


Figure 6.45: *Basic Successive Approximation ADC (Feedback Subtraction ADC)*

The fundamental timing diagram for a typical SAR ADC is shown in Figure 6.46. The end of conversion is generally indicated by an end-of-convert (EOC), data-ready (DRDY), or a busy signal (actually, *not*-BUSY indicates end of conversion). The polarities and name of this signal may be different for different SAR ADCs, but the fundamental concept is the same. At the beginning of the conversion interval, the signal goes high (or low) and remains in that state until the conversion is completed, at which time it goes low (or high). The trailing edge is generally an indication of valid output

data, but the data sheet should be carefully studied—in some ADCs additional delay is required before the output data is valid.

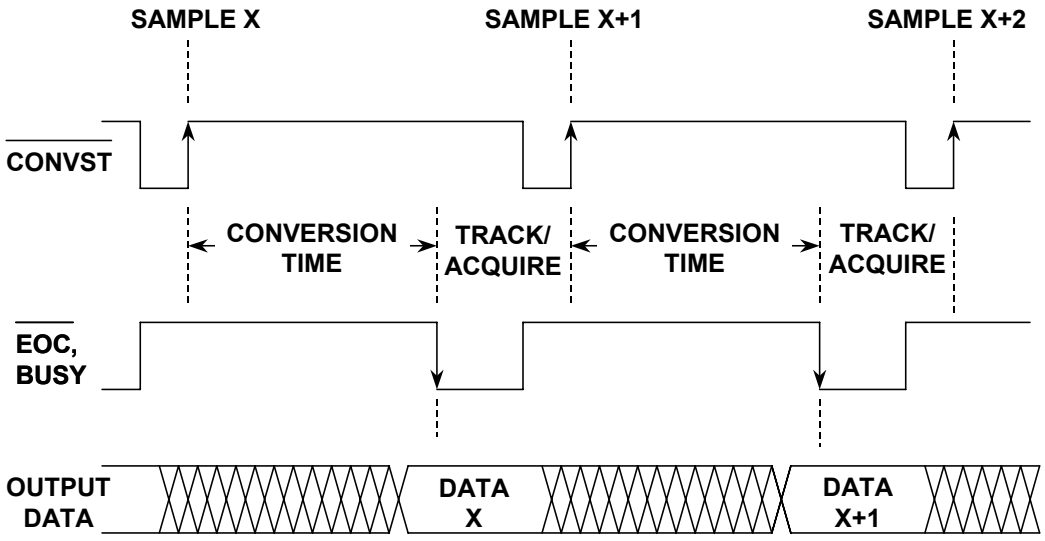


Figure 6.46: *Typical SAR ADC Timing*

An N-bit conversion takes N steps. It would seem on superficial examination that a 16-bit converter would have twice the conversion time of an 8-bit one, but this is not the case. In an 8-bit converter, the DAC must settle to 8-bit accuracy before the bit decision is made, whereas in a 16-bit converter, it must settle to 16-bit accuracy, which takes a lot longer. In practice, 8-bit successive approximation ADCs can convert in a few hundred nanoseconds, while 16-bit ones will generally take several microseconds.

While there are some variations, the fundamental timing of most SAR ADCs is similar and relatively straightforward. The conversion process is initiated by asserting a CONVERT START signal. This signal is typically named something like $\overline{\text{CONVST}}$ or CS. This signal is a usually a negative-going pulse whose positive-going edge actually initiates the conversion. The internal sample-and-hold (SHA) amplifier is placed in the hold mode on this edge, and the various bits are determined using the SAR algorithm. The negative-going edge of the $\overline{\text{CONVST}}$ pulse causes a signal typically called $\overline{\text{EOC}}$ (End Of Conversion) or BUSY to go high. When the conversion is complete, the BUSY line goes low (or $\overline{\text{EOC}}$ goes high), indicating the completion of the conversion process. In most cases the trailing edge of the BUSY line can be used as an indication that the output data is valid and can be used to strobe the output data into an external register.

There may also be other control lines. And sometimes control lines have dual function. This is primarily done when the chip is pin limited. Because of the many variations in terminology and design, the individual data sheet should always be consulted when using a specific ADC.

It should also be noted that some SAR ADCs require an external high frequency clock in addition to the CONVERT START command. In most cases, there is no need to synchronize the two. The frequency of the external clock, if required, generally falls in the range of 1 MHz to 30 MHz depending on the conversion time and resolution of the ADC. Other SAR ADCs have an internal oscillator which is used to perform the conversions and only require the CONVERT START command. Because of their architecture, SAR ADCs generally allow single-shot conversion at any repetition rate from dc to the converter's maximum conversion rate.

Notice that the overall accuracy and linearity of the SAR ADC is determined primarily by the internal DAC. Until recently, most precision SAR ADCs used laser-trimmed thin-film DACs to achieve the desired accuracy and linearity. The thin-film resistor trimming process adds cost, and the thin-film resistor values may be affected when subjected to the mechanical stresses of packaging.

For these reasons, switched capacitor (or charge-redistribution) DACs have become popular in newer SAR ADCs. The advantage of the switched capacitor DAC is that the accuracy and linearity is primarily determined by photolithography, which in turn controls the capacitor plate area and the capacitance as well as matching. In addition, small capacitors can be placed in parallel with the main capacitors which can be switched in and out under control of autocalibration routines to achieve high accuracy and linearity without the need for thin-film laser trimming. Temperature tracking between the switched capacitors can be better than 1 ppm/ºC, thereby offering a high degree of temperature stability.

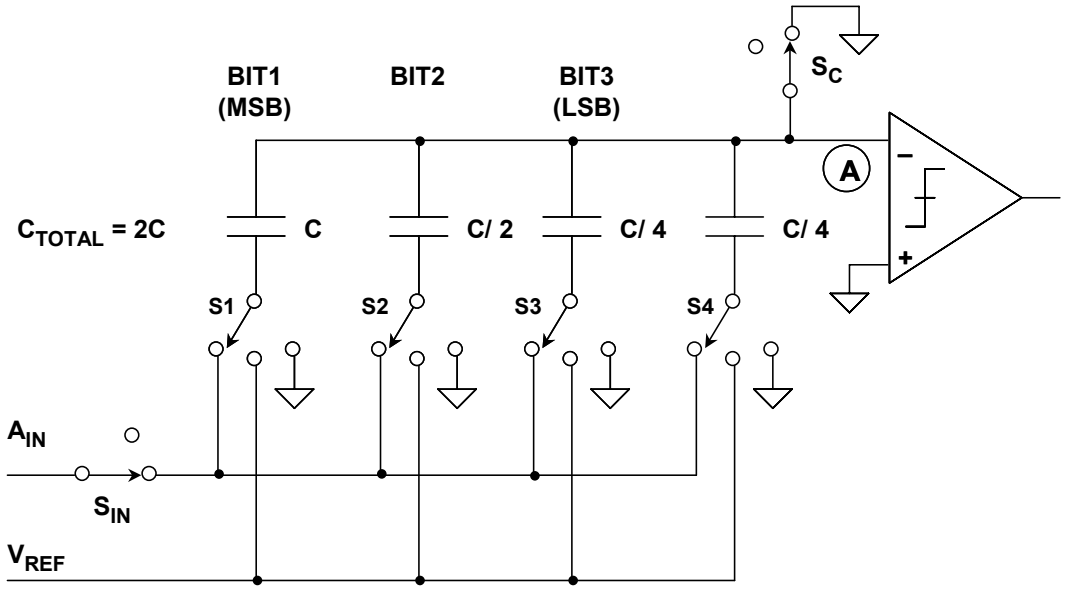


Figure 6.47: *3-Bit Switched Capacitor DAC*

A simple 3-bit capacitor DAC is shown in Figure 6.47. The switches are shown in the *track*, or *sample* mode where the analog input voltage, A_{IN}, is constantly charging and discharging the parallel combination of all the capacitors. The *hold* mode is initiated by opening S_{IN}, leaving the sampled analog input voltage on the capacitor array. Switch S_C is then opened allowing the voltage at node A to move as the bit switches are manipulated. If S1, S2, S3, and S4 are all connected to ground, a voltage equal to $-A_{IN}$ appears at node A. Connecting S1 to V_{REF} adds a voltage equal to $V_{REF}/2$ to $-A_{IN}$. The comparator then makes the MSB bit decision, and the SAR either leaves S1 connected to V_{REF} or connects it to ground depending on the comparator output (which is high or low depending on whether the voltage at node A is negative or positive, respectively). A similar process is followed for the remaining two bits. At the end of the conversion interval, S1, S2, S3, S4, and S_{IN} are connected to A_{IN}, S_C is connected to ground, and the converter is ready for another cycle.

Note that the extra LSB capacitor (C/4 in the case of the 3-bit DAC) is required to make the total value of the capacitor array equal to 2C so that binary division is accomplished when the individual bit capacitors are manipulated.

The operation of the capacitor DAC (cap DAC) is similar to an R-2R resistive DAC. When a particular bit capacitor is switched to V_{REF}, the voltage divider created by the bit capacitor and the total array capacitance (2 C) adds a voltage to node A equal to the weight of that bit. When the bit capacitor is switched to ground, the same voltage is subtracted from node A.

An example of charge redistribution successive approximation ADCs is Analog Devices' PulSAR™ series. The AD7677 is a 16-bit, 1-MSPS, PulSAR, fully differential, ADC that operates from a single 5 V power supply (see Figure 6.48). The part contains a high speed 16-bit sampling ADC, an internal conversion clock, error correction circuits, and both serial and parallel system interface ports. The AD7677 is hardware factory calibrated and comprehensively tested to ensure such ac parameters as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional dc parameters of gain, offset, and linearity. It features a very high sampling rate mode (Warp) and, for asynchronous conversion rate applications, a fast mode (Normal) and, for low power applications, a reduced power mode (Impulse) where the power is scaled with the throughput.

The operation of a successive approximation ADC is as follows. Using Figure 6.49 as an example, one side of the balance is loaded with half scale (in this case 32 lbs.). Call this the proof mass. The test mass is then put on the other side of the balance. If the test mass is greater, as it is in this case, the proof mass is retained, otherwise it is discarded. Next a proof mass equal to ¼ scale is added. Again, if the test mass is still greater the proof mass is retained, otherwise it is rejected. It the example it is rejected. This process is continued, each time cutting the proof mass in half, until the desired resolution is reached. The proof masses are added up. This will equal the mass of the test mass, to the resolution of the test.

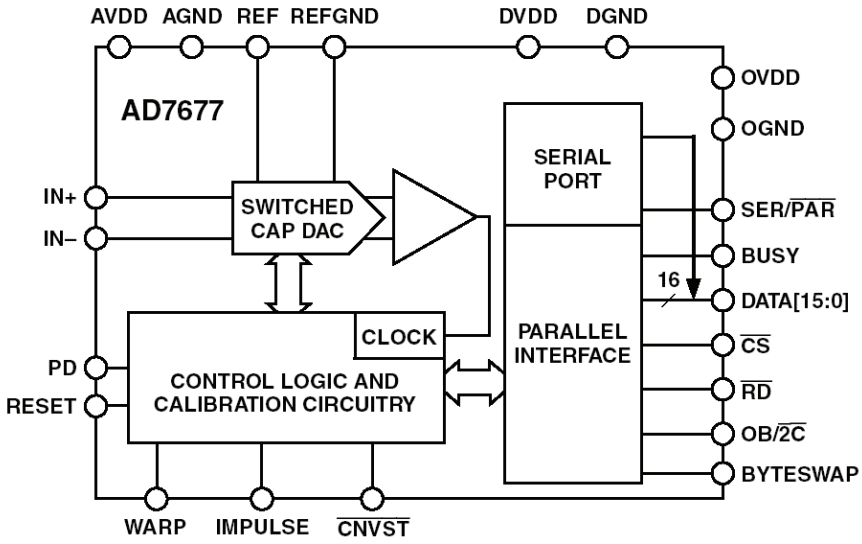


Figure 6.48: *AD7677 16-Bit 1-MSPS Switched Capacitor PulSAR ADC*

In a SAR ADC the proof mass is a voltage provided by the DAC. It is compared to the input, corresponding to the test mass, by the comparator. Keeping track of output of each test and setting the DAC is accomplished by the successive approximation register.

The digital output is basically serial in nature, but SAR ADCs are generally available in both serial and parallel output formats.

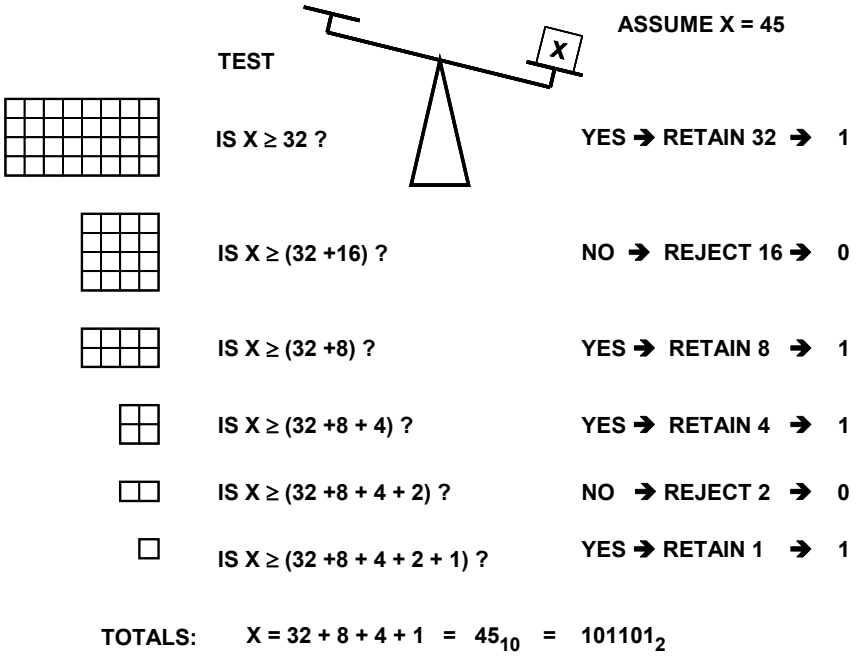


Figure 6.49: *Successive Approximation ADC Algorithm*

Flash Converters

Flash ADCs (sometimes called *parallel* ADCs) are the fastest type of ADC and use large numbers of comparators. An N-bit flash ADC consists of 2^N resistors and $2^N–1$ comparators arranged as in Figure 6.50. Each comparator has a reference voltage which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a "1" logic output, and all the comparators above that point will have a reference voltage larger than the input voltage and a "0" logic output. The $2^N–1$ comparator outputs therefore behave in a way analogous to a mercury thermometer, and the output code at this point is sometimes called a *thermometer* code. Since $2^N–1$ data outputs are not really practical, they are processed by a decoder to generate an N-bit binary output.

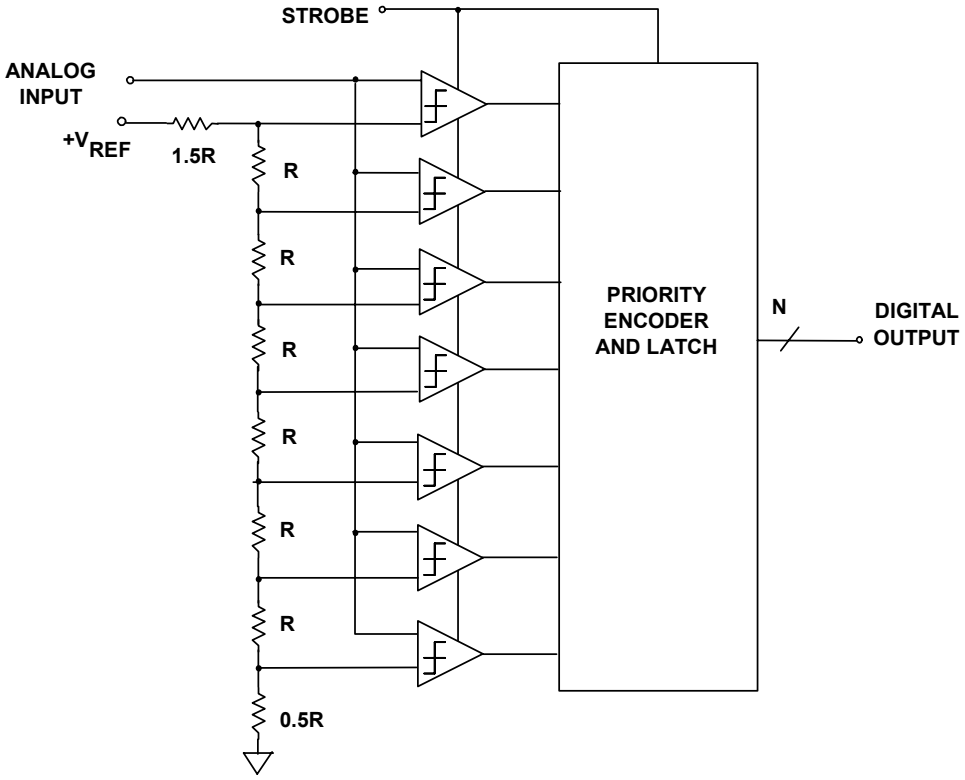


Figure 6.50: *3-Bit All-Parallel (Flash) Converter*

The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder N-bit output by only a few gate delays on top of that, so the process is very fast. However, the architecture uses large numbers of resistors and comparators and is limited to low resolutions, and if it is to be fast, each comparator must run at relatively high power levels. Hence, the problems of flash ADCs include limited resolution, high power dissipation because of the large number of high speed comparators (especially at sampling rates greater than 50 MSPS), and relatively large (and therefore expensive) chip sizes. In addition, the resistance of the reference resistor chain must be kept low to supply

adequate bias current to the fast comparators, so the voltage reference has to source quite large currents (typically > 10 mA).

Each comparator has a voltage-variable junction capacitance, and this signal-dependent capacitance results in most flash ADCs having reduced ENOB and higher distortion at high input frequencies. For this reason, most flash converters must be driven with a wideband op amp which is tolerant to the capacitive load presented by the converter as well as high speed transients developed on the input.

Power dissipation is always a big consideration in flash converters, especially at resolutions above eight bits. A clever technique was used AD9410 10-bit, 210 MSPS ADC called *interpolation* to minimize the number of preamplifiers in the flash converter comparators and also reduce the power (2.1 W). The method is shown in Figure 6.51 (see reference).

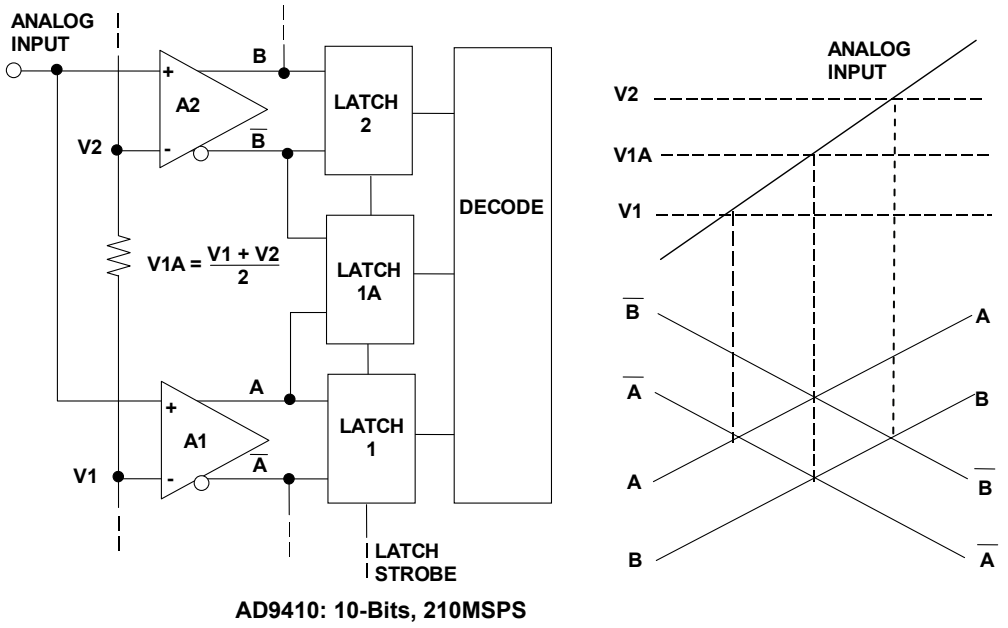


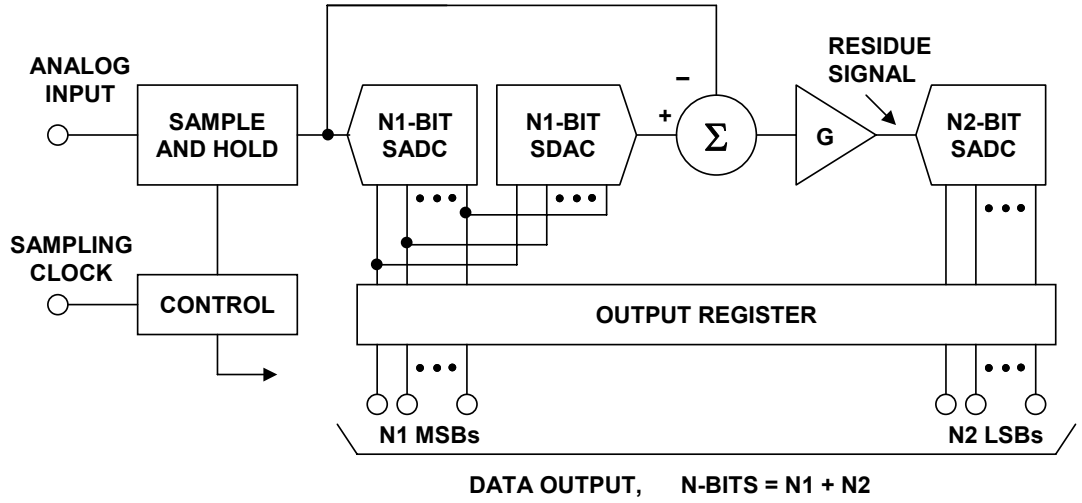
Figure 6.51: *"Interpolating" Flash Reduces the Number of Preamplifiers by Factor of Two*

The preamplifiers (labeled "A1," "A2," etc.) are low-gain g_m stages whose bandwidth is proportional to the tail currents of the differential pairs. Consider the case for a positive-going ramp input which is initially below the reference to AMP A1, V1. As the input signal approaches V1, the differential output of A1 approaches zero (i.e., $A = \overline{A}$), and the decision point is reached. The output of A1 drives the differential input of LATCH 1. As the input signals continues to go positive, A continues to go positive, and $\overline{B}$ begins to go negative. The interpolated decision point is determined when $A = \overline{B}$. As the input continues positive, the third decision point is reached when $B = \overline{B}$. This novel architecture reduces the ADC input capacitance and thereby minimizes its change with signal level and the associated distortion. The AD9410 also uses an input sample-and-hold circuit for improved ac linearity.

Subranging, Error Corrected, and Pipelined ADCs

A basic, two-stage N-bit subranging ADC is shown in Figure 6.52. The ADC is based on two separate conversions—a coarse conversion (N1 bits) in the MSB sub-ADC (SADC) followed by a fine conversion (N2 bits) in the LSB sub-ADC. Early subranging ADCs nearly always used flash converters as building blocks, but a number of recent ADCs utilize other architectures for the individual ADCs.

The conversion process begins placing the sample-and-hold in the hold mode followed by a coarse N1-bit sub-ADC (SADC) conversion of the MSBs. The digital outputs of the MSB converter drive an N1-bit sub-DAC (SDAC) which generates a coarsely quantized version of the analog input signal. The N1-bit SDAC output is subtracted from the held analog signal, amplified, and applied to the N2-bit LSB SADC. The amplifier provides gain, G, sufficient to make the "residue" signal exactly fill the input range of the N2 SADC. The output data from the N1 SADC and the N2 SADC are latched into the output registers yielding the N-bit digital output code, where N = N1 + N2.



See: R. Staffin and R. Lohman, "Signal Amplitude Quantizer," U.S. Patent 2,869,079, Filed December 19, 1956, Issued January 13, 1959

Figure 6.52: *N-bit Two-Stage Subranging ADC*

In order for this simple subranging architecture to work satisfactorily, both the N1 SADC and SDAC (although they only have N1 bits of resolution) must be better than N-bits accurate. The residue signal offset and gain must be adjusted such that it precisely fills the range of the N2 SADC as shown in Figure 3.66A. If the residue signal drifts by more than 1 LSB (referenced to the N2 SADC), then there will be missing codes as shown in Figure 3.66B where the residue signal enters the out-of-range regions labeled "X" and "Y." Any nonlinearity or drift in the N1 SADC will also cause missing codes if it exceeds 1 LSB referenced to N-bits. In practice, an 8-bit subranging ADC with N1 = 4 bits and N2 = 4 bits represents a realistic limit to this architecture in order to maintain no missing codes over a reasonable operating temperature range.

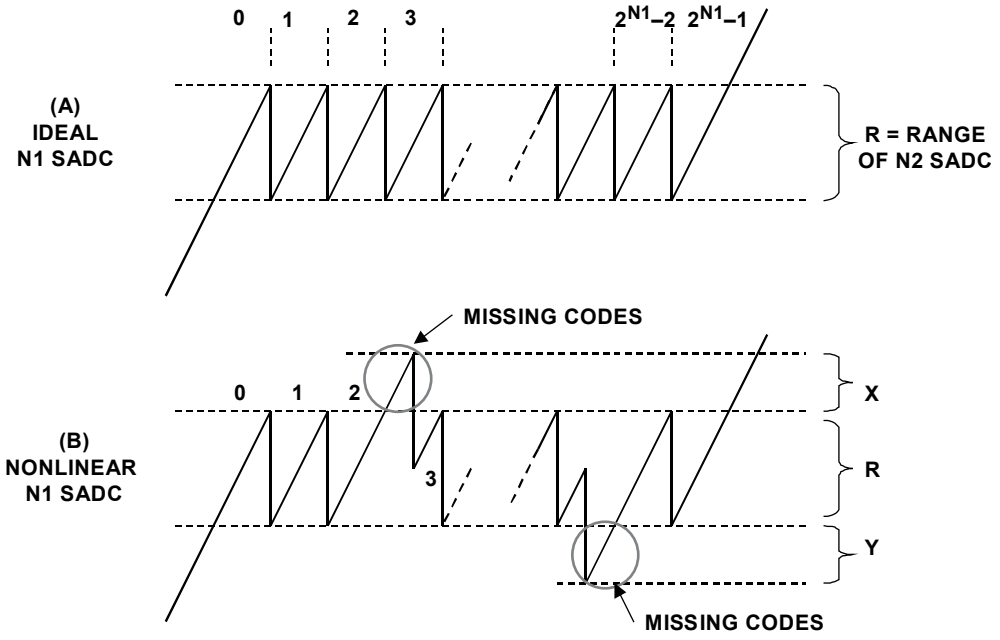


Figure 6.53: *Residue Waveforms at Input of N2 Sub-ADC*

When the interstage alignment is not correct, missing codes will appear in the overall ADC transfer function as shown in Figure 6.54. If the residue signal goes into positive overrange (the "X" region), the output first "sticks" on a code and then "jumps" over a region leaving missing codes. The reverse occurs if the residue signal is negative overrange.

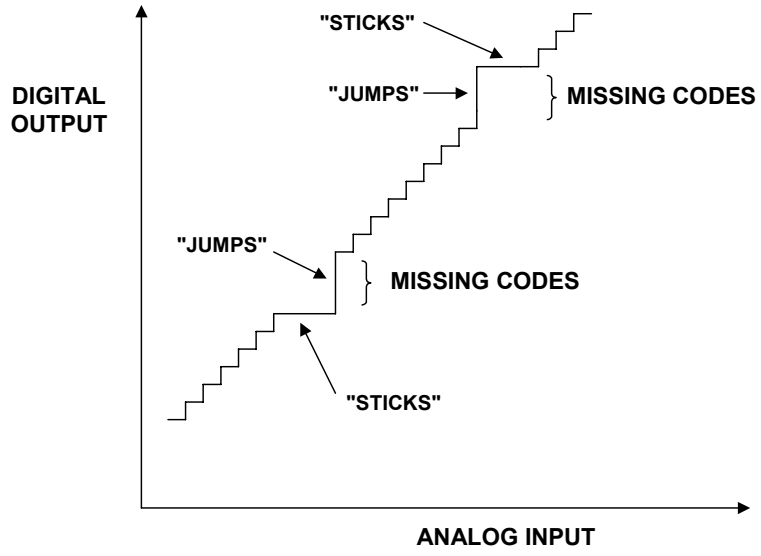


Figure 6.54: *Missing Codes Due to MSB SADC Nonlinearity or Interstage Misalignment*

In order to reliably achieve higher than 8-bit resolution using the subranging approach, a technique generally referred to as *digital corrected subranging*, *digital error correction*, *overlap bits*, *redundant bits*, etc. is utilized.

Figure 6.55 shows two methods that can be used to design a pipeline stage in a subranging ADC. Figure 6.55A shows two pipelined stages which use an interstage T/H in order to provide interstage gain and give each stage the maximum possible amount of time to process the signal at its input. In Figure 6.55B a multiplying DAC is used to provide the appropriate amount of interstage gain as well as the subtraction function.

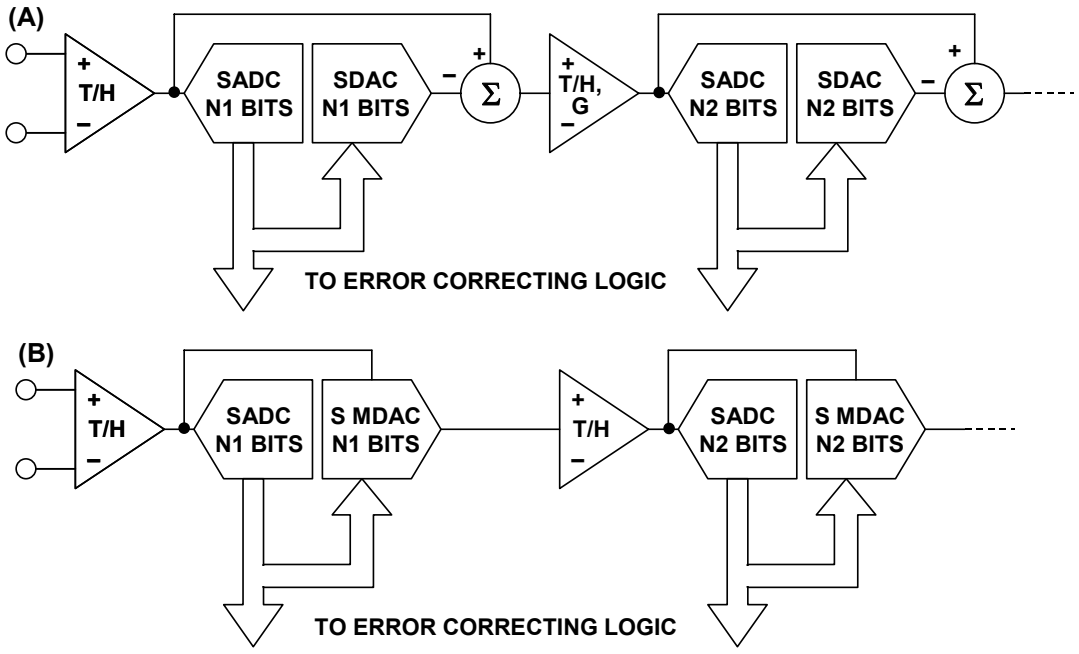


Figure 6.55: *Generalized Pipeline Stages in a Subranging ADC with Error Correction*

The term "pipelined" architecture refers to the ability of one stage to process data from the previous stage during any given clock cycle. At the end of each phase of a particular clock cycle, the output of a given stage is passed on to the next stage using the T/H functions and new data is shifted into the stage. Of course this means that the digital outputs of all but the last stage in the "pipeline" must be stored in the appropriate number of shift registers so that the digital data arriving at the correction logic corresponds to the same sample.

Figure 6.56 shows a timing diagram of a typical pipelined subranging ADC. Notice that the phases of the clocks to the T/H amplifiers are alternated from stage to stage such that when a particular T/H in the ADC enters the hold mode it holds the sample from the preceding T/H, and the preceding T/H returns to the track mode. The held analog signal is passed along from stage to stage until it reaches the final stage in the pipelined ADC—in this case, a flash converter. When operating at high sampling rates, it is critical that the differential sampling clock be kept at a 50% duty cycle for optimum performance. Duty

cycles other than 50% affect all the T/H amplifiers in the chain—some will have longer than optimum track times and shorter than optimum hold times; while others suffer exactly the reverse condition. Several newer pipelined ADCs including the 12-bit, 65-MSPS AD9235 and the 12-bit, 210-MSPS AD9430 have on-chip clock conditioning circuits to control the internal duty cycle while allowing some variation in the external clock duty cycle.

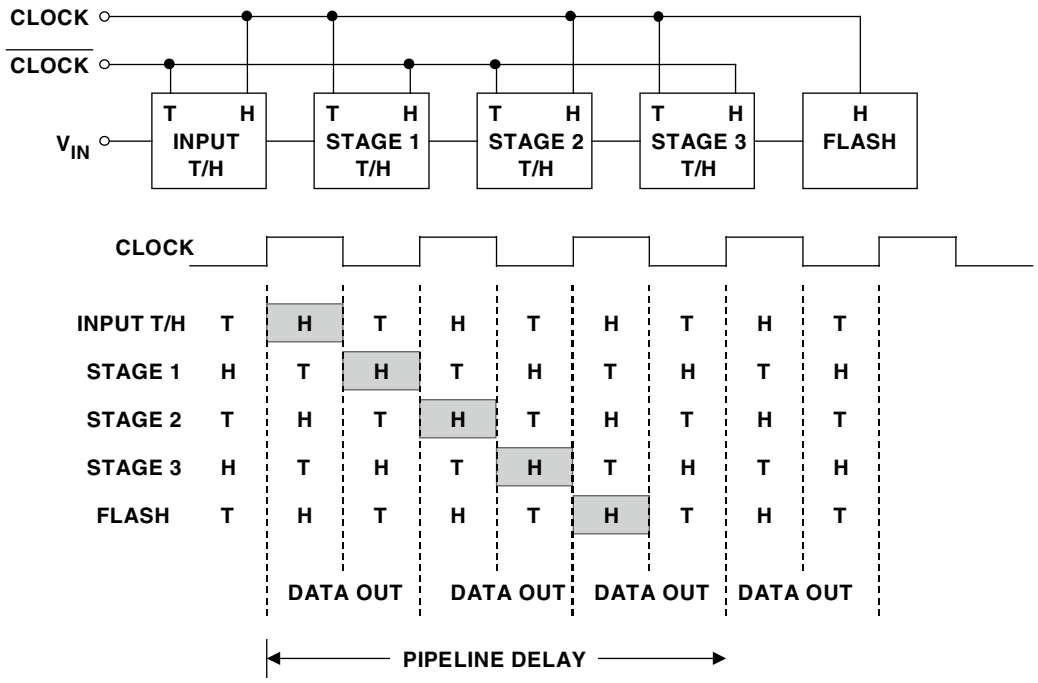


Figure 6.56: *Clock Issues in Pipelined ADCs*

The effects of the "pipeline" delay (sometimes called latency) in the output data as shown in Figure 6.57 for the AD9235 12-bit 65-MSPS ADC where there is a 7-clock cycle pipeline delay.

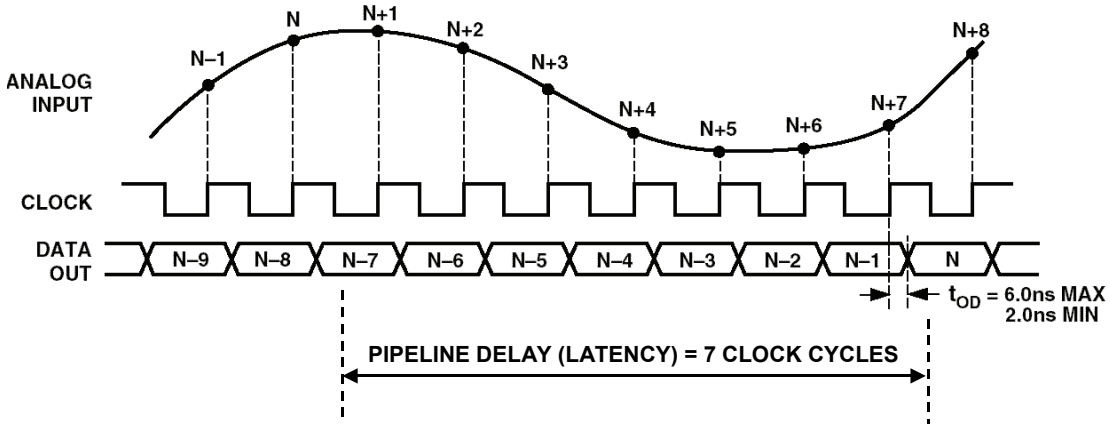


Figure 6.57: *Typical Pipelined ADC Timing for AD9235 12-Bit, 65-MSPS ADC*

Note that the pipeline delay is a function of the number of stages and the particular architecture of the ADC under consideration—the data sheet should always be consulted for the exact details of the relationship between the sampling clock and the output data timing. In many applications the pipeline delay will not be a problem, but if the ADC is inside a feedback loop the pipeline delay may cause instability. The pipeline delay can also be troublesome in multiplexed applications or when operating the ADC in a "single-shot" mode. Other ADC architectures—such as successive approximation—may be better suited to these types of applications.

The pipelined error correcting ADC has become very popular in modern ADCs requiring wide dynamic range and low levels of distortion. There are many possible ways to design a pipelined ADC, and we will now look at just a few of the tradeoffs. Figure 6.58A shows a pipelined ADC designed with identical stages of k-bits each. This architecture uses the same core hardware in each stage, offers a few other advantages, but does necessarily optimize the ADC for best possible performance. Figure 6.58B shows the simplest form of this architecture where k = 1.

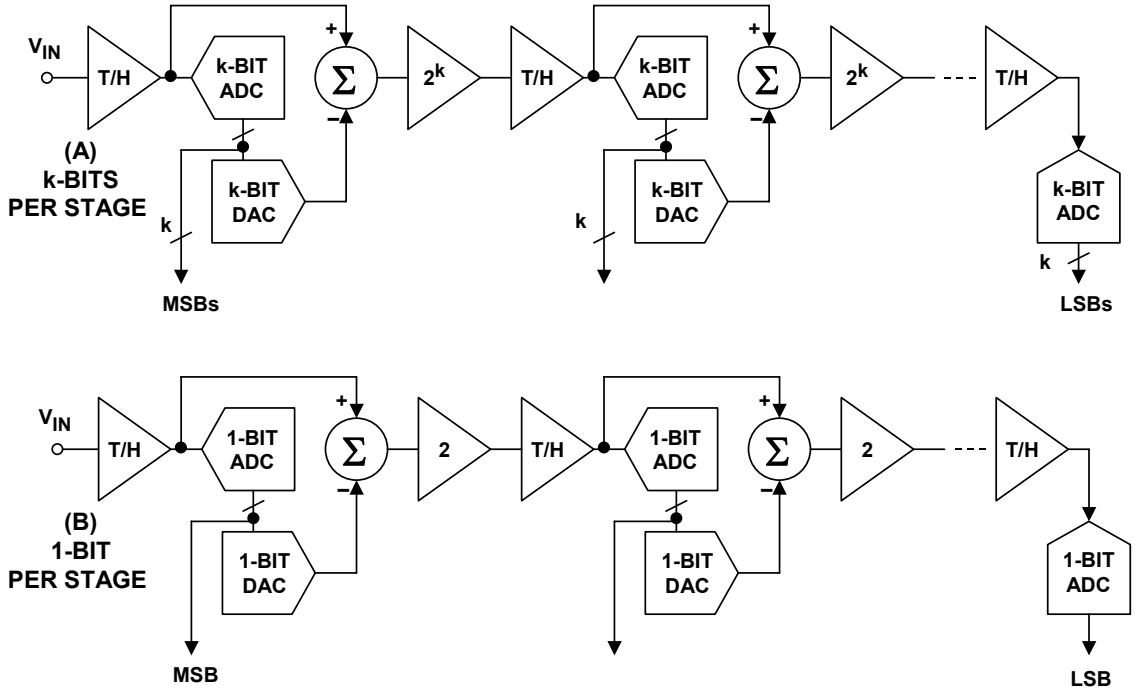


Figure 6.58: *Basic Pipelined ADC with Identical Stages*

In order to optimize performance at the 12-bit level, for example, 1-bit per stage pipeline is more commonly used with a multibit front-end and back-end ADC as shown in Figure 6.59.

Another less popular type of error corrected subranging architecture is the *recirculating* subranging ADC. The concept is similar to the error corrected subranging architecture previously discussed, but in this architecture, the residue signal is recirculated through a single ADC and DAC stage using switches and a programmable gain amplifier (PGA).

The major problem with this technique is the PGA. Its gain bandwidth product will limit the frequency response at higher gains. Also matching of the various gains could be problematic.

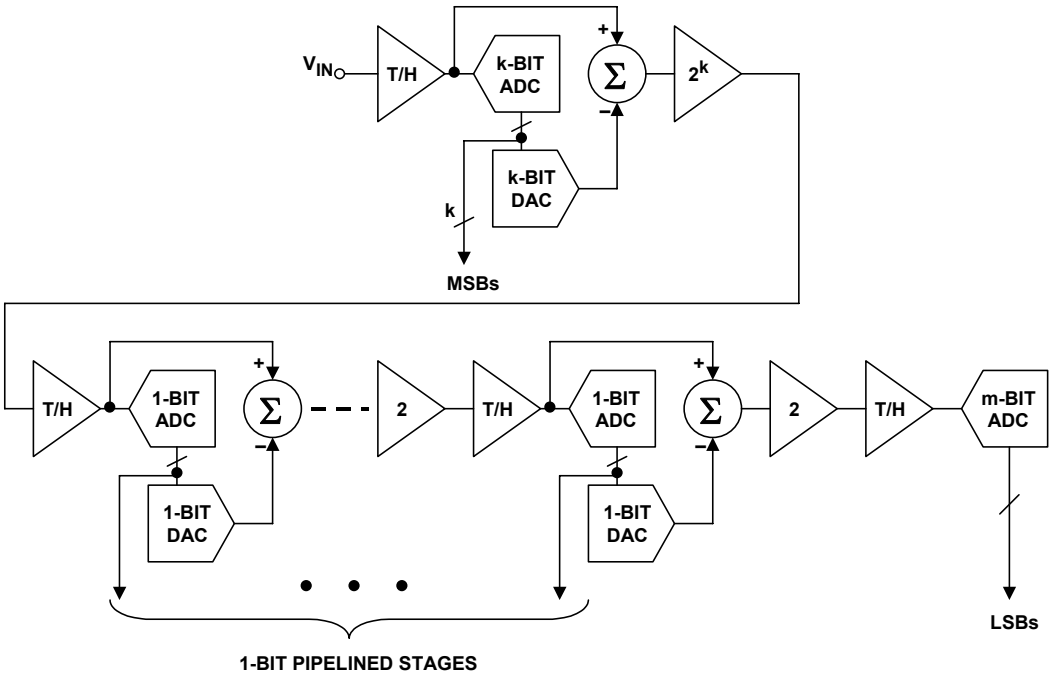


Figure 6.59: *Multibit and 1-Bit Pipelined Core Combined*

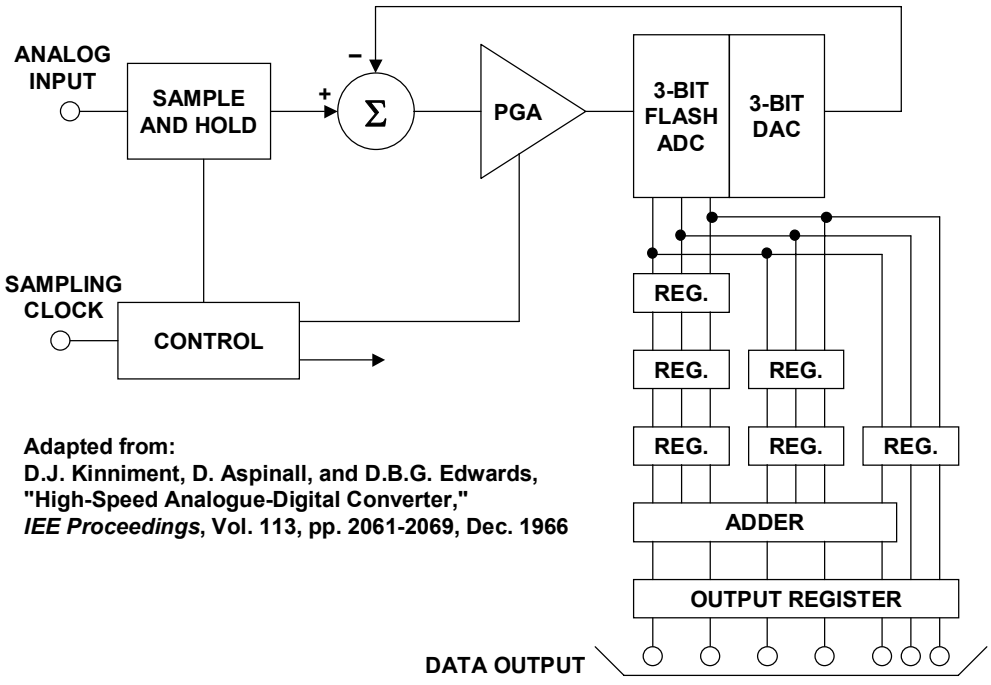
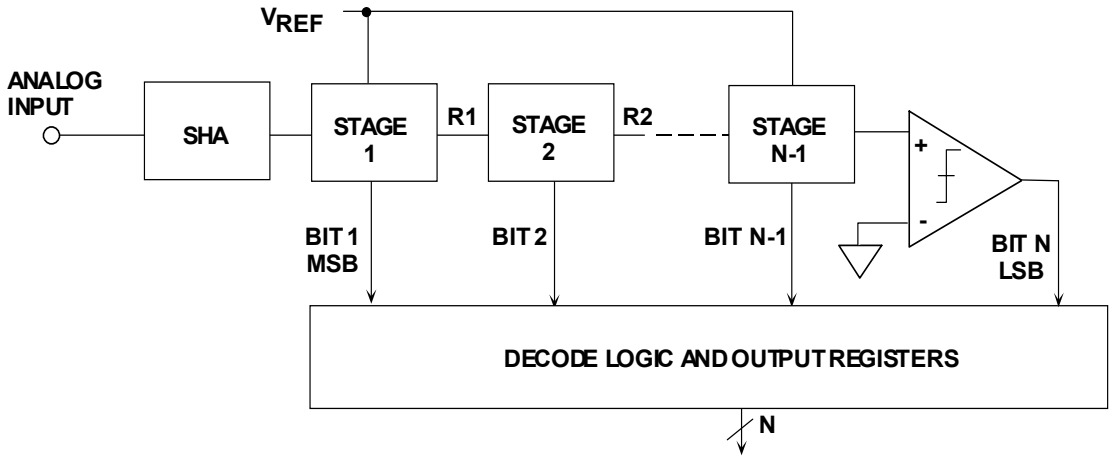


Figure 6.60: *Kinniment, et. al., 1966 Pipelined 7-bit, 9-MSPS Recirculating ADC Architecture*

Serial Bit-Per-Stage Binary and Gray Coded (Folding) ADCs

Various architectures exist for performing A/D conversion using one stage per bit. Figure 6.61 shows the overall concept. In fact, a multistage subranging ADC with one bit per stage and no error correction is one form as previously discussed. In this approach, the input signal must be held constant during the entire conversion cycle. There are N stages, each of which has a bit output and a *residue* output. The residue output of one stage is the input to the next. The last bit is detected with a single comparator as shown.



B. D. Smith, "An Unusual Electronic Analog-Digital Conversion Method," *IRE Transactions on Instrumentation*, June 1956, pp. 155-160.

Figure 6.61: *Generalized Bit-Per-Stage ADC Architecture*

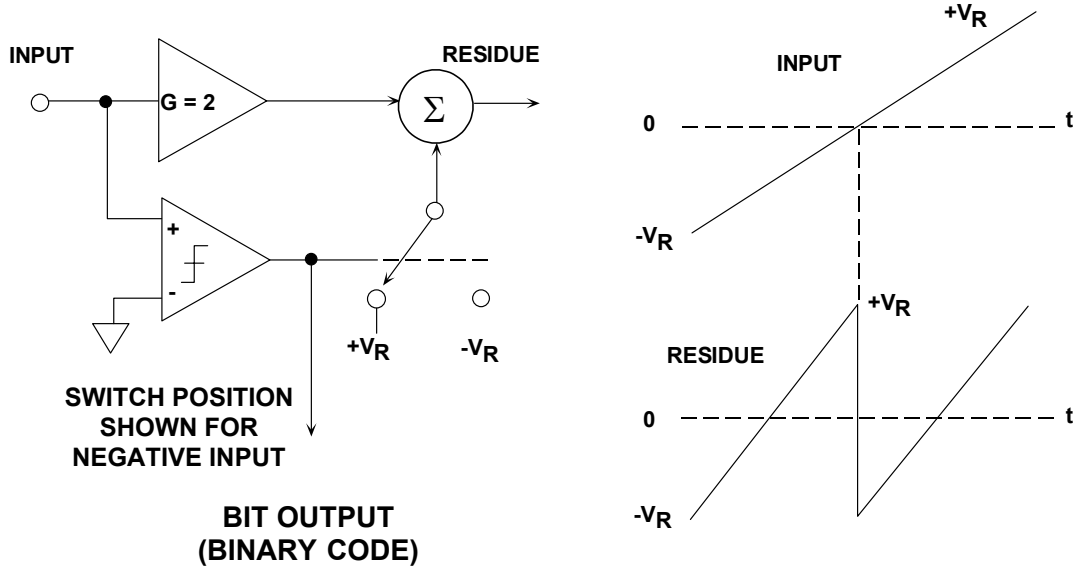


Figure 6.62: *Single-Stage Transfer Function for Binary ADC*

The basic stage for performing a single binary bit conversion is shown in Figure 6.62. It consists of a gain-of-two amplifier, a comparator, and a 1-bit DAC. Assume that this is the first stage of the ADC. The MSB is simply the polarity of the input, and that is detected with the comparator which also controls the 1-bit DAC. The 1-bit DAC output is summed with the output of the gain-of-two amplifier. The resulting residue output is then applied to the next stage. In order to better understand how the circuit works, the diagram shows the residue output for the case of a linear ramp input voltage which traverses the entire ADC range, $-V_R$ to $+V_R$. Notice that the polarity of the residue output determines the binary bit output of the next stage.

A simplified 3-bit serial-binary ADC is shown in Figure 6.63, and the residue outputs are shown in Figure 6.64. Again, the case is shown for a linear ramp input voltage whose range is between $-V_R$ and $+V_R$. Each residue output signal has discontinuities which correspond to the point where the comparator changes state and causes the DAC to switch. The fundamental problem with this architecture is the discontinuity in the residue output waveforms. Adequate settling time must be allowed for these transients to propagate through all the stages and settle at the final comparator input. As presented here, the prospects of making this architecture operate at high speed are dismal. However using the 1.5-bit-per stage pipelined architecture previously discussed in this section makes it much more attractive at high speeds.

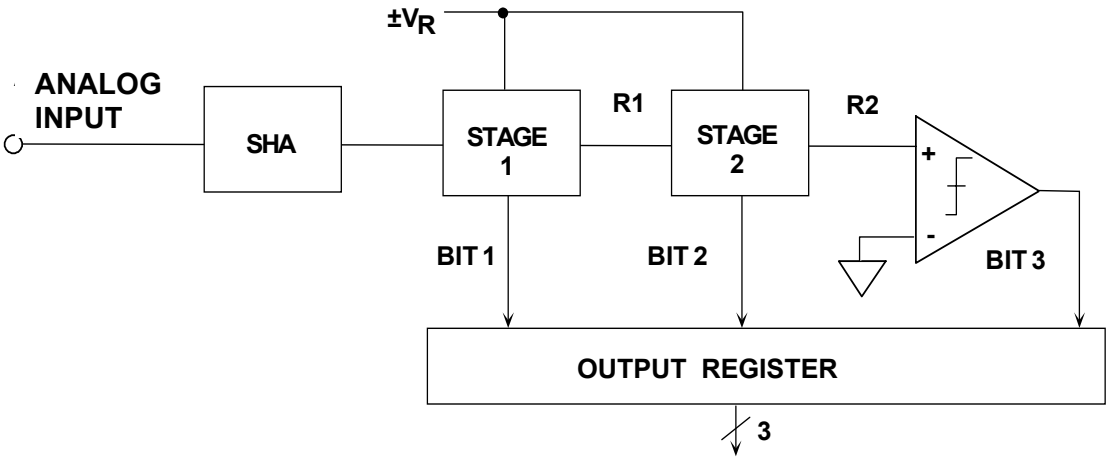


Figure 6.63: *3-Bit Serial ADC with Binary Output*

Although the binary method is discussed in his paper, B. D. Smith also describes a much preferred bit-per-stage architecture based on absolute value amplifiers (magnitude amplifiers, or simply *MagAMPs*™). This scheme has often been referred to as *serial-Gray* (since the output coding is in Gray code), or *folding* converter because of the shape of the transfer function. Performing the conversion using a transfer function that produces an initial Gray code output has the advantage of minimizing discontinuities in the residue output waveforms and offers the potential of operating at much higher speeds than the binary approach.

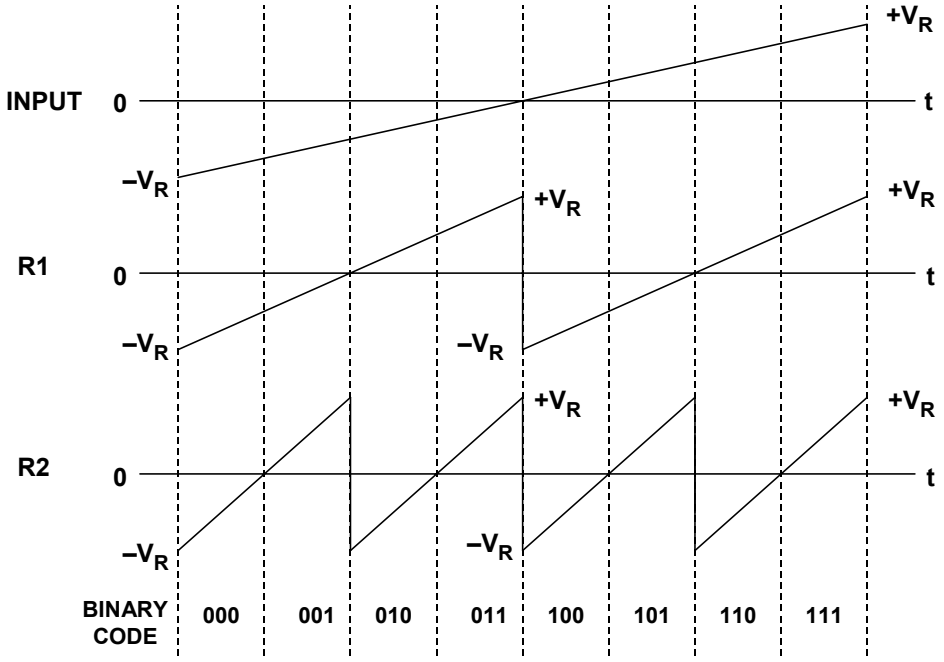


Figure 6.64: *Input and Residue Waveforms of 3-Bit Binary Ripple ADC*

The basic folding stage is shown functionally in Figure 6.65 along with its transfer function. The input to the stage is assumed to be a linear ramp voltage whose range is between $-V_R$ and $+V_R$. The comparator detects the polarity of the input signal and provides the Gray bit output for the stage. It also determines whether the overall stage gain is +2 or –2. The reference voltage V_R is summed with the switch output to generate the residue signal which is applied to the next stage. The polarity of the residue signal determines the Gray bit for the next stage. The transfer function for the folding stage is also shown in Figure 6.65.

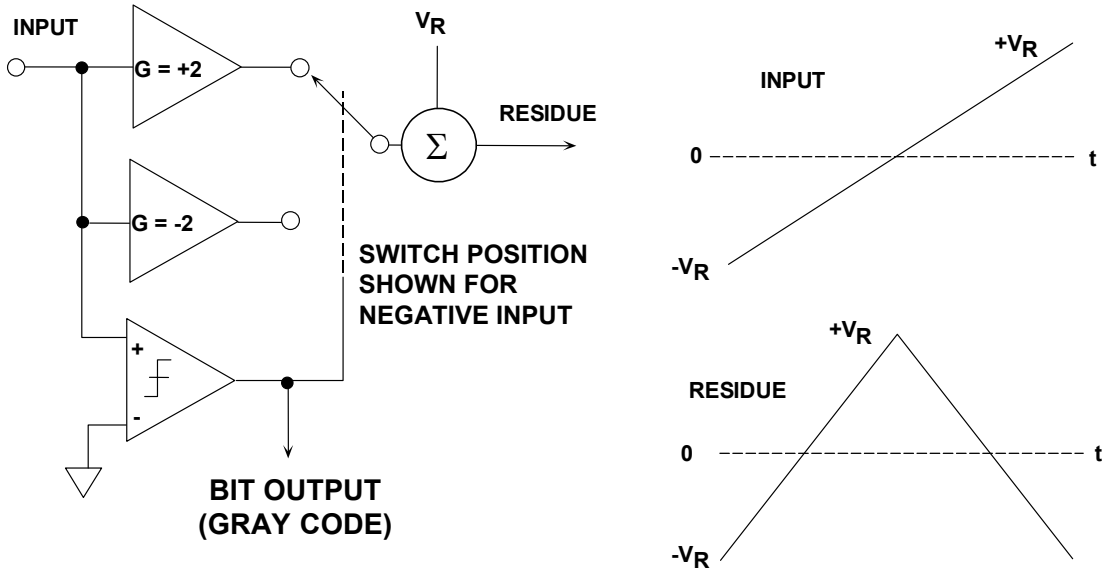


Figure 6.65: *Folding Stage Functional Equivalent Circuit*

A 3-bit MagAMP folding ADC is shown in Figure 6.66, and the corresponding residue waveforms in Figure 6.67. As in the case of the binary ripple ADC, the polarity of the residue output signal of a stage determines the value of the Gray bit for the next stage. The polarity of the input to the first stage determines the Gray MSB; the polarity of R1 output determines the Gray bit-2; and the polarity of R2 output determines the Gray bit-3. Notice that unlike the binary ripple ADC, there is no abrupt transition in any of the folding stage residue output waveforms. This makes operation at high speeds quite feasible.

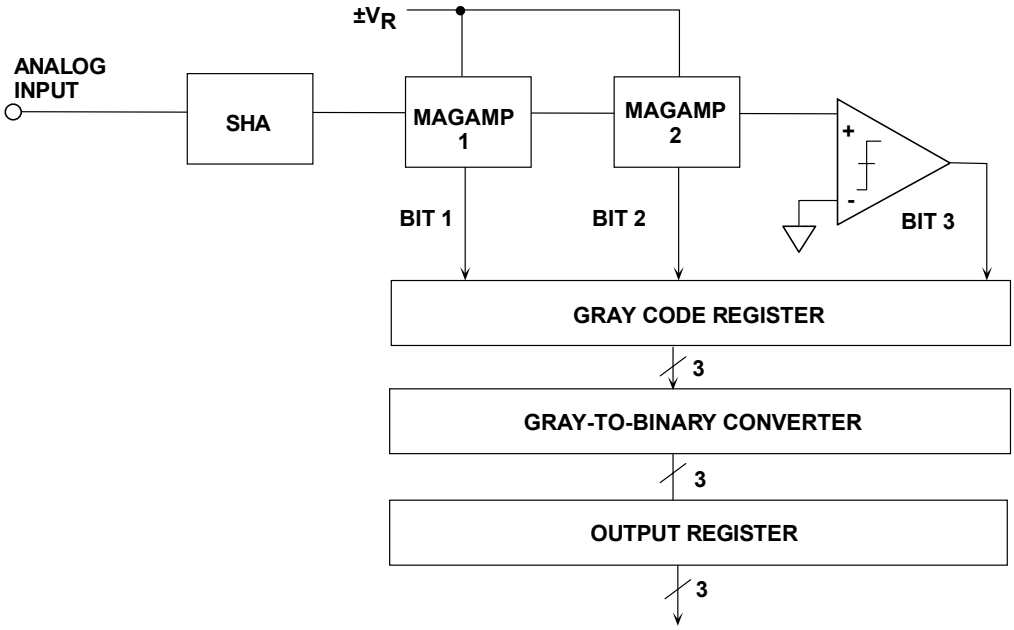


Figure 6.66: *3-bit Folding ADC Block Diagram*

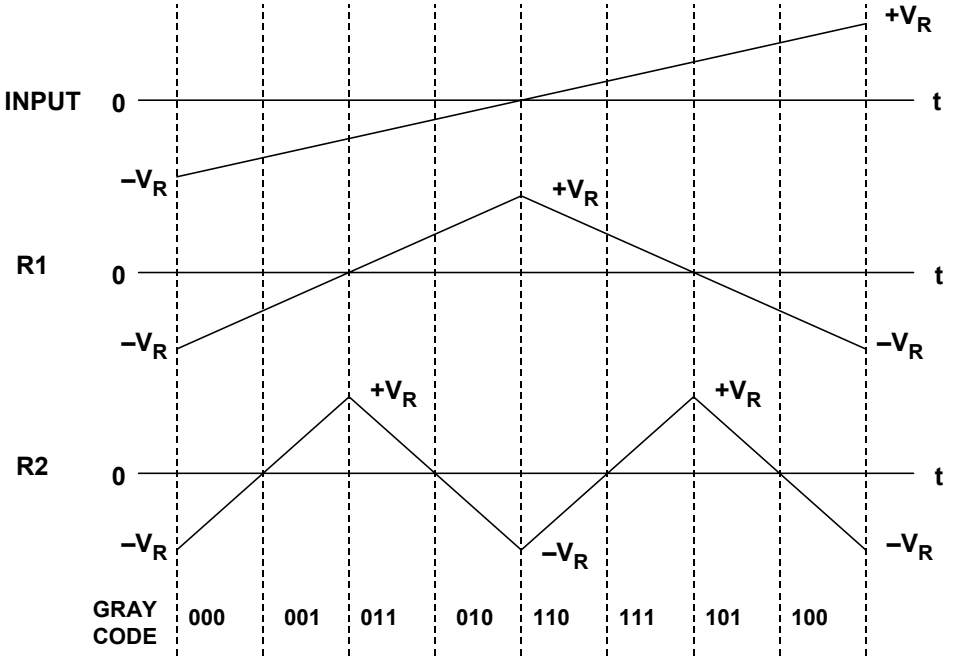


Figure 6.67: *Input and Residue Waveforms for 3-Bit Folding ADC*

Modern IC circuit designs implement the transfer function using current-steering open-loop gain techniques which can be made to operate much faster. Fully differential stages (including the SHA) also provide speed, lower distortion, and yield 8-bit accurate folding stages with no requirement for thin film resistor laser trimming.

An example of a fully differential gain-of-two MagAMP folding stage is shown in Figure 6.68. The differential input signal is applied to the degenerated-emitter differential pair Q1, Q2 and the comparator. The differential input voltage is converted into a differential current which flows in the collectors of Q1, Q2. If +IN is greater than –IN, cascode-connected transistors Q3, Q6 are on, and Q4, Q6 are off. The differential signal currents therefore flow through the collectors of Q3, Q6 into level-shifting transistors Q7, Q8, and into the output load resistors, developing the differential output voltage between +OUT and –OUT. The overall differential voltage gain of the circuit is two.

If +IN is less than –IN (negative differential input voltage), the comparator changes stage and turns Q4, Q5 on and Q3, Q6 off. The differential signal currents flow from Q5 to Q7 and from Q4 to Q8, thereby maintaining the same relative polarity at the differential output as for a positive differential input voltage. The required offset voltage is developed by adding a current I_{OFF} to the emitter current of Q7 and subtracting it from the emitter current of Q8.

The differential residue output voltage of the stage drives the next stage input, and the comparator output represents the Gray code output for the stage.

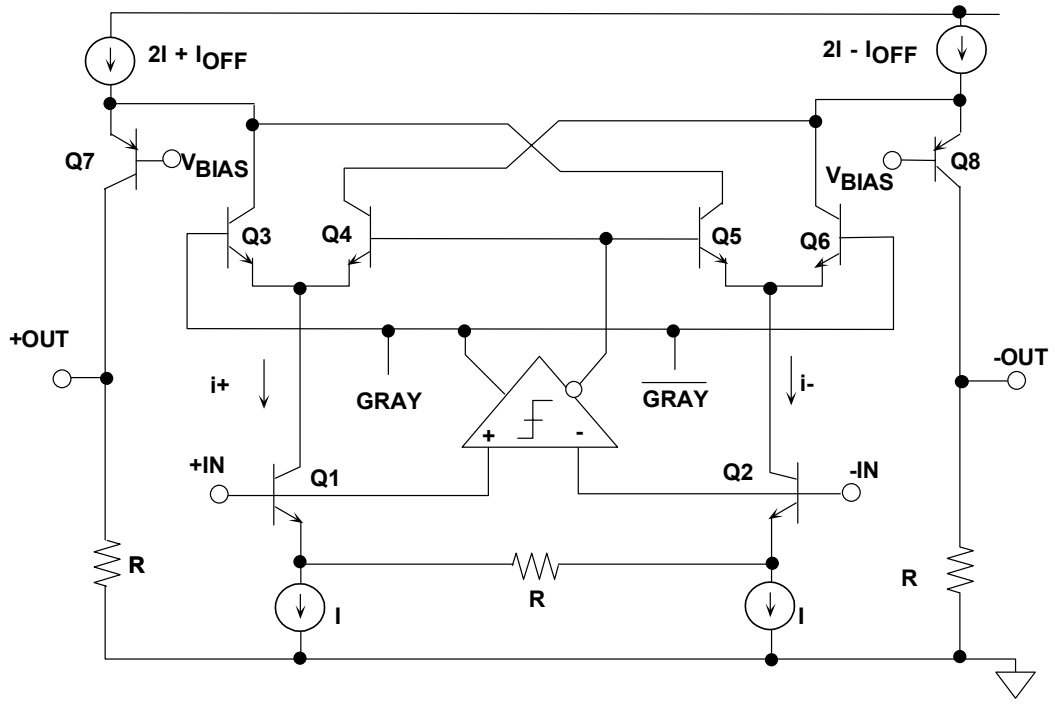


Figure 6.68: *A Modern Current-Steering MagAMP Stage*

The MagAMP architecture offers lower power and can be extended to sampling rates previously dominated by flash converters. For example, the AD9054A 8-bit, 200 MSPS ADC is shown in Figure 6.69. The first five bits (Gray code) are derived from five differential MagAMP stages. The differential residue output of the fifth MagAMP stage drives a 3-bit flash converter, rather than a single comparator.

The Gray-code output of the five MagAMPs and the binary-code output of the 3-bit flash are latched, all converted into binary, and latched again in the output data register. Because of the high data rate, a demultiplexed output option is provided.

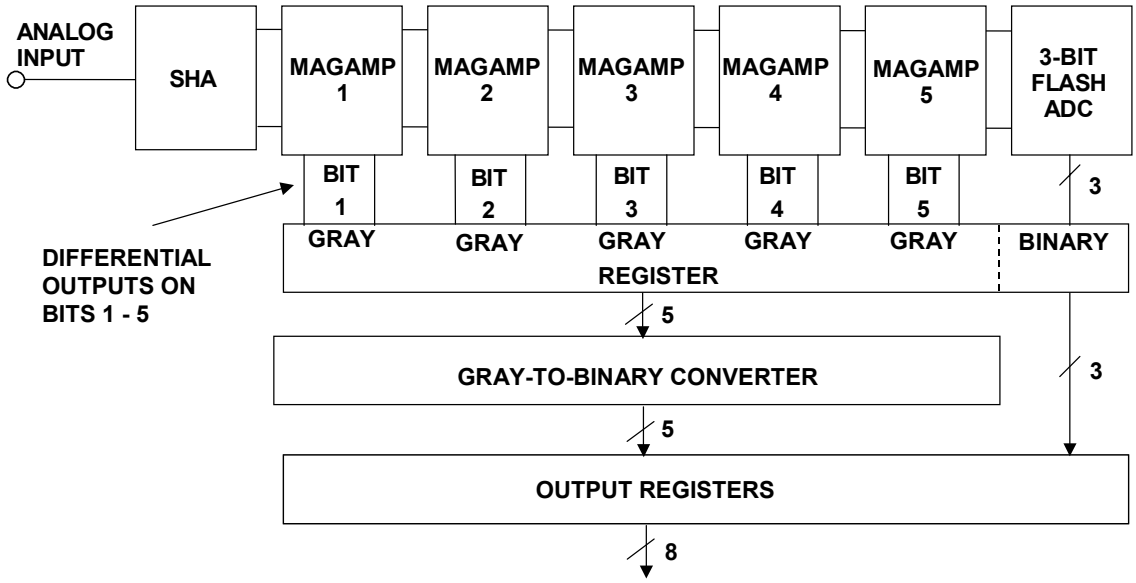
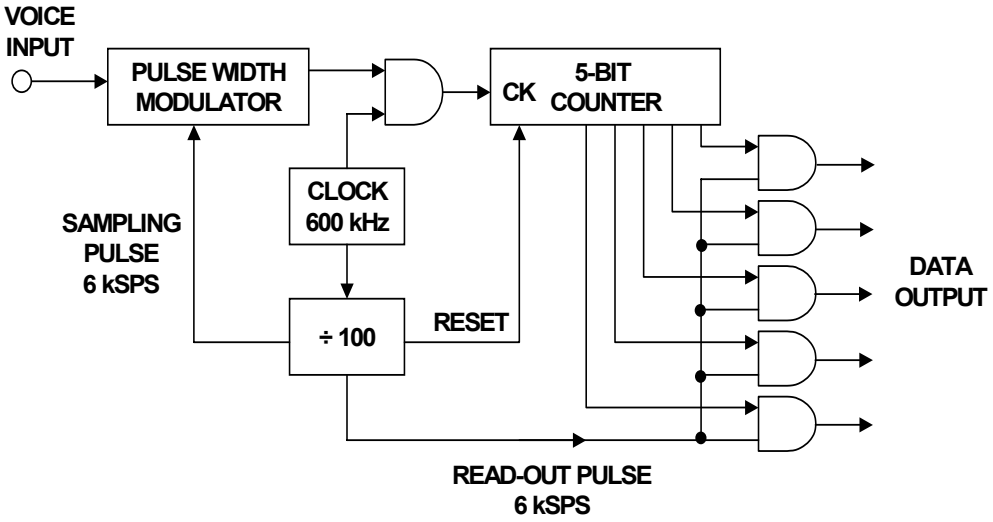


Figure 6.69: *AD9054A 8-bit, 200-MSPS ADC Functional Diagram*

Counting and Integrating ADC Architectures

Although counting-based ADCs are not well suited for high speed applications, they are ideal for high resolution, low frequency applications, especially when combined with integrating techniques.



Adapted from: Alec Harley Reeves, "Electric Signaling System,"
***U.S. Patent 2,272,070*, Filed November 22, 1939, Issued February 3, 1942**

Figure 6.70: *A. H. Reeves' 5-bit Counting ADC*

The counting ADC technique (see Figure 6.70) basically uses a sampling pulse to take a sample of the analog signal, set an R/S flip-flop, and simultaneously start a controlled ramp voltage. The ramp voltage is compared with the input, and when they are equal, a pulse is generated which resets the R/S flip-flop. The output of the flip-flop is a pulse whose width is proportional to the analog signal at the sampling instant. This pulse width modulated (PWM) pulse controls a gated oscillator, and the number of pulses out of the gated oscillator represents the quantized value of the analog signal. This pulse train can be easily converted to a binary word by driving a counter. In Reeves' system, a master clock of 600 kHz was used, and a 100:1 divider generated the 6-kHz sampling pulses. The system uses a 5-bit counter, and 31 counts (out of the 100 counts between sampling pulses) therefore represents a full-scale signal. The technique can obviously be extended to higher resolutions.

Charge Run-Down ADCs

The charge run-down ADC architecture shown in Figure 6.71 first samples the analog input and stores the voltage on a fixed capacitor. The capacitor is then discharged with a constant current source, and the time required for complete discharge is measured using a counter. Notice that in this approach, the overall accuracy is dependent on the magnitude of the capacitor, the magnitude of the current source, as well as the accuracy of the timebase.

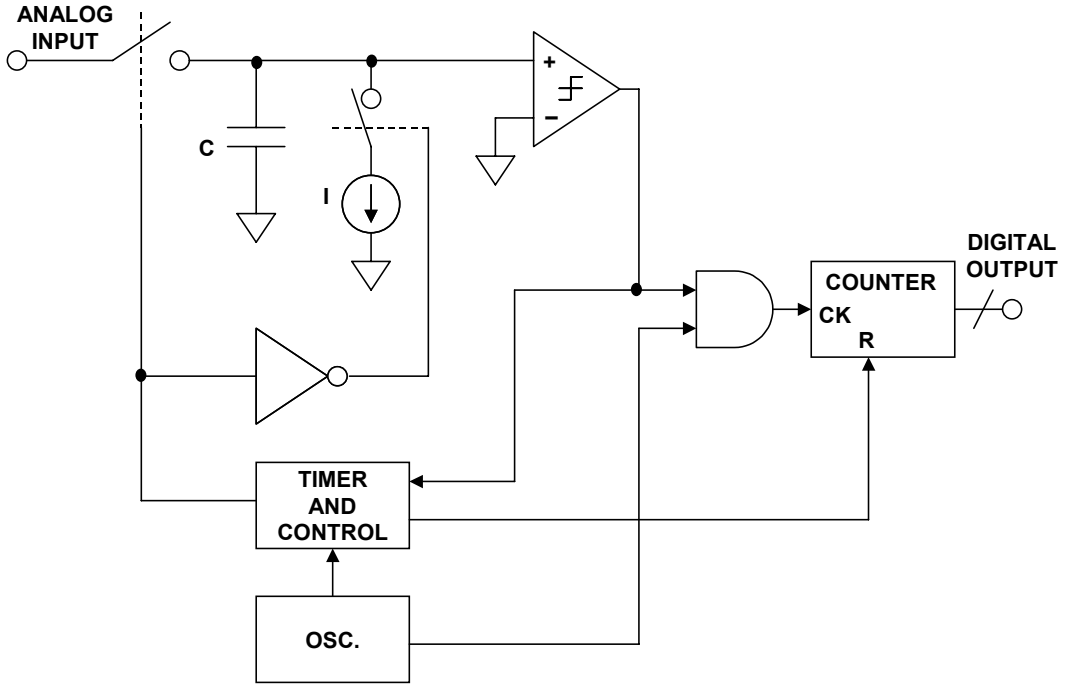


Figure 6.71 *Charge Run-Down ADC*

Ramp Run-Up ADCs

In the ramp run-up architecture shown in Figure 6.71, a ramp generator is started at the beginning of the conversion cycle. The counter then measures the time required for the ramp voltage to equal the analog input voltage. The counter output is therefore proportional to the value of the analog input. In an alternate version (shown dotted in Figure 6.72), the ramp voltage generator is replaced by a DAC which is driven by the counter output. The advantage of using the ramp is that the ADC is always monotonic, whereas overall monotonicity is determined by the DAC when it is used as a substitute.

The accuracy of the ramp run-up ADC depends on the accuracy of the ramp generator (or the DAC) as well as the oscillator.

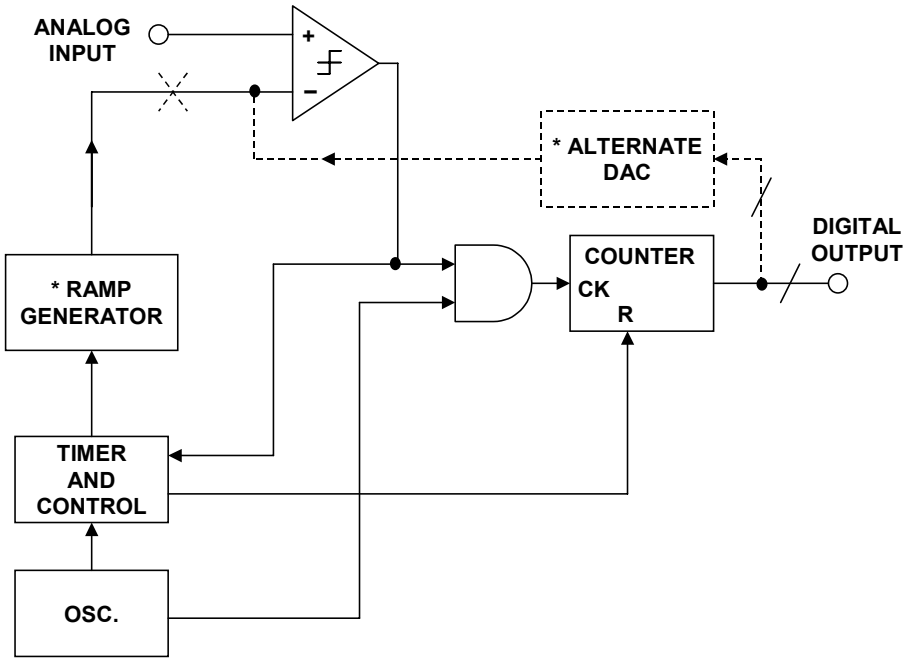


Figure 6.72: *Ramp Run-Up ADC*

Tracking ADCs

The tracking ADC architecture shown in Figure 6.73 continually compares the input signal with a reconstructed representation of the input signal. The up/down counter is controlled by the comparator output. If the analog input exceeds the DAC output, the counter counts up until they are equal. If the DAC output exceeds the analog input, the counter counts down until they are equal. It is evident that if the analog input changes slowly, the counter will follow, and the digital output will remain close to its correct value. If the analog input suddenly undergoes a large step change, it will be many hundreds or thousands of clock cycles before the output is again valid. The tracking ADC therefore responds quickly to slowly changing signals, but slowly to a quickly changing one.

The simple analysis above ignores the behavior of the ADC when the analog input and DAC output are nearly equal. This will depend on the exact nature of the comparator and counter. If the comparator is a simple one, the DAC output will cycle by 1 LSB from just above the analog input to just below it, and the digital output will, of course, do the same —there will be 1 LSB of flicker. Note that the output in such a case steps every clock cycle, irrespective of the exact value of analog input, and hence always has unity Mark/Space ratio. In other words, there is no possibility of taking a mean value of the digital output and increasing resolution by oversampling.

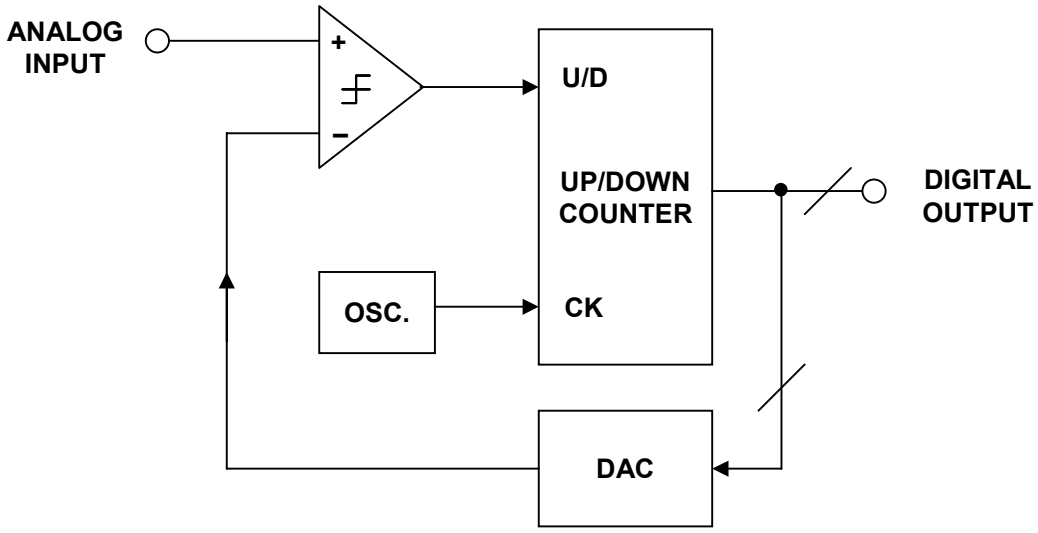


Figure 6.73: *Tracking ADC*

A more satisfactory, but more complex arrangement would be to use a window comparator with a window 1-2 LSB wide. When the DAC output is high or low the system behaves as in the previous description, but if the DAC output is within the window, the counter stops. This arrangement eliminates the flicker, provided that the DAC DNL never allows the DAC output to step across the window for 1 LSB change in code.

Tracking ADCs are not very common. Their slow step response makes them unsuitable for many applications, but they do have one asset: their output is *continuously* available. Most ADCs perform conversions: i.e., on receipt of a "start convert" command (which may be internally generated), they perform a conversion and, after a delay, a result becomes available. Providing that the analog input changes slowly, the output of a tracking ADC is always available. This is valuable in synchro-to-digital and resolver to digital converters (SDCs and RDCs), and this is the application where tracking ADCs are most often used. Another valuable characteristic of tracking ADCs is that a fast transient on the analog input causes the output to change only one count. This is very useful in noisy environments. Notice the similarity between a tracking ADC and a successive approximation ADC. Replacing the up/down counter with SAR logic yields the architecture for a successive approximation ADC.

Voltage-to-Frequency Converters (VFCs)

A voltage-to-frequency converter (VFC) is an oscillator whose frequency is linearly proportional to a control voltage (a high accuracy VCO). The VFC/counter ADC is monotonic and free of missing codes, integrates noise, and can consume very little power. It is also very useful for telemetry applications, since the VFC, which is small, cheap, and low-powered can be mounted on the experimental subject (patient, wild animal, artillery shell, etc.) and communicate with the counter by a telemetry link as shown in Figure 6.74.

There are two common VFC architectures: the *current- steering multivibrator VFC* and the *charge-balance VFC*. The charge-balanced VFC may be made in *asynchronous* or *synchronous* (clocked) forms. There are many more VFO (variable frequency oscillator) architectures, including the ubiquitous 555 timer, but the key feature of VFCs is linearity—few VFOs are very linear.

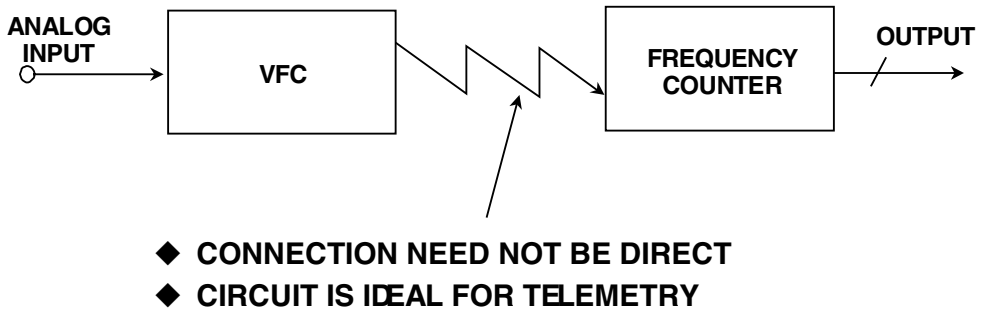


Figure 6.74: *Voltage-to-Frequency Converter (VFC) and Frequency Counter Make a Low Cost, Versatile, High-Resolution ADC*

The current-steering multivibrator VFC is actually a current-to-frequency converter rather than a VFC, but, as shown in Figure 6.75, practical circuits invariably contain a voltage-to-current converter at the input. The principle of operation is evident: the current discharges the capacitor until a threshold is reached, and when the capacitor terminals are reversed, the half-cycle repeats itself. The waveform across the capacitor is a linear tri-wave, but the waveform on either terminal with respect to ground is the more complex waveform shown.

Practical VFCs of this type have linearities around 14-bits, and comparable stability, although they may be used in ADCs with higher resolutions without missing codes. The performance limits are set by comparator threshold noise, threshold temperature coefficient, and the stability and dielectric absorption (DA) of the capacitor, which is generally a discrete component. The comparator/voltage reference structure shown in the diagram is more of a representation of the function performed than the actual circuit used, which is much more integrated with the switching, and correspondingly harder to analyze.

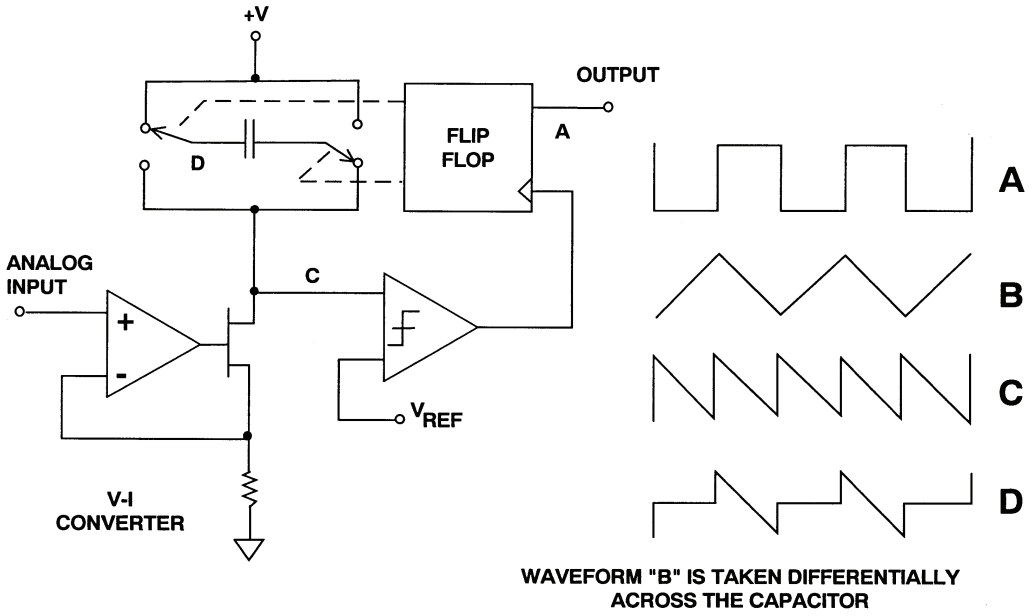


Figure 6.75: *A Current Steering VFC*

This type of VFC is simple, inexpensive, and low powered, and most run from a wide range of supply voltages. They are ideally suited for low cost medium accuracy (12 bit) ADC and data telemetry applications.

The charge balance VFC shown in Figure 6.76 is more complex, more demanding in its supply voltage and current requirements, and more accurate. It is capable of 16-bit to 18-bit linearity.

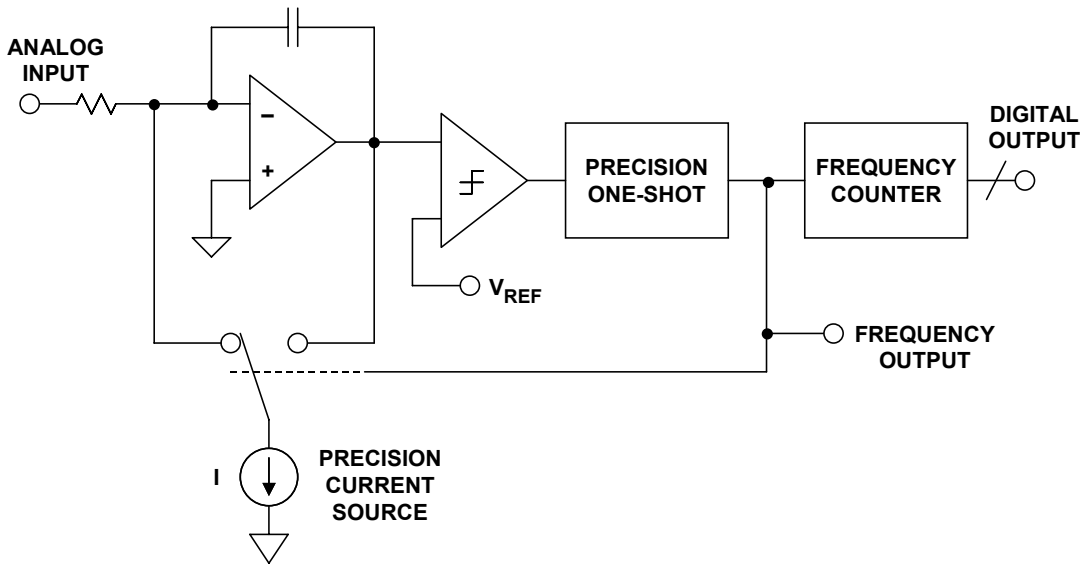


Figure 6.76: *Charge Balance Voltage-to-Frequency Converter (VFC)*

The integrator capacitor charges from the signal as shown in Figure 6.76. When it passes the comparator threshold, a fixed charge is removed from the capacitor, but the input current continues to flow during the discharge, so no input charge is lost. The fixed charge is defined by the precision current source and the pulse width of the precision monostable. The output pulse rate is thus accurately proportional to the rate at which the integrator charges from the input.

At low frequencies, the limits on the performance of this VFC are set by the stability of the current source and the monostable timing (which depends on the monostable capacitor, among other things). The absolute value and temperature stability of the integration capacitor do not affect the accuracy, although its leakage and dielectric absorption (DA) do. At high frequencies, second-order effects, such as switching transients in the integrator and the precision of the monostable when it is retriggered very soon after the end of a pulse, take their toll on accuracy and linearity.

The changeover switch in the current source addresses the integrator transient problem. By using a changeover switch instead of the on/off switch more common on older VFC designs: (a) there are no on/off transients in the precision current source and (b) the output stage of the integrator sees a constant load—most of the time the current from the source flows directly in the output stage; during charge balance, it still flows in the output stage, but through the integration capacitor.

The stability and transient behavior of the precision monostable present more problems, but the issue may be avoided by replacing the monostable with a clocked bistable multivibrator. This arrangement is known as a *synchronous* VFC or SVFC and is shown in Figure 6.77.

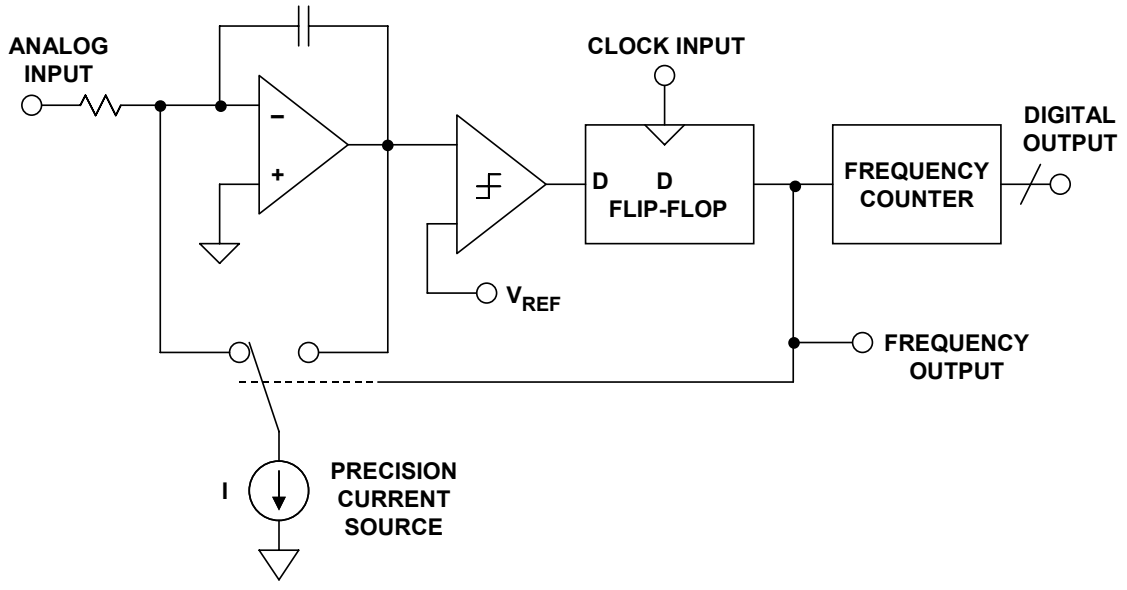


Figure 6.77: *Synchronous VFC (SVFC)*

The difference from the previous circuit is quite small, but the charge balance pulse length is now defined by two successive edges of the external clock. If this clock has low jitter, the charge will be very accurately defined. The output pulse will also be synchronous with the clock. SVFCs of this type are capable of up to 18-bit linearity and excellent temperature stability.

This synchronous behavior is convenient in many applications, since synchronous data transfer is often easier to handle than asynchronous. It does mean, however, that the output of an SVFC is not a pure tone (plus harmonics, of course) like a conventional VFC, but contains components harmonically related to the clock frequency. The display of an SVFC output on an oscilloscope is especially misleading and is a common cause of confusion—a change of input to a VFC produces a smooth change in the output frequency, but a change to an SVFC produces a change in probability density of output pulses N and N+1 clock cycles after the previous output pulse, which is often misinterpreted as severe jitter and a sign of a faulty device (see Figure 6.78).

Another problem with SVFCs is nonlinearity at output frequencies related to the clock frequency. If we study the transfer characteristic of an SVFC, we find nonlinearities close to sub-harmonics of the clock frequency F_C as shown in Figure 6.79. They can be found at $F_C/3$, $F_C/4$, and $F_C/6$. This is due to stray capacitance on the chip (and in the circuit layout!) and coupling the clock signal into the SVFC comparator which causes the device to behave as an injection-locked, phase-locked loop (PLL). This problem is intrinsic to SVFCs, but is not often serious: if the circuit card is well laid out, and clock amplitude and dv/dts kept as low as practical, the effect is a discontinuity in the transfer characteristic of less than 8 LSBs (at 18-bit resolution) at $F_C/3$ and $F_C/4$, and less at other sub-harmonics. This is frequently tolerable, since the frequencies where it occurs are known. Of course, if the circuit layout or decoupling is poor, the effect may be much larger, but this is the fault of poor design and not the SVFC itself.

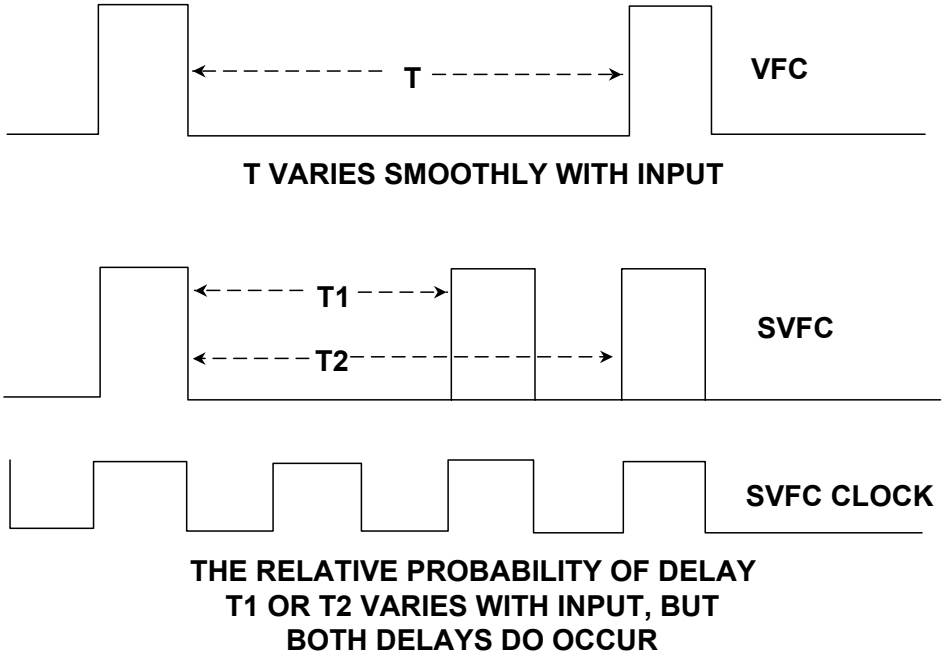


Figure 6.78: *VFC and SVFC Waveforms*

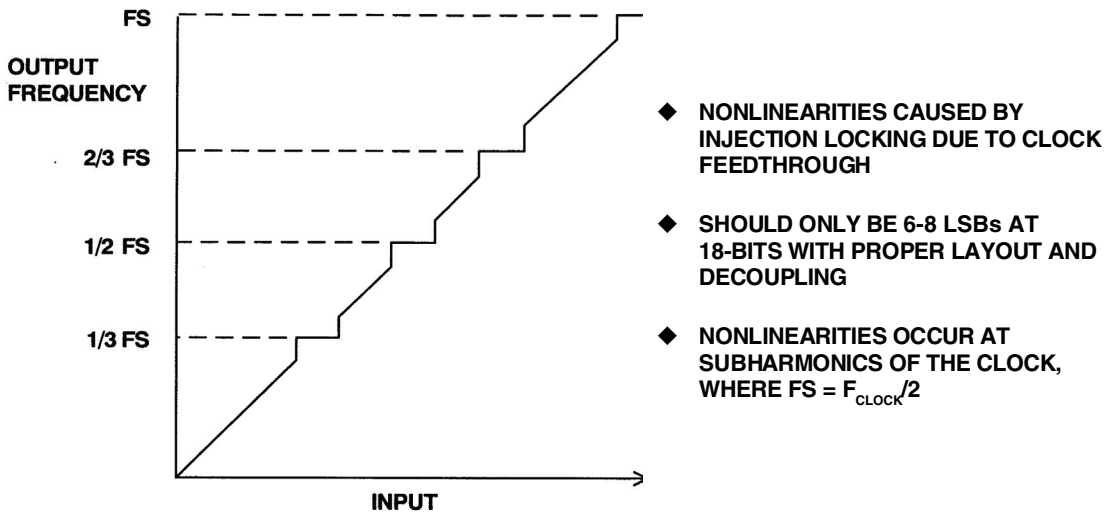


Figure 6.79: *SVFC Nonlinearity*

It is evident that the SVFC is quantized, while the basic VFC is not. It does NOT follow from this that the counter/VFC ADC has higher resolution (neglecting nonlinearities) than the counter/SVFC ADC, because the clock in the counter also sets a limit to the resolution.

When a VFC has a large input, it runs quickly and (counting for a short time) gives good resolution, but it is hard to get good resolution in a reasonable sample time with a slow-running VFC. In such a case, it may be more practical to measure the period of the VFC output (this does not work for an SVFC), but of course the resolution of this system deteriorates as the input (and the frequency) increases. However, if the counter/timer arrangement is made "smart," it is possible to measure the approximate VFC frequency and the exact period of not one, but N cycles (where the value of N is determined by the approximate frequency), and maintain high resolution over a wide range of inputs. The AD1170 modular ADC released in 1986 is an example of this architecture.

VFCs have more applications than as a component in ADCs. Since their output is a pulse stream, it may easily be sent over a wide range of transmission media (PSN, radio, optical, IR, ultrasonic, etc.). It need not be received by a counter, but by another VFC configured as a frequency-to-voltage converter (FVC). This gives an analog output, and a VFC-FVC combination is a very useful way of sending a precision analog signal across an isolation barrier.

Dual Slope/Multi-Slope ADCs

The dual-slope ADC architecture was truly a breakthrough in ADCs for high resolution applications such as digital voltmeters (DVMs), etc. A simplified diagram is shown in Figure 6.80, and the integrator output waveforms are shown in Figure 6.81.

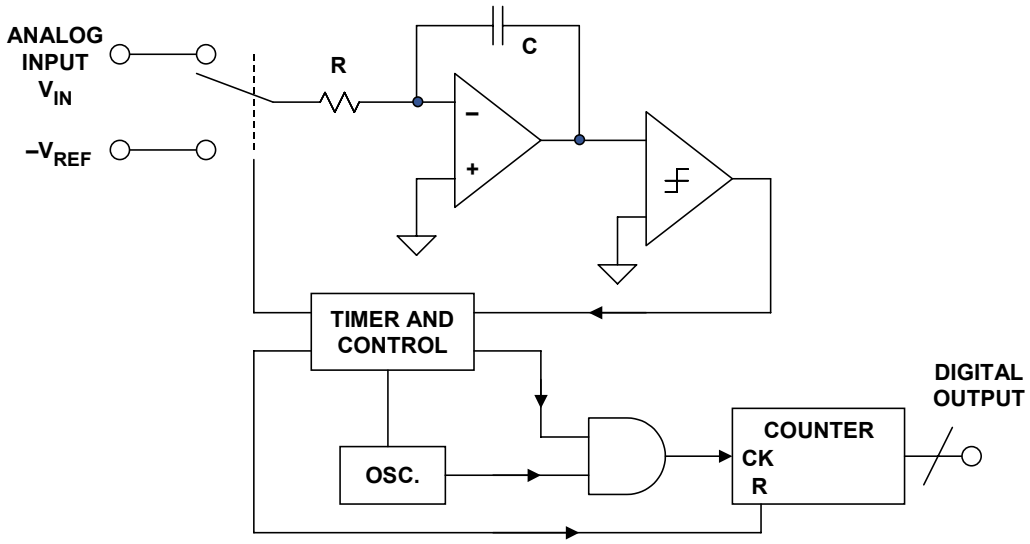
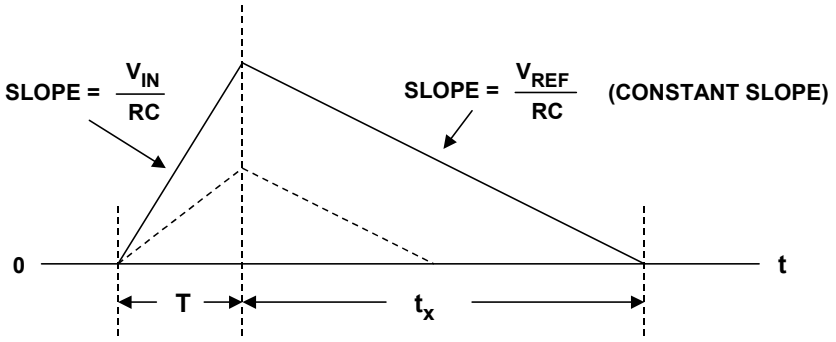


Figure 6.80: *Dual slope ADC*



$$\frac{V_{IN}}{RC}\,T = \frac{V_{REF}}{RC}\,t_x$$

$$t_x = \frac{V_{IN}}{V_{REF}}\,T$$

HIGH NORMAL MODE REJECTION AT MULTIPLES OF $\frac{1}{T}$

Figure 6.81: *Dual Slope ADC Integrator Output Waveforms*

The input signal is applied to an integrator; at the same time a counter is started, counting clock pulses. After a predetermined amount of time (T), a reference voltage having opposite polarity is applied to the integrator. At that instant, the accumulated charge on

the integrating capacitor is proportional to the average value of the input over the interval T. The integral of the reference is an opposite-going ramp having a slope of V_{REF}/RC. At the same time, the counter is again counting from zero. When the integrator output reaches zero, the count is stopped, and the analog circuitry is reset. Since the charge gained is proportional to $V_{IN} \cdot T$, and the equal amount of charge lost is proportional to $V_{REF} \cdot t_x$, then the number of counts relative to the full scale count is proportional to t_x/T, or V_{IN}/V_{REF}. If the output of the counter is a binary number, it will therefore be a binary representation of the input voltage.

Dual-slope integration has many advantages. Conversion accuracy is independent of both the capacitance and the clock frequency, because they affect both the up-slope and the down-slope by the same ratio.

The fixed input signal integration period results in rejection of noise frequencies on the analog input that have periods that are equal to or a sub-multiple of the integration time T. Proper choice of T can therefore result in excellent rejection of 50-Hz or 60-Hz line ripple as shown in Figure 6.82.

Errors caused by bias currents and the offset voltages of the integrating amplifier and the comparator as well as gain errors can be cancelled by using additional charge/discharge cycles to measure "zero" and "full-scale" and using the results to digitally correct the initial measurement, as in the quad-slope architecture.

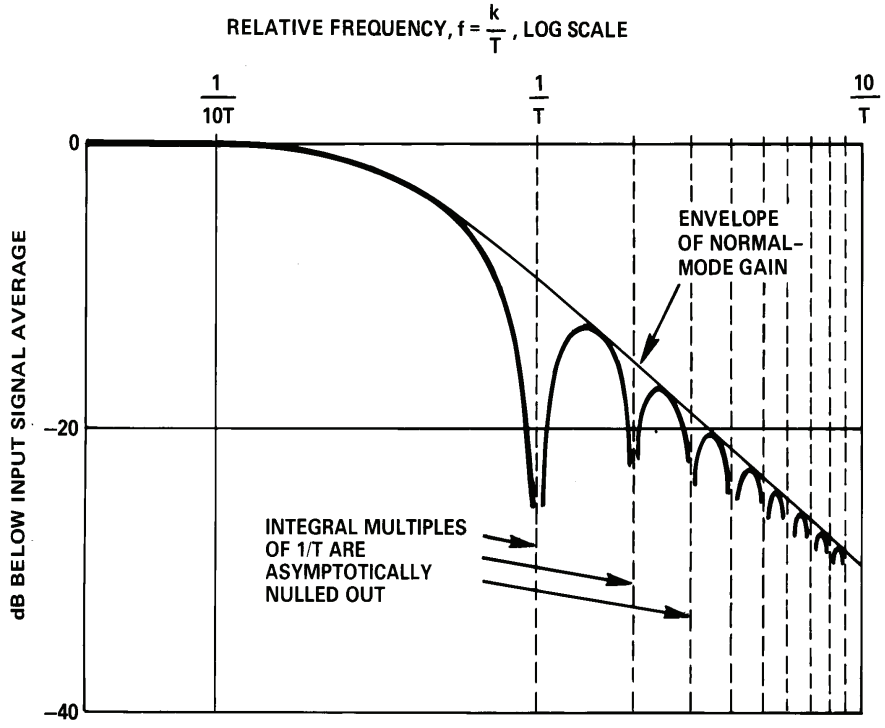


Figure 6.82: *Frequency Response of Integrating ADC*

The triple-slope architecture retains the advantages of the dual-slope, but greatly increases the conversion speed at the cost of added complexity. The increase in conversion speed is achieved by accomplishing the reference integration (ramp-down) at two distinct rates: a high-speed rate, and a "vernier" lower speed rate. The counter is likewise divided into two sections, one for the MSBs and one for the LSBs. In a properly designed triple-slope converter, a significant increase in speed can be achieved while retaining the inherent linearity, differential linearity, and stability characteristics associated with dual-slope ADCs.

Resolver-to-Digital Converters (RDCs) and Synchros

Machine-tool and robotics manufacturers have increasingly turned to resolvers and synchros to provide accurate angular and rotational information. These devices excel in demanding factory applications requiring small size, long-term reliability, absolute position measurement, high accuracy, and low noise operation.

A diagram of a typical synchro and resolver is shown in Figure 6.83. Both synchros and resolvers employ single-winding rotors that revolve inside fixed stators. In the case of a simple synchro, the stator has three windings oriented 120º apart and electrically connected in a Y-connection. Resolvers differ from synchros in that their stators have only two windings oriented at 90º.

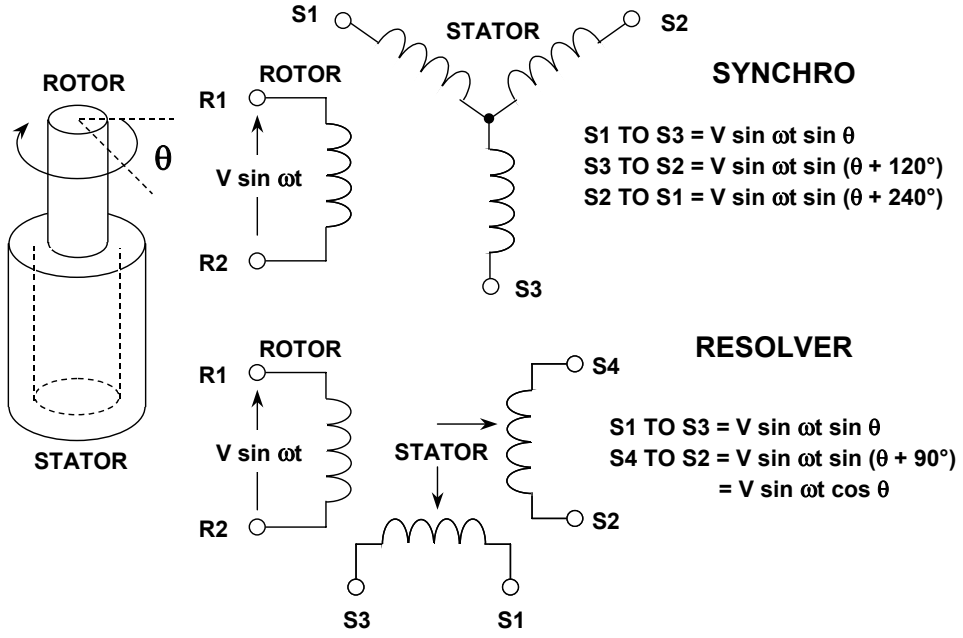


Figure 6.83: *Synchros and Resolvers*

Because synchros have three stator coils in a 120º orientation, they are more difficult than resolvers to manufacture and are therefore more costly. Today, synchros find decreasing use, except in certain military and avionic retrofit applications.

Modern resolvers, in contrast, are available in a brushless form that employ a transformer to couple the rotor signals from the stator to the rotor. The primary winding of this transformer resides on the stator, and the secondary on the rotor. Other resolvers use more traditional brushes or slip rings to couple the signal into the rotor winding. Brushless resolvers are more rugged than synchros because there are no brushes to break or dislodge, and the life of a brushless resolver is limited only by its bearings. Most resolvers are specified to work over 2 V to 40 V rms and at frequencies from 400 Hz to 10 kHz. Angular accuracies range from 5 arc-minutes to 0.5 arc-minutes. (There are

60 arc-minutes in one degree, and 60 arc-seconds in one arc-minute. Hence, one arc-minute is equal to 0.0167 degrees).

In operation, synchros and resolvers resemble rotating transformers. The rotor winding is excited by an ac reference voltage, at frequencies up to a few kHz. The magnitude of the voltage induced in any stator winding is proportional to the sine of the angle, θ, between the rotor coil axis and the stator coil axis. In the case of a synchro, the voltage induced across any pair of stator terminals will be the vector sum of the voltages across the two connected coils.

For example, if the rotor of a synchro is excited with a reference voltage, Vsinωt, across its terminals R1 and R2, then the stator's terminal will see voltages in the form:

$$S1 \text{ to } S3 = V \sin\omega t \sin\theta \quad \text{Eq. 6.1}$$
$$S3 \text{ to } S2 = V \sin\omega t \sin(\theta + 120^\circ) \quad \text{Eq. 6.2}$$
$$S2 \text{ to } S1 = V \sin\omega t \sin(\theta + 240^\circ), \quad \text{Eq. 6.3}$$

where θ is the shaft angle.

In the case of a resolver, with a rotor ac reference voltage of Vsinωt, the stator's terminal voltages will be:

$$S1 \text{ to } S3 = V \sin\omega t \sin\theta \quad \text{Eq. 6.4}$$
$$S4 \text{ to } S2 = V \sin\omega t \sin(\theta + 90^\circ) = V \sin\omega t \cos\theta. \quad \text{Eq. 6.5}$$

It should be noted that the 3-wire synchro output can be easily converted into the resolver-equivalent format using a Scott-T transformer. Therefore, the following signal processing example describes only the resolver configuration.

A typical resolver-to-digital converter (RDC) is shown functionally in Figure 6.84. The two outputs of the resolver are applied to cosine and sine multipliers. These multipliers incorporate sine and cosine lookup tables and function as multiplying digital-to-analog converters. Begin by assuming that the current state of the up/down counter is a digital number representing a trial angle, φ. The converter seeks to adjust the digital angle, φ, continuously to become equal to, and to track θ, the analog angle being measured. The resolver's stator output voltages are written as:

$$V_1 = V \sin\omega t \sin\theta \quad \text{Eq. 6.6}$$
$$V_2 = V \sin\omega t \cos\theta \quad \text{Eq. 6.7}$$

where θ is the angle of the resolver's rotor. The digital angle φ is applied to the cosine multiplier, and its cosine is multiplied by V_1 to produce the term:

$$V \sin\omega t \sin\theta \cos\varphi. \quad \text{Eq. 6.8}$$

The digital angle φ is also applied to the sine multiplier and multiplied by V_2 to product the term:

$$V \sin\omega t \cos\theta \sin\varphi. \quad \text{Eq. 6.9}$$

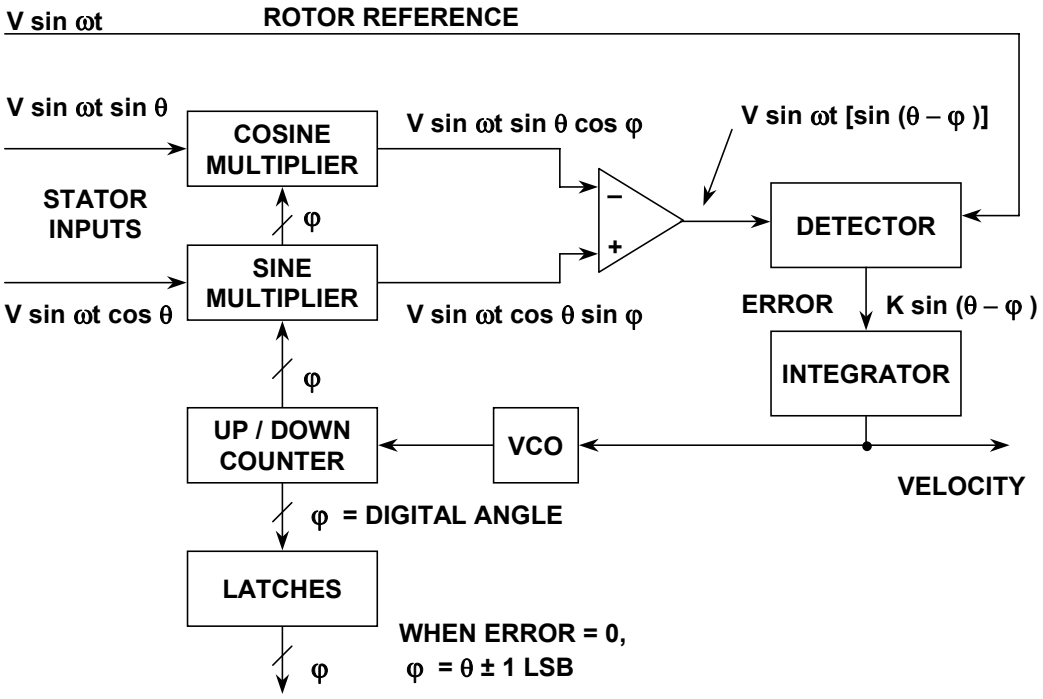


Figure 6.84: *Resolver-to-Digital Converter (RDC)*

These two signals are subtracted from each other by the error amplifier to yield an ac error signal of the form:

$$V \sin\omega t\,[\sin\theta \cos\varphi - \cos\theta \sin\varphi]. \qquad \text{Eq. 6.10}$$

Using a simple trigonometric identity, this reduces to:

$$V \sin\omega t\,[\sin(\theta - \varphi)]. \qquad \text{Eq. 6.11}$$

The detector synchronously demodulates this ac error signal, using the resolver's rotor voltage as a reference. This results in a dc error signal proportional to $\sin(\theta - \varphi)$.

The dc error signal feeds an integrator, the output of which drives a voltage-controlled-oscillator (VCO). The VCO, in turn, causes the up/down counter to count in the proper direction to cause:

$$\text{Sin}(\theta - \varphi) \rightarrow 0. \qquad \text{Eq. 6.12}$$

When this is achieved,

$$\theta - \varphi \rightarrow 0, \qquad \text{Eq. 6.13}$$

and therefore

$$\varphi = \theta \qquad \text{Eq. 6.14}$$

to within one count. Hence, the counter's digital output,φ, represents the angle θ. The latches enable this data to be transferred externally without interrupting the loop's tracking.

This circuit is equivalent to a so-called type-2 servo loop, because it has, in effect, two integrators. One is the counter, which accumulates pulses; the other is the integrator at the output of the detector. In a type-2 servo loop with a constant rotational velocity input, the output digital word continuously follows, or tracks the input, without needing externally derived convert commands, and with no steady state phase lag between the digital output word and actual shaft angle. An error signal appears only during periods of acceleration or deceleration.

As an added bonus, the tracking RDC provides an analog dc output voltage directly proportional to the shaft's rotational velocity. This is a useful feature if velocity is to be measured or used as a stabilization term in a servo system, and it makes tachometers unnecessary.

Since the operation of an RDC depends only on the ratio between input signal amplitudes, attenuation in the lines connecting them to resolvers doesn't substantially affect performance. For similar reasons, these converters are not greatly susceptible to waveform distortion. In fact, they can operate with as much as 10% harmonic distortion on the input signals; some applications actually use square-wave references with little additional error.

Tracking ADCs are therefore ideally suited to RDCs. While other ADC architectures, such as successive approximation, could be used, the tracking converter is the most accurate and efficient for this application.

Because the tracking converter doubly integrates its error signal, the device offers a high degree of noise immunity (12 dB per octave rolloff). The net area under any given noise spike produces an error. However, typical inductively coupled noise spikes have equal positive and negative going waveforms. When integrated, this results in a zero net error signal. The resulting noise immunity, combined with the converter's insensitivity to voltage drops, lets the user locate the converter at a considerable distance from the resolver. Noise rejection is further enhanced by the detector's rejection of any signal not at the reference frequency, such as wideband noise.

The AD2S90 is one of a number of integrated RDCs offered by Analog Devices. The general architecture is similar to that of Figure 6.83. Further details on synchro and resolver-to-digital converters can be found in the references.

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SECTION 6.3: SIGMA-DELTA CONVERTERS

Historical Perspective

The sigma-delta (Σ-Δ) ADC architecture had its origins in the early development phases of pulse code modulation (PCM) systems—specifically, those related to transmission techniques called *delta modulation* and *differential PCM*. (An excellent discussion of both the history and concepts of the sigma-delta ADC can be found by Max Hauser in Reference 1).

The driving force behind delta modulation and differential PCM was to achieve higher transmission efficiency by transmitting the *changes* (delta) in value between consecutive samples rather than the actual samples themselves.

In *delta modulation*, the analog signal is quantized by a one-bit ADC (a comparator) as shown in Figure 6.85A. The comparator output is converted back to an analog signal with a 1-bit DAC, and subtracted from the input after passing through an integrator. The shape of the analog signal is transmitted as follows: a 1 indicates that a positive excursion has occurred since the last sample, and a 0 indicates that a negative excursion has occurred since the last sample.

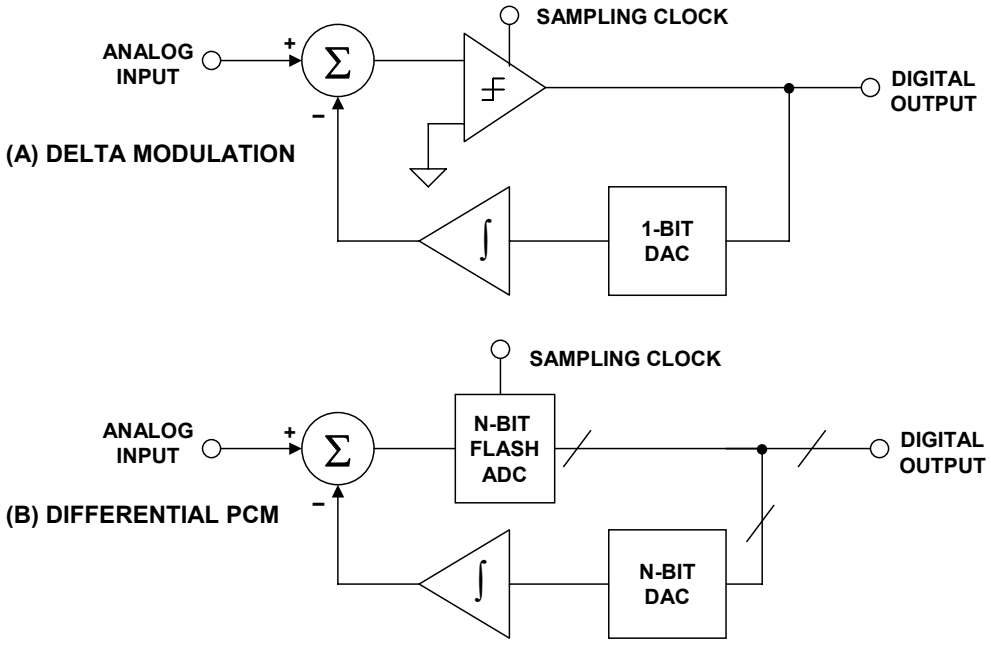

Figure 6.85: *Delta Modulation and Differential PCM*

If the analog signal remains at a fixed dc level for a period of time, a pattern alternating of 0s and 1s is obtained. It should be noted that *differential PCM* (see Figure 6.85B) uses

exactly the same concept except a multibit ADC is used rather than a comparator to derived the transmitted information.

Since there is no limit to the number of pulses of the same sign that may occur, delta modulation systems are capable of tracking signals of any amplitude. In theory, there is no peak clipping. However, the theoretical limitation of delta modulation is that the analog signal must not change too rapidly. The problem of slope clipping is shown in Figure 6.86. Here, although each sampling instant indicates a positive excursion, the analog signal is rising too quickly, and the quantizer is unable to keep pace.

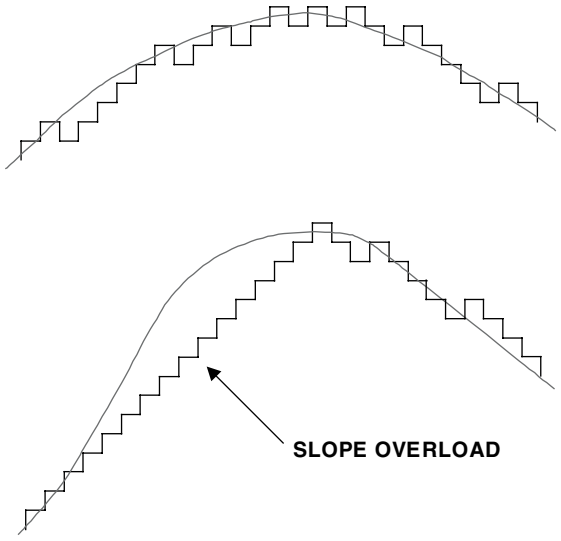

Figure 6.86: *Quantization Using Delta Modulation*

Slope clipping can be reduced by increasing the quantum step size or increasing the sampling rate. Differential PCM uses a multibit quantizer to effectively increase the quantum step sizes at the increase of complexity. Tests have shown that in order to obtain the same quality as classical PCM, delta modulation requires very high sampling rates, typically 20× the highest frequency of interest, as opposed to Nyquist rate of 2×.

For these reasons, delta modulation and differential PCM have never achieved any significant degree of popularity, however a slight modification of the delta modulator leads to the basic sigma-delta architecture, one of the most popular high resolution ADC architectures in use today.

The basic single and multibit first-order sigma-delta ADC architecture is shown in Figures 6.87A and 6.87B, respectively. Note that the integrator operates on the error signal, whereas in a delta modulator, the integrator is in the feedback loop. The basic oversampling sigma-delta modulator increases the overall signal-to-noise ratio at low frequencies by shaping the quantization noise such that most of it occurs outside the bandwidth of interest. The digital filter then removes the noise outside the bandwidth of interest, and the decimator reduces the output data rate back to the Nyquist rate.

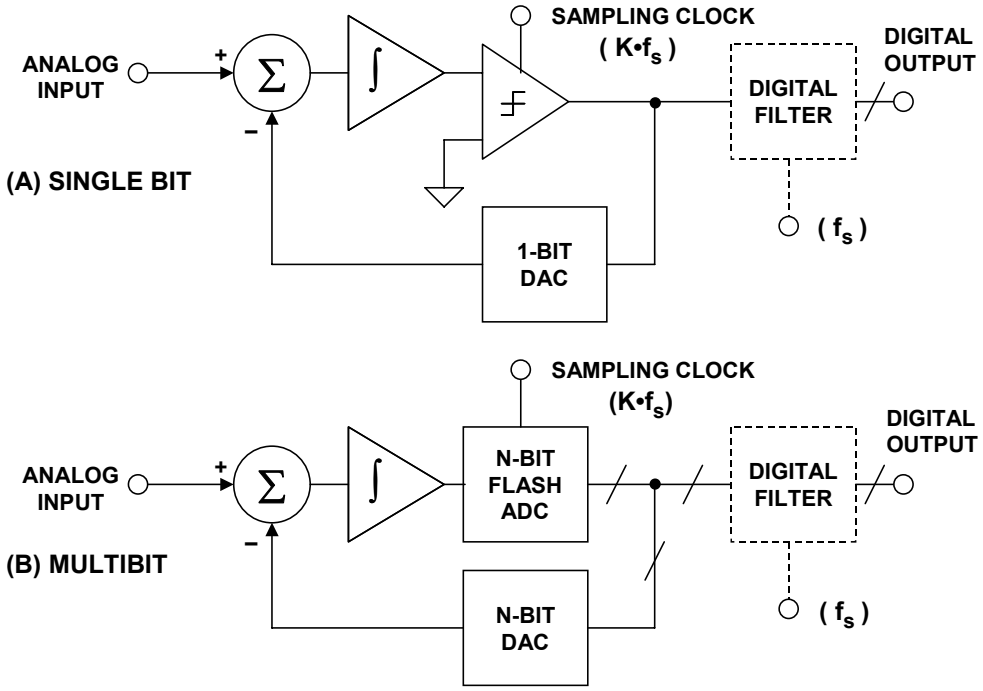

Figure 6.87: *Single and Multibit Sigma-Delta ADCs*

The IC sigma-delta ADC offers several advantages over the other architectures, especially for high resolution, low frequency applications. First and foremost, the single-bit sigma-delta ADC is inherently monotonic and requires no laser trimming. The sigma-delta ADC also lends itself to low cost foundry CMOS processes because of the digitally intensive nature of the architecture. Examples of early monolithic sigma-delta ADCs are given in References 13-21. Since that time there has been a constant stream of process and design improvements in the fundamental architecture proposed in the early works cited above.

Sigma-Delta (Σ-Δ) or Delta-Sigma (Δ-Σ)? Editor's Notes from *Analog Dialogue* Vol. 24-2, 1990, by Dan Sheingold

This is not the most earth-shaking of controversies, and many readers may wonder what the fuss is all about—if they wonder at all. The issue is important to both editor and readers because of the need for consistency; we'd like to use the same name for the same thing whenever it appears. But *which* name? In the case of the modulation technique that led to a new oversampling A/D conversion mechanism, we chose *sigma-delta*. Here's why.

Ordinarily, when a new concept is named by its creators, the name sticks; it should not be changed unless it is erroneous or flies in the face of precedent. The seminal paper on this subject was published in 1962 (References 9, 10), and its authors chose the name "delta-sigma modulation," since it was based on *delta* modulation but included an integration (summation, hence Σ).

Delta-sigma was apparently unchallenged until the 1970s, when engineers at AT&T were publishing papers using the term *sigma-delta*. Why? According to Hauser (Reference 1), the precedent had been to name variants of delta modulation with adjectives preceding the word "delta." Since the form of modulation in question is a variant of delta modulation, the sigma, used as an adjective—so the argument went—should precede the delta.

Many engineers who came upon the scene subsequently used whatever term caught their fancy, often without knowing why. It was even possible to find *both* terms used interchangeably in the same paper. As matters stand today, sigma-delta is in widespread use, probably for the majority of citations. Would its adoption be an injustice to the inventors of the technique?

We think not. Like others, we believe that the name delta-sigma is a departure from precedent. Not just in the sense of grammar, but also in relation to the hierarchy of operations. Consider a block diagram for embodying an analog root-mean-square (finding the square root of the mean of a squared signal) computer. First the signal is squared, then it is integrated, and finally it is rooted (see Figure 6.88).

If we were to name the overall function after the causal order of operations, it would have to be called a "square mean root" function. But naming in order of the *hierarchy* of its mathematical operations gives us the familiar—and undisputed—name, *root mean-square*. Consider now a block diagram for taking a difference (delta), and then integrating it (sigma).

Its causal order would give *delta-sigma*, but in functional hierarchy it is *sigma-delta*, since it computes the integral of a difference. We believe that the latter term is correct and follows precedent; and we have adopted it as our standard.

Dan Sheingold, 1990.

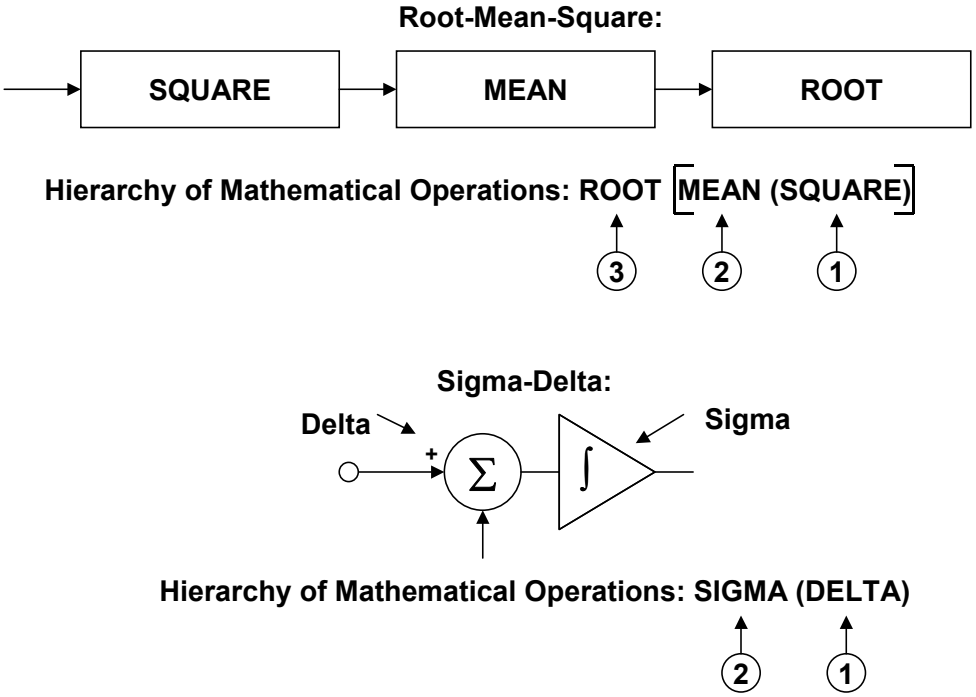

Figure 6.88: *Sigma-Delta (Σ-Δ) or Delta-Sigma (Δ-Σ)?*

Basics of Sigma-Delta ADCs

Sigma-Delta Analog-Digital Converters (Σ-Δ ADCs) have been known for over thirty years, but only recently has the technology (high density digital VLSI) existed to manufacture them as inexpensive monolithic integrated circuits. They are now used in many applications where a low cost, low bandwidth, low power, high resolution ADC is required.

There have been innumerable descriptions of the architecture and theory of Σ-Δ ADCs, but most commence with a maze of integrals and deteriorate from there. Some engineers who do not understand the theory of operation of Σ-Δ ADCs and are convinced, from study of a typical published article, which it is too complex to comprehend easily.

There is nothing particularly difficult to understand about Σ-Δ ADCs, as long as you avoid the detailed mathematics, and this section has been written in an attempt to clarify the subject. A Σ-Δ ADC contains very simple analog electronics (a comparator, voltage reference, a switch, and one or more integrators, and analog summing circuits), and quite complex digital computational circuitry. This circuitry consists of a digital signal processor (DSP) which acts as a filter (generally, but not invariably, a low-pass filter). It is not necessary to know precisely how the filter works to appreciate what it does. To understand how a Σ-Δ ADC works, familiarity with the concepts of *oversampling, quantization noise shaping, digital filtering,* and *decimation* is required.

Let us consider the technique of over-sampling with an analysis in the frequency domain. Where a dc conversion has a *quantization error* of up to ½ LSB, a sampled data system has *quantization noise*. A perfect classical N-bit sampling ADC has an rms quantization noise of $q/\sqrt{12}$ uniformly distributed within the Nyquist band of dc to $f_s/2$ (where q is the value of an LSB and f_s is the sampling rate) as shown in Figure 6.89A. Therefore, its SNR with a full-scale sinewave input will be (6.02N + 1.76) dB. If the ADC is less than perfect, and its noise is greater than its theoretical minimum quantization noise, then its *effective* resolution will be less than N-bits. Its actual resolution (often known as its Effective Number of Bits or ENOB) will be defined by:

$$\text{ENOB} = \frac{\text{SNR} - 1.76\text{dB}}{6.02\text{dB}}. \qquad \text{Eq. 6.15}$$

If we choose a much higher sampling rate, Kf_s (see Figure 6.89B), the rms quantization noise remains $q/\sqrt{12}$, but the noise is now distributed over a wider bandwidth dc to $Kf_s/2$. If we then apply a digital low-pass filter (LPF) to the output, we remove much of the quantization noise, but do not affect the wanted signal—so the ENOB is improved. We have accomplished a high resolution A/D conversion with a low resolution ADC. The factor K is generally referred to as the *oversampling ratio*. It should be noted at this point that oversampling has an added benefit in that it relaxes the requirements on the analog antialiasing filter.

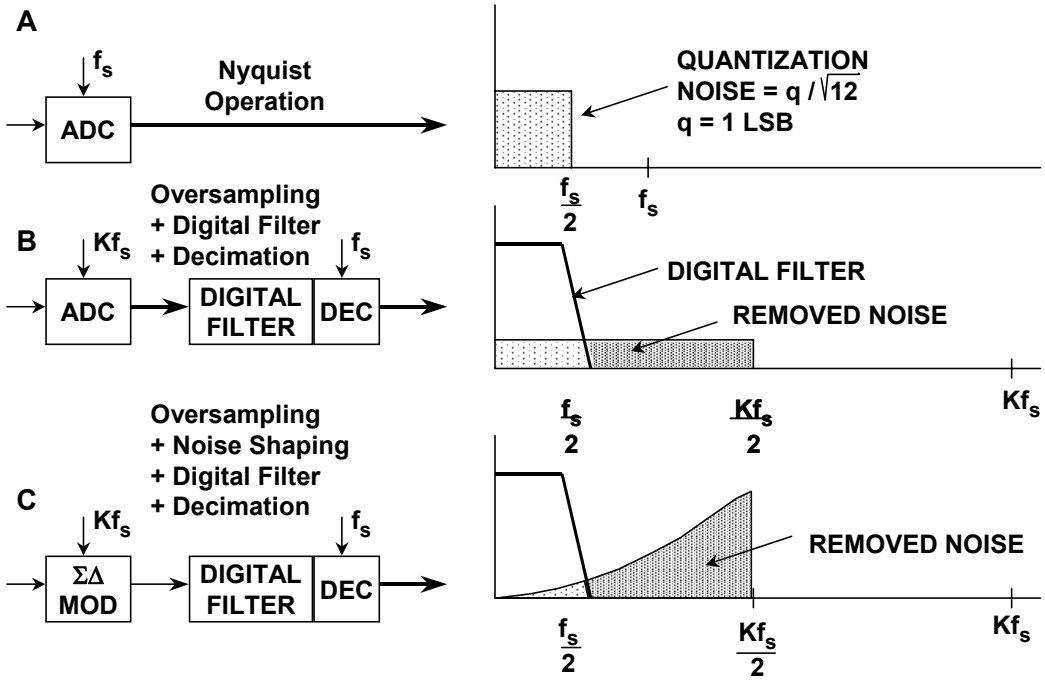

Figure 6.89: *Oversampling, Digital Filtering, Noise Shaping, and Decimation*

Since the bandwidth is reduced by the digital output filter, the output data rate may be lower than the original sampling rate (Kf_s) and still satisfy the Nyquist criterion. This may be achieved by passing every Mth result to the output and discarding the remainder. The process is known as "decimation" by a factor of M. Despite the origins of the term (*decem* is Latin for ten), M can have any integer value, provided that the output data rate is more than twice the signal bandwidth. Decimation does not cause any loss of information (see Figure 6.89B).

If we simply use oversampling to improve resolution, we must oversample by a factor of 2^{2N} to obtain an N-bit increase in resolution. The Σ-Δ converter does not need such a high oversampling ratio because it not only limits the signal passband, but also shapes the quantization noise so that most of it falls outside this passband as shown in Figure 6.89C.

If we take a 1-bit ADC (generally known as a comparator), drive it with the output of an integrator, and feed the integrator with an input signal summed with the output of a 1-bit DAC fed from the ADC output, we have a first-order Σ-Δ modulator as shown in Figure 6.90. Add a digital low-pass filter (LPF) and decimator at the digital output, and we have a Σ-Δ ADC—the Σ-Δ modulator shapes the quantization noise so that it lies above the passband of the digital output filter, and the ENOB is therefore much larger than would otherwise be expected from the oversampling ratio.

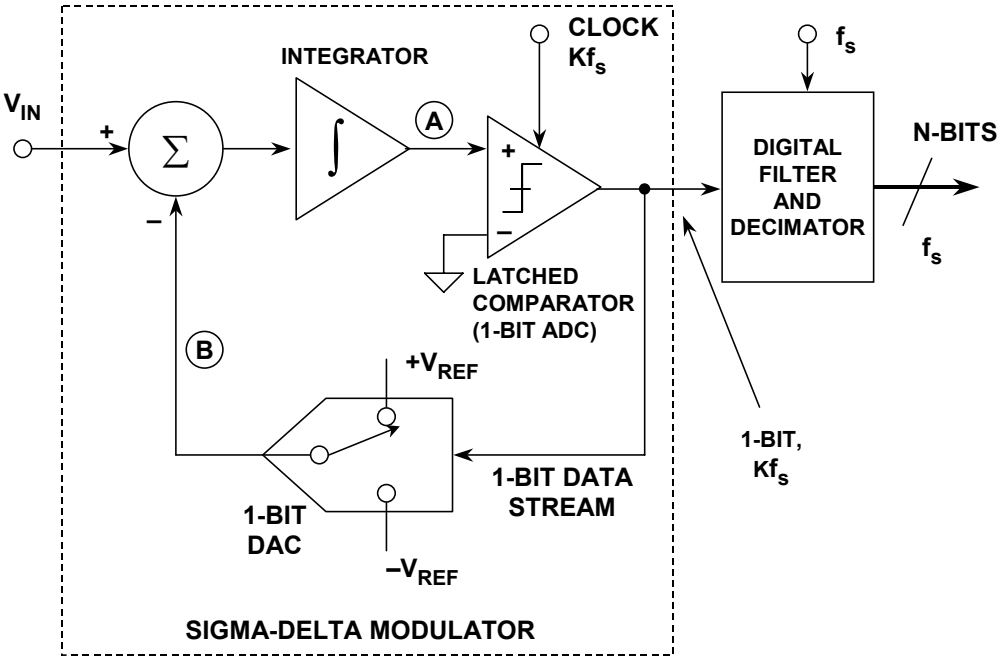

Figure 6.90: *First-Order Sigma-Delta ADC*

Intuitively, a Σ-Δ ADC operates as follows. Assume a dc input at V_{IN}. The integrator is constantly ramping up or down at node A. The output of the comparator is fed back through a 1-bit DAC to the summing input at node B. The negative feedback loop from the comparator output through the 1-bit DAC back to the summing point will force the average dc voltage at node B to be equal to V_{IN}. This implies that the average DAC output voltage must equal to the input voltage V_{IN}. The average DAC output voltage is controlled by the *ones-density* in the 1-bit data stream from the comparator output. As the input signal increases towards $+V_{REF}$, the number of "ones" in the serial bit stream increases, and the number of "zeros" decreases. Similarly, as the signal goes negative towards $-V_{REF}$, the number of "ones" in the serial bit stream decreases, and the number of "zeros" increases. From a very simplistic standpoint, this analysis shows that the average value of the input voltage is contained in the serial bit stream out of the comparator. The digital filter and decimator process the serial bit stream and produce the final output data.

For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged, will a meaningful value result. The sigma-delta modulator is very difficult to analyze in the time domain because of this apparent randomness of the single-bit data output. If the input signal is near positive full-scale, it is clear that there will be more 1s than 0s in the bit stream. Likewise, for signals near negative full-scale, there will be more 0s than 1s in the bit stream. For signals near midscale, there will be approximately an equal number of 1s and 0s. Figure 6.91 shows the output of the integrator for two input conditions. The first is for an input of zero (midscale). To decode the output, pass the output samples through a simple digital low-pass filter that averages every four samples. The output of the filter is 2/4. This value represents bipolar zero. If more samples are averaged, more dynamic range is achieved. For example, averaging four samples gives two bits of

resolution, while averaging eight samples yields 4/8, or three bits of resolution. In the bottom waveform of Figure 6.91, the average obtained for four samples is 3/4, and the average for eight samples is 6/8.

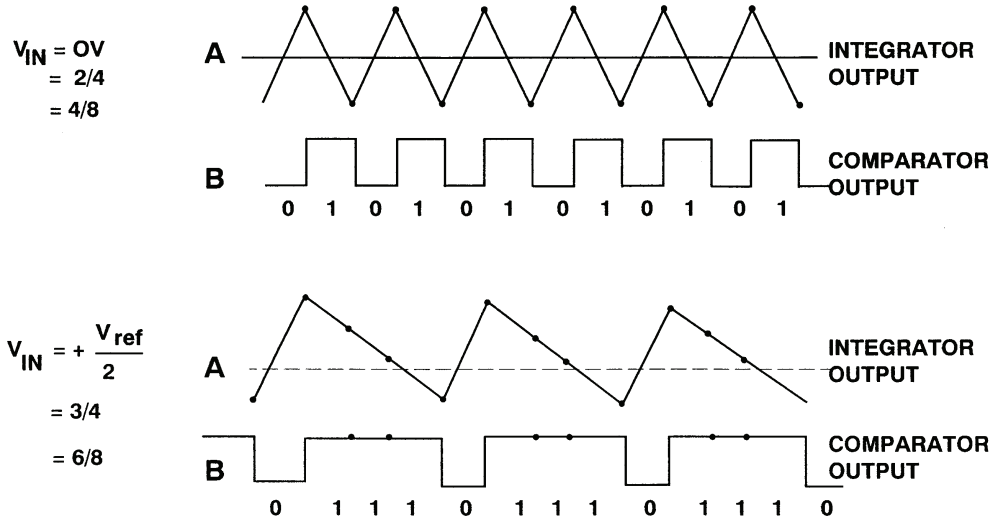

Figure 6.91: *Sigma-Delta Modulator Waveforms*

Further time-domain analysis is not productive, and the concept of noise shaping is best explained in the frequency domain by considering the simple Σ-Δ modulator model in Figure 6.92.

The integrator in the modulator is represented as an analog low-pass filter with a transfer function equal to H(f) = 1/f. This transfer function has an amplitude response which is inversely proportional to the input frequency. The 1-bit quantizer generates quantization noise, Q, which is injected into the output summing block. If we let the input signal be X, and the output Y, the signal coming out of the input summer must be X – Y. This is multiplied by the filter transfer function, 1/f, and the result goes to one input to the output summer. By inspection, we can then write the expression for the output voltage Y as:

$$Y = \frac{1}{f}(X - Y) + Q. \qquad \text{Eq. 6.16}$$

This expression can easily be rearranged and solved for Y in terms of X, f, and Q:

$$Y = \frac{X}{f+1} + \frac{Q \cdot f}{f+1}. \qquad \text{Eq. 6.17}$$

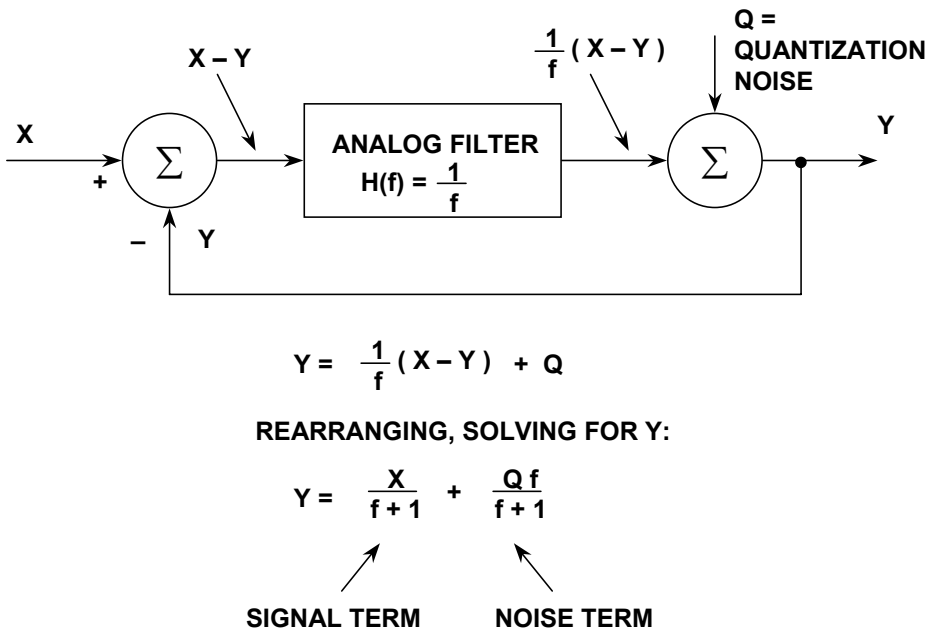

Figure 6.92: *Simplified Frequency Domain Linearized Model of a Sigma-Delta Modulator*

Note that as the frequency f approaches zero, the output voltage Y approaches X with no noise component. At higher frequencies, the amplitude of the signal component approaches zero, and the noise component approaches Q. At high frequency, the output consists primarily of quantization noise. In essence, the analog filter has a low-pass effect on the signal, and a high-pass effect on the quantization noise. Thus the analog filter performs the noise shaping function in the Σ-Δ modulator model.

For a given input frequency, higher order analog filters offer more attenuation. The same is true of Σ-Δ modulators, provided certain precautions are taken.

By using more than one integration and summing stage in the Σ-Δ modulator, we can achieve higher orders of quantization noise shaping and even better ENOB for a given over-sampling ratio as is shown in Figure 6.93 for both a first and second-order Σ-Δ modulator.

The block diagram for the second-order Σ-Δ modulator is shown in Figure 6.94. Third, and higher, order Σ-Δ ADCs were once thought to be potentially unstable at some values of input—recent analyses using *finite* rather than infinite gains in the comparator have shown that this is not necessarily so, but even if instability does start to occur, it is not important, since the DSP in the digital filter and decimator can be made to recognize incipient instability and react to prevent it.

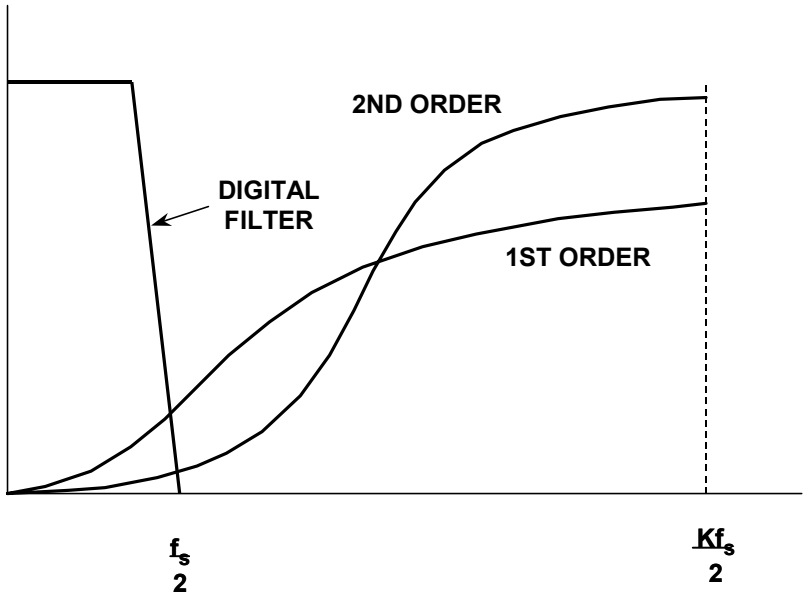

Figure 6.93: *Sigma-Delta Modulators Shape Quantization Noise*

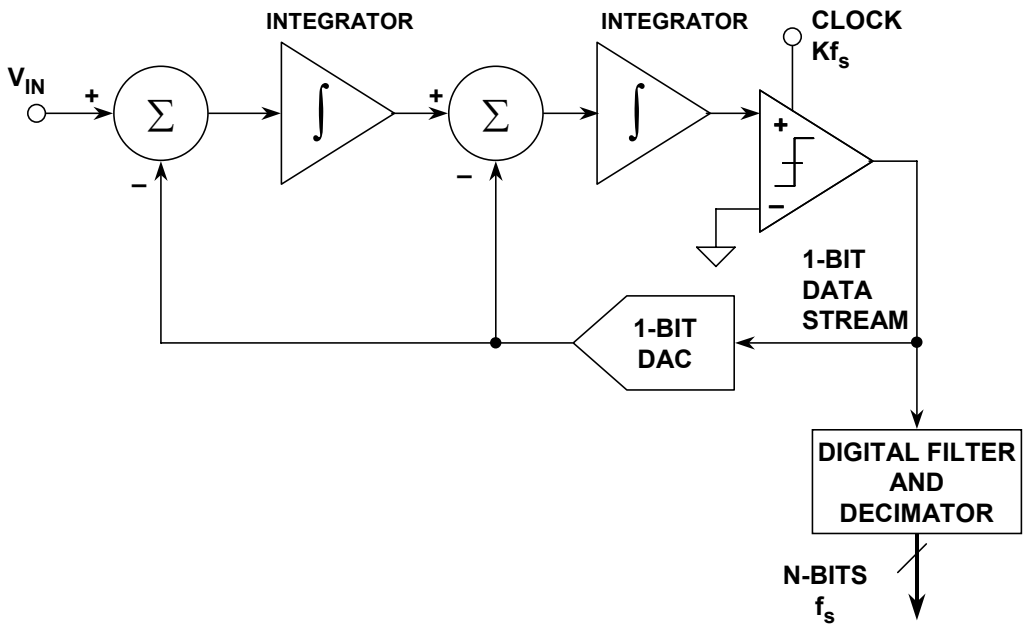

Figure 6.94: *Second-Order Sigma-Delta ADC*

Figure 6.95 shows the relationship between the order of the Σ-Δ modulator and the amount of over-sampling necessary to achieve a particular SNR. For instance, if the oversampling ratio is 64, an ideal second-order system is capable of providing an SNR of about 80 dB. This implies approximately 13 effective number of bits (ENOB). Although the filtering done by the digital filter and decimator can be done to any degree of precision desirable, it would be pointless to carry more than 13 binary bits to the outside world. Additional bits would carry no useful signal information, and would be buried in the quantization noise unless post-filtering techniques were employed. Additional

resolution can be obtained by increasing the oversampling ratio and/or by using a higher-order modulator.

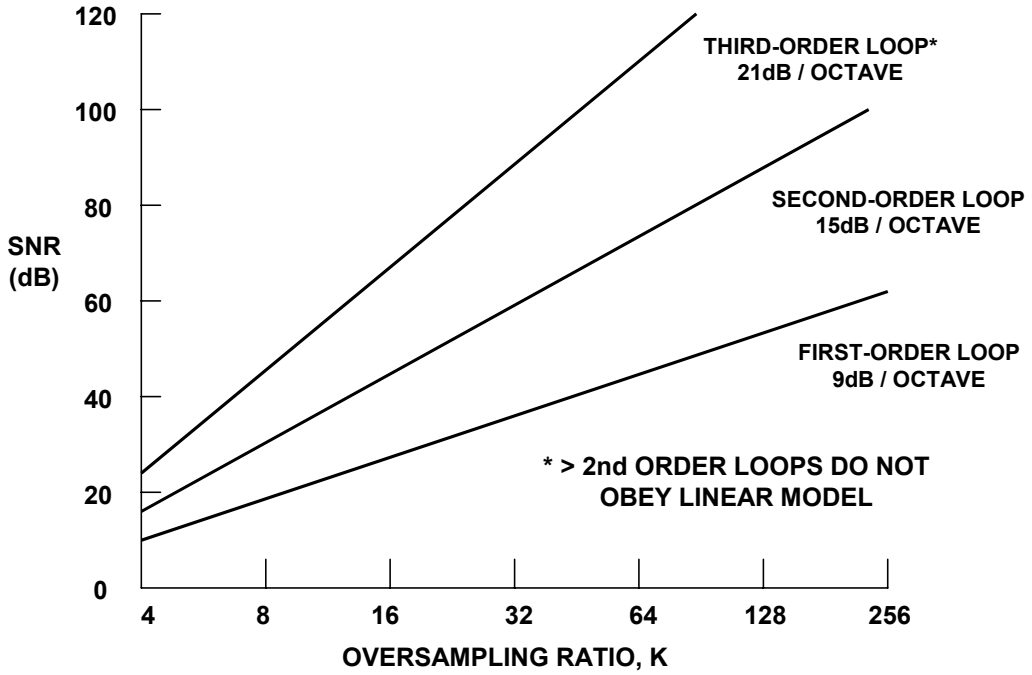

Figure 6.95: *SNR vs. Oversampling Ratio for First, Second, and Third-Order Loops*

Idle Tone Considerations

In our discussion of sigma-delta ADCs up to this point, we have made the assumption that the quantization noise produced by the sigma-delta modulator is random and uncorrelated with the input signal. Unfortunately, this is not entirely the case, especially for the first-order modulator. Consider the case where we are averaging 16 samples of the modulator output in a 4-bit sigma-delta ADC.

Figure 6.96 shows the bit pattern for two input signal conditions: an input signal having the value 8/16, and an input signal having the value 9/16. In the case of the 9/16 signal, the modulator output bit pattern has an extra 1 every 16th output. This will produce energy at $f_s/16$, which translates into an unwanted tone. If the oversampling ratio is less than 16, this tone will fall into the pass band. In audio applications these tones are referred to as "idle tones."

Figure 6.97 shows the correlated idling pattern behavior for a first order sigma-delta modulator, and Figure 6.98 shows the relatively uncorrelated pattern for a second-order modulator. For this reason, virtually all sigma-delta ADCs contain at least a second-order modulator loop.

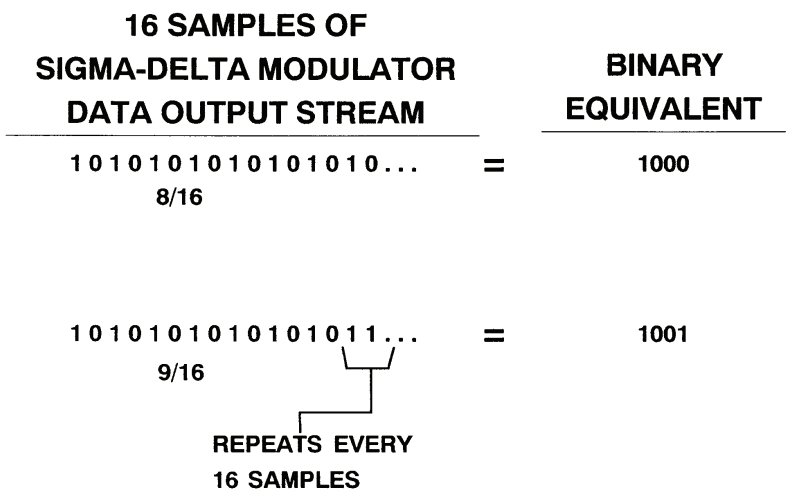

Figure 6.96: *Repetitive Bit Pattern in Sigma-Delta Modulator Output*

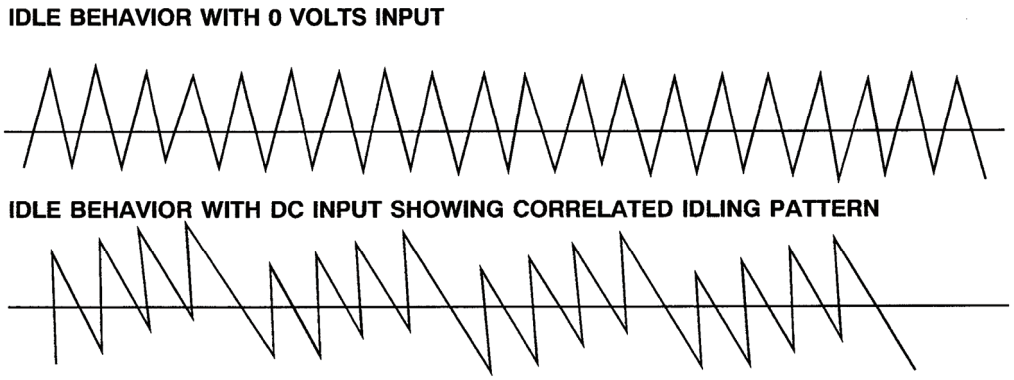

Figure 6.97: *Idling Patterns for First-Order Sigma-Delta Modulator (Integrator Output)*

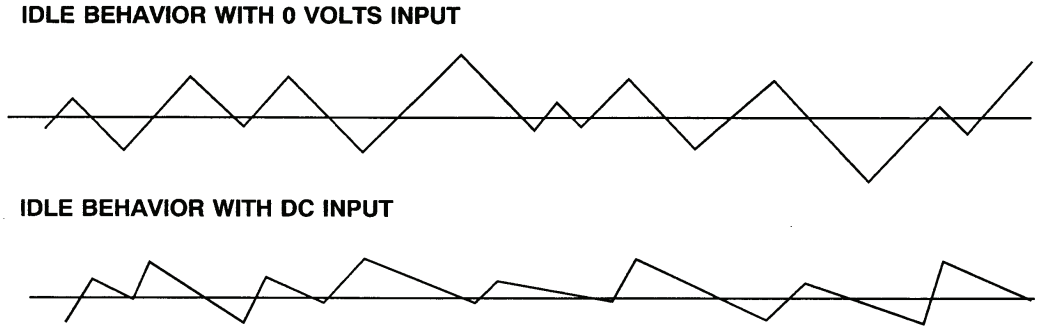

Figure 6.98: *Idling Patterns for Second-Order Sigma-Delta Modulator (Integrator Output)*

Higher Order Loop Considerations

In order to achieve wide dynamic range, sigma-delta modulator loops greater than second-order are necessary, but present real design challenges. First of all, the simple linear models previously discussed are no longer fully accurate. Loops of order greater than two are generally not guaranteed to be stable under all input conditions. The instability arises because the comparator is a nonlinear element whose effective "gain" varies inversely with the input level. This mechanism for instability causes the following behavior: if the loop is operating normally, and a large signal is applied to the input that overloads the loop, the average gain of the comparator is reduced. The reduction in comparator gain in the linear model causes loop instability. This causes instability even when the signal that caused it is removed. In actual practice, such a circuit would normally oscillate on power-up due to initial conditions caused by turn-on transients. As an example, the AD1879 dual audio ADC released in 1994 by Analog Devices used a fifth-order loop. Extensive nonlinear stabilization techniques were required in this and similar higher order loop designs (References 22-26).

Multibit Sigma-Delta Converters

So far we have considered only sigma-delta converters which contain a single-bit ADC (comparator) and a single-bit DAC (switch). The block diagram of Figure 6.99 shows a multi-bit sigma-delta ADC which uses an n-bit flash ADC and an n-bit DAC. Obviously, this architecture will give a higher dynamic range for a given oversampling ratio and order of loop filter. Stabilization is easier, since second-order loops can generally be used. Idling patterns tend to be more random thereby minimizing tonal effects.

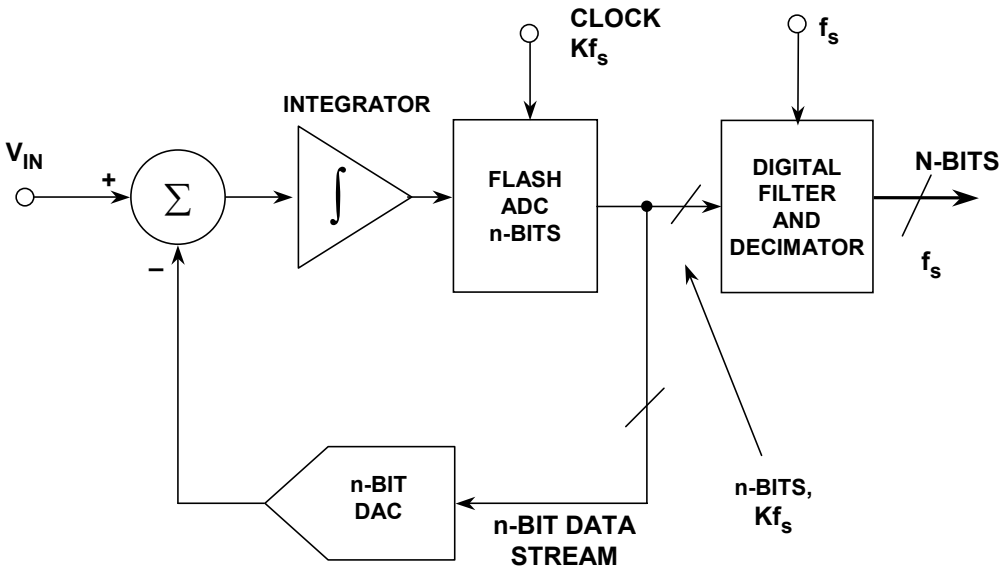

Figure 6.99: *Multibit Sigma-Delta ADC*

The real disadvantage of this technique is that the linearity depends on the DAC linearity, and thin film laser trimming is required to approach 16-bit performance levels. This makes the multi-bit architecture extremely impractical to implement on mixed-signal ICs using traditional binary DAC techniques.

However, fully decoded thermometer DACs coupled with proprietary data scrambling techniques as used in a number of Analog Devices' audio ADCs and DACs, including the 24-bit stereo AD1871 (see References 27 and 28) can achieve high SNR and low distortion using the multibit architecture. A simplified block diagram of the AD1871 ADC is shown in Figure 6.100.

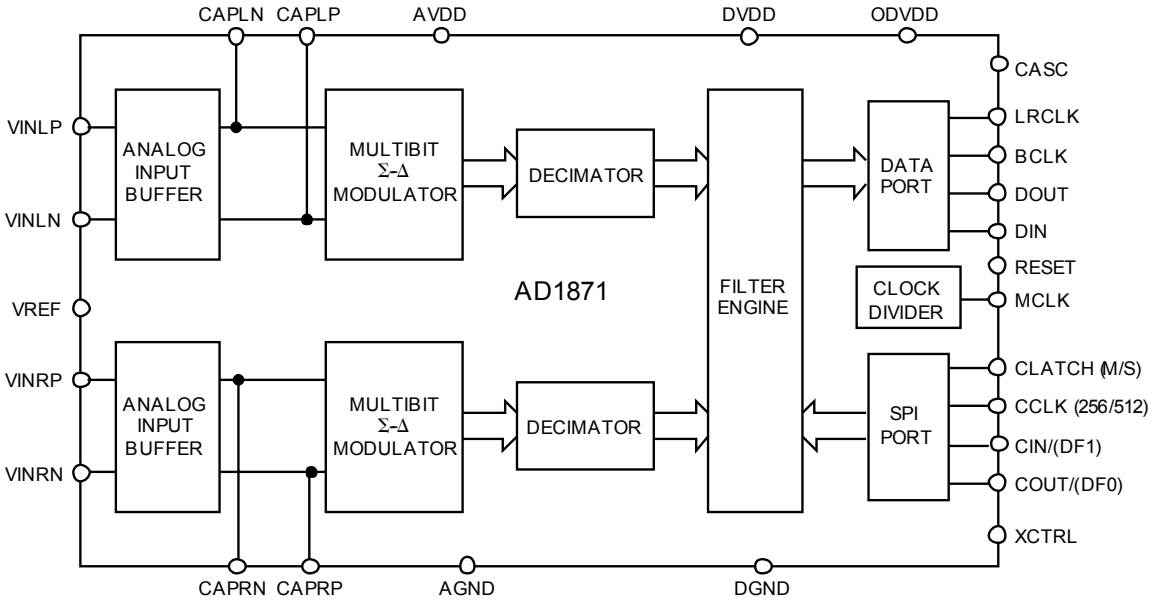

Figure 6.100: *AD1871 24-Bit, 96-kSPS Stereo Audio Multibit Sigma-Delta ADC*

The AD1871's analog Σ-Δ modulator section comprises a second-order multibit implementation using Analog Device's proprietary technology for best performance. As shown in Figure 6.101, the two analog integrator blocks are followed by a flash ADC section that generates the multibit samples.

The output of the flash ADC, which is thermometer encoded, is decoded to binary for output to the filter sections and is scrambled for feedback to the two integrator stages. The modulator is optimized for operation at a sampling rate of 6.144 MHz (which is $128 \times f_s$ at 48-kHz sampling and $64 \times f_s$ at 96-kHz sampling). The A-weighted dynamic range of the AD1871 is typically 105 dB.

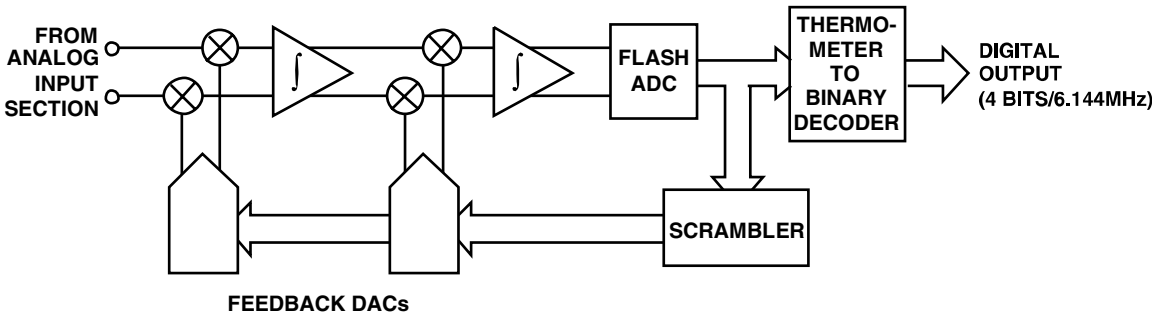

Figure 6.101: *Details of the AD1871 Second-Order Modulator and Data Scrambler*

Digital Filter Implications

The digital filter is an integral part of all sigma-delta ADCs—there is no way to remove it. The settling time of this filter affects certain applications especially when using sigma-delta ADCs in multiplexed applications. The output of a multiplexer can present a step function input to an ADC if there are different input voltages on adjacent channels. In fact, the multiplexer output can represent a full-scale step voltage to the sigma-delta ADC when channels are switched. Adequate filter settling time must be allowed, therefore, in such applications. This does not mean that sigma-delta ADCs shouldn't be used in multiplexed applications, just that the settling time of the digital filter must be considered. Some newer sigma-delta ADCs are actually optimized for use in multiplexed applications.

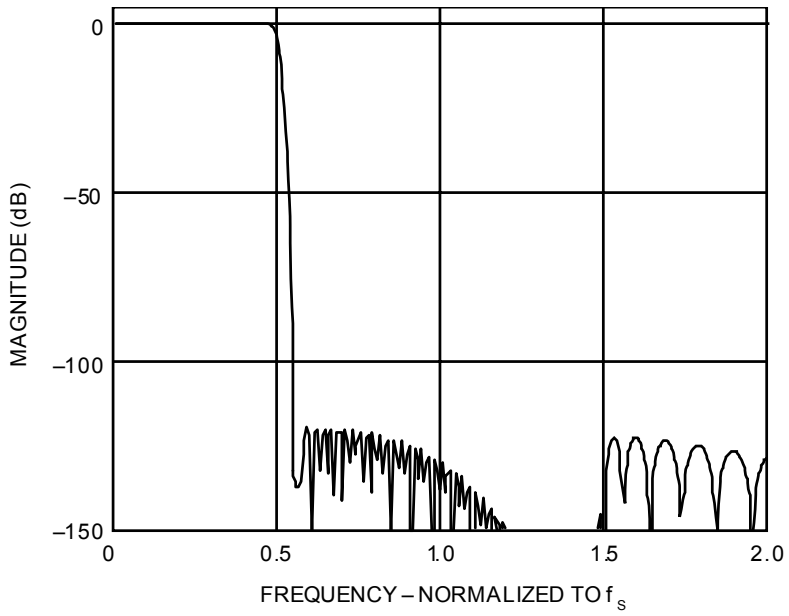

Figure 6.102: *AD1871 24-Bit, 96-kSPS Stereo Sigma-Delta ADC Digital Filter Characteristics*

For example, the group delay through the AD1871 digital filter is 910 µs (sampling at 48 kSPS) and 460 µs (sampling at 96 kSPS)—this represents the time it takes for a step function input to propagate through one-half the number of taps in the digital filter. The total settling time is therefore approximately twice the group delay time. The input oversampling frequency is 6.144 MSPS for both conditions. The frequency response of the digital filter in the AD1871 ADC is shown in Figure 6.102.

In other applications, such as low frequency, high resolution 24-bit measurement sigma-delta ADCs (such as the AD77xx-series), other types of digital filters may be used. For instance, the $SINC^3$ response is popular because it has zeros at multiples of the throughput rate. For instance a 10-Hz throughput rate produces zeros at 50 Hz and 60 Hz which aid in ac power line rejection. The frequency response of a typical Σ-Δ ADC, the AD7730 is shown if Figure 6.103.

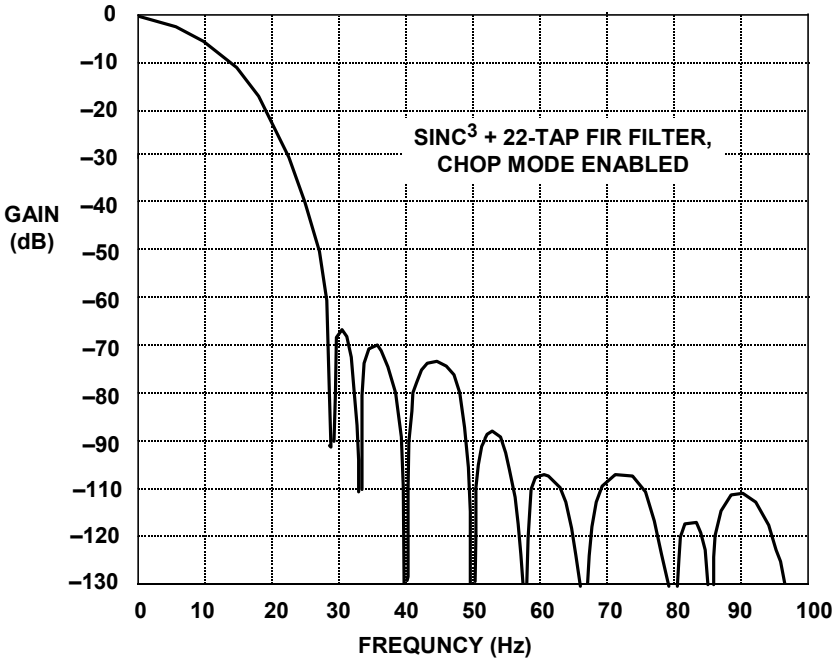

Figure 6.103: *AD7730 Digital Filter Response*

High Resolution Measurement Sigma-Delta ADCs

In order to better understand the capability of sigma-delta measurement ADCs and the power of the technique, a modern example, the AD7730, will be examined in detail. The AD7730 is a member of the AD77XX family and is shown in Figure 6.104. This ADC was specifically designed to interface directly to bridge outputs in weigh scale applications. The device accepts low level signals directly from a bridge and outputs a serial digital word. There are two buffered differential inputs which are multiplexed, buffered, and drive a PGA. The PGA can be programmed for four differential unipolar analog input ranges: 0 V to +10 mV, 0 V to +20 mV, 0 V to +40 mV, and 0 V to +80 mV and four differential bipolar input ranges: ±10 mV, ±20 mV, ±40 mV, and ±80 mV.

The maximum peak-to-peak, or noise-free resolution achievable is 1 in 230,000 counts, or approximately 18-bits. It should be noted that the noise-free resolution is a function of input voltage range, filter cutoff, and output word rate. Noise is greater using the smaller input ranges where the PGA gain must be increased. Higher output word rates and associated higher filter cutoff frequencies will also increase the noise.

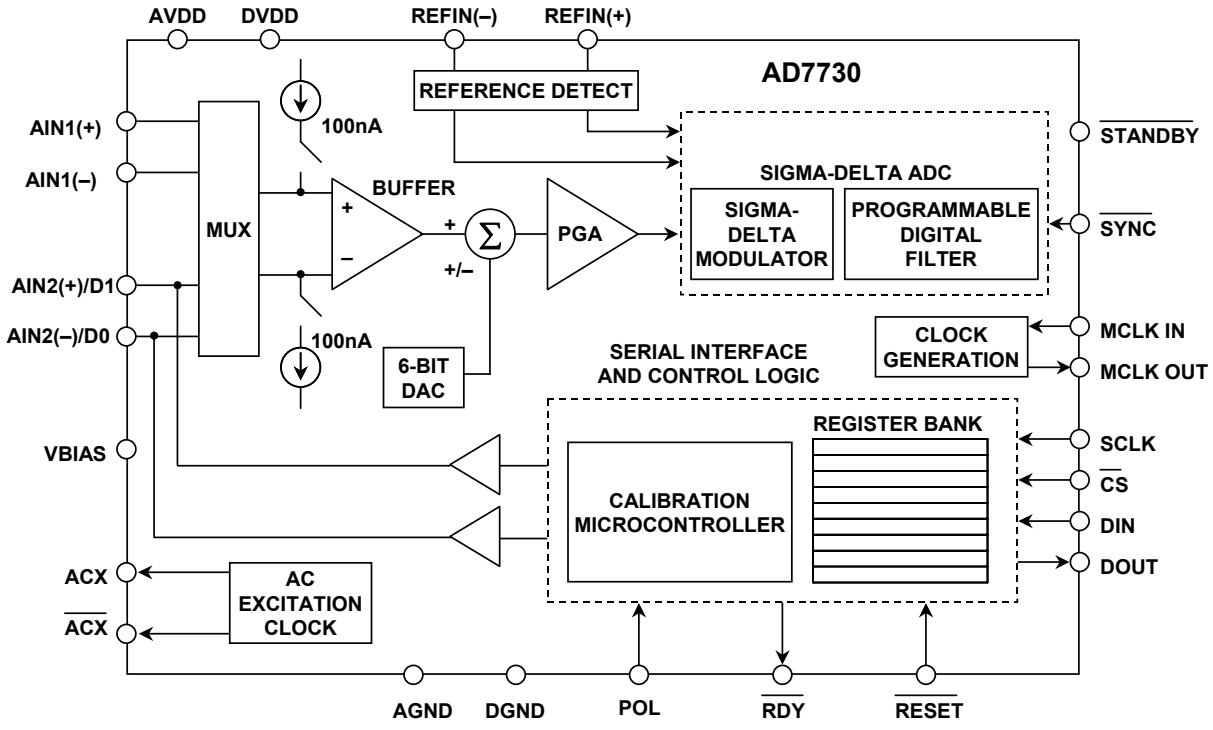

Figure 6.104: *AD7730 Sigma-Delta Single-Supply Bridge ADC*

The analog inputs are buffered on-chip allowing relatively high source impedances. Both analog channels are differential, with a common-mode voltage range that comes within 1.2 V of AGND and 0.95 V of AVDD. The reference input is also differential, and the common-mode range is from AGND to AVDD.

The 6-bit DAC is controlled by on-chip registers and can remove TARE (pan weight) values of up to ±80 mV from the analog input signal range. The resolution of the TARE function is 1.25 mV with a +2.5 V reference and 2.5 mV with a +5 V reference.

The output of the PGA is applied to the Σ-Δ modulator and programmable digital filter. The serial interface can be configured for three-wire operation and is compatible with microcontrollers and digital signal processors. The AD7730 contains self-calibration and system-calibration options and has an offset drift of less than 5 nV/ºC and a gain drift of less than 2 ppm/ºC. This low offset drift is obtained using a *chop* mode which operates similarly to a chopper-stabilized amplifier.

The oversampling frequency of the AD7730 is 4.9152 MHz, and the output data rate can be set from 50 Hz to 1200 Hz. The accuracy of the output of the ADC is dependant on the output data rate as shown in Tables I and II of Figure 6.105. These are taken from the AD7730. Note that the accuracy is also dependent on the PGA gain as well.

Table I. Output Noise vs. Input Range and Update Rate (CHP = 1)

Typical Output RMS Noise in nV

Output Data Rate	–3 dB Frequency	SF Word	Settling Time Normal Mode	Settling Time Fast Mode	Input Range = ±80 mV	Input Range = ±40 mV	Input Range = ±20 mV	Input Range = ±10 mV
50 Hz	1.97 Hz	2048	460 ms	60 ms	115	75	55	40
100 Hz	3.95 Hz	1024	230 ms	30 ms	155	105	75	60
150 Hz	5.92 Hz	683	153 ms	20 ms	200	135	95	70
200 Hz*	7.9 Hz	512	115 ms	15 ms	225	145	100	80
400 Hz	15.8 Hz	256	57.5 ms	7.5 ms	335	225	160	110

*Power-On Default

Table II. Peak-to-Peak Resolution vs. Input Range and Update Rate (CHP = 1)

Peak-to-Peak Resolution in Counts (Bits)

Output Data Rate	–3 dB Frequency	SF Word	Settling Time Normal Mode	Settling Time Fast Mode	Input Range = ±80 mV	Input Range = ±40 mV	Input Range = ±20 mV	Input Range = ±10 mV
50 Hz	1.97 Hz	2048	460 ms	60 ms	230k (18)	175k (17.5)	120k (17)	80k (16.5)
100 Hz	3.95 Hz	1024	230 ms	30 ms	170k (17.5)	125k (17)	90k (16.5)	55k (16)
150 Hz	5.92 Hz	683	153 ms	20 ms	130k (17)	100k (16.5)	70k (16)	45k (15.5)
200 Hz*	7.9 Hz	512	115 ms	15 ms	120k (17)	90k (16.5)	65k (16)	40k (15.5)
400 Hz	15.8 Hz	256	57.5 ms	7.5 ms	80k (16.5)	55k (16)	40k (15.5)	30k (15)

*Power-On Default

Figure 6.105: *Resolution vs. Output Data Rate and Gain for the AD7730*

This is easy to understand. The quantization is performed at the master clock rate (4.9152 MHz). If the data rate is increased, there is less time for filtering, so the measured result is noisier. Also as gain is increased, noise is increased as well.

While the output data word is 24 bits wide, there will not be a constant 24-bit data output, even with the input grounded. As seen in Table I, the maximum accuracy is on the order of 18 bits peak-to-peak. This gives rise to a new way of specifying accuracy. This is noise free counts. For the AD7730 this is 230,000.

The clock source can be provided via an external clock or by connecting a crystal oscillator across the MCLK IN and MCLK OUT pins.

The AD7730 can accept input signals from a dc-excited bridge. It can also handle input signals from an ac-excited bridge by using the ac excitation clock signals (ACX and $\overline{\text{ACX}}$). These are non-overlapping clock signals used to synchronize the external switches which drive the bridge. The ACX clocks are demodulated on the AD7730 input. The AD7730 contains two 100 nA constant current generators, one source current from AVDD to AIN(+) and one sink current from AIN(–) to AGND. The currents are switched to the selected analog input pair under the control of a bit in the Mode Register. These currents can be used in checking that a sensor is still operational before attempting to take measurements on that channel. If the currents are turned on and a full-scale reading is obtained, then the sensor has gone open circuit. If the measurement is 0 V, the sensor has gone short circuit. In normal operation, the burnout currents are turned off by setting the proper bit in the Mode Register to 0.

The AD7730 contains an internal programmable digital filter. The filter consists of two sections: a first stage filter, and a second stage filter. The first stage is a sinc^3 low-pass filter. The cutoff frequency and output rate of this first stage filter is programmable. The second stage filter has three modes of operation. In its normal mode, it is a 22-tap FIR filter that processes the output of the first stage filter. When a step change is detected on the analog input, the second stage filter enters a second mode (*FAST*Step™) where it performs a variable number of averages for some time after the step change, and then the second stage filter switches back to the FIR filter mode. The third option for the second stage filter (SKIP mode) is that it is completely bypassed so the only filtering provided on the AD7730 is the first stage. Both the *FAST*Step mode and SKIP mode can be enabled or disabled via bits in the control register. Again, there will be an affect on accuracy.

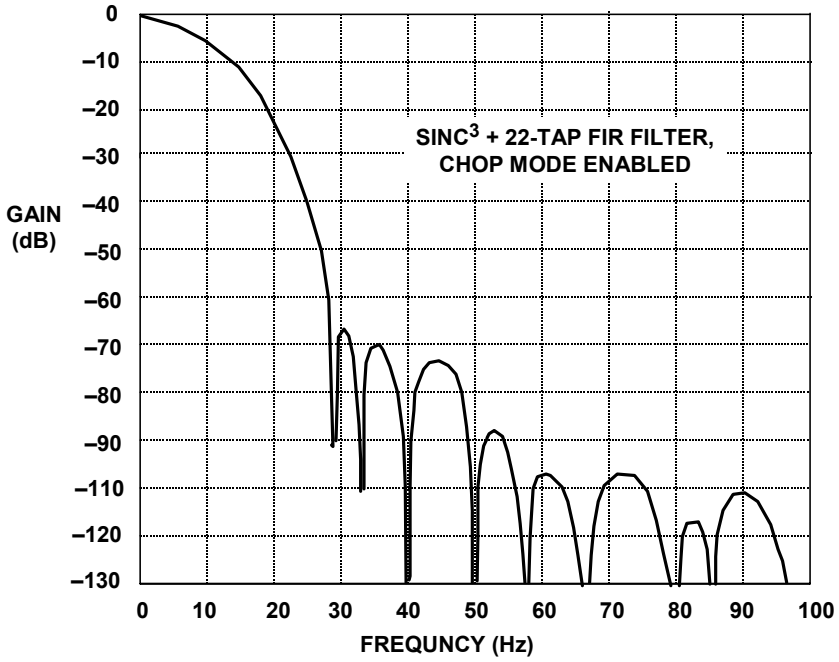

Figure 6.106: *AD7730 Digital Filter Response*

Figure 6.106 shows the full frequency response of the AD7730 when the second stage filter is set for normal FIR operation. This response is with the chop mode enabled and an

output word rate of 200 Hz and a clock frequency of 4.9152 MHz. The response is shown from dc to 100 Hz. The rejection at 50 Hz ± 1 Hz and 60 Hz ± 1 Hz is better than 88 dB.

Figure 6.107 shows the step response of the AD7730 with and without the *FAST*Step mode enabled. The vertical axis shows the code value and indicates the settling of the output to the input step change. The horizontal axis shows the number of output words required for that settling to occur. The positive input step change occurs at the 5th output.

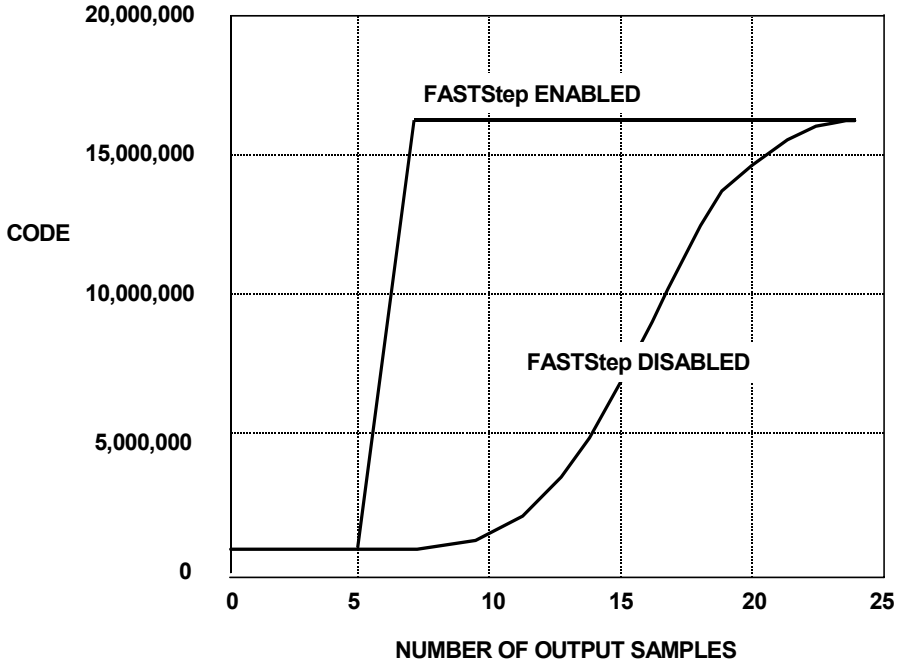

Figure 6.107: *AD7730 Digital Filter Settling Time Showing FASTStep Mode*

In the normal mode (*FAST*Step disabled), the output has not reached its final value until the 23rd output word. In *FAST*Step mode with chopping enabled, the output has settled to the final value by the 7th output word. Between the 7th and the 23rd output, the *FAST*Step mode produces a settled result, but with additional noise compared to the specified noise level for normal operating conditions. It starts at a noise level comparable to the SKIP mode, and as the averaging increases ends up at the specified noise level. The complete settling time required for the part to return to the specified noise level is the same for *FAST*Step mode and normal mode. The *FAST*Step mode gives a much earlier indication of where the output channel is going and its new value. This feature is very useful in weigh scale applications to give a much earlier indication of the weight, or in an application scanning multiple channels where the user does not have to wait the full settling time to see if a channel has changed.

Note, however, that the *FAST*Step mode is not particularly suitable for multiplexed applications because of the excess noise associated with the settling time. For multiplexed applications, the full 23-cycle output word interval should be allowed for settling to a new channel. This points out the fundamental issue of using Σ-Δ ADCs in

multiplexed applications. There is no reason why they won't work, provided the internal digital filter is allowed to settle fully after switching channels.

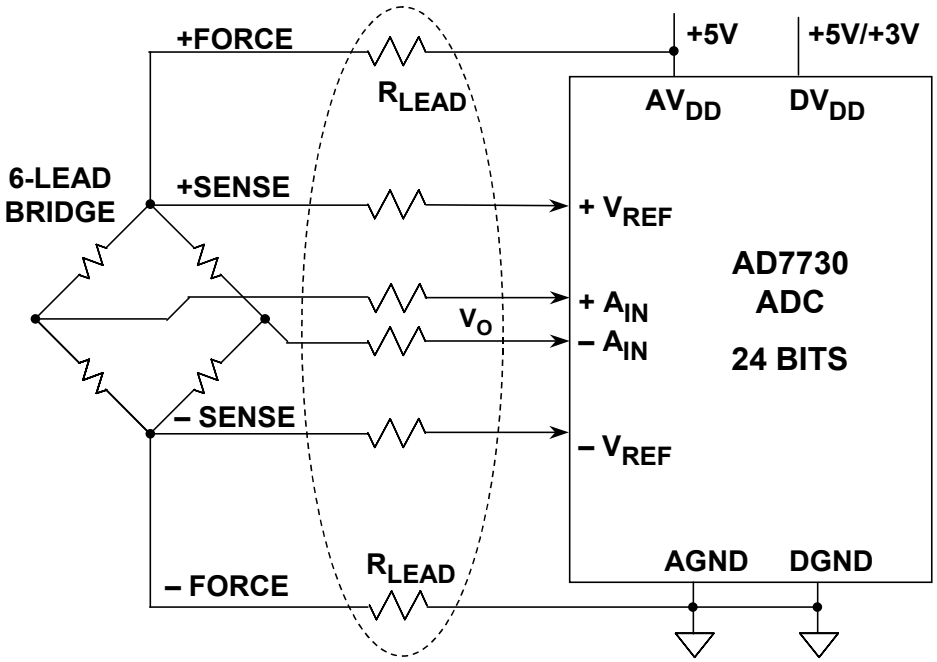

Figure 6.108: *AD7730 Bridge Application (Simplified Schematic)*

The AD7730 gives the user access to the on-chip calibration registers allowing an external microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part from prestored values in external E^2PROM. This gives the microprocessor much greater control over the AD7730's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^2PROM. Since the calibration coefficients are derived by performing a conversion on the input voltage provided, the accuracy of the calibration can only be as good as the noise level the part provides in the normal mode. To optimize calibration accuracy, it is recommended to calibrate the part at its lowest output rate where the noise level is lowest. The coefficients generated at any output rate will be valid for all selected output update rates. This scheme of calibrating at the lowest output data rate does mean that the duration of the calibration interval is longer.

The AD7730 requires an external voltage reference, however, the power supply may be used as the reference in the ratiometric bridge application shown in Figure 6.108. In this configuration, the bridge output voltage is directly proportional to the bridge drive voltage which is also used to establish the reference voltages to the AD7730. Variations in the supply voltage will not affect the accuracy. The SENSE outputs of the bridge are used for the AD7730 reference voltages in order to eliminate errors caused by voltage drops in the lead resistances.

Band-pass Sigma-Delta Converters

The Σ-Δ ADCs that we have described so far contain integrators, which are low-pass filters, whose pass band extends from dc. Thus, their quantization noise is pushed up in frequency. At present, most commercially available Σ-Δ ADCs are of this type (although some which are intended for use in audio or telecommunications applications contain band-pass rather than low-pass digital filters to eliminate any system dc offsets). But there is no particular reason why the filters of the Σ-Δ modulator should be LPFs, except that traditionally ADCs have been thought of as being baseband devices, and that integrators are somewhat easier to construct than band-pass filters. If we replace the integrators in a Σ-Δ ADC with band-pass filters (BPFs) as shown in Figure 6.109, the quantization noise is moved up and down in frequency to leave a virtually noise-free region in the pass band (see References 31, 32, and 33). If the digital filter is then programmed to have its pass band in this region, we have a Σ-Δ ADC with a band-pass, rather than a low-pass characteristic. Such devices would appear to be useful in direct IF-to-digital conversion, digital radios, ultrasound, and other undersampling applications. However, the modulator and the digital BPF must be designed for the specific set of frequencies required by the system application, thereby somewhat limiting the flexibility of this approach.

In an undersampling application of a band-pass Σ-Δ ADC, the minimum sampling frequency must be at least twice the signal bandwidth, BW. The signal is centered around a carrier frequency, f_C. A typical digital radio application using a 455-kHz center frequency and a signal bandwidth of 10 kHz is described in Reference 32. An oversampling frequency Kf_S = 2 MSPS and an output rate f_S = 20 kSPS yielded a dynamic range of 70 dB within the signal bandwidth.

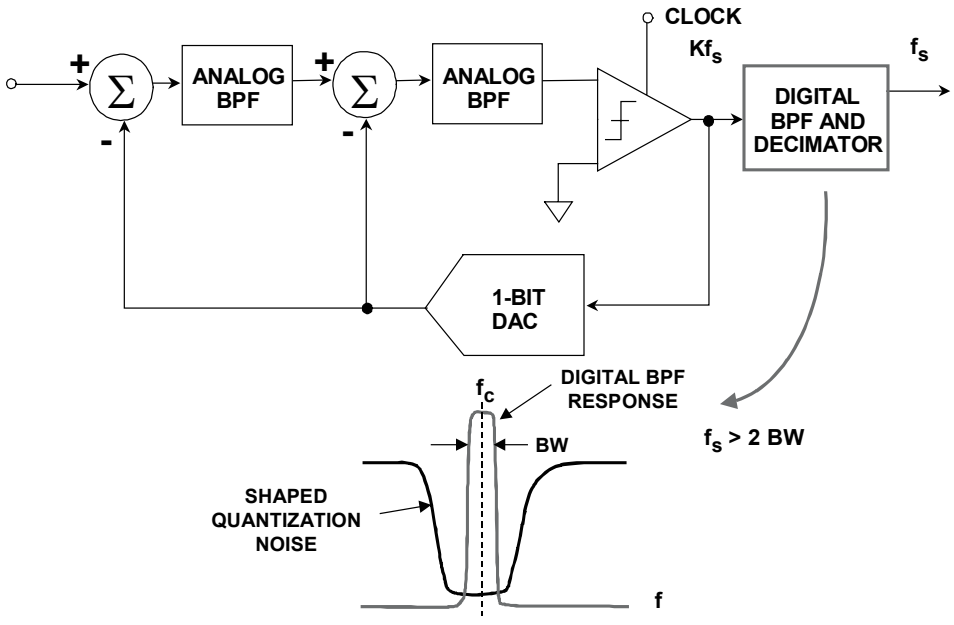

Figure 6.109: *Replacing Integrators with Resonators Gives a Band-Pass Sigma-Delta ADC*

Another example of a band-pass is the AD9870 IF Digitizing Subsystem having a nominal oversampling frequency of 18 MSPS, a center frequency of 2.25 MHz, and a bandwidth of 10 kHz to 150 kHz (see details in Reference 33).

Sigma-Delta DACs

Sigma-delta DACs operate very similarly to sigma-delta ADCs, however in a sigma-delta DAC, the noise shaping function is accomplished with a digital modulator rather than an analog one.

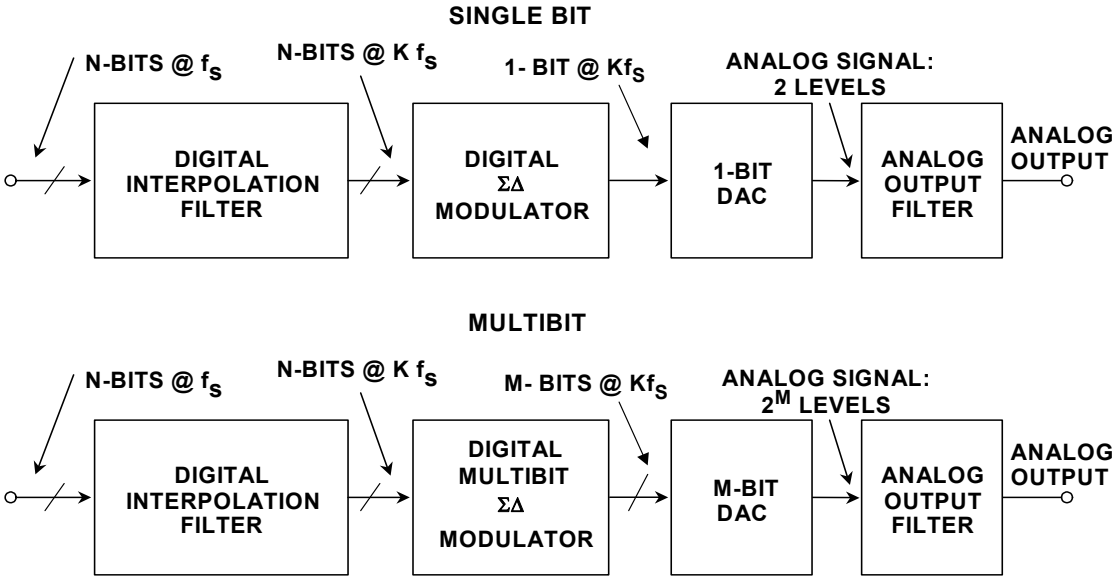

Figure 6.110: *Sigma-Delta DACs*

A Σ-Δ DAC, unlike the Σ-Δ ADC, is mostly digital (see Figure 6.110A). It consists of an "interpolation filter" (a digital circuit which accepts data at a low rate, inserts zeros at a high rate, and then applies a digital filter algorithm and outputs data at a high rate), a Σ-Δ modulator (which effectively acts as a low-pass filter to the signal but as a high-pass filter to the quantization noise, and converts the resulting data to a high speed bit stream), and a 1-bit DAC whose output switches between equal positive and negative reference voltages. The output is filtered in an external analog LPF. Because of the high oversampling frequency, the complexity of the LPF is much less than the case of traditional Nyquist operation.

It is possible to use more than one bit in the Σ-Δ DAC, and this leads to the *multibit* architecture shown in Figure 3.147B. The concept is similar to that of interpolating DACs previously discussed in Chapter 2, with the addition of the digital sigma-delta modulator. In the past, multibit DACs have been difficult to design because of the accuracy requirement on the n-bit internal DAC (this DAC, although only n-bits, must have the linearity of the final number of bits, N). The AD185x-series of audio DACs, however,

use a proprietary *data scrambling* technique (*called data directed scrambling*) which overcomes this problem and produces excellent performance with respect to all audio specifications (see References 27 and 28). For instance, the AD1853 dual 24-bit, 92 kSPS DAC has greater than 104 dB THD + N at a 48 kSPS sampling rate.

One of the newest members of this family is the AD1955 multibit sigma-delta audio DAC shown in Figure 6.111. The AD1955 also uses data directed scrambling, supports a multitude of DVD audio formats, and has an extremely flexible serial port. THD + N is typically 110 dB.

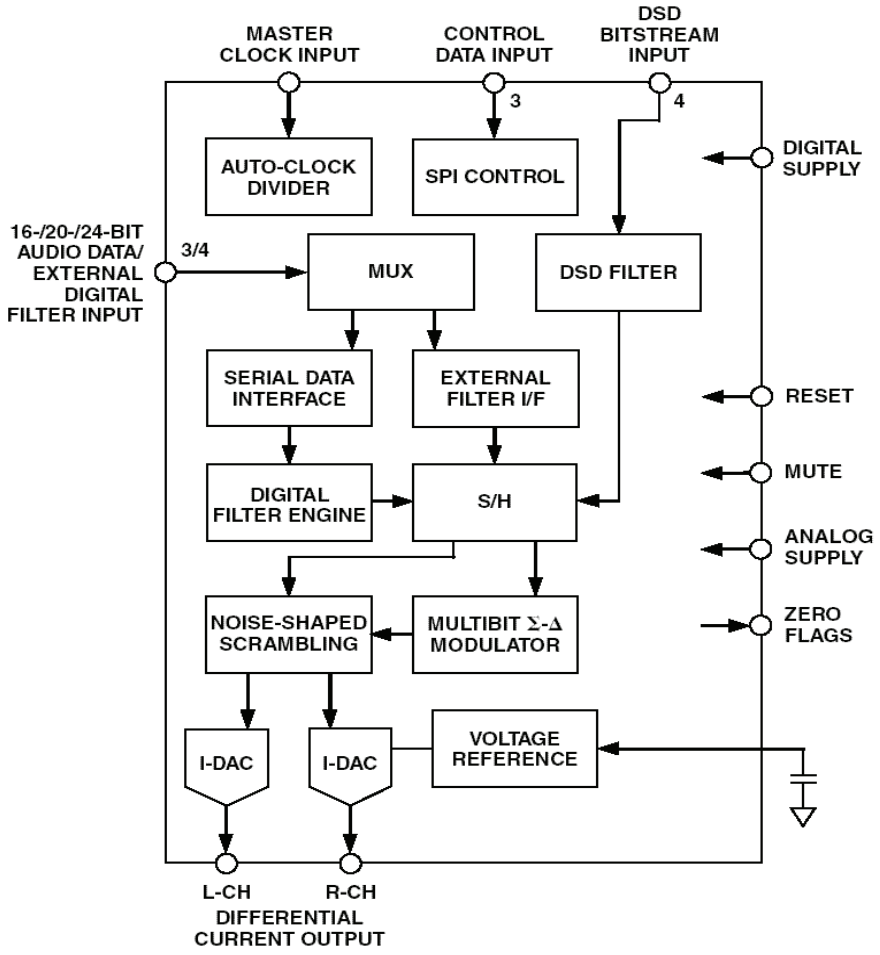

Figure 6.111: *AD1955 Multibit Sigma-Delta Audio DAC*

Summary

Sigma-delta ADCs and DACs have proliferated into many modern applications including measurement, voice-band, audio, etc. The technique takes full advantage of low cost CMOS processes and therefore makes integration with highly digital functions such as DSPs practical. Resolutions up to 24-bits are currently available, and the requirements on analog antialiasing/anti-imaging filters are greatly relaxed due to oversampling. Modern techniques such as the multibit data scrambled architecture minimize problems with idle tones which plagued early sigma-delta products.

Many sigma-delta converters offer a high level of user programmability with respect to output data rate, digital filter characteristics, and self-calibration modes. Multichannel sigma-delta ADCs are now available for data acquisition systems, and most users are well-educated with respect to the settling time requirements of the internal digital filter in these applications.

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Notes:

SECTION 6.4: DEFINING THE SPECIFICATONS

In specifying a converter there are basically two sets of specifications used for data converters. They can simplistically be divided into dc and ac specifications. Which you are more concerned with is based primarily on the application. DC specifications are more common with lower frequency applications. Here we are measuring against a reference. In ac specifications we are less concerned with absolute accuracy and more concerned with relative accuracy. This is not to say the reference is unimportant. It's just that we are typically interested in a relative number rather than an absolute. Distortion is always relative to the fundamental, for instance. While there is no direct conversion between the two, it is possible to infer that you need good linearity to get good distortion. It is rare to have a converter specified both ways.

Another point that should be made here is the difference between resolution and accuracy. While the two terms sometimes tend to be used interchangeably, they are not the same thing.

Resolution can be defined as the number of bits in the data word of the converter. Accuracy is the number of those bits that meet the specifications. As an example, an audio converter may have a data bus width of 24 bits, but only a signal to noise (SNR) range of 120 dB. 120 dB roughly corresponds to an accuracy of 20 bits. While 120 dB is not poor performance, it is not 24 bit performance.

You should keep in mind the magnitude in volts as well as in bits of the resolution of the converter that you are considering. This is shown in Figure 6.112 for a full-scale level of 2 V (note that there is some rounding off of the voltages in this table). This level is not uncommon for modern systems and is the typical standard for line level audio measurement. Remember that Gaussian noise of the system will probably set the lower limit of the accuracy spec. For example, 600 nV is the Johnson Noise in a 10 kHz BW of a 2.2 kΩ resistor @ 25°C. This corresponds to approximately 21.5 bits.

And some systems use even smaller full scales. Notably the AD7730 Σ-Δ ADC system is designed to operate with full-scale inputs down to 10 mV. With a 24-bit resolution this means a LSB weighting of 596 μV.

RESOLUTION N	2^N	VOLTAGE (2 V FS)	ppm FS	% FS	dB FS
2-bit	4	500 mV	250,000	25	– 12
4-bit	16	125 mV	62,500	6.25	– 24
6-bit	64	31.2 mV	15,625	1.56	– 36
8-bit	256	7.81 mV	3,906	0.39	– 48
10-bit	1,024	1.95 mV	977	0.098	– 60
12-bit	4,096	488 μV	244	0.024	– 72
14-bit	16,384	122 μV	61	0.0061	– 84
16-bit	65,536	30.5 μV	15	0.0015	– 96
18-bit	262,144	7.62 μV	4	0.0004	– 108
20-bit	1,048,576	1.9 μV	1	0.0001	– 120
22-bit	4,194,304	476 nV	0.24	0.000024	– 132
24-bit	16,777,216	119 nV	0.06	0.000006	– 144

Figure 6.112: *LSB size for a 2 V Full-Scale Input*

SECTION 6.5: DAC AND ADC STATIC TRANSFER FUNCTIONS AND DC ERRORS

The four primary dc errors in a data converter are *offset error*, *gain error*, and two types of *linearity error (differential and integral)*. Offset and gain errors are analogous to offset and gain errors in amplifiers as shown in Figure 6.113 for a bipolar input range. (Though offset error and zero error, which are identical in amplifiers and unipolar data converters, are not identical in bipolar converters and should be carefully distinguished.)

The transfer characteristics of both DACs and ADCs may be expressed as D = K + GA, where D is the digital code, A is the analog signal, and K and G are constants. In a unipolar converter, K is zero, and in an offset bipolar converter, it is –1 MSB. The offset error is the amount by which the actual value of K differs from its ideal value.

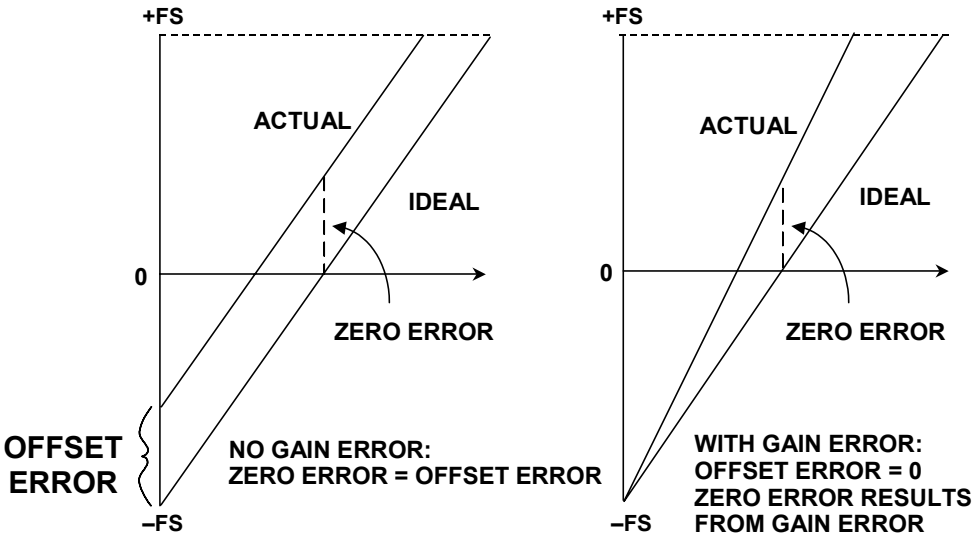


Figure 6.113: *Data Converter Offset and Gain Error*

The gain error is the amount by which G differs from its ideal value, and is generally expressed as the percentage difference between the two, although it may be defined as the gain error contribution (in mV or LSB) to the total error at full-scale. These errors can usually be trimmed by the data converter user. Note, however, that amplifier offset is trimmed at zero input, and then the gain is trimmed near to full-scale. The trim algorithm for a bipolar data converter is not so straightforward.

The integral linearity error of a converter is also analogous to the linearity error of an amplifier, and is defined as the maximum deviation of the actual transfer characteristic of the converter from a straight line, and is generally expressed as a percentage of full-scale (but may be given in LSBs). For an ADC, the most popular convention is to draw the straight line through the mid-points of the codes, or the code centers. There are two common ways of choosing the straight line: *end point* and *best straight line* as shown in Figure 6.114.

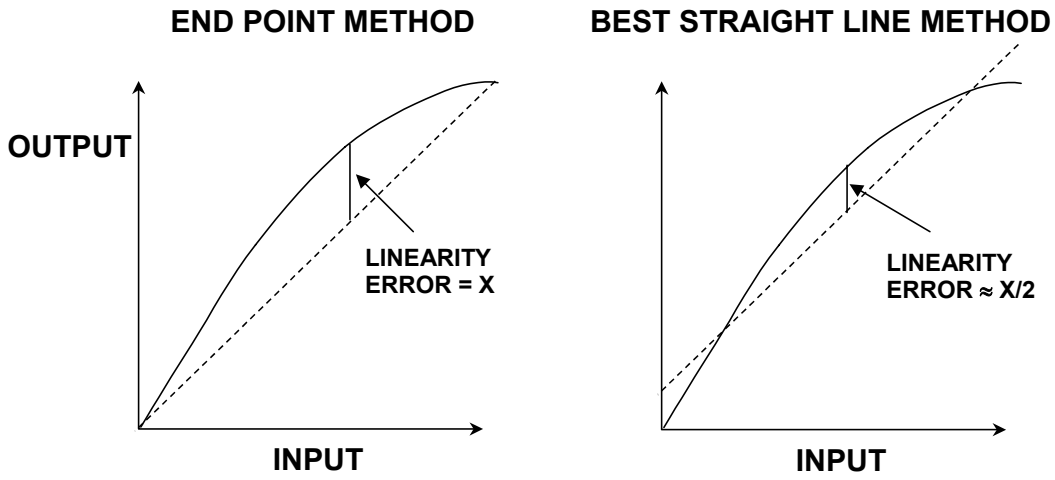


Figure 6.114: *Method of Measuring Integral Linearity Errors (Same Converter on Both Graphs)*

In the *endpoint* system, the deviation is measured from the straight line through the origin and the full-scale point (after gain adjustment). This is the most useful integral linearity measurement for measurement and control applications of data converters (since error budgets depend on deviation from the ideal transfer characteristic, not from some arbitrary "best fit"), and is the one normally adopted by Analog Devices, Inc.

The *best straight line*, however, does give a better prediction of distortion in ac applications, and also gives a lower value of "linearity error" on a data sheet. The best fit straight line is drawn through the transfer characteristic of the device using standard curve fitting techniques, and the maximum deviation is measured from this line. In general, the integral linearity error measured in this way is only 50% of the value measured by end point methods. This makes the method good for producing impressive data sheets, but it is less useful for error budget analysis. For ac applications, it is even better to specify distortion than dc linearity, so it is rarely necessary to use the best straight line method to define converter linearity.

The other type of converter nonlinearity is *differential nonlinearity* (DNL). This relates to the linearity of the code transitions of the converter. In the ideal case, a change of 1 LSB in digital code corresponds to a change of exactly 1 LSB of analog signal. In a DAC, a change of 1 LSB in digital code produces exactly 1 LSB change of analog output, while in an ADC there should be exactly 1 LSB change of analog input to move from one digital transition to the next. Differential linearity error is defined as the maximum amount of deviation of any quantum (or LSB change) in the entire transfer function from its ideal size of 1 LSB.

Where the change in analog signal corresponding to 1 LSB digital change is more or less than 1 LSB, there is said to be a DNL error. The DNL error of a converter is normally defined as the maximum value of DNL to be found at any transition across the range of the converter. Figure 6.115 shows the nonideal transfer functions for a DAC and an ADC and shows the effects of the DNL error.

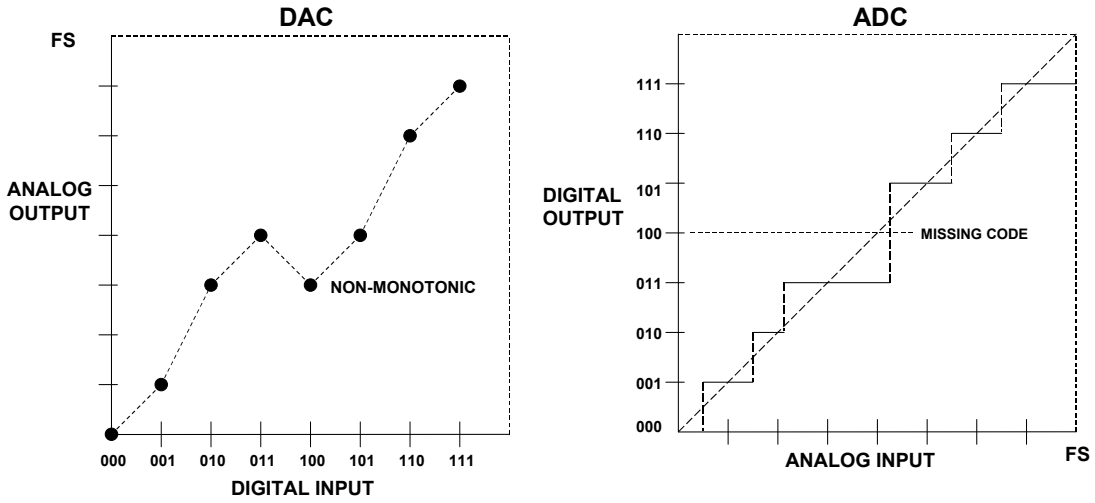


Figure 6.115: *Transfer Functions for Nonideal 3-Bit DAC and ADC*

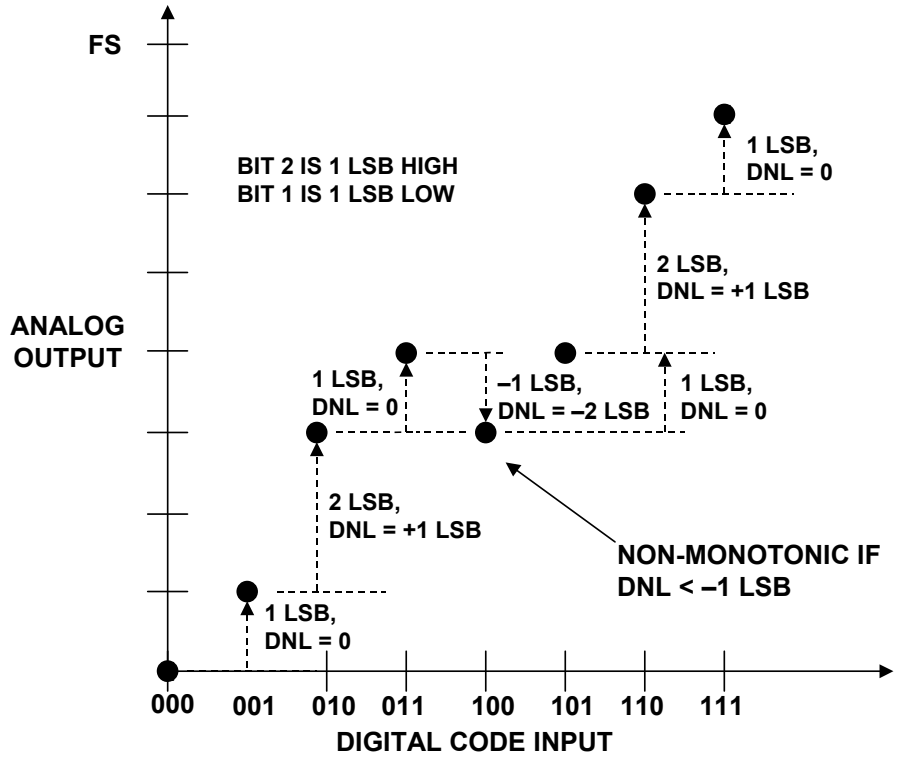


Figure 6.116: *Details of DAC Differential Nonlinearity*

The DNL of a DAC is examined more closely in Figure 6.116. If the DNL of a DAC is less than –1 LSB at any transition, the DAC is *nonmonotonic* i.e., its transfer characteristic contains one or more localized maxima or minima. A DNL greater than +1 LSB does not cause nonmonotonicity, but is still undesirable. In many DAC applications (especially closed-loop systems where nonmonotonicity can change negative feedback to positive feedback), it is critically important that DACs are monotonic. DAC monotonicity

is often explicitly specified on data sheets, although if the DNL is guaranteed to be less than 1 LSB (i.e., |DNL| ≤ 1 LSB) then the device must be monotonic, even without an explicit guarantee.

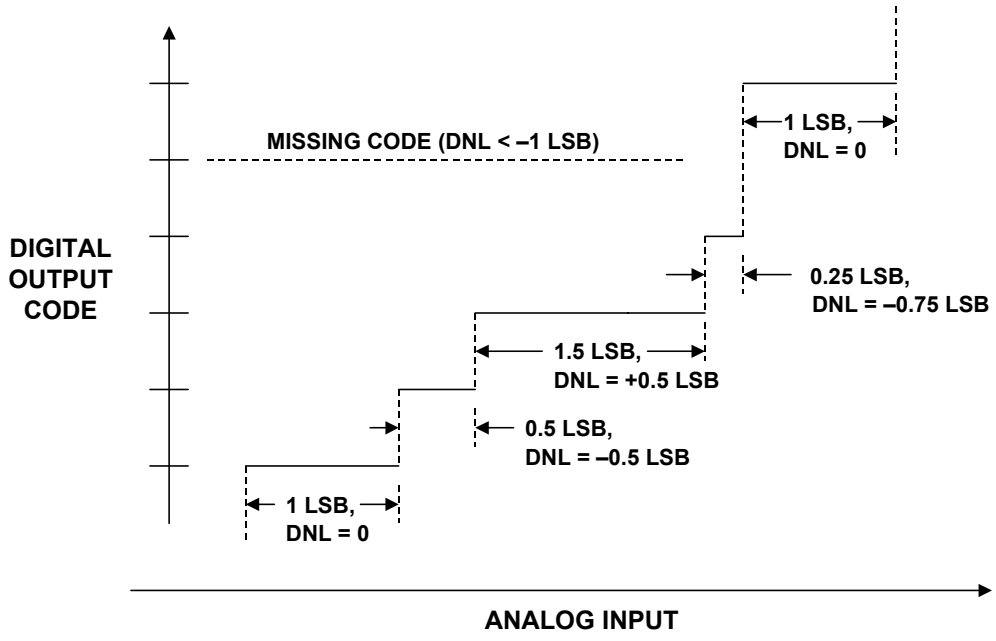


Figure 6.117: *Details of ADC Differential Nonlinearity*

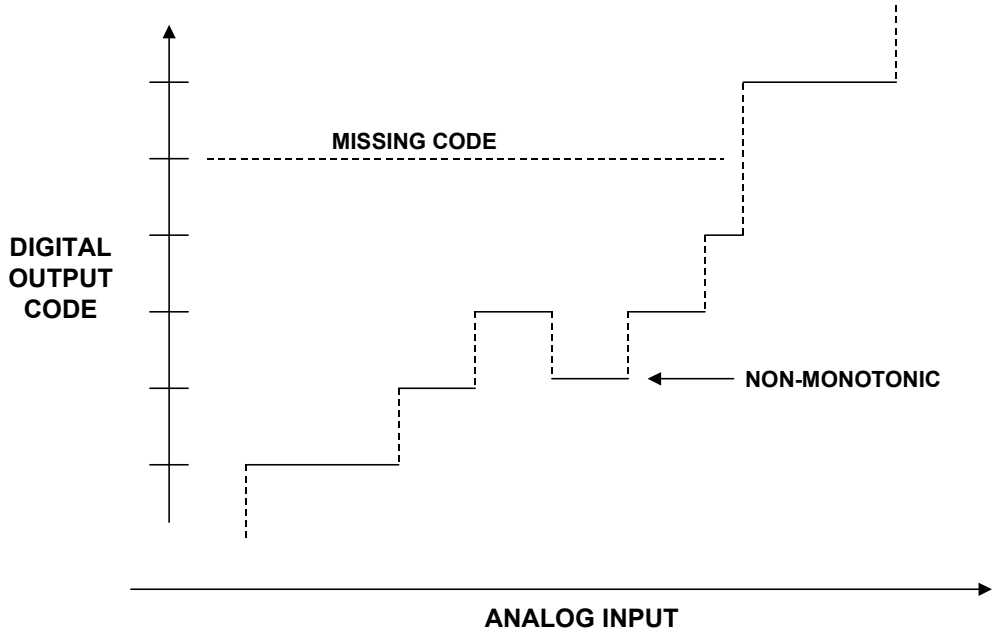


Figure 6.118: *Nonmonotonic ADC with Missing Code*

In Figure 6.117, the DNL of an ADC is examined more closely on an expanded scale. ADCs can be nonmonotonic, but a more common result of excess DNL in ADCs is *missing codes*. Missing codes in an ADC are as objectionable as nonmonotonicity in a DAC. Again, they result from DNL < –1 LSB.

Not only can ADCs have missing codes, they can also be nonmonotonic as shown in Figure 6.118. As in the case of DACs, this can present major problems—especially in servo applications.

In a DAC, there can be no missing codes—each digital input word will produce a corresponding analog output. However, DACs can be nonmonotonic as previously discussed. In a straight binary DAC, the most likely place a nonmonotonic condition can develop is at midscale between the two codes: 011…11 and 100…00. If a nonmonotonic condition occurs here, it is generally because the DAC is not properly calibrated or trimmed. A successive approximation ADC with an internal nonmonotonic DAC will generally produce missing codes but remain monotonic. However it is possible for an ADC to be nonmonotonic—again depending on the particular conversion architecture. Figure 6.118 shows the transfer function of an ADC which is nonmonotonic and has a missing code.

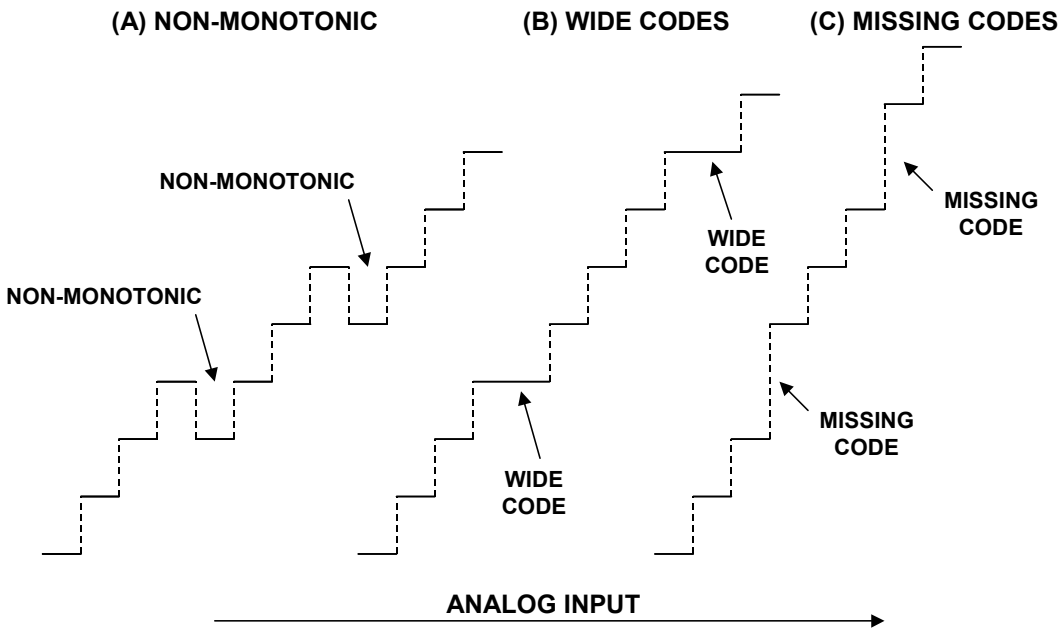


Figure 6.119: *Errors Associated with Improperly Trimmed Subranging ADC*

ADCs which use the *subranging* architecture divide the input range into a number of coarse segments, and each coarse segment is further divided into smaller segments—and ultimately the final code is derived. This process is described in more detail in Chapter 4 of this book. An improperly trimmed subranging ADC may exhibit nonmonotonicity, wide codes, or missing codes at the subranging points as shown in Figure 6.119 A, B, and C, respectively. This type of ADC should be trimmed so that drift due to aging or temperature produces wide codes at the sensitive points rather than nonmonotonic or missing codes.

Defining missing codes is more difficult than defining nonmonotonicity. All ADCs suffer from some inherent transition noise as shown in Figure 6.120 (think of it as the flicker between adjacent values of the last digit of a DVM). As resolutions and bandwidths become higher, the range of input over which transition noise occurs may approach, or even exceed, 1 LSB. High resolution wideband ADCs generally have internal noise sources which can be reflected to the input as effective input noise summed with the signal. The effect of this noise, especially if combined with a negative DNL error, may be that there are some (or even all) codes where transition noise is present for the whole range of inputs. There are therefore some codes for which there is *no* input which will *guarantee* that code as an output, although there may be a range of inputs which will *sometimes* produce that code.

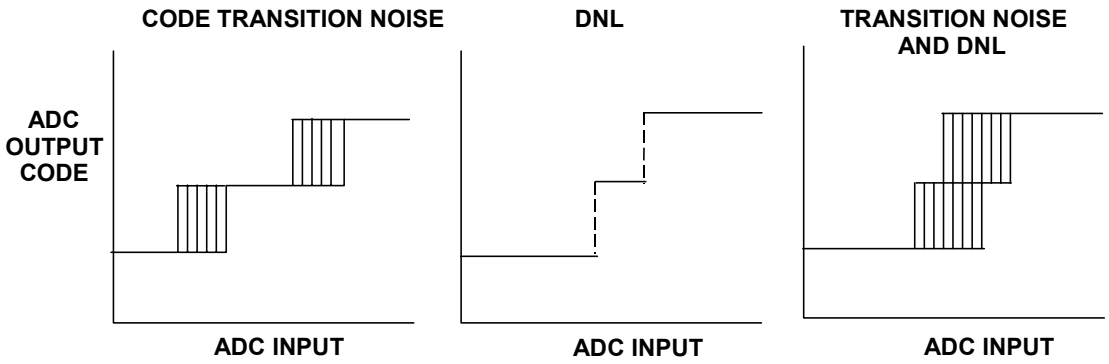


Figure 6.120: *Combined Effects of Code Transition Noise and DNL*

For low resolution ADCs, it may be reasonable to define *no missing codes* as a combination of transition noise and DNL which guarantees some level (perhaps 0.2 LSB) of noise-free code for all codes. However, this is impossible to achieve at the very high resolutions achieved by modern sigma-delta ADCs, or even at lower resolutions in wide bandwidth sampling ADCs. In these cases, the manufacturer must define noise levels and resolution in some other way. Which method is used is less important, but the data sheet should contain a clear definition of the method used and the performance to be expected. A complete discussion of effective input noise follows later in this chapter.

The discussion thus far has not dealt with the most important dc specifications associated with data converters. Other less important specifications require only a definition.

Accuracy, Absolute. Absolute accuracy error of a *DAC* is the difference between actual analog output and the output that is expected when a given digital code is applied to the converter. Error is usually commensurate with resolution, i.e., less 1/2 LSB of full-scale, for example. However, accuracy may be much better than resolution in some applications; for example, a 4-bit reference supply having only 16 discrete digitally chosen levels would have a resolution of 1/16, but it might have an accuracy to within 0.01 % of each ideal value.

Absolute accuracy error of an *ADC* at a given output code is the difference between the actual and the theoretical analog input voltages required to produce that code. Since the code can be produced by any analog voltage in a finite band (see *Quantizing Uncertainty*), the "input required to produce that code" is defined as the midpoint of the band of inputs that will produce that code. For example, if 5 volts, ±1.2 mV, will theoretically produce a 12-bit half-scale code of 1000 0000 0000, then a converter for which any voltage from 4.997 V to 4.999 V will produce that code will have absolute error of (1/2)(4.997 + 4.999) – 5 V = +2 mV.

Sources of error include gain (calibration) error, zero error, linearity errors, and noise. Absolute accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

Accuracy, Logarithmic DACs. The difference (measured in dB) between the actual transfer function and the ideal transfer function, as measured after calibration of gain error at 0 dB.

Accuracy, Relative. Relative accuracy error, expressed in %, ppm, or fractions of 1 LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated (see *Full-Scale Range*).

Since the discrete analog values that correspond to the digital values ideally lie on a straight line, the specified worst case relative accuracy error of a linear
ADC or DAC can be interpreted as a measure of end-point nonlinearity (see *Linearity).*

The "discrete points" of a DAC transfer characteristic are measured by the actual analog outputs. The "discrete points" of an ADC transfer characteristic are the midpoints of the quantization bands at each code (see *Accuracy, Absolute).*

Temperature Coefficient. In general, temperature instabilities are expressed as %/°C, ppm/°C, fractions of 1 LSB per degree C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, TC) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include gain, linearity, offset (bipolar), and zero.

a. *Gain Tempco:* Two factors principally affect converter gain stability with temperature. In fixed-reference converters, the reference voltage will vary with temperature. The reference circuitry and switches (and comparator in aid converters) will also contribute to the overall gain TC.

b. *Linearity Tempco:* Sensitivity of linearity (integral and/or differential linearity) to temperature, in % FSR/°C or ppm FSR/°C, over the specified range. Monotonic behavior in DACs is achieved if the differential nonlinearity is less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a temperature range, and/or implied by a statement that the device is monotonic over the specified temperature range. To avoid missing codes in noiseless ADCs, it is sufficient that the differential

nonlinearity error magnitude be greater than –1 LSB at any temperature in the range of interest. The differential nonlinearity temperature coefficient is often implied by the statement that there are no missed codes when operating within a specified temperature range. In DACs, the differential nonlinearity TC is often implied by the statement that the DAC is monotonic over a specified temperature range.

c. *Zero TC (unipolar converters):* The temperature stability of a unipolar fixed-reference DAC, measured in % FSR/°C or ppm FSR/°C, is principally affected by current leakage (current-output DAC), and offset voltage and bias current of the output op amp (voltage-output DAC). The zero stability of an ADC is dependent on the zero stability of the DAC or integrator and/or the input buffer and the comparator. It is typically expressed in μV/°C or in percent or ppm of full-scale range (FSR) per degree C.

d. *Offset Tempco:* The temperature coefficient of the all-DAC-switches-off (minus full-scale) point of a bipolar converter (in % FSR/°C or ppm FSR/°C) depends on three major factors—the tempco of the reference source, the voltage zero-stability of the output amplifier, and the tracking capability of the bipolar-offset resistors and the gain resistors. In an ADC, the corresponding tempco of the negative full-scale point depends on similar quantities—the tempco of the reference source, the voltage stability of the input buffer and the sample-and-hold, and the tracking capabilities of the bipolar offset resistors and the gain-setting resistors.

Common-Mode Range. Common-mode rejection usually varies with the magnitude of the range through which the input signal can swing, determined by the sum of the common-mode and the differential voltage. *Common-mode range* is that range of *total* input voltage over which specified common-mode rejection is maintained. For example, if the common-mode signal is ±5 V and the differential signal is ±5 V, the common-mode range is ±10 V.

Common-Mode Rejection (CMR) is a measure of the change in output voltage when both inputs are changed by equal amounts of ac and/or dc voltage. Common-mode rejection is usually expressed either as a ratio (e.g., CMRR = 1,000,000:1), or in decibels: CMR = $20\log_{10}$CMRR; if CMRR = 10^6, CMR = 120 dB. A CMRR of 10^6 means that 1 volt of common mode is processed by the device as though it were a differential signal of 1-microvolt at the input.

CMR is usually specified for a full-range common-mode voltage change (CMV), at a given frequency, and a specified imbalance of source impedance (e.g., 1 kΩ source unbalance, at 60 Hz). In amplifiers, the common-mode rejection ratio is defined as the ratio of the signal gain, G, to the common-mode gain (the ratio of common-mode signal appearing at the output to the CMV at the input.

Common-Mode Voltage (CMV). A voltage that appears in common at both input terminals of a device, with respect to its output reference (usually "ground"). For inputs, V_1 and V_2, with respect to ground, CMV = ½(V_1 + V_2). An ideal differential-input device would ignore CMV. *Common-mode error (CME)* is any error at the output due to the common-mode input voltage. The errors due to supply-voltage variation, an internal common- mode effect, are specified separately.

Compliance-Voltage Range. For a current source (e.g., a current-output DAC), the maximum range of (output) terminal voltage for which the device will maintain the specified current-output characteristics.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance. The real and complex impedances measured at each analog input port of an ADC. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range. The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180 degrees and taking the peak measurement again. Then the difference is computed between both peak measurements.

Full-Scale Range (FSR). For binary ADCs and DACs, that magnitude of voltage, current, or-in a multiplying DAC-gain, of which the MSB is specified to be exactly one-half or for which any bit or combination of bits is tested against its (their) prescribed ideal ratio(s). FSR is independent of resolution; the value of the LSB (voltage, current, or gain) is 2^{-N} FSR. There are several other terms, with differing meanings, that are often used in the context of discussions or operations involving full-scale range. They are:

Full-scale—similar to full-scale range, but pertaining to a single polarity. Thus, full-scale for a unipolar device is twice the prescribed value of the MSB and has the same polarity. For a bipolar device, *positive or negative full-scale* is that positive or negative value, of which the next bit after the polarity bit is tested to be one-half.

Span—the scalar voltage or current range corresponding to FSR.

All-1's—All bits on, the condition used, in conjunction with *all-zeros,* for gain adjustment of an ADC or DAC, in accordance with the manufacturer's instructions. Its magnitude, for a binary device, is $(1 - 2^{-N})$ FSR. *All-1's* is a *positive-true* definition of a specific magnitude relationship; for complementary coding the "all-l's" code will actually be all zeros. To avoid confusion, all-l's should never be called "full-scale;" FSR and FS are independent of the number of bits, all-l's isn't.

All-0's—All bits off, the condition used in offset (and gain) adjustment of a DAC or ADC, according to the manufacturer's instructions. All-0's corresponds to zero output in a unipolar DAC and negative full-scale in an offset bipolar DAC with positive output reference. In a sign-magnitude device, all-0's refers to all bits after the sign bit. Analogous to "all-l's," "all-0's" is a *positive-true* definition of the *all-bits-off* condition; in a complementary-coded device, it is expressed by all ones. To avoid confusion, all-0's should not be called "zero" unless it accurately corresponds to true analog zero output from a DAC.

The best way of defining the critical points for an actual device is a brief table of critical codes and the ideal voltages, currents, or gains to which they correspond, with the conditions for measurement defined.

Gain: The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10 volts full-scale. In a multiplying DAC or ratiometric ADC, it is indeed a gain. In a device with fixed internal reference, it is expressed as the full-scale magnitude of the output parameter (e.g., 10 volts or 2 milliamperes). In a fixed-reference converter, where the use of the internal reference is optional, the converter gain and the reference may be specified separately. Gain and zero adjustment are discussed under *zero.*

Impedance, Input: The dynamic load of an ADC presented to its input source. In unbuffered CMOS switched-capacitor ADCs, the presence of current transients at the converter's clock frequency mandates that the converter be driven from a low impedance (at the frequencies contained in the transients) in order to accurately convert. For buffered-input ADCs, the input impedance is generally represented by a resistive and capacitive component.

Input-Referred Noise (Effective Input Noise): Input-referred noise can be viewed as the net effect of all internal ADC noise sources referred to the input. It is generally expressed in *LSBs rms*, but can also be expressed as a voltage. It can be converted to a peak-to-peak value by multiplying by the factor 6.6. The peak-to-peak input-referred noise can then be used to calculate the *noise-free code resolution*. (See *noise-free code resolution*).

Leakage Current, Output: Current which appears at the output terminal of a DAC with all bits "off." For a converter with two complementary outputs (for example, many fast CMOS DACs), output leakage current is the current measured at OUT 1, with all digital inputs *low—and* the current measured at OUT 2, with all digital inputs *high.*

Output Propagation Delay: For an ADC having a single-ended sampling (or ENCODE) clock input, the delay between the 50% point of the sampling clock and the time when all output data bits are within valid logic levels. For an ADC having differential sampling clock inputs, the delay is measured with respect to the zero-crossing of the differential sampling clock signal.

Output Voltage Tolerance: For a reference, the maximum deviation from the normal output voltage at 25°C and specified input voltage, as measured by a device traceable to a recognized fundamental voltage standard.

Overload: An input voltage exceeding the ADC's full-scale input range producing an overload condition.

Overvoltage Recovery Time: Overvoltage recovery time is defined as the amount of time required for an ADC to achieve a specified accuracy after an overvoltage (usually 50% greater than full-scale range), measured from the time the overvoltage signal reenters the converter's range. The ADC should act as an ideal limiter for out-of-range signals, producing a positive or negative full-scale code during the overvoltage condition. Some ADCs provide over- and under-range flags to allow gain-adjustment circuits to be activated.

Overrange, Overvoltage: An input signal that exceeds the input range of an ADC, but is less than an overload.

Power-Supply Rejection Ratio (PSRR: The ratio of a change in dc power supply voltage to the resulting change in the specified device error, expressed in percentage, parts per million, or fractions of 1 LSB. It may also be expressed logarithmically, in dB (PSR = 20 $\log_{10}$ (PSRR)).

Power Supply Sensitivity. The sensitivity of a converter to changes in the power supply voltages is normally expressed in terms of percent-of-full-scale change in analog value or fractions of 1 LSB—(DAC output, ADC output code-center) for a 1% dc change in the power supply, e.g., 0.05%/% ΔV_S. Power supply sensitivity may also be expressed in relation to a specified maximum dc shift of power supply voltage. A converter might be considered "good" if the change in reading at full-scale does not exceed ±½ LSB for a 3% change in power supply voltage. Even better specs are necessary for converters designed for direct battery operation.

Ratiometric: The output of an ADC is a digital number proportional to the *ratio* of (some measure of) the input to a reference voltage. Most requirements for conversions call for an absolute measurement, i.e., against a fixed reference; but this presumes that the signal applied to the converter is either reference independent, or in some way derived from another fixed reference. However, real references are not truly fixed; the references for both the converter and the signal source vary with time, temperature, loading, etc. Therefore, if the converter is used with signal sources that also rely on references (for example, strain-gage bridges, RTDs, thermistors), it makes sense to replace this multiplicity of references by a single system reference; reference-caused errors will tend to cancel out. This can be done by using the converter's internal reference (if it has one) as the system reference. Another way is to use a separate external system reference, which also becomes the reference for a *ratiometric* converter.

Over limited ranges, ratiometric conversion can also serve as a substitute for analog or digital signal division (where the denominator changes by less than ½LSB during the conversion). The signal input is the numerator; the reference input is the denominator.

Total Unadjusted Error: A comprehensive specification on some devices which includes full-scale error, relative-accuracy and zero-code errors, under a specified set of conditions.

Notes:

SECTION 6.6: DATA CONVERTER AC ERRORS

This section examines the ac errors associated with data converters. Many of the errors and specifications apply equally to ADCs and DACs, while some are more specific to one or the other. All possible specifications are not discussed here, only the most popular ones.

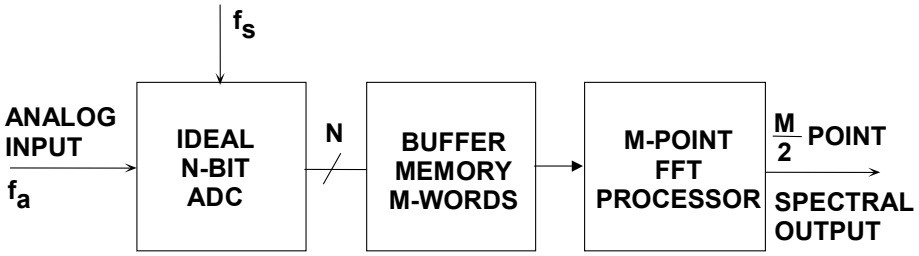


Figure 6.121: *Dynamic Performance Analysis of an Ideal N-bit ADC*

In most applications, the input to the ADC is a band of frequencies (usually summed with some noise), so the quantization noise tends to be random. In spectral analysis applications (or in performing FFTs on ADCs using spectrally pure sinewaves—see Figure 6.121), however, the correlation between the quantization noise and the signal depends upon the ratio of the sampling frequency to the input signal. This is demonstrated in Figure 6.122, where an ideal 12-bit ADCs output is analyzed using a 4096-point FFT. In the left-hand FFT plot, the ratio of the sampling frequency to the input frequency was chosen to be exactly 32, and the worst harmonic is about 76 dB below the fundamental. The right hand diagram shows the effects of slightly offsetting the ratio to 4096/127 = 32.25196850394, showing a relatively random noise spectrum, where the SFDR is now about 92 dBc. In both cases, the rms value of all the noise components is approximately $q/\sqrt{12}$, but in the first case, the noise is concentrated at harmonics of the fundamental.

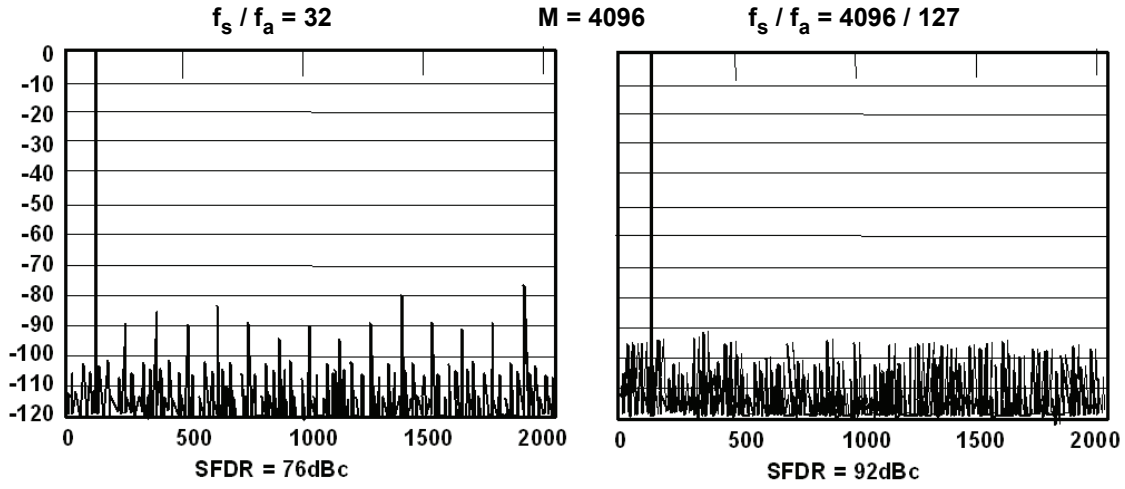


Figure 6.122: *Effect of Ratio of Sampling Clock to Input Frequency on SFDR for Ideal 12-bit ADC*

Note that this variation in the apparent harmonic distortion of the ADC is an artifact of the sampling process and the correlation of the quantization error with the input frequency. In a practical ADC application, the quantization error generally appears as random noise because of the random nature of the wideband input signal and the additional fact that there is a usually a small amount of system noise which acts as a *dither* signal to further randomize the quantization error spectrum.

It is important to understand the above point, because single-tone sine wave FFT testing of ADCs is a universally accepted method of performance evaluation. In order to accurately measure the harmonic distortion of an ADC, steps must be taken to ensure that the test setup truly measures the ADC distortion, not the artifacts due to quantization noise correlation. This is done by properly choosing the frequency ratio and sometimes by injecting a small amount of noise (dither) with the input signal. The exact same precautions apply to measuring DAC distortion with an analog spectrum analyzer.

Figure 6.123 shows the FFT output for an ideal 12-bit ADC. Note that the average value of the noise floor of the FFT is approximately 100 dB below full-scale, but the theoretical SNR of a 12-bit ADC is 74 dB. The FFT noise floor is *not* the SNR of the ADC, because the FFT acts like an analog spectrum analyzer with a bandwidth of f_s/M, where M is the number of points in the FFT. The theoretical FFT noise floor is therefore $10\log_{10}(M/2)$ dB below the quantization noise floor due to the *processing gain* of the FFT. In the case of an ideal 12-bit ADC with an SNR of 74 dB, a 4096-point FFT would result in a processing gain of $10\log_{10}(4096/2) = 33$ dB, thereby resulting in an overall FFT noise floor of 74 + 33 = 107 dBc. In fact, the FFT noise floor can be reduced even further by going to larger and larger FFTs; just as an analog spectrum analyzer's noise floor can be reduced by narrowing the bandwidth. When testing ADCs using FFTs, it is important to ensure that the FFT size is large enough so that the distortion products can be distinguished from the FFT noise floor itself.

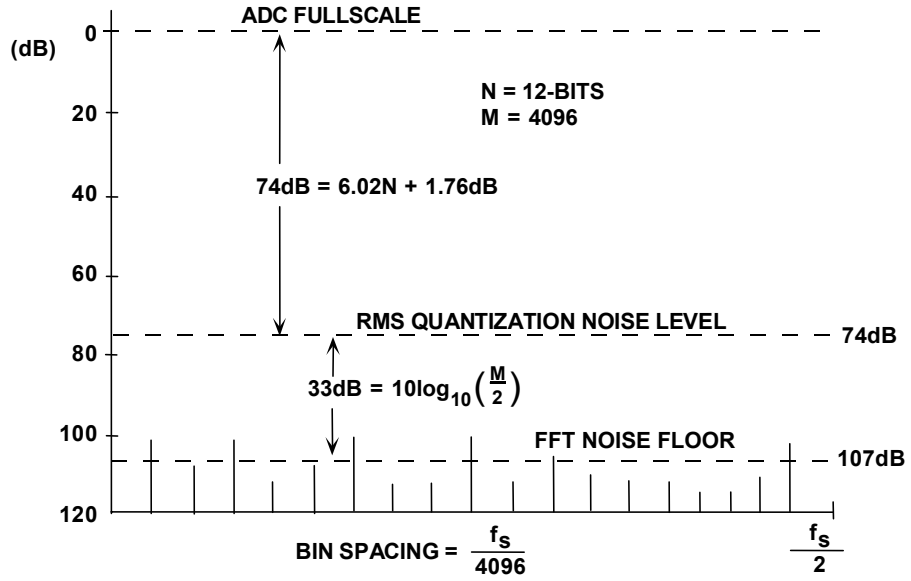


Figure 6.123: *Noise Floor for an Ideal 12-bit ADC Using 4096-point FFT*

Noise in Practical ADCs

A practical sampling ADC (one that has an integral sample-and-hold), regardless of architecture, has a number of noise and distortion sources as shown in Figure 6.124. The wideband analog front-end buffer has wideband noise, nonlinearity, and also finite bandwidth. The SHA introduces further nonlinearity, bandlimiting, and aperture jitter. The actual quantizer portion of the ADC introduces quantization noise, and both integral and differential nonlinearity. In this discussion, assume that sequential outputs of the ADC are loaded into a buffer memory of length M and that the FFT processor provides the spectral output. Also assume that the FFT arithmetic operations themselves introduce no significant errors relative to the ADC. However, when examining the output noise floor, the FFT processing gain (dependent on M) must be considered.

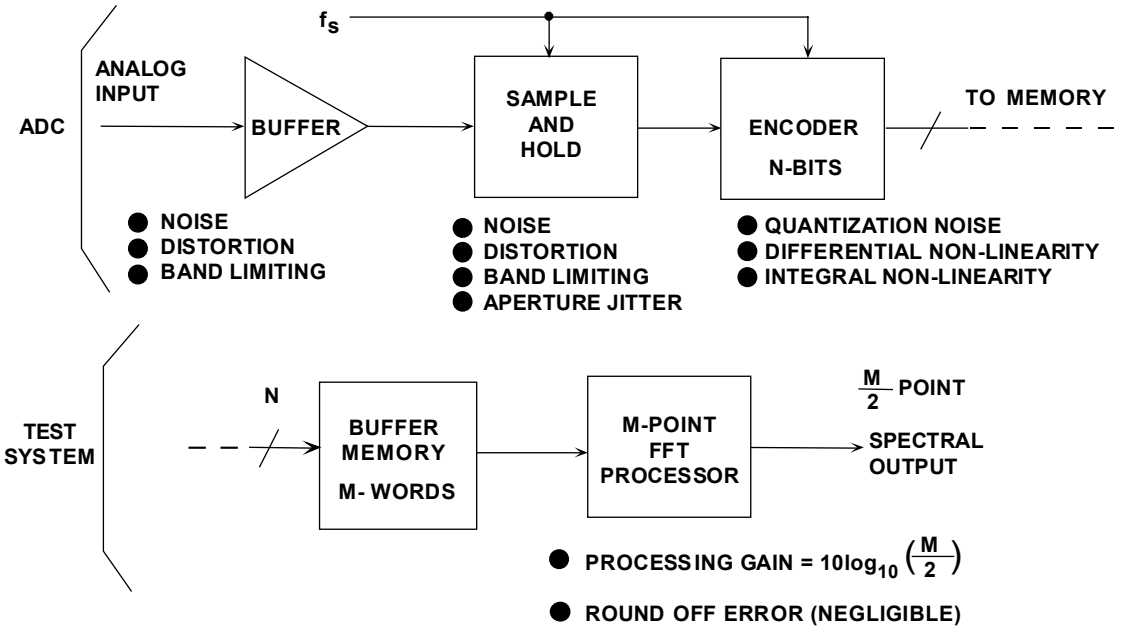


Figure 6.124: *ADC Model Showing Noise and Distortion Sources*

Equivalent Input Referred Noise

Wideband ADC internal circuits produce a certain amount of rms noise due to resistor and kT/C noise. This noise is present even for dc-input signals, and accounts for the fact that the output of most wideband (or high resolution) ADCs is a distribution of codes, centered around the nominal value of a dc input (see Figure 6.125). To measure its value, the input of the ADC is either grounded or connected to a heavily decoupled voltage source, and a large number of output samples are collected and plotted as a histogram (sometimes referred to as a *grounded-input* histogram). Since the noise is approximately Gaussian, the standard deviation of the histogram is easily calculated (see Reference 6), corresponding to the effective input rms noise. It is common practice to express this rms noise in terms of LSBs rms, although it can be expressed as an rms voltage referenced to the ADC full-scale input range.

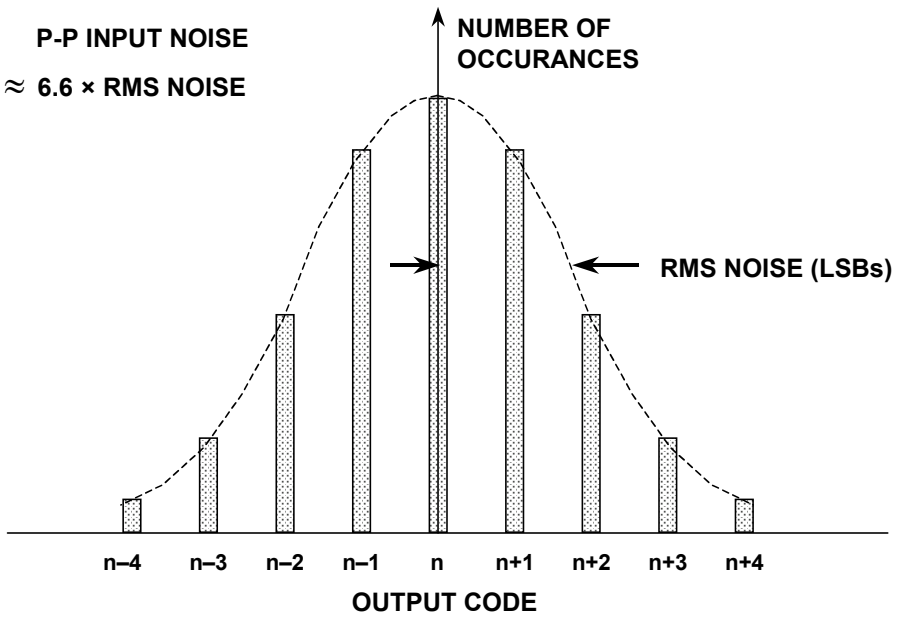


Figure 6.125: *Effect of Input-Referred Noise on ADC "Grounded Input" Histogram*

Noise-Free (Flicker-Free) Code Resolution

The *noise-free code resolution* of an ADC is the number of bits beyond which it is impossible to distinctly resolve individual codes. The cause is the effective input noise (or input-referred noise) associated with all ADCs and described above. This noise can be expressed as an rms quantity, usually having the units of *LSBs rms*. Multiplying by a factor of 6.6 converts the rms noise into peak-to-peak noise (expressed in *LSBs peak-to-peak*). The total range of an N-bit ADC is 2^N LSBs. The noise-free (or flicker-free) resolution can be calculated using the equation:

$$\text{Noise-Free Code Resolution} = \log_2 (2^N/\text{Peak-to-Peak Noise}). \qquad \text{Eq. 6.17}$$

The specification is generally associated with high-resolution sigma-delta measurement ADCs, but is applicable to all ADCs.

The ratio of the FS range to the *rms* input noise is sometimes used to calculate resolution. In this case, the term *effective resolution* is used. Note that under identical conditions, effective resolution is larger than noise-free code resolution by $\log_2(6.6)$, or approximately 2.7 bits.

$$\text{Effective Resolution} = \log_2 (2^N/\text{RMS Input Noise}) \qquad \text{Eq. 6.18}$$

$$\text{Effective Resolution} = \text{Noise-Free Code Resolution} + 2.7 \text{ bits}. \qquad \text{Eq. 6.19}$$

The calculations are summarized in Figure 6.126.

- Effective Input Noise = $e_{n\ rms}$
- Peak-to-Peak Input Noise = $6.6\ e_{n\ rms}$
- Noise-Free Code Resolution $= \log_2 \left[\frac{\text{Peak-to-Peak Input Range}}{\text{Peak-to-Peak Input Noise}} \right]$

$$= \log_2 \left[\frac{2^N}{\text{Peak-to-Peak Input Noise (LSBs)}} \right]$$

- "Effective Resolution" $= \log_2 \left[\frac{\text{Peak-to-Peak Input Range}}{\text{RMS Input Noise}} \right]$

$$= \log_2 \left[\frac{2^N}{\text{RMS Input Noise (LSBs)}} \right]$$

$$= \text{Noise-Free Code Resolution} + 2.7 \text{ bits}$$

Figure 6.126: *Calculating Noise-Free (Flicker-Free) Code Resolution from Input-Referred Noise*

Dynamic Performance of Data Converters

There are various ways to characterize the ac performance of ADCs. In the early years of ADC technology (over 30 years ago) there was little standardization with respect to ac specifications, and measurement equipment and techniques were not well understood or available. Over nearly a 30 year period, manufacturers and customers have learned more about measuring the dynamic performance of converters, and the specifications shown in Figure 6.127 represent the most popular ones used today. Practically all the specifications represent the converter's performance in the frequency domain. The FFT is the heart of practically all these measurements and is discussed in more detail in a latter section.

Integral and Differential Nonlinearity Distortion Effects

One of the first things to realize when examining the nonlinearities of data converters is that the transfer function of a data converter has artifacts which do not occur in conventional linear devices such as op amps or gain blocks. The overall integral nonlinearity of an ADC is due to the integral nonlinearity of the front-end and SHA as well as the overall integral nonlinearity in the ADC transfer function. However, *differential nonlinearity is due exclusively to the encoding process* and may vary considerably dependent on the ADC encoding architecture. Overall integral nonlinearity produces distortion products whose amplitude varies as a function of the input signal amplitude. For instance, second-order intermodulation products increase 2 dB for every

1-dB increase in signal level, and third-order products increase 3 dB for every 1-dB increase in signal level.

- **Harmonic Distortion**
- **Worst Harmonic**
- **Total Harmonic Distortion (THD)**
- **Total Harmonic Distortion Plus Noise (THD + N)**
- **Signal-to-Noise-and-Distortion Ratio (SINAD, or S/N +D)**
- **Effective Number of Bits (ENOB)**
- **Signal-to-Noise Ratio (SNR)**
- **Analog Bandwidth (Full-Power, Small-Signal)**
- **Spurious Free Dynamic Range (SFDR)**
- **Two-Tone Intermodulation Distortion**
- **Multi-tone Intermodulation Distortion**
- **Noise Power Ratio (NPR)**
- **Adjacent Channel Leakage Ratio (ACLR)**
- **Noise Figure**
- **Settling Time, Overvoltage Recovery Time**

Figure 6.127: *Quantifying Data Converter Dynamic Performance*

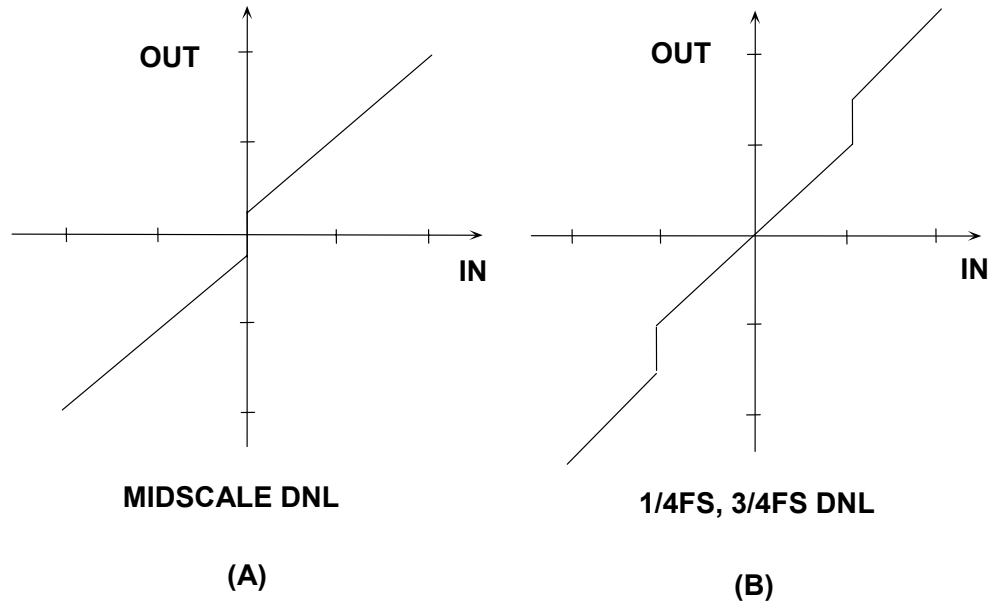


Figure 6.128: *Typical ADC/ DAC DNL Errors (Exaggerated)*

The differential nonlinearity in the ADC transfer function produces distortion products which not only depend on the amplitude of the signal but the positioning of the differential nonlinearity errors along the ADC transfer function. Figure 6.128 shows two

ADC transfer functions having differential nonlinearity. The left-hand diagram shows an error which occurs at mid-scale. Therefore, for both large and small signals, the signal crosses through this point producing a distortion product which is relatively independent of the signal amplitude. The right-hand diagram shows another ADC transfer function which has differential nonlinearity errors at 1/4 full-scale and 3/4 full-scale. Signals which are above 1/2 scale peak-to-peak will exercise these codes and produce distortion, while those less than 1/2 scale peak-to-peak will not.

Most high-speed ADCs are designed so that differential nonlinearity is spread across the entire ADC range. Therefore, for signals which are within a few dB of full-scale, the overall integral nonlinearity of the transfer function determines the distortion products. For lower level signals, however, the harmonic content becomes dominated by the differential nonlinearities and does not generally decrease proportionally with decreases in signal amplitude.

Harmonic Distortion, Worst Harmonic, Total Harmonic Distortion (THD), Total Harmonic Distortion Plus Noise (THD + N)

There are a number of ways to quantify the distortion of an ADC. An FFT analysis can be used to measure the amplitude of the various harmonics of a signal. The harmonics of the input signal can be distinguished from other distortion products by their location in the frequency spectrum. Figure 6.129 shows a 7 MHz input signal sampled at 20 MSPS and the location of the first 9 harmonics. Aliased harmonics of f_a fall at frequencies equal to $|\pm Kf_s \pm nf_a|$, where n is the order of the harmonic, and K = 0, 1, 2, 3, ... The second and third harmonics are generally the only ones specified on a data sheet because they tend to be the largest, although some data sheets may specify the value of the *worst* harmonic.

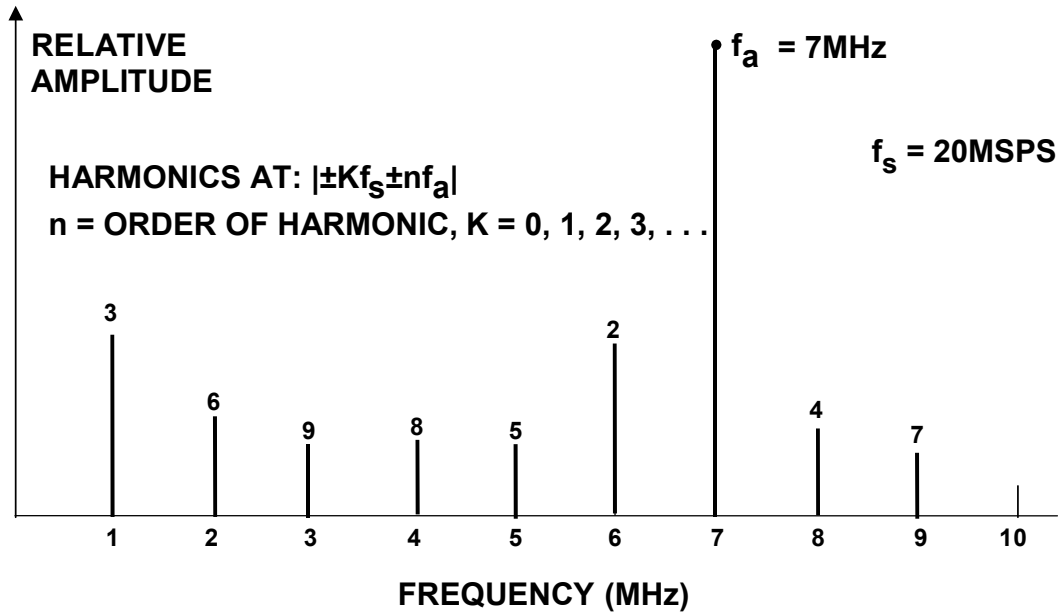


Figure 6.129: *Location of Distortion Products: Input Signal = 7 MHz, Sampling Rate = 20 MSPS*

Harmonic distortion is normally specified in dBc (decibels below *carrier*), although at audio frequencies it may be specified as a percentage. Harmonic distortion is generally specified with an input signal near full-scale (generally 0.5 dB to 1 dB below full-scale to prevent clipping), but it can be specified at any level. For signals much lower than full-scale, other distortion products due to the DNL of the converter (not direct harmonics) may limit performance.

Total harmonic distortion (THD) is the ratio of the rms value of the fundamental signal to the mean value of the root-sum-square of its harmonics (generally, only the first five are significant). THD of an ADC is also generally specified with the input signal close to full-scale, although it can be specified at any level.

Total harmonic distortion plus noise (THD + N) is the ratio of the rms value of the fundamental signal to the mean value of the root-sum-square of its harmonics plus all noise components (excluding dc). The bandwidth over which the noise is measured must be specified. In the case of an FFT, the bandwidth is dc to $f_s/2$. (If the bandwidth of the measurement is dc to $f_s/2$, THD + N is equal to SINAD—see below).

Signal-to-Noise-and-Distortion Ratio (SINAD), Signal-to-Noise Ratio (SNR), and Effective Number of Bits (ENOB)

SINAD and SNR deserve careful attention, because there is still some variation between ADC manufacturers as to their precise meaning. Signal-to-noise-and Distortion (SINAD, or S/(N + D) is the ratio of the rms signal amplitude to the mean value of the root-sum-square (rss) of all other spectral components, *including harmonics*, but excluding dc (see Figure 6.130). SINAD is a good indication of the overall dynamic performance of an ADC as a function of input frequency because it includes all components which make up noise (including thermal noise) and distortion. It is often plotted for various input amplitudes. SINAD is equal to THD + N if the bandwidth for the noise measurement is the same. A typical plot for the AD9226 12-bit, 65-MSPS ADC is shown in Figure 6.131.

- **SINAD (Signal-to-Noise-and-Distortion Ratio):**
  - **The ratio of therms signal amplitude to the meanvalue of the root-sum-squares (RSS) of all other spectral components, including harmonics, but excluding DC.**

- **ENOB (Effective Number ofBits):**

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\text{dB}}{6.02}$$

- **SNR (Signal-to-Noise Ratio, or Signal-to-Noise Ratio Without Harmonics:**
  - **The ratio of therms signal amplitude to the meanvalue of the root-sum-squares (RSS) of all other spectral components, excluding the first 5 harmonics and DC**

Figure 6.130: *SINAD, ENOB, and SNR*

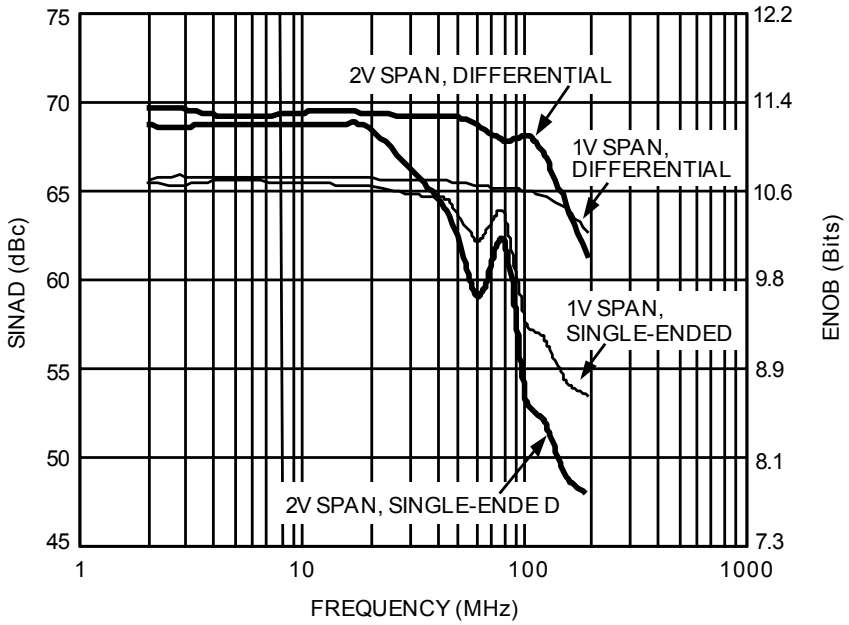


Figure 6.131: *AD9226 12-bit, 65-MSPS ADC SINAD and ENOB for Various Input Full-Scale Spans (Range)*

The SINAD plot shows where the ac performance of the ADC degrades due to high frequency distortion and is usually plotted for frequencies well above the Nyquist frequency so that performance in undersampling applications can be evaluated. SINAD is often converted to *effective-number-of-bits* (ENOB) using the relationship for the theoretical SNR of an ideal N-bit ADC: SNR = 6.02N + 1.76 dB. The equation is solved for N, and the value of SINAD is substituted for SNR:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\text{dB}}{6.02}. \qquad \text{Eq. 6.20}$$

Signal-to-noise ratio (SNR, or *SNR-without-harmonics*) is calculated the same as SINAD except that the signal harmonics are excluded from the calculation, leaving only the noise terms. In practice, it is only necessary to exclude the first five harmonics since they dominate. The SNR plot will degrade at high frequencies, but not as rapidly as SINAD because of the exclusion of the harmonic terms.

Many current ADC data sheets somewhat loosely refer to SINAD as SNR, so the engineer must be careful when interpreting these specifications.

Analog Bandwidth

The analog bandwidth of an ADC is that frequency at which the spectral output of the *fundamental* swept frequency (as determined by the FFT analysis) is reduced by 3 dB. It may be specified for either a small signal (SSBW—*small signal bandwidth*), or a full-

scale signal (FPBW—*full power bandwidth*), so there can be a wide variation in specifications between manufacturers.

The small signal bandwidth will be larger than the full power bandwidth. This issue is one of slew rate for the analog portion of the converter. This is similar to the bandwidth specifications of an op amp.

Like an amplifier, the analog bandwidth specification of a converter does not imply that the ADC maintains good distortion performance up to its bandwidth frequency. In fact, the SINAD (or ENOB) of most ADCs will begin to degrade considerably before the input frequency approaches the actual 3 dB bandwidth frequency. Figure 6.132 shows ENOB and full-scale frequency response of an ADC with a FPBW of 1 MHz, however, the ENOB begins to drop rapidly above 100 kHz.

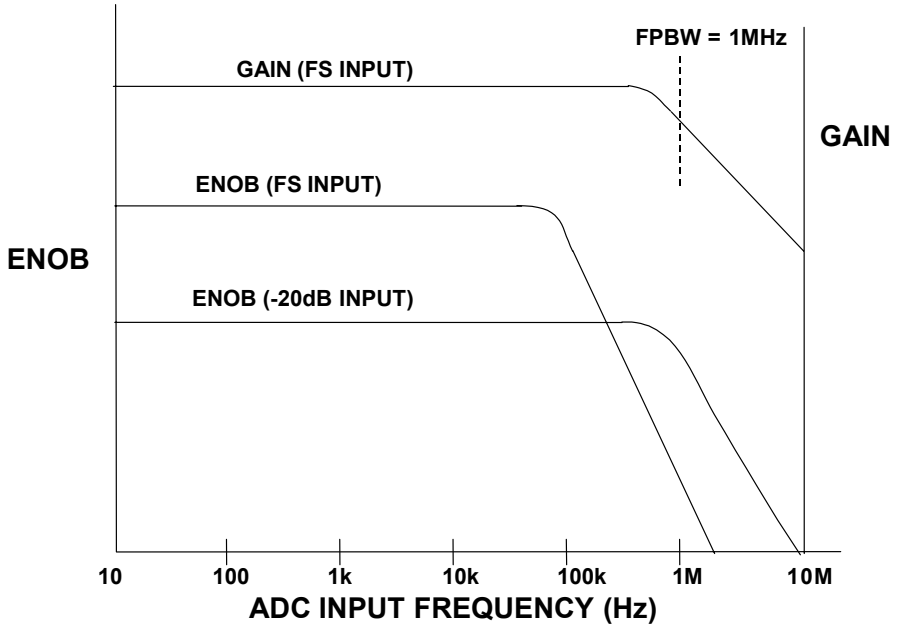


Figure 6.132: *ADC Gain (Bandwidth) and ENOB vs. Frequency Shows Importance of ENOB Specification*

In some systems, notably video applications the bandwidth is specified to the level at which the level is reduced by 0.1 dB.

Spurious-Free Dynamic Range (SFDR)

Probably the most significant specification for an ADC used in a communications application is its *spurious-free dynamic range* (SFDR). The SFDR specification is to ADCs what the third order intercept specification is to mixers and LNAs. SFDR of an ADC is defined as the ratio of the rms signal amplitude to the rms value of the *peak spurious spectral content* measured over the bandwidth of interest. Unless otherwise stated, the bandwidth is assumed to be the Nyquist bandwidth dc to $f_s/2$.

Occasionally the frequency spectrum is divided into an *in-band* region (containing the signals of interest) and an *out-of-band* region (signals here are filtered out digitally). In this case there may be an *in-band SFDR* specification and an *out-of-band SFDR* specification, respectively.

SFDR is generally plotted as a function of signal amplitude and may be expressed relative to the signal amplitude (dBc) or the ADC full-scale (dBFS) as shown in Figure 6.133.

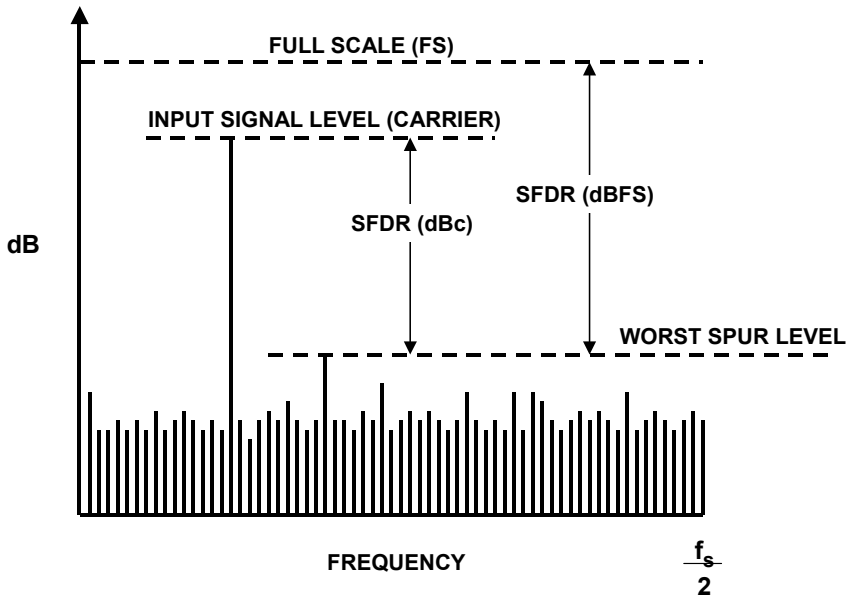


Figure 6.133: *Spurious-Free Dynamic Range (SFDR)*

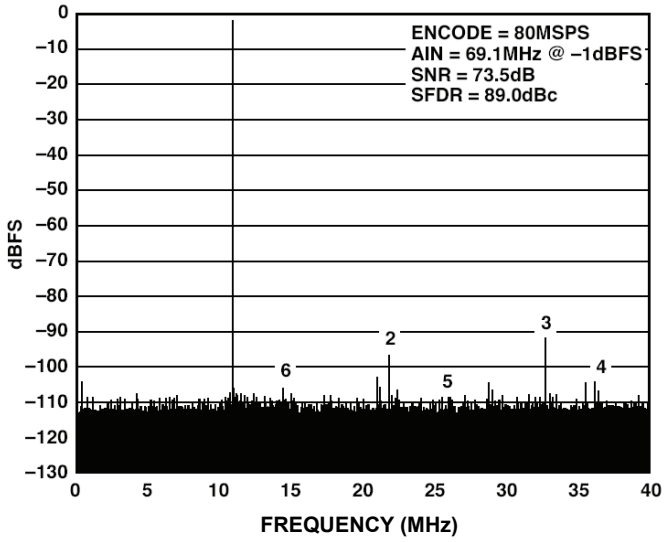


Figure 6.134: *AD6645 14-bit, 80-MSPS ADC SFDR for 69.1 MHz Input*

For a signal near full-scale, the peak spectral spur is generally determined by one of the first few harmonics of the fundamental. However, as the signal falls several dB below full-scale, other spurs generally occur which are not direct harmonics of the input signal. This is because of the differential nonlinearity of the ADC transfer function as discussed earlier. Therefore, SFDR considers *all* sources of distortion, regardless of their origin.

The AD6645 is a 14-bit, 80-MSPS wideband ADC designed for communications applications where high SFDR is important. The single-tone SFDR for a 69.1-MHz input and a sampling frequency of 80 MSPS is shown in Figure 6.134. Note that a minimum of 89 dBc SFDR is obtained over the entire first Nyquist zone (dc to 40 MHz).

SFDR as a function of signal amplitude is shown in Figure 6.135 for the AD6645. Notice that over the entire range of signal amplitudes, the SFDR is greater than 90 dBFS. The abrupt changes in the SFDR plot are due to the differential nonlinearities in the ADC transfer function. The nonlinearities correspond to those shown in Figure 6.128B, and are offset from mid-scale such that input signals less than about 65 dBFS do not exercise any of the points of increased DNL. It should be noted that the SFDR can be improved by injecting a small out-of-band dither signal—at the expense of a slight degradation in SNR.

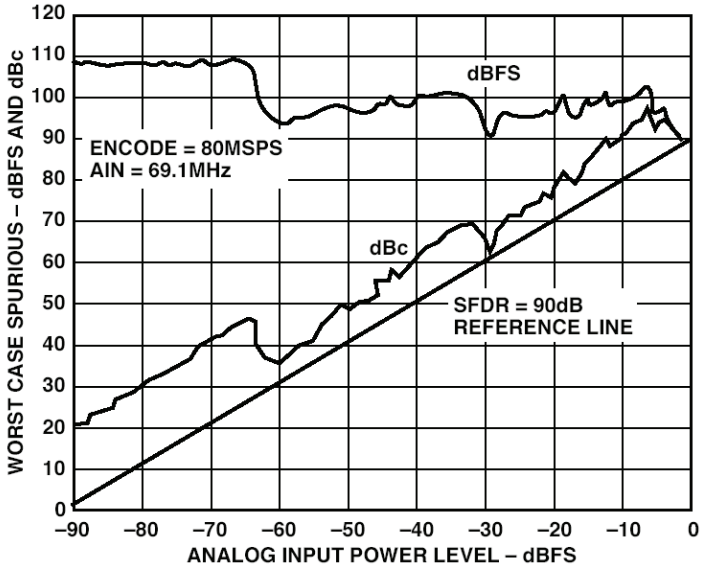


Figure 6.135: *AD6645 14-bit, 80 MSPS ADC SFDR vs. Input Power Level for 69.1 MHz Input*

SFDR is generally much greater than the ADCs theoretical N-bit SNR (6.02N + 1.76 dB). For example, the AD6645 is a 14-bit ADC with an SFDR of 90 dBc and a typical SNR of 73.5 dB (the theoretical SNR for 14-bits is 86 dB). This is because there is a fundamental distinction between noise and distortion measurements. The process gain of the FFT (33 dB for a 4096-point FFT) allows frequency spurs well below the noise floor to be observed. Adding extra resolution to an ADC may serve to increase its SNR but may or may not increase its SFDR.

Two Tone Intermodulation Distortion (IMD)

Two tone IMD is measured by applying two spectrally pure sine waves to the ADC at frequencies f_1 and f_2, usually relatively close together. The amplitude of each tone is set slightly more than 6 dB below full-scale so that the ADC does not clip when the two tones add in-phase. The locations of the second and third-order products are shown in Figure 6.136. Notice that the second-order products fall at frequencies which can be removed by digital filters. However, the third-order products $2f_2 - f_1$ and $2f_1 - f_2$ are close to the original signals and are more difficult to filter. Unless otherwise specified, two-tone IMD refers to these third-order products. The value of the IMD product is expressed in dBc relative to the value of *either* of the two original tones, and not to their sum.

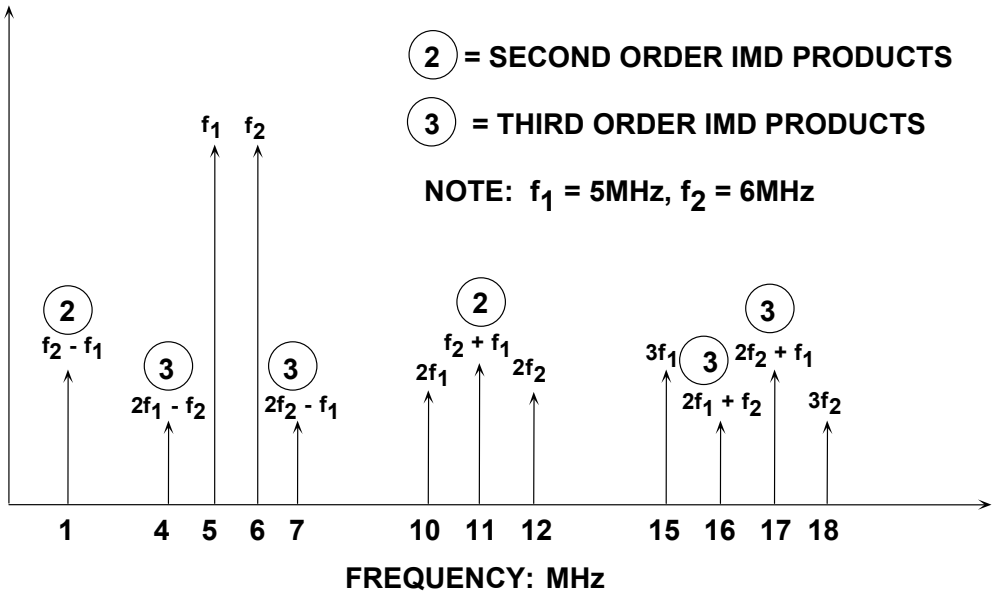


Figure 6.136: *Second and Third-Order Intermodulation Products for f_1 = 5 MHz, f_2 = 6 MHz*

Note, however, that if the two tones are close to $f_s/4$, then the aliased third harmonics of the fundamentals can make the identification of the actual $2f_2 - f_1$ and $2f_1 - f_2$ products difficult. This is because the third harmonic of $f_s/4$ is $3f_s/4$, and the alias occurs at $f_s - 3f_s/4 = f_s/4$. Similarly, if the two tones are close to $f_s/3$, the aliased second harmonics may interfere with the measurement. The same reasoning applies here; the second harmonic of $f_s/3$ is $2f_s/3$, and its alias occurs at $f_s - 2f_s/3 = f_s/3$.

Multitone Spurious-Free Dynamic Range

Two-tone and multitone SFDR is often measured in communications applications. The larger number of tones more closely simulates the wideband frequency spectrum of cellular telephone systems such as AMPS or GSM. Figure 6.137 shows the 2-tone intermodulation performance of the AD6645 14-bit, 80 MSPS ADC. The input tones are at 55.25 MHz and 56.25 MHz and are located in the second Nyquist Zone.

The aliased tones therefore occur at 23.75 MHz and 24.75 MHz in the first Nyquist Zone. High SFDR increases the receiver's ability to capture small signals in the presence of large ones, and prevents the small signals from being masked by the intermodulation products of the larger ones. Figure 6.138 shows the AD6645 two-tone SFDR as a function of input signal amplitude for the same input frequencies.

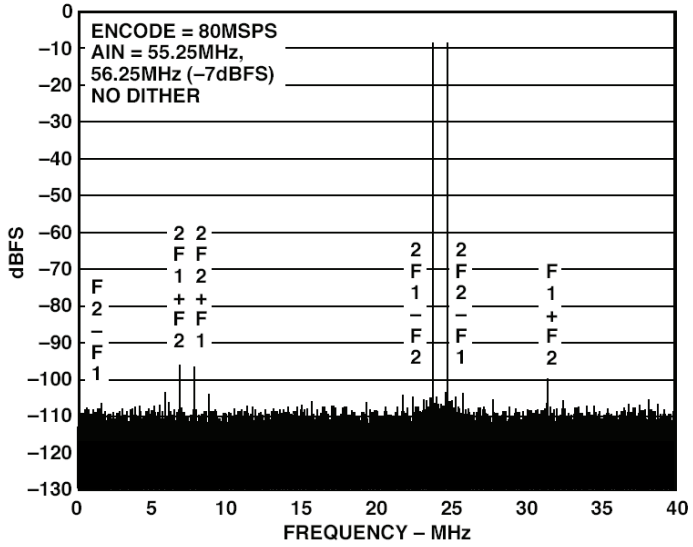


Figure 6.137: *Two-Tone SFDR for AD6645 14-bit, 80-MSPS ADC, Input Tones: 55.25 MHz and 56.25 MHz*

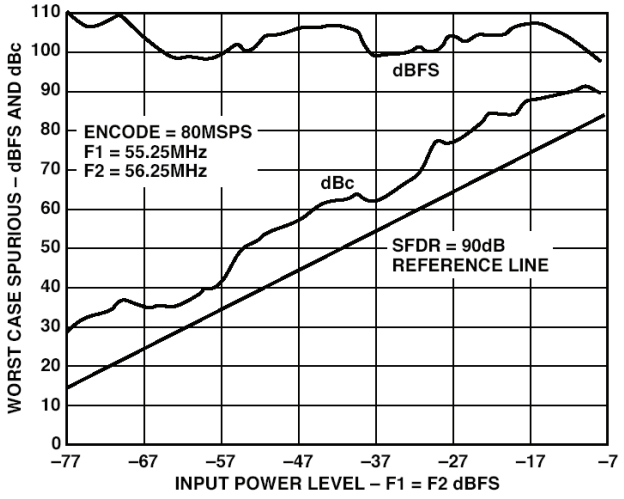


Figure 6.138: *Two-Tone SFDR vs. Input Amplitude for AD6645 14-bit, 80-MSPS ADC*

Second- and Third-Order Intercept Points, 1 dB Compression Point

Third-order IMD products are especially troublesome in multichannel communications systems where the channel separation is constant across the frequency band. Third-order IMD products can mask out small signals in the presence of larger ones.

In amplifiers, it is common practice to specify the third-order IMD products in terms of the *third-order intercept* point, as is shown by Figure 6.139. Two spectrally pure tones are applied to the system. The output signal power in a single tone (in dBm) as well as the relative amplitude of the third-order products (referenced to a single tone) is plotted as a function of input signal power. The fundamental is shown by the *slope = 1* curve in the diagram. If the system nonlinearity is approximated by a power series expansion, it can be shown that second-order IMD amplitudes increase 2 dB for every 1-dB of signal increase, as represented by *slope = 2* curve in the diagram.

Similarly, the third-order IMD amplitudes increase 3 dB for every 1-dB of signal increase, as indicated by the *slope = 3* plotted line. With a low level two-tone input signal, and two data points, one can draw the second and third order IMD lines as they are shown in Figure 6.139 (using the principle that a point and a slope define a straight line).

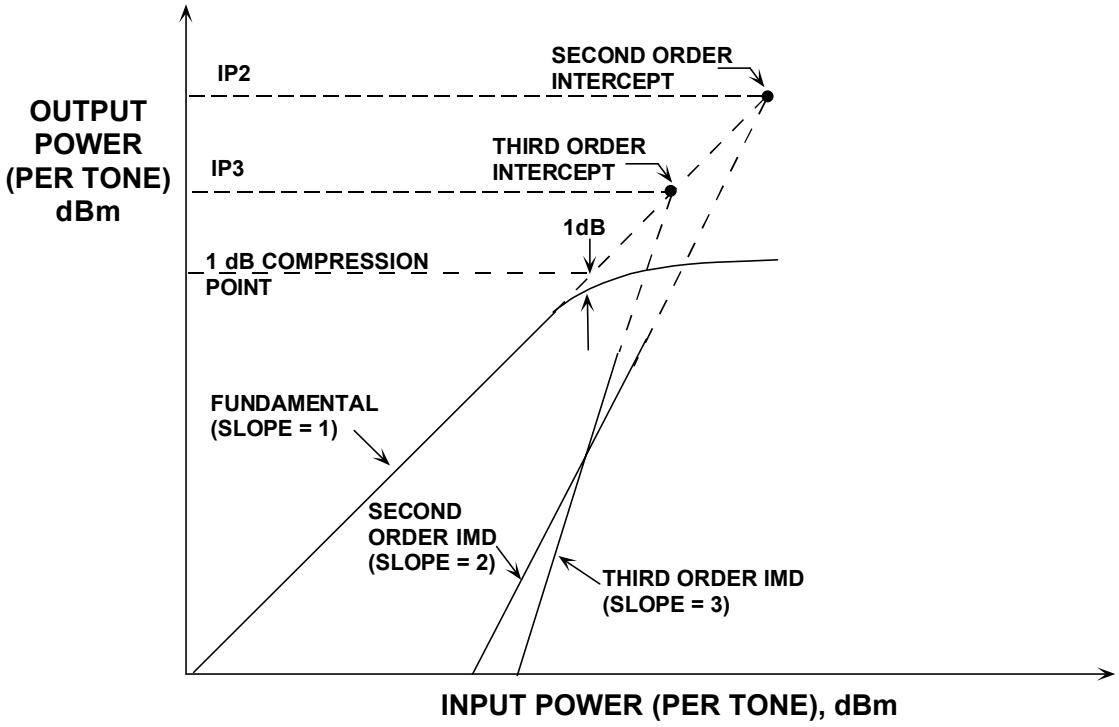


Figure 6.139: *Definition of Intercept Points and 1 dB Compression Points for Amplifiers*

Once the input reaches a certain level however, the output signal begins to soft-limit, or compress. A parameter of interest here is the *1 dB compression point*. This is the point where the output signal is compressed 1 dB from an ideal input/output transfer function.

This is shown in Figure 6.139 within the region where the ideal slope = 1 line becomes dotted, and the actual response exhibits compression (solid).

Nevertheless, both the second- and third-order intercept lines may be extended, to intersect the (dotted) extension of the ideal output signal line. These intersections are called the *second* and *third-order intercept points*, respectively, or IP2 and IP3. These power level values are usually referenced to the output power of the device delivered to a matched load (usually, but not necessarily 50 Ω) expressed in dBm.

It should be noted that IP2, IP3, and the 1 dB compression point are all a function of frequency, and as one would expect, the distortion is worse at higher frequencies.
For a given frequency, knowing the third order intercept point allows calculation of the approximate level of the third-order IMD products as a function of output signal level.

The concept of *second and third-order intercept points* is not valid for an ADC, because the distortion products do not vary in a predictable manner (as a function of signal amplitude). The ADC does not gradually begin to compress signals approaching full-scale (there is no 1 dB compression point); it acts as a *hard limiter* as soon as the signal exceeds the ADC input range, thereby suddenly producing extreme amounts of distortion because of clipping. On the other hand, for signals much below full-scale, the distortion floor remains relatively constant and is independent of signal level. This is shown graphically in Figure 6.140.

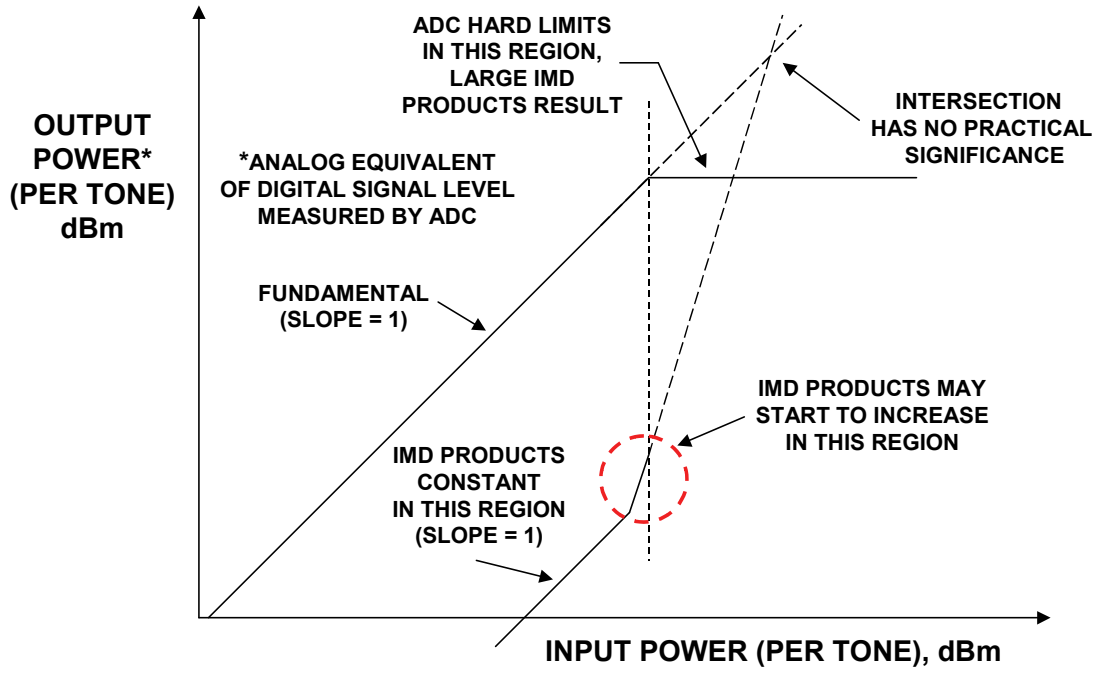


Figure 6.140: *Intercept Points for Data Converters Have No Practical Significance*

The IMD curve in Figure 6.140 is divided into three regions. For low level input signals, the IMD products remain relatively constant regardless of signal level. This implies that as the input signal increases 1 dB, the ratio of the signal to the IMD level will increase

1 dB also. When the input signal is within a few dB of the ADC full-scale range, the IMD may start to increase (but it might not in a very well-designed ADC). The exact level at which this occurs is dependent on the particular ADC under consideration—some ADCs may not exhibit significant increases in the IMD products over their full input range, however most will. As the input signal continues to increase beyond full-scale, the ADC should as an ideal limiter, and the IMD products become very large.

For these reasons, the 2nd and 3rd order IMD intercept points are not specified for ADCs. It should be noted that essentially the same arguments apply to DACs. In either case, the single- or multi-tone SFDR specification is the most accepted way to measure data converter distortion.

Wideband CDMA (W-CDMA) Adjacent Channel Power Ratio (ACPR) and Adjacent Channel Leakage Ratio (ADLR)

A wideband CDMA channel has a bandwidth of approximately 3.84 MHz, and channel spacing is 5 MHz. The ratio in dBc between the measured power within a channel relative to its adjacent channel is defined as the *adjacent channel power ratio* (ACPR).

The ratio in dBc between the measured power within the channel bandwidth relative to the noise level in an adjacent empty carrier channel is defined as *adjacent channel leakage ratio* (ACLR).

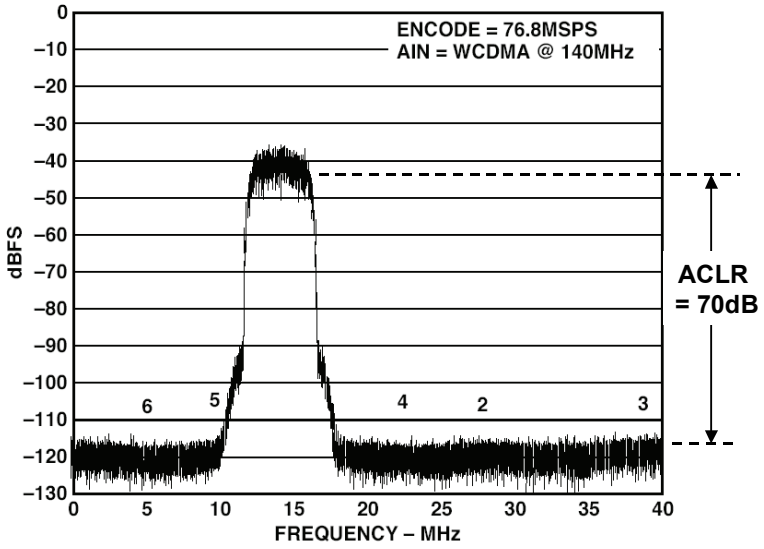


Figure 6.141: *Wideband CDMA (W-CDMA) Adjacent Channel Leakage Ratio (ACLR)*

Figure 6.141 shows a single wideband CDMA channel centered at 140 MHz sampled at a frequency of 76.8 MSPS using the AD6645. This is a good example of undersampling (direct IF-to-digital conversion).The signal lies within the third Nyquist zone: $3f_s/2$ to $2f_s$

(115.2 MHz to 153.6 MHz). The aliased signal within the first Nyquist zone is therefore centered at $2f_s - f_a = 153.6 - 140 = 13.6$ MHz. The diagram also shows the location of the aliased harmonics. For example, the second harmonic of the input signal occurs at $2 \times 140 = 280$ MHz, and the aliased component occurs at $4f_s - 2f_a = 4 \times 76.8 - 280 = 307.2 - 280 = 27.2$ MHz.

Noise Power Ratio (NPR)

Noise power ratio has been used extensively to measure the transmission characteristics of Frequency Division Multiple Access (FDMA) communications links (see Reference 7). In a typical FDMA system, 4-kHz wide voice channels are "stacked" in frequency bins for transmission over coaxial, microwave, or satellite equipment. At the receiving end, the FDMA data is demultiplexed and returned to 4-kHz individual baseband channels. In an FDMA system having more than approximately 100 channels, the FDMA signal can be approximated by Gaussian noise with the appropriate bandwidth. An individual 4-kHz channel can be measured for "quietness" using a narrow-band notch (band-stop) filter and a specially tuned receiver which measures the noise power inside the 4-kHz notch (see Figure 6.142).

Noise Power Ratio (NPR) measurements are straightforward. With the notch filter out, the rms noise power of the signal inside the notch is measured by the narrowband receiver. The notch filter is then switched in, and the residual noise inside the slot is measured. The ratio of these two readings expressed in dB is the NPR. Several slot frequencies across the noise bandwidth (low, midband, and high) are tested to characterize the system adequately. NPR measurements on ADCs are made in a similar manner except the analog receiver is replaced by a buffer memory and an FFT processor.

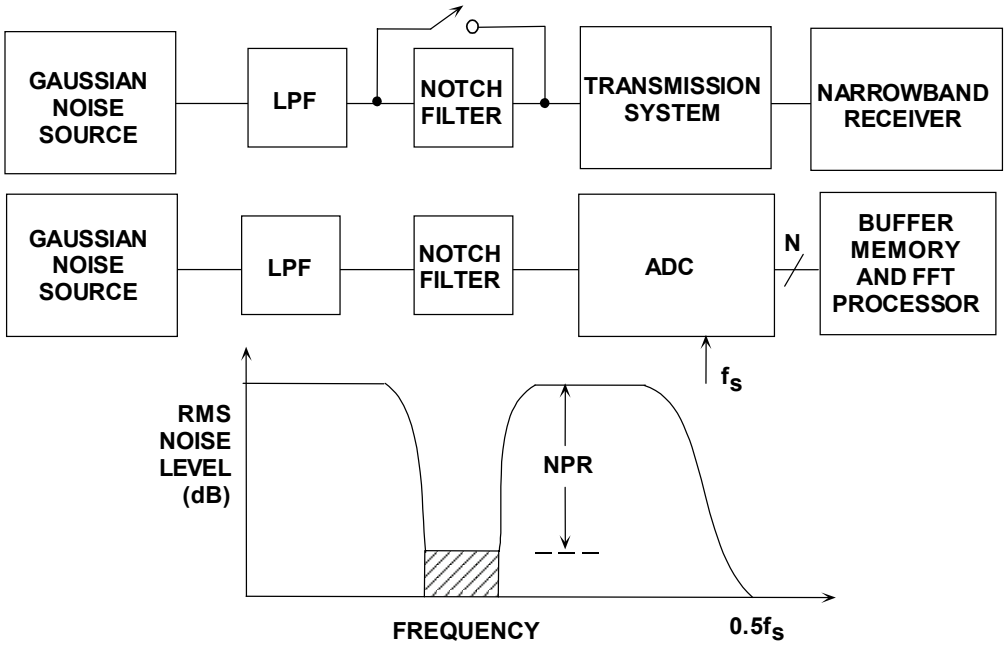


Figure 6.142: *Noise Power Ratio (NPR) Measurements*

The NPR is plotted as a function of rms noise level referred to the peak range of the system. For very low noise loading level, the undesired noise (in nondigital systems) is primarily thermal noise and is independent of the input noise level. Over this region of the curve, a 1 dB increase in noise loading level causes a 1 dB increase in NPR. As the noise loading level is increased, the amplifiers in the system begin to overload, creating intermodulation products which cause the noise floor of the system to increase. As the input noise increases further, the effects of "overload" noise predominate, and the NPR is reduced dramatically. FDMA systems are usually operated at a noise loading level a few dB below the point of maximum NPR.

In a digital system containing an ADC, the noise within the slot is primarily quantization noise when low levels of noise input are applied. The NPR curve is linear in this region. As the noise level increases, there is a one-for-one correspondence between the noise level and the NPR. At some level, however, “clipping” noise caused by the hard-limiting action of the ADC begins to dominate. A theoretical curve for 10, 11, and 12-bit ADCs is shown in Figure 6.143 (see Reference 8).

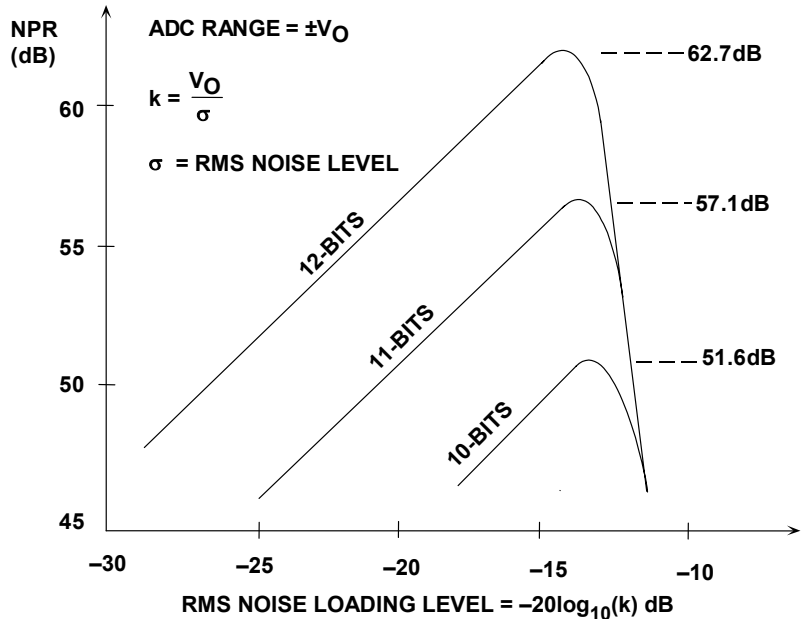


Figure 6.143: *Theoretical NPR for 10, 11, 12-bit ADCs*

Figure 6.144 shows the maximum theoretical NPR and the noise loading level at which the maximum value occurs for 8 bit to 16 bit ADCs. The ADC input range is 2 V_O peak-to-peak. The rms noise level is σ, and the noise-loading factor k (crest factor) is defined as V_O/σ , the peak-to-rms ratio (k is expressed either as numerical ratio or in dB).

In multi-channel high frequency communication systems where there is little or no phase correlation between channels, NPR can also be used to simulate the distortion caused by a large number of individual channels, similar to an FDMA system. A notch filter is placed between the noise source and the ADC, and an FFT output is used in place of the analog receiver. The width of the notch filter is set for several MHz as shown in Figure

2.65 for the AD9430 12-bit 170-MSPS ADC. The notch is centered at 19 MHz, and the NPR is the "depth" of the notch. An ideal ADC will only generate quantization noise inside the notch; however a practical one has additional noise components due to additional noise and intermodulation distortion caused by ADC imperfections. Notice that the NPR is about 57 dB compared to 62.7 dB theoretical.

BITS	k OPTIMUM	k(dB)	MAX NPR (dB)
8	3.92	11.87	40.60
9	4.22	12.50	46.05
10	4.50	13.06	51.56
11	4.76	13.55	57.12
12	5.01	14.00	62.71
13	5.26	14.41	68.35
14	5.49	14.79	74.01
15	5.72	15.15	79.70
16	5.94	15.47	85.40

ADC Range = $\pm V_O$
$k = V_O / \sigma$
σ = RMS Noise Level

Figure 6.144: *Theoretical Maximum NPR for 8 bit to 16 bit ADCs*

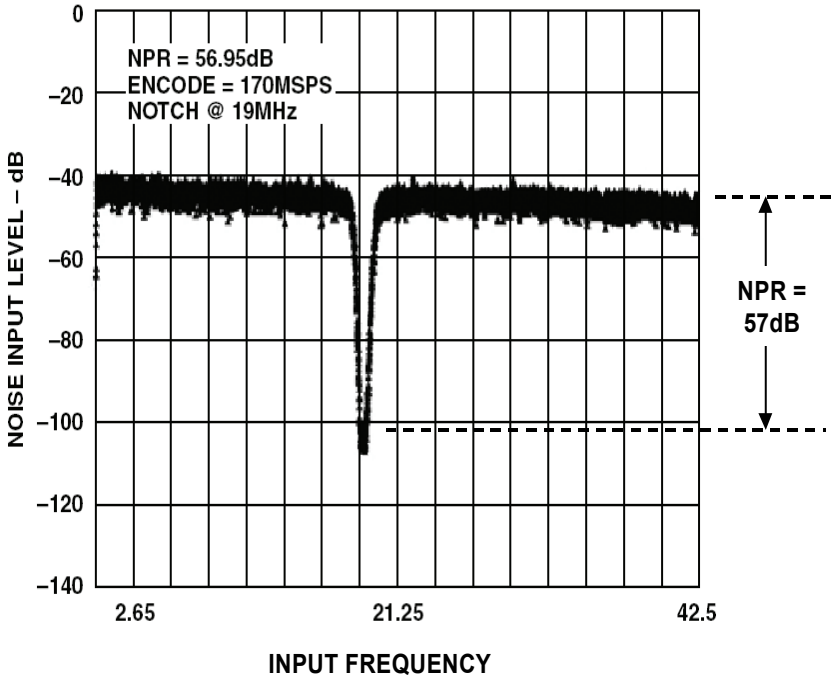


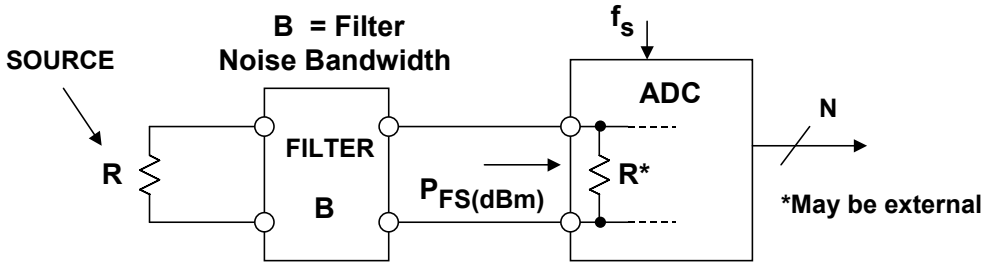
Figure 6.145: *AD9430 12-bit, 170 MSPS ADC NPR Measures 57 dB (62.7 dB Theoretical)*

Noise Factor (F) and Noise Figure (NF)

Noise figure (NF) is a popular specification among RF system designers. It is used to characterize RF amplifiers, mixers, etc., and widely used as a tool in radio receiver design. Many excellent textbooks on communications and receiver design treat noise figure extensively (see Reference 9, for example)—it is not the purpose of this discussion to discuss the topic in much detail, but only how it applies to data converters.

Since many wideband operational amplifiers and ADCs are now being used in RF applications, the inevitable day has come where the noise figure of these devices becomes important. As discussed in Reference 10, in order to determine the noise figure of an op amp correctly, one must not only know op amp voltage and current noise, but the exact circuit conditions—closed-loop gain, gain-setting resistor values, source resistance, bandwidth, etc. Calculating the noise figure for an ADC is even more of a challenge as will be seen.

Figure 6.146 shows the basic model for defining the noise figure of an ADC. The *noise factor*, F, is simply defined as the ratio of the total effective input noise power of the ADC to the amount of that noise power caused by the source resistance alone. Because the impedance is matched, the square of the voltage noise can be used instead of noise power. The *noise figure*, NF, is simply the noise factor expressed in dB, $NF = 10\log_{10}F$.



$$\text{NOISE FACTOR (F)} = \frac{\text{(TOTAL EFFECTIVE INPUT NOISE)}^2}{\text{(TOTAL INPUT NOISE DUE TO SOURCE R)}^2}$$

$$\text{NOISE FIGURE (NF)} = 10\log_{10}\left[\frac{\text{(TOTAL EFFECTIVE INPUT NOISE)}^2}{\text{(TOTAL INPUT NOISE DUE TO SOURCE R)}^2}\right]$$

Note: Noise Must be Measured Over the Filter Noise Bandwidth, B

Figure 6.146: *Noise Figure for ADCs: Use with Caution!*

This model assumes the input to the ADC comes from a source having a resistance, R, and that the input is band-limited to $f_S/2$ with a filter having a noise bandwidth equal to $f_S/2$. It is also possible to further band-limit the input signal resulting in oversampling and process gain, and this condition will be discussed shortly.

It is also assumed that the input impedance to the ADC is equal to the source resistance. Many ADCs have a high input impedance, so this termination resistance may be external to the ADC or used in parallel with the internal resistance to produce an equivalent termination resistance equal to R. The full-scale input power is the power of a sine wave whose peak-to-peak amplitude fills the entire ADC input range. The full-scale input sine wave given by the following equation has a peak-to-peak amplitude of 2 V_O corresponding to the peak-to-peak input range of the ADC:

$$v(t) = V_O \sin 2\pi ft \qquad \text{Eq. 6.21}$$

The full-scale power in this sine wave is given by:

$$P_{FS} = \frac{(V_O / \sqrt{2})^2}{R} = \frac{V_O{}^2}{2R} \qquad \text{Eq. 6.22}$$

It is customary to express this power in dBm (referenced to 1 mW) as follows:

$$P_{FS(dBm)} = 10 \log_{10}\left[\frac{P_{FS}}{1mW}\right]. \qquad \text{Eq. 6.23}$$

The *noise bandwidth* of a nonideal brick wall filter is defined as the bandwidth of an ideal brick wall filter which will pass the same noise power as the nonideal filter. Therefore, the noise bandwidth of a filter is always greater than the 3 dB bandwidth of the filter by a factor which depends upon the sharpness of the cutoff region of the filter. Figure 2.68 shows the relationship between the noise bandwidth and the 3 dB bandwidth for Butterworth filters up to 5 poles. Note that for two poles, the noise bandwidth and 3 dB bandwidth are within 11% of each other, and beyond that the two quantities are essentially equal.

NUMBER OF POLES	NOISE BW / 3dB BW
1	1.57
2	1.11
3	1.05
4	1.03
5	1.02

Figure 6.147: *Relationship Between Noise Bandwidth and 3 dB Bandwidth for Butterworth Filter*

The first step in the NF calculation is to calculate the effective input noise of the ADC from its SNR. The SNR of the ADC is given for a variety of input frequencies, so be sure to use the value corresponding to the input frequency of interest. Also, make sure that the harmonics are not included in the SNR number—some ADC data sheets may confuse SINAD with SNR. Once the SNR is known, the equivalent input rms voltage noise can be calculated starting from the equation:

$$\mathrm{SNR} = 20\log_{10}\left[\frac{V_{\mathrm{FS\ RMS}}}{V_{\mathrm{NOISE\ RMS}}}\right] \qquad \text{Eq. 6.24}$$

Solving for $V_{NOISE\ RMS}$:

$$V_{\mathrm{NOISE\ RMS}} = V_{\mathrm{FS\ RMS}} \cdot 10^{-\mathrm{SNR}/20} \qquad \text{Eq. 6.25}$$

This is the total effective input rms noise voltage at the carrier frequency measured over the Nyquist bandwidth, dc to $f_s/2$. Note that this noise includes the source resistance noise. These results are summarized in Figure 6.148.

- **Start with the SNR of the ADC measured at the carrier frequency (Note: this SNR value does not include the harmonics of the fundamental and is measured over the Nyquist bandwidth, dc to $f_S/2$)**

$$\mathbf{SNR = 20\ log_{10}\ \frac{V_{FS\text{-}RMS}}{V_{NOISE\text{-}RMS}}}$$

$$\mathbf{V_{NOISE\text{-}RMS} = V_{FS\text{-}RMS}\ 10^{-SNR\ /\ 20}}$$

- **This is the total ADC effective input noise at the carrier frequency measured over the Nyquist bandwidth, dc to $f_S/2$**

Figure 6.148: *Calculating ADC Total Effective Input Noise from SNR*

The next step is to actually calculate the noise figure. In Figure 2.70 notice that the amount of the input voltage noise due to the source resistance is the voltage noise of the source resistance √(4kTBR) divided by two, or √(kTBR) because of the 2:1 attenuator formed by the ADC input termination resistor.

The expression for the noise factor F can be written:

$$F = \frac{V_{\mathrm{NOISE\ RMS}}^{2}}{\mathrm{kTRB}} = \left[\frac{V_{\mathrm{FS\ RMS}}^{2}}{R}\right]\left[\frac{1}{kT}\right]\left[10^{-\mathrm{SNR}/10}\right]\left[\frac{1}{B}\right] \qquad \text{Eq. 6.24}$$

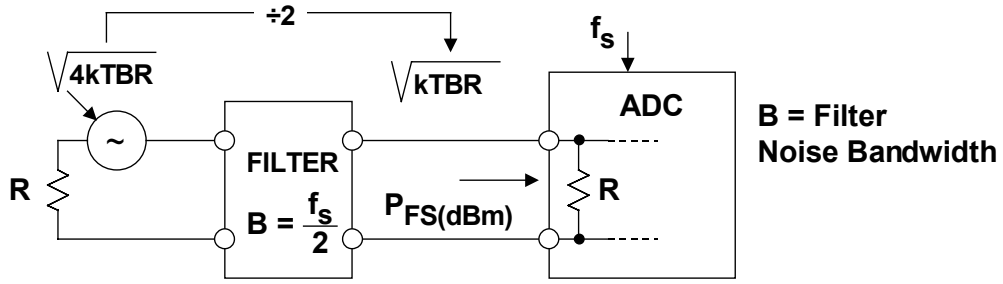
The noise figure is obtained by converting F into dB and simplifying:

$$NF = 10_{10}\log F = P_{FS(dBm)} + 174\ dBm - SNR - 10_{10}\log B, \qquad \text{Eq. 6.25}$$

Where SNR is in dB, B in Hz, T = 300 K, k = 1.38×10^{-23} J/K.

Oversampling and filtering can be used to decrease the noise figure as a result of the process gain as has been previously discussed. In this case, the signal bandwidth B is less than $f_s/2$. Figure 6.149 shows the correction factor which results in the following equation:

$$NF = 10_{10}\log F = P_{FS(dBm)} + 174\ dBm - SNR - 10\log_{10}[f_s/2B] - 10\log_{10}B. \qquad \text{Eq. 6.26}$$



$$V_{NOISE\text{-}RMS} = V_{FS\text{-}RMS}\ 10^{-SNR/20}$$

$$F = \frac{V_{NOISE\text{-}RMS}^{2}}{kTRB} = \left[\frac{V_{FS\text{-}RMS}^{2}}{R}\right]\left[\frac{1}{kT}\right]\left[10^{-SNR/10}\right]\left[\frac{1}{B}\right]$$

$$NF = 10\log_{10}F = P_{FS(dBm)} + 174dBm - SNR - 10\log_{10}B,$$

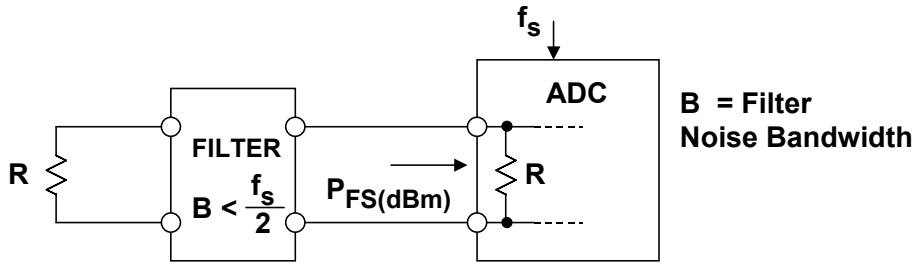
where SNR is in dB, B in Hz, T = 300K, $k = 1.38 \times 10^{-23}$ J/K

Figure 6.149: *ADC Noise Figure in Terms of SNR, Sampling Rate and Input Power*

Figure 6.151 shows an example NF calculation for the AD6645 14-bit, 80-MSPS ADC. A 52.3 Ω resistor is added in parallel with the AD6645 input impedance of 1 kΩ to make the net input impedance 50 Ω. The ADC is operating under Nyquist conditions, and the SNR of 74 dB is the starting point for the calculations using Eq. 6.26. A noise figure of 34.8 dB is obtained.

Figure 6.152 shows how using an RF transformer with voltage gain can improve the noise figure. Figure 6.152A shows a 1:1 turns ratio, and the noise figure (from Figure 6.151) is 34.8. Figure 6.152B shows a transformer with a 1:2 turns ratio. The 249 Ω resistor in parallel with the AD6645 internal resistance results in a net input

impedance of 200 Ω. The noise figure is improved by 6 dB because of the noise-free voltage gain of the transformer. Figure 6.152C shows a transformer with a 1:4 turns ratio. The AD6645 input is paralleled with a 4.02 kΩ resistor to make the net input impedance 800 Ω. The noise figure is improved by another 6 dB. Transformers with higher turns ratios are not generally practical because of bandwidth and distortion limitations.

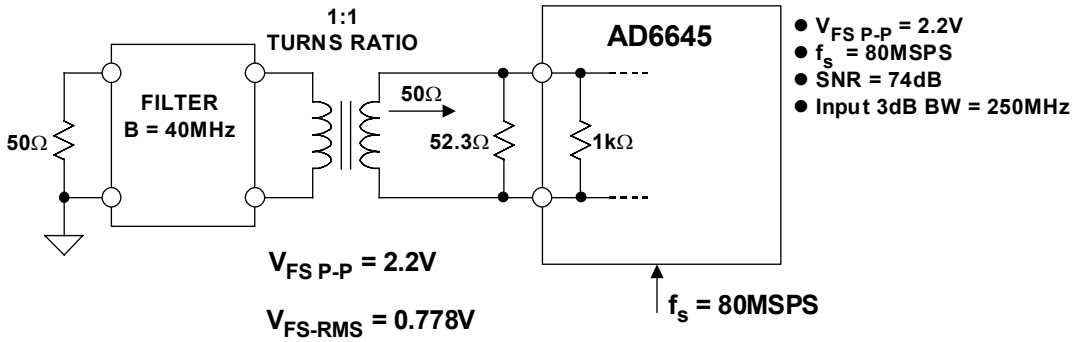


$$NF = P_{FS(dBm)} + 174dBm - SNR - 10\log_{10}\left[\frac{f_S/2}{B}\right] - 10\log_{10}B,$$

Measured DC to $f_S/2$ | Process Gain

where SNR is in dB, B in Hz, $T = 300K$, $k = 1.38 \times 10^{-23}$ J/K

Figure 6.150: *Effect of Oversampling and Process Gain on ADC Noise Figure*



$V_{FS\ P-P} = 2.2V$

$V_{FS-RMS} = 0.778V$

$$P_{FS} = \frac{(0.778)^2}{50} = 12.1mW$$

$P_{FS(dBm)} = +10.8dBm$

$$NF = P_{FS(dBm)} + 174dBm - SNR - 10\log_{10}B$$

$$= +10.8dBm + 174dBm - 74dB - 10\log_{10}(40 \times 10^6)$$

$$= 34.8dB$$

Figure 6.151: *Example Calculation of Noise Figure Under Nyquist Conditions for AD6645*

Even with the 1:4 turns ratio transformer, the overall noise figure for the AD6645 was still 22.8 dB, still relatively high by RF standards. The solution is to provide low noise high gain stages ahead of the ADC. Figure 6.153 shows how the Friis equation is used to calculate the noise factor for cascaded gain stages. Notice that high gain in the first stage reduces the contribution of the noise factor of the second stage—the noise factor of the first stage dominates the overall noise factor.

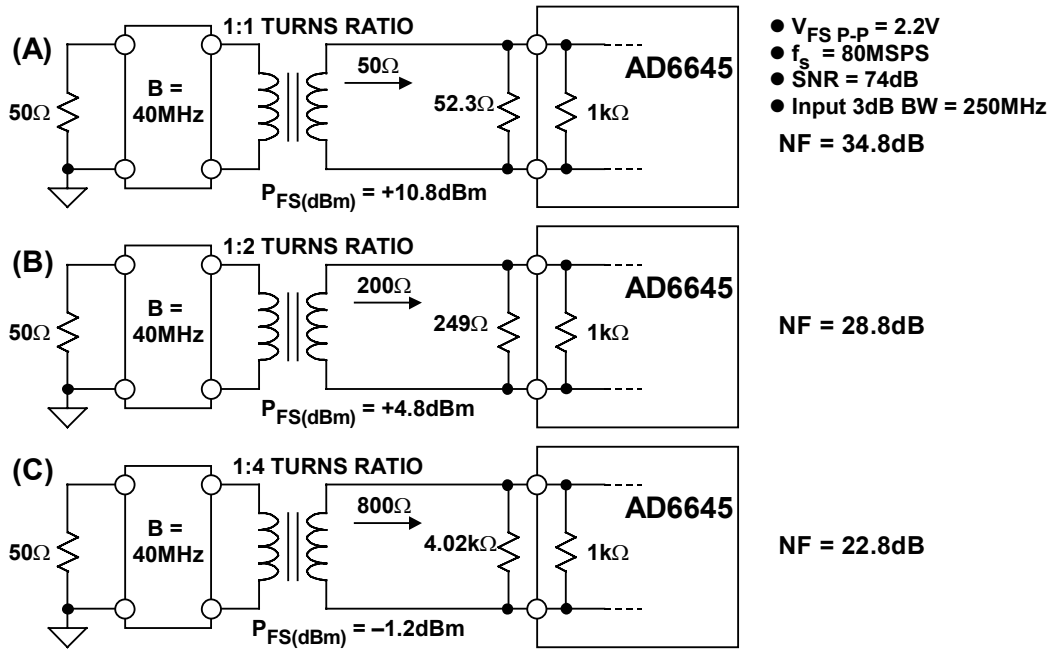


Figure 6.152: *Using RF Transformers to Improve Overall ADC Noise Figure*

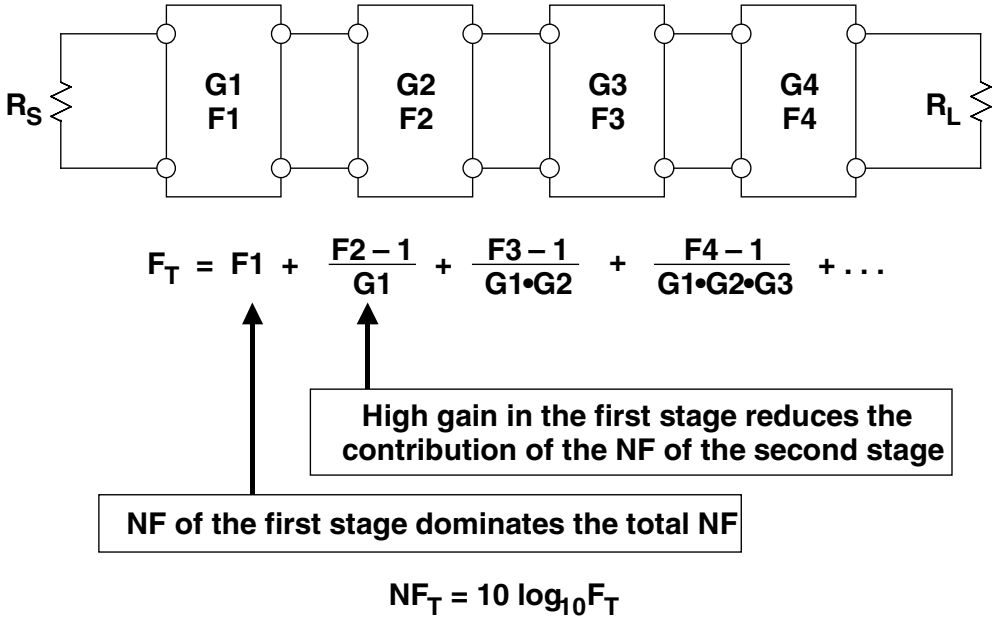
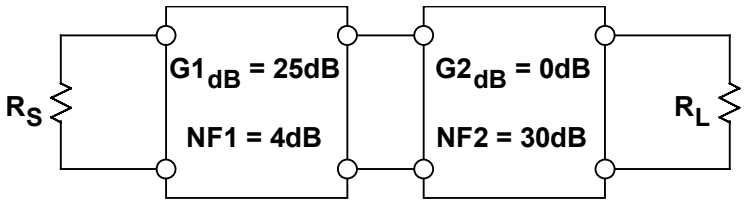


Figure 6.153: *Cascaded Noise Figure Using the Friis Equation*

Figure 6.154 shows the effects of a high gain (25 dB), low noise (NF = 4 dB) stage placed in front of a relatively high NF stage (30 dB)—the noise figure of the second stage is typical of high performance ADCs. The overall noise figure is 7.53 dB, only 3.53 dB higher than the first stage noise figure of 4 dB.



$$G1 = 10^{25/10} = 10^{2.5} = 316, \quad F1 = 10^{4/10} = 10^{0.4} = 2.51$$

$$G2 = 1, \quad F2 = 10^{30/10} = 10^{3} = 1000$$

$$F_T = F1 + \frac{F2 - 1}{G1} = 2.51 + \frac{1000 - 1}{316} = 2.51 + 3.16 = 5.67$$

$$NF_T = 10 \log_{10} 5.67 = 7.53dB$$

- The first stage dominates the overall NF
- It should have the highest gain possible with the lowest NF possible

Figure 6.154: *Example of Two-Stage Cascaded Network*

In summary, applying the noise figure concept to characterize wideband ADCs must be done with extreme caution to prevent misleading results. Simply trying to minimize the noise figure using the equations can actually increase circuit noise.

For instance, NF decreases with increasing source resistance according to the calculations, but increased source resistance increases circuit noise. Also, NF decreases with increasing ADC input bandwidth if there is no input filtering. This is also contradictory, because widening the bandwidth increases noise. In both these cases, the circuit noise increases, and the NF decreases. The reason NF decreases is that the source noise makes up a larger component of the total noise (which remains relatively constant because the ADC noise is much greater than the source noise); therefore according to the calculation, NF decreases, but actual circuit noise increases.

It is true that on a stand-alone basis ADCs have relatively high noise figures compared to other RF parts such as LNAs or mixers. In the system the ADC should be preceded with low-noise gain blocks as shown in the example of Figure 6.154.

Aperture Time, Aperture Delay Time and Aperture Jitter

Perhaps the most misunderstood and misused ADC and sample-and-hold (or track-and-hold) specifications are those that include the word *aperture*. The most essential dynamic property of a SHA is its ability to disconnect quickly the hold capacitor from the input buffer amplifier as shown in Figure 6.155. The short (but non-zero) interval required for this action is called *aperture time (or sampling aperture)*, t_a. The actual value of the voltage that is held at the end of this interval is a function of both the input signal slew rate and the errors introduced by the switching operation itself. Figure 6.155 shows what happens when the hold command is applied with an input signal of two arbitrary slopes labeled as 1 and 2. For clarity, the sample-to-hold pedestal and switching transients are ignored. The value that is finally held is a delayed version of the input signal, averaged over the aperture time of the switch as shown in Figure 6.155. The first-order model assumes that the final value of the voltage on the hold capacitor is approximately equal to the average value of the signal applied to the switch over the interval during which the switch changes from a low to high impedance (t_a).

The model shows that the finite time required for the switch to open (t_a) is equivalent to introducing a small delay t_e in the sampling clock driving the SHA. This delay is constant and may either be positive or negative. The diagram shows that the same value of t_e works for the two signals, even though the slopes are different. This delay is called *effective aperture delay time*, *aperture delay time*, or simply *aperture delay*, t_e. In an ADC, the aperture delay time is referenced to the input of the converter, and the effects of the analog propagation delay through the input buffer, t_{da} and the digital delay through the switch driver, t_{dd}, must be considered. Referenced to the ADC inputs, aperture time, t_e', is defined as the time difference between the analog propagation delay of the front-end buffer, t_{da}, and the switch driver digital delay, t_{dd}, plus one-half the aperture time, $t_a/2$.

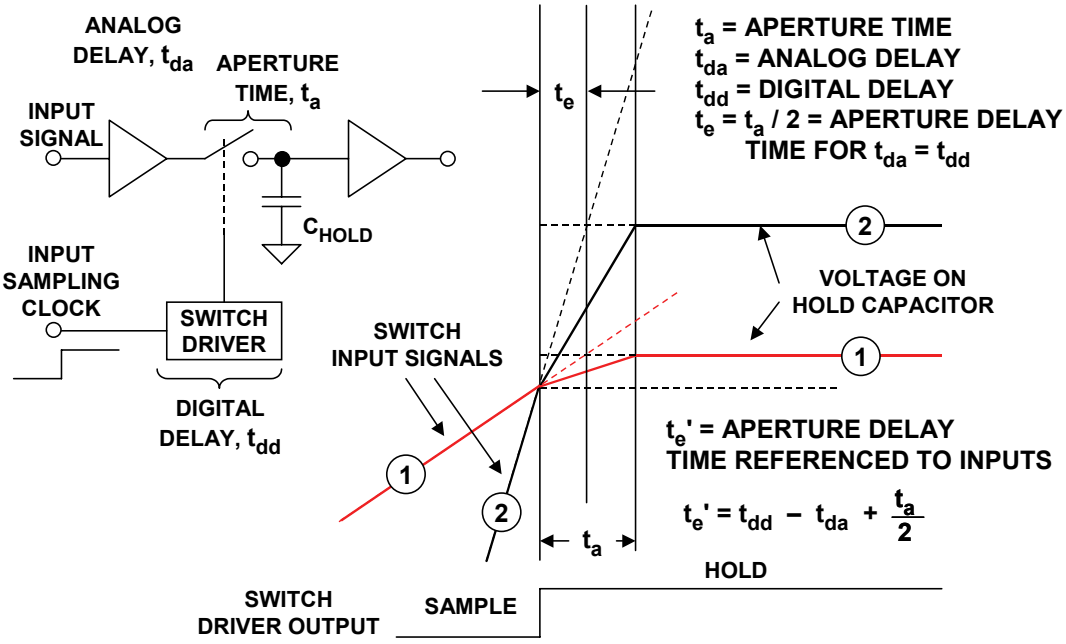


Figure 6.155: *Sample-and-Hold Waveforms and Definitions*

The effective aperture delay time is usually positive, but may be negative if the sum of one-half the aperture time, $t_a/2$, and the switch driver digital delay, t_{dd}, is less than the propagation delay through the input buffer, t_{da}. The aperture delay specification thus establishes when the input signal is actually sampled with respect to the sampling clock edge.

Aperture delay time can be measured by applying a bipolar sine wave signal to the ADC and adjusting the synchronous sampling clock delay such that the output of the ADC is mid-scale (corresponding to the zero-crossing of the sine wave). The relative delay between the input sampling clock edge and the actual zero-crossing of the input sine wave is the aperture delay time (see Figure 6.156).

Aperture delay produces no errors (assuming it is relatively short with respect to the hold time), but acts as a fixed delay in either the sampling clock input or the analog input (depending on its sign). However, in simultaneous sampling applications or in direct I/Q demodulation where two or more ADCs must be well matched, variations in the aperture delay between converters can produce errors on fast slewing signals. In these applications, the aperture delay mismatches must be removed by properly adjusting the phases of the individual sampling clocks to the various ADCs.

If, however, there is *sample-to-sample* variation in aperture delay (*aperture jitter*), then a corresponding voltage error is produced as shown in Figure 6.157. This sample-to-sample variation in the instant the switch opens is called *aperture uncertainty*, or *aperture jitter* and is usually measured in rms picoseconds. The amplitude of the associated output error is related to the rate-of-change of the analog input. For any given value of aperture jitter, the aperture jitter error increases as the input dv/dt increases. The effects of phase jitter on the external sampling clock (or the analog input for that matter) produce exactly the same type or error.

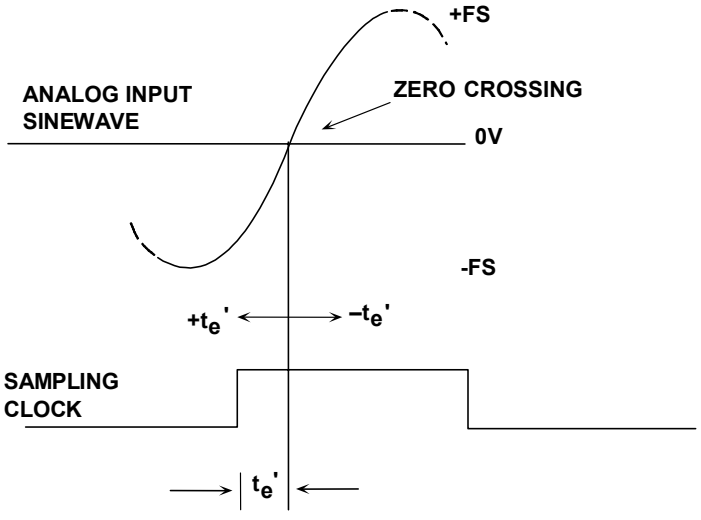


Figure 6.156: *Effective Aperture Delay Time Measured with Respect to ADC Input*

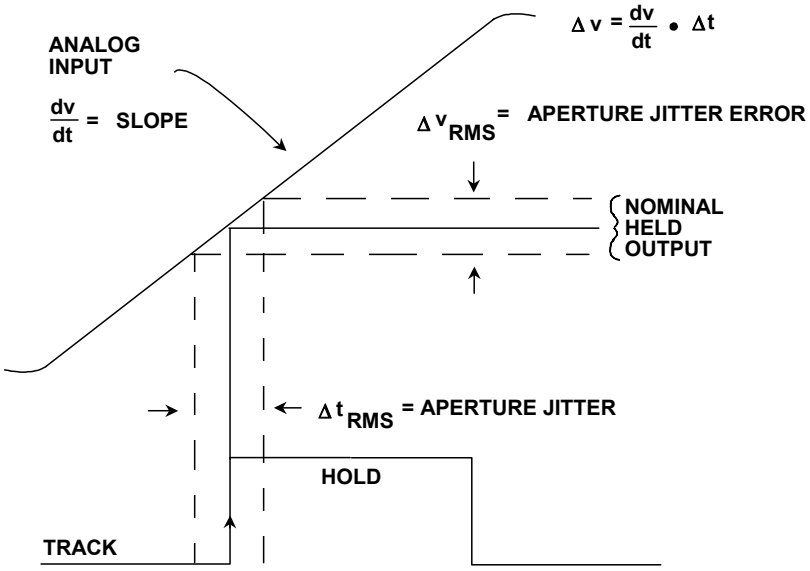


Figure 6.157: *Effects of Aperture Jitter and Sampling Clock Jitter*

The effects of aperture and sampling clock jitter on an ideal ADCs SNR can be predicted by the following simple analysis. Assume an input signal given by

$$v(t) = V_O \sin 2\pi ft \qquad \text{Eq. 6.27}$$

The rate of change of this signal is given by:

$$dv/dt = 2\pi fV_O \cos 2\pi ft. \qquad \text{Eq. 6.28}$$

The rms value of dv/dt can be obtained by dividing the amplitude, $2\pi fV_O$, by $\sqrt{2}$:

$$dv/dt|_{rms} = 2\pi fV_O / \sqrt{2}. \qquad \text{Eq. 6.29}$$

Now let Δv_{rms} = the rms voltage error and Δt = the rms aperture jitter t_j, and substitute:

$$\Delta v_{rms} / t_j = 2\pi fV_O / \sqrt{2}. \qquad \text{Eq. 6.30}$$

Solving for Δv_{rms} :

$$\Delta v_{rms} = 2\pi fV_O t_j / \sqrt{2}. \qquad \text{Eq. 6.31}$$

The rms value of the full-scale input sinewave is $V_O/\sqrt{2}$, therefore the rms signal to rms noise ratio is given by

$$\text{SNR} = 20\log_{10}\left[\frac{V_O/\sqrt{2}}{\Delta v_{rms}}\right] = 20\log_{10}\left[\frac{V_O/\sqrt{2}}{2\pi fV_O t_j/\sqrt{2}}\right] = 20\log_{10}\left[\frac{1}{2\pi f\, t_j}\right]. \qquad \text{Eq. 6.32}$$

This equation assumes an infinite resolution ADC where aperture jitter is the only factor in determining the SNR. This equation is plotted in Figure 6.158 and shows the serious effects of aperture and sampling clock jitter on SNR, especially at higher input/output frequencies. Therefore, extreme care must be taken to minimize phase noise in the sampling/reconstruction clock of any sampled data system.

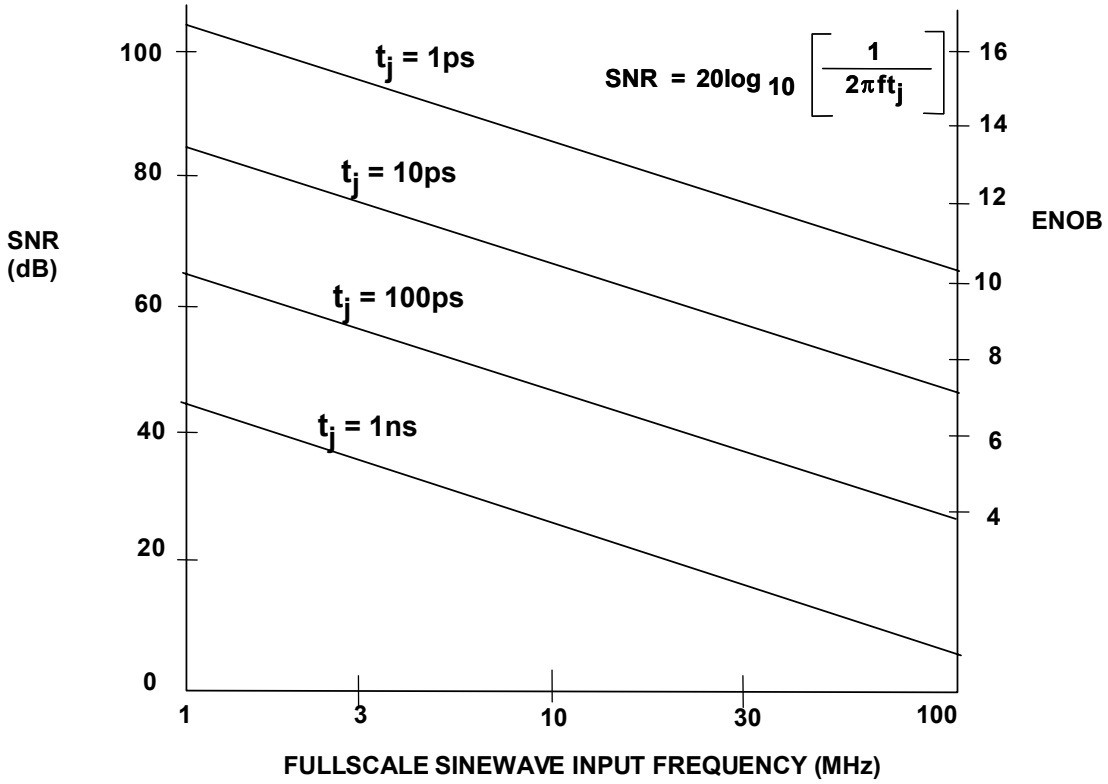


Figure 6.158: *SNR Due to Aperture Jitter and Sampling Clock Jitter*

This care must extend to all aspects of the clock signal: the oscillator itself (for example, a 555 timer is absolutely inadequate, but even a quartz crystal oscillator can give problems if it uses an active device which shares a chip with noisy logic); the transmission path (these clocks are very vulnerable to interference of all sorts), and phase noise introduced in the ADC or DAC. As discussed, a very common source of phase noise in converter circuitry is aperture jitter in the integral sample-and-hold (SHA) circuitry, however the total rms jitter will be composed of a number of components—the actual SHA aperture jitter often being the least of them.

A Simple Equation for the Total SNR of an ADC

A relatively simple equation for the ADC SNR in terms of sampling clock and aperture jitter, DNL, effective input noise, and the number of bits of resolution is shown in Figure 6.159. The equation combines the various error terms on an rms basis. The average DNL error, ε, is computed from histogram data. This equation is used in Figure 6.160 to predict the SNR performance of the AD6645 14-bit, 80-MSPS ADC as a function of sampling clock and aperture jitter.

$$SNR = -20\log_{10}\left[(2\pi \times f_a \times t_{j\,rms})^2 + \frac{2}{3}\left[\frac{1+\varepsilon}{2^N}\right]^2 + \left[\frac{2 \times \sqrt{2} \times V_{NOISErms}}{2^N}\right]^2\right]^{\frac{1}{2}}$$

SAMPLING CLOCK JITTER — QUANTIZATION NOISE, DNL — EFFECTIVE INPUT NOISE

f_a = Analog input frequency of fullscale input sinewave

$t_{j\,rms}$ = Combined rms jitter of internal ADC and external clock

ε = Average DNL of the ADC (typically 0.41 LSB for AD6645)

N = Number of bits in the ADC

$V_{NOISErms}$ = Effective input noise of ADC (typically 0.9LSB rms for AD6645)

If $t_j = 0$, $\varepsilon = 0$, and $V_{NOISErms} = 0$, the above equation reduces to the familiar:

$$SNR = 6.02\,N + 1.76dB$$

Figure 6.159: *Relationship Between SNR, Sampling Clock Jitter, Quantization Noise, DNL, and Input Noise*

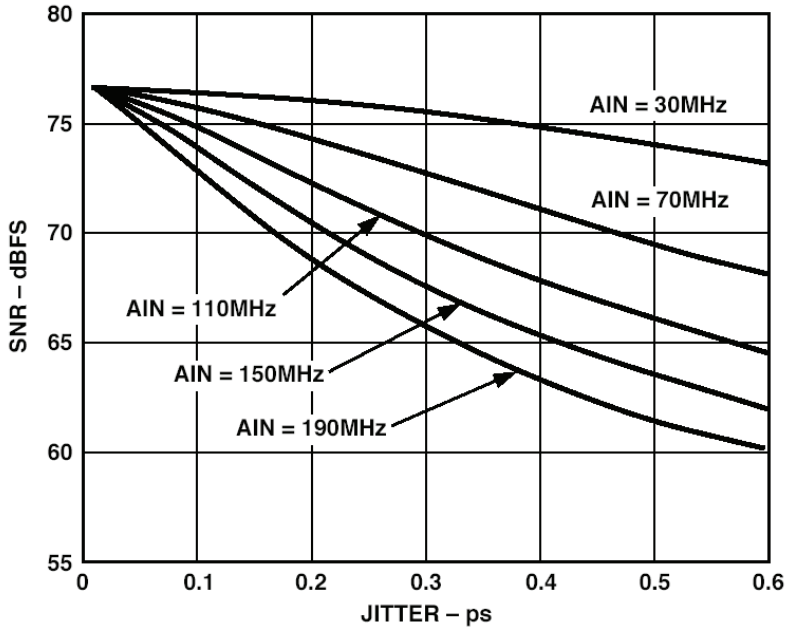


Figure 6.160: *AD6645 SNR vs. Aperture Jitter*

Two decades or so ago, sampling ADCs were built up from a separate SHA and ADC. Interface design was difficult, and a key parameter was aperture jitter in the SHA. Today, most sampled data systems use *sampling* ADCs which contain an integral SHA. The aperture jitter of the SHA may not be specified as such, but this is not a cause of concern if the SNR or ENOB is clearly specified, since a guarantee of a specific SNR is an implicit guarantee of an adequate aperture jitter specification. However, the use of an additional high-performance SHA will sometimes improve the high-frequency ENOB of a even the best sampling ADC by presenting "dc" to the ADC, and may be more cost-effective than replacing the ADC with a more expensive one.

ADC Transient Response and Overvoltage Recovery

Most high speed ADCs designed for communications applications are specified primarily in the frequency domain. However, in general purpose data acquisition applications the transient response (or settling time) of the ADC is important. The *transient response* of an ADC is the time required for the ADC to settle to rated accuracy (usually 1 LSB) after the application of a full-scale step input. The typical response of a general-purpose 12 bit, 10-MSPS ADC is shown in Figure 6.161, showing a 1 LSB settling time of less than 40 ns. The settling time specification is critical in the typical data acquisition system application where the ADC is being driven by an analog multiplexer as shown in Figure 6.162. The multiplexer output can deliver a full-scale sample-to-sample change to the ADC input. If both the multiplexer and the ADC have not both settled to the required accuracy, channel-to-channel crosstalk will result, even though only dc or low frequency signals are present on the multiplexer inputs.

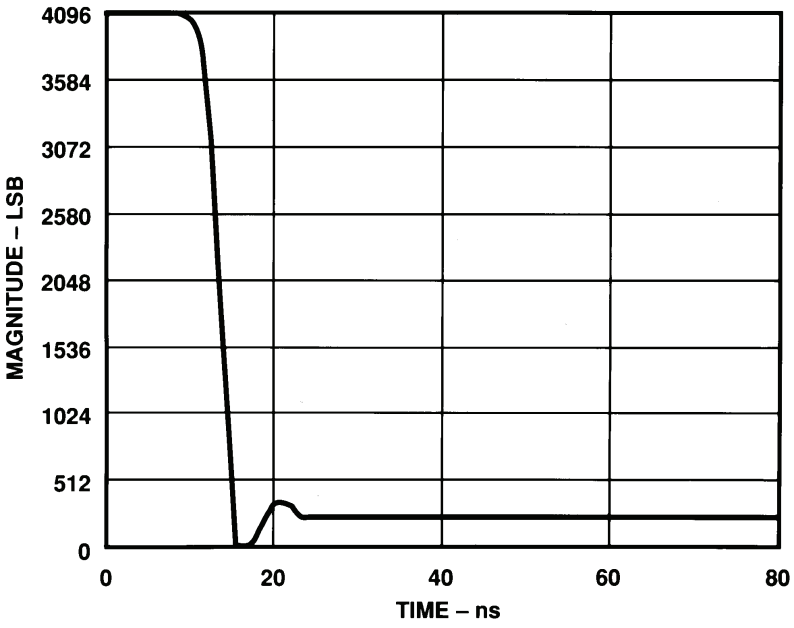


Figure 6.161: *ADC Transient Response (Settling Time)*

Most ADCs have settling times which are less than $1/f_{s\ max,}$ even if not specified. However sigma-delta ADCs have a built in digital filter which can take several output sample intervals to settle. This should be kept in mind when using sigma-delta ADCs in multiplexed applications.

The importance of settling time in multiplexed systems can be seen in Figure 6.163, where the ADC input is modeled as a single-pole filter having a corresponding time constant, $\tau = RC$. The required number of time constants to settle to a given accuracy (1 LSB) is shown. A simple example will illustrate the point.

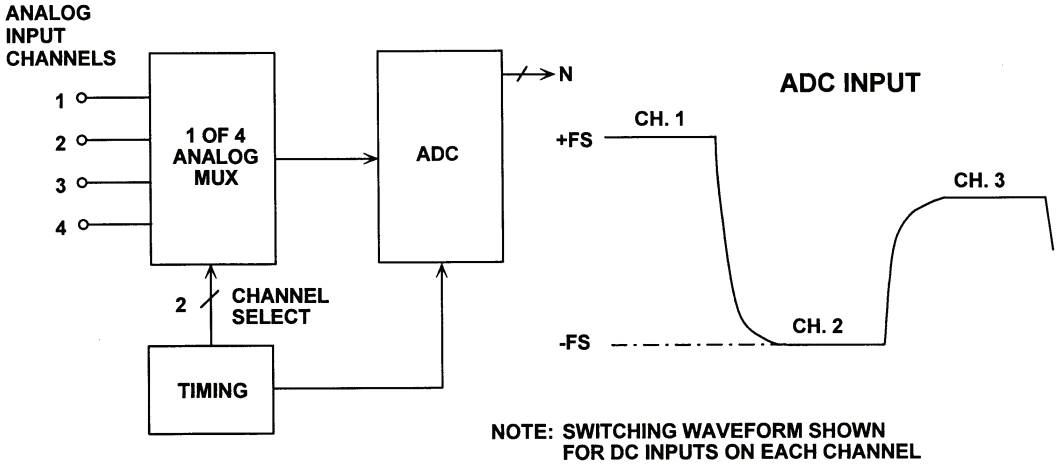


Figure 6.162: *Settling Time is Critical in Multiplexed Applications*

RESOLUTION, # OF BITS	LSB (%FS)	# OF TIME CONSTANTS
6	1.563	4.16
8	0.391	5.55
10	0.0977	6.93
12	0.0244	8.32
14	0.0061	9.70
16	0.00153	11.09
18	0.00038	12.48
20	0.000095	13.86
22	0.000024	15.25

Figure 6.163: *Settling Time as a Function of Time Constant for Various Resolutions*

Assume a multiplexed 16-bit data acquisition system uses an ADC with a sampling frequency f_s = 100 kSPS. The ADC must settle to 16-bit accuracy for a full-scale step function input in less than $1/f_s$ = 10µs. The chart shows that 11.09 time constants are

required to settle to 16-bit accuracy. The input filter time constant must therefore be less than τ = 10 μs/11.09 = 900 ns. The corresponding, risetime $t_r = 2.2\tau$ = 1.98 μs. The required ADC full power input bandwidth can now be calculated from BW = $0.35/t_r$ = 177 kHz. This neglects the settling time of the multiplexer and second-order settling time effects in the ADC.

Overvoltage recovery time is defined as that amount of time required for an ADC to achieve a specified accuracy, measured from the time the overvoltage signal re-enters the converter's range, as shown in Figure 6.164. This specification is usually given for a signal which is 50% outside the ADC's input range. Needless to say, the ADC should act as an ideal limiter for out-of-range signals and should produce either the positive full-scale code or the negative full-scale code during the overvoltage condition. Some converters provide over- and under-range flags to allow gain-adjustment circuits to be activated. Care should always be taken to avoid overvoltage signals which will damage an ADC input.

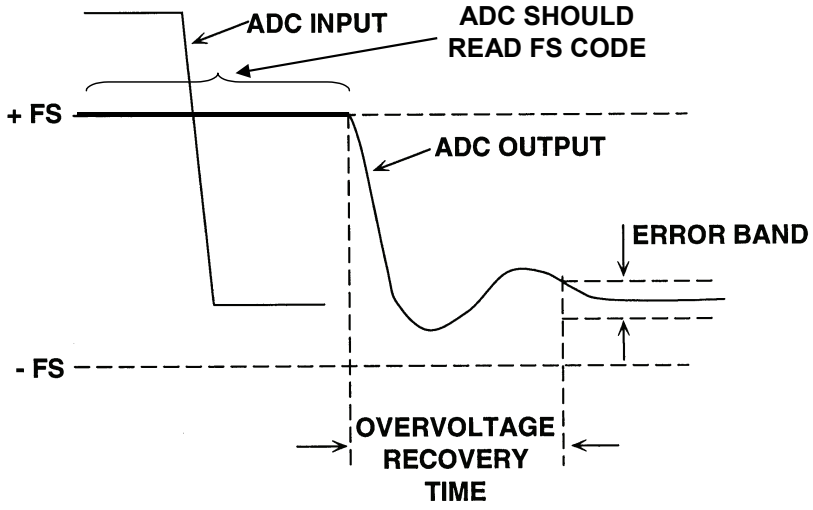


Figure 6.164: *Overvoltage Recovery Time*

ADC Sparkle Codes, Metastable States, and Bit Error Rate (BER)

A primary concern in the design of many digital communications systems using ADCs is the bit error rate (BER). Unfortunately, ADCs contribute to the BER in ways that are not predictable by simple analysis. This section describes the mechanisms within the ADCs that can contribute to the error rate, ways to minimize the problem, and methods for measuring the BER.

Random noise, regardless of the source, creates a finite probability of errors (deviations from the expected output). Before describing the error code sources, however, it is important to define what constitutes an ADC error code. Noise generated prior to, or inside the ADC can be analyzed in the traditional manner. Therefore, an ADC error code is any deviation from the expected output that is not attributable to the equivalent input noise of the ADC. Figure 6.165 illustrates an exaggerated output of a low amplitude sine

wave applied to an ADC that has error codes. Note that the noise of the ADC creates some uncertainty in the output. These anomalies are not considered error codes, but are simply the result of ordinary noise and quantization. The large errors are more significant and are not expected. These errors are random and so infrequent that an SNR test of the ADC will rarely detect them. These types of errors plagued a few of the early ADCs for video applications, and were given the name *sparkle codes* because of their appearance on a TV screen as small white dots or "sparkles" under certain test conditions. These errors have also been called *rabbits* or *flyers*. In digital communications applications, this type of error increases the overall system bit error rate (BER).

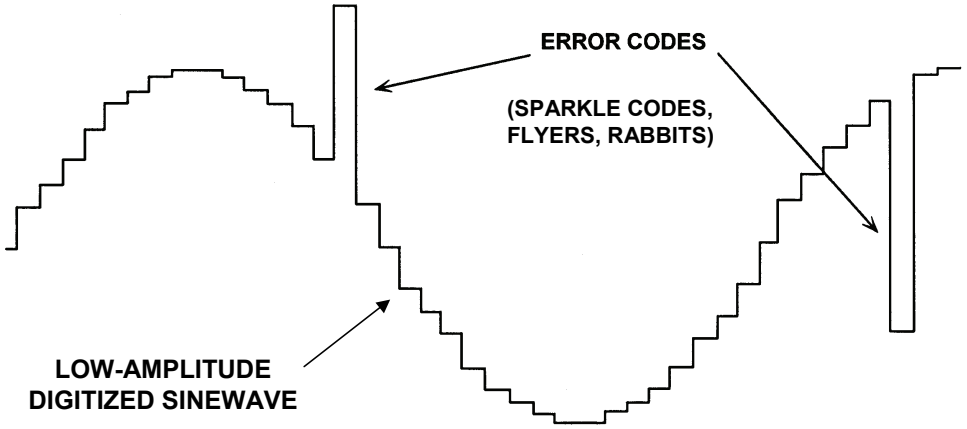


Figure 6.165: *Exaggerated Output of ADC Showing Error Codes*

In order to understand the causes of the error codes, we will first consider the case of a simple flash converter. The comparators in a flash converter are latched comparators usually arranged in a master-slave configuration. If the input signal is in the center of the threshold of a particular comparator, that comparator will balance, and its output will take a longer period of time to reach a valid logic level after the application of the latch strobe than the outputs of its neighboring comparators which are being overdriven. This phenomenon is known as *metastability* and occurs when a balanced comparator cannot reach a valid logic level in the time allowed for decoding. If simple binary decoding logic is used to decode the thermometer code, a metastable comparator output may result in a large output code error. Consider the case of a simple 3 bit flash converter shown in Figure 6.167. Assume that the input signal is exactly at the threshold of Comparator 4 and random noise is causing the comparator to toggle between a 1 and a 0 output each time a latch strobe is applied. The corresponding binary output should be interpreted as either 011 or 100. If, however, the comparator output is in a metastable state, the simple binary decoding logic shown may produce binary codes 000, 011, 100, or 111. The codes 000 and 111 represent a one-half scale departure from the expected codes.

The probability of errors due to metastability increases as the sampling rate increases because less time is available for a metastable comparator to settle.

Various measures have been taken in flash converter designs to minimize the metastable state problem. Decoding schemes described in References 12 to 15 minimize the magnitude of these errors. Optimizing comparator designs for regenerative gain and small time constants is another way to reduce these problems.

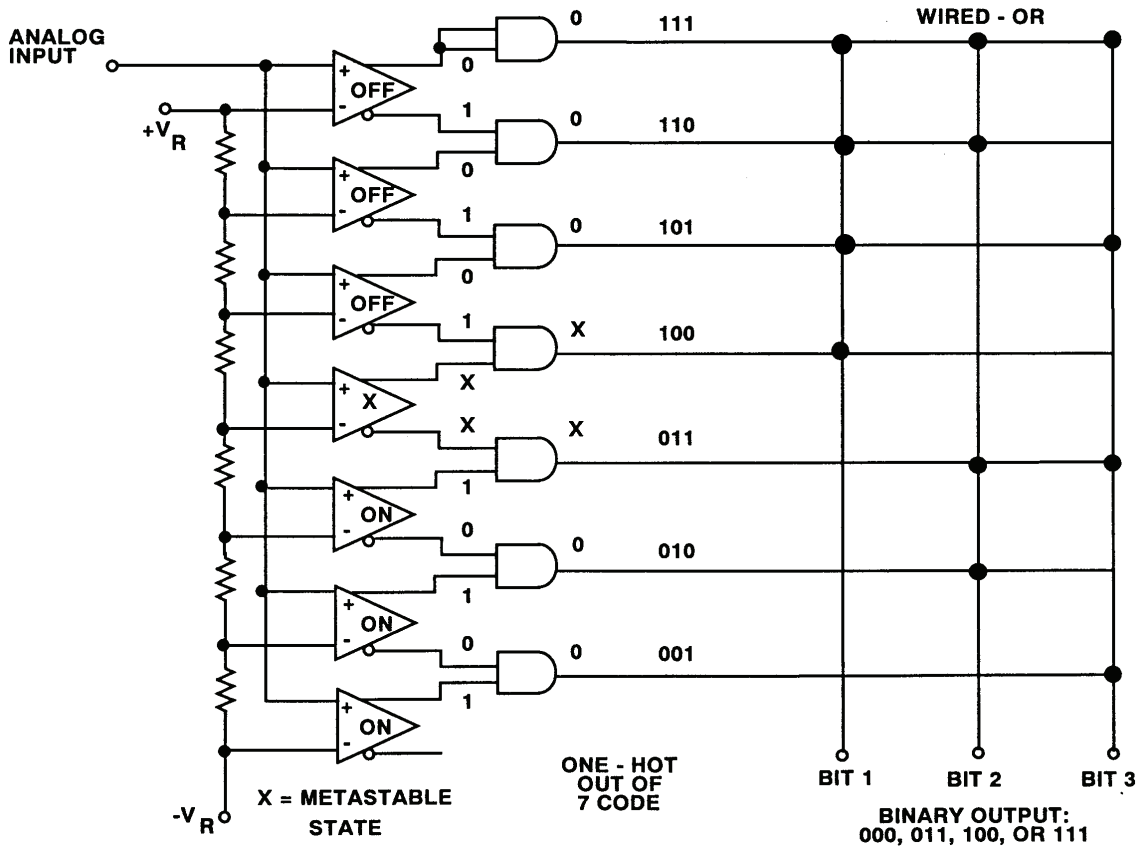


Figure 6.166: *Metastable Comparator Output States May Cause Error Codes in Data Converters*

Metastable state errors may also appear in successive approximation and subranging ADCs which make use of comparators as building blocks. The same concepts apply, although the magnitudes and locations of the errors may be different.

Establishing the BER of a well-behaved ADC is a difficult, time-consuming task; a single unit can sometimes be tested for days without an error. For example, tests on a typical 8-bit flash converter operating at a sampling rate of 75 MSPS yield a BER of approximately 3.7×10^{-12} (1 error per hour) with an error limit of 4 LSBs. Meaningful tests for longer periods of time require special attention to EMI/RFI effects (possibly requiring a shielded screen room), isolated power supplies, etc. Figure 6.167 shows the average time between errors as a function of BER for a sampling frequency of 75 MSPS.

This illustrates the difficulty in measuring low BER because the long measurement times increase the probability of power supply transients, noise, etc. causing an error.

Bit Error Rate (BER)	Average Time Between Errors
1×10^{-8}	1.3 seconds
1×10^{-9}	13.3 seconds
1×10^{-10}	2.2 minutes
1×10^{-11}	22 minutes
1×10^{-12}	3.7 hours
1×10^{-13}	1.5 days
1×10^{-14}	15 days

Figure 6.167: *Average Time Between Errors vs. BER When Sampling at 75 MSPS*

DAC Dynamic Performance

The ac specifications which are most likely to be important with DACs are *settling time*, *glitch impulse area*, *distortion,* and *Spurious-Free Dynamic Range (SFDR)*.

DAC Settling Time

The settling time of a DAC is the time from a change of digital code to when the output comes within *and remains within* some error band as shown in Figure 6.168. With amplifiers, it is hard to make comparisons of settling time, since their error bands may differ from amplifier to amplifier, but with DACs the error band will almost invariably be ±1 or ±½ LSB.

The settling time of a DAC is made up of four different periods: the *switching time* or *dead time* (during which the digital switching, but not the output, is changing), the *slewing time* (during which the rate of change of output is limited by the slew rate of the DAC output), the *recovery time* (when the DAC is recovering from its fast slew and may overshoot), and the *linear settling time* (when the DAC output approaches its final value in an exponential or near-exponential manner). If the slew time is short compared to the other three (as is usually the case with current output DACs), then the settling time will be largely independent of the output step size. On the other hand, if the slew time is a significant part of the total, then the larger the step, the longer the settling time.

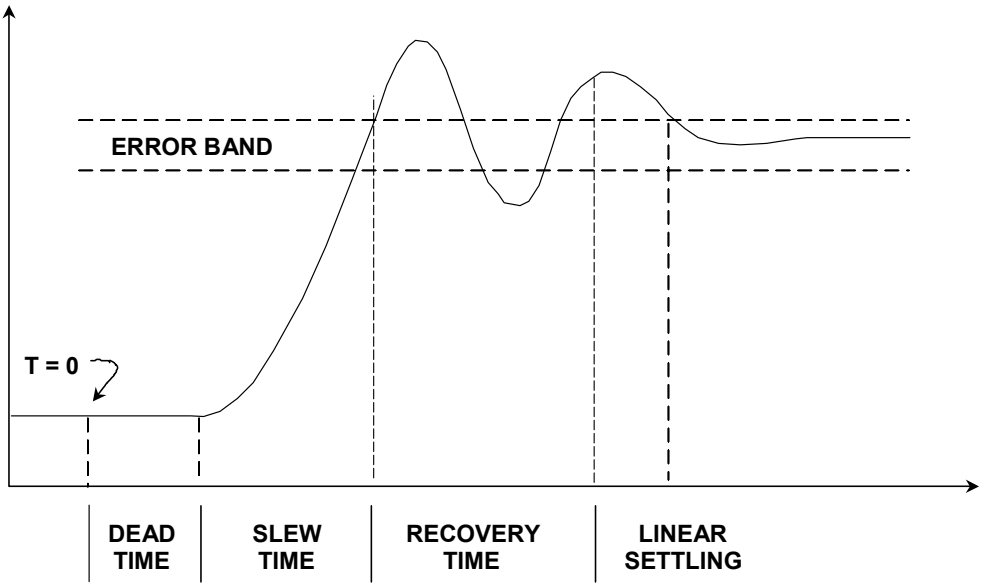


Figure 6.168: *DAC Settling Time*

Settling time is especially important in video display applications. For example a standard 1024 × 768 display updated at a 60 Hz refresh rate must have a pixel rate of 1024 × 768 × 60 Hz = 47.2 MHz with no overhead. Allowing 35% overhead time increases the pixel frequency to 64 MHz corresponding to a pixel duration of

$1/(64 \times 10^6) = 15.6$ ns. In order to accurately reproduce a single fully-white pixel located between two black pixels, the DAC settling time should be less than the pixel duration time of 15.6 ns.

Higher resolution displays require even faster pixel rates. For example, a 2048 × 2048 display requires a pixel rate of approximately 330 MHz at a 60 Hz refresh rate.

Glitch Impulse Area

Ideally, when a DAC output changes it should move from one value to its new one monotonically. In practice, the output is likely to overshoot, undershoot, or both (see Figure 6.169). This uncontrolled movement of the DAC output during a transition is known as a *glitch*. It can arise from two mechanisms: capacitive coupling of digital transitions to the analog output, and the effects of some switches in the DAC operating more quickly than others and producing temporary spurious outputs.

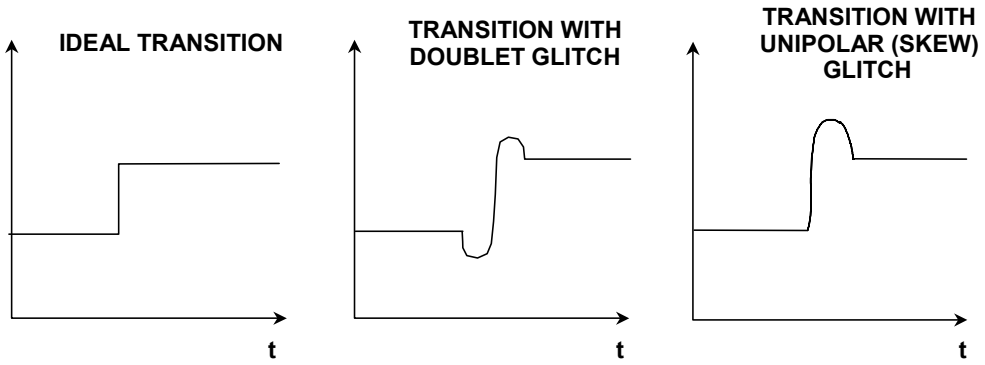


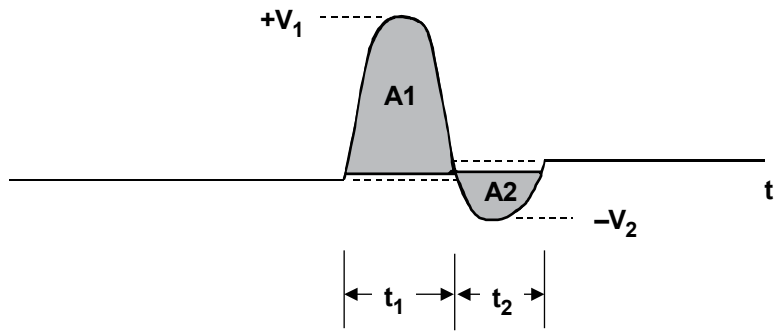
Figure 6.169: *DAC Transitions (Showing Glitch)*

Capacitive coupling frequently produces roughly equal positive and negative spikes (sometimes called a *doublet* glitch) which more or less cancel in the longer term. The glitch produced by switch timing differences is generally unipolar, much larger and of greater concern.

Glitches can be characterized by measuring the *glitch impulse area*, sometimes inaccurately called glitch energy. The term *glitch energy* is a misnomer, since the unit for glitch impulse area is Volt-seconds (or more probably μV-sec or pV-sec. The *peak glitch area* is the area of the largest of the positive or negative glitch areas. The glitch impulse area is the net area under the voltage-versus-time curve and can be estimated by approximating the waveforms by triangles, computing the areas, and subtracting the negative area from the positive area as shown in Figure 6.170.

The mid-scale glitch produced by the transition between the codes 0111...111 and 1000...000 is usually the worst glitch. Glitches at other code transition points (such as 1/4 and 3/4 full-scale) are generally less. Figure 6.171 shows the mid-scale glitch for a fast low-glitch DAC. The peak and net glitch areas are estimated using triangles as described

above. Settling time is measured from the time the waveform leaves the initial 1 LSB error band until it enters and remains within the final 1LSB error band. The step size between the transition regions is also 1 LSB.



- PEAK GLITCH IMPULSE AREA = A1 $\approx \frac{V_1 \cdot t_1}{2}$
- NET GLITCH IMPULSE AREA = A1 – A2 $\approx \frac{V_1 \cdot t_1}{2} - \frac{V_2 \cdot t_2}{2}$

Figure 6.170: *Calculating Net Glitch Impulse Area*

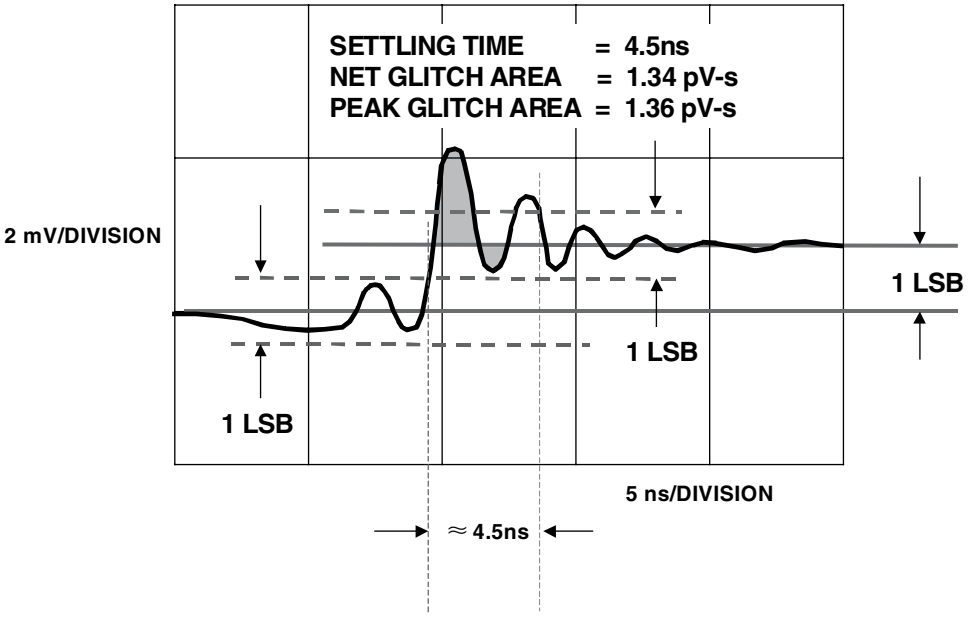


Figure 6.171: *DAC Mid-scale Glitch Shows 1.34 pV-s Net Impulse Area and Settling Time of 4.5 ns*

DAC SFDR and SNR

DAC settling time is important in applications such as RGB raster scan video display drivers, but frequency-domain specifications such as SFDR are generally more important in communications.

If we consider the spectrum of a waveform reconstructed by a DAC from digital data, we find that in addition to the expected spectrum (which will contain one or more frequencies, depending on the nature of the reconstructed waveform), there will also be noise and distortion products. Distortion may be specified in terms of harmonic distortion, Spurious Free Dynamic Range (SFDR), intermodulation distortion, or all of the above. Harmonic distortion is defined as the ratio of harmonics to fundamental when a (theoretically) pure sine wave is reconstructed, and is the most common specification. Spurious free dynamic range is the ratio of the worst spur (usually, but not necessarily always a harmonic of the fundamental) to the fundamental.

Code-dependent glitches will produce both out-of-band and in-band harmonics when the DAC is reconstructing a digitally generated sine wave as in a Direct Digital Synthesis (DDS) system. The mid-scale glitch occurs twice during a single cycle of a reconstructed sine wave (at each mid-scale crossing), and will therefore produce a second harmonic of the sine wave, as shown in Figure 6.172. Note that the higher order harmonics of the sine wave, which alias back into the Nyquist bandwidth (dc to $f_s/2$), cannot be filtered.

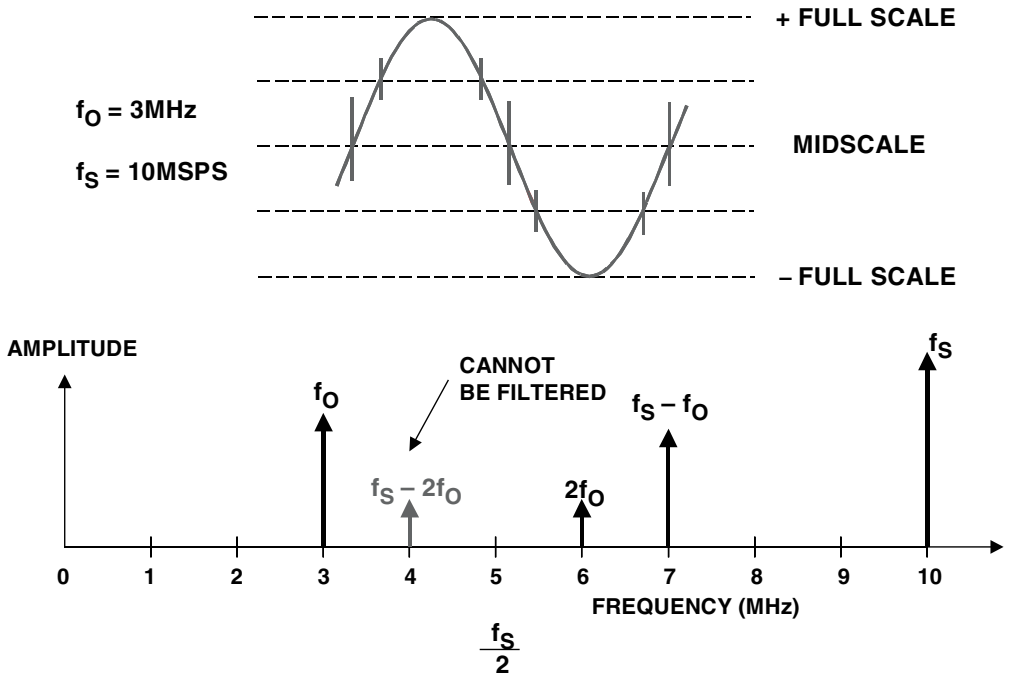


Figure 6.172: *Effect of Code-Dependent Glitches on Spectral Output*

It is difficult to predict the harmonic distortion or SFDR from the glitch area specification alone. Other factors, such as the overall linearity of the DAC, also contribute to distortion. In addition, certain ratios between the DAC output frequency and the sampling

clock cause the quantization noise to concentrate at harmonics of the fundamental thereby increasing the distortion at these points.

It is therefore customary to test reconstruction DACs in the frequency domain (using a spectrum analyzer) at various clock rates and output frequencies as shown in Figure 6.173. Typical SFDR for the 16-bit AD9777 Transmit TxDAC™ is shown in Figure 6.174. The clock rate is 160 MSPS, and the output frequency is swept to 50 MHz. As in the case of ADCs, quantization noise will appear as increased harmonic distortion if the ratio between the clock frequency and the DAC output frequency is an integer number. These ratios should be avoided when making the SFDR measurements.

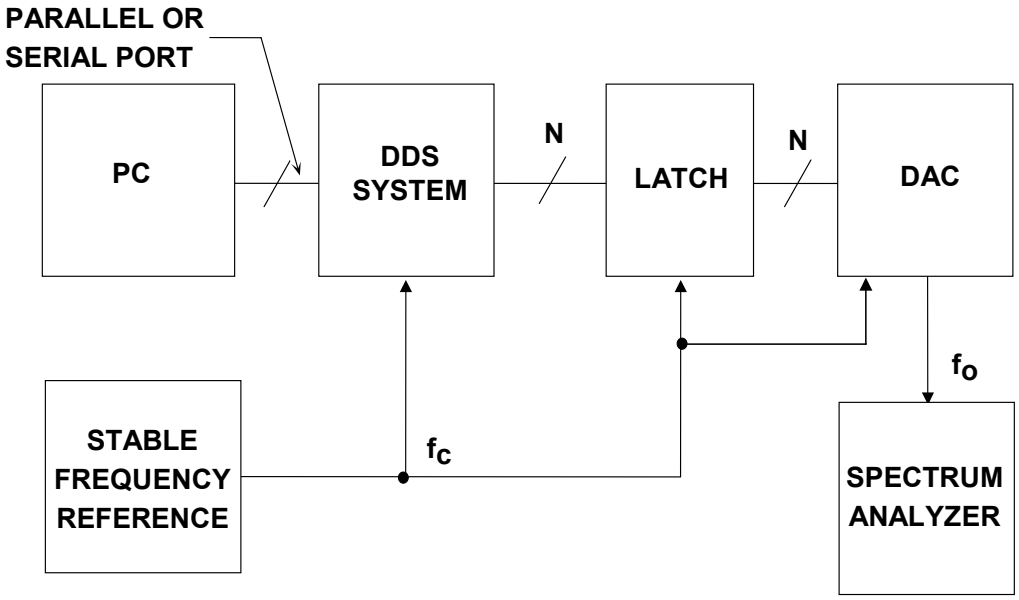


Figure 6.173: *Test Setup for Measuring DAC SFDR*

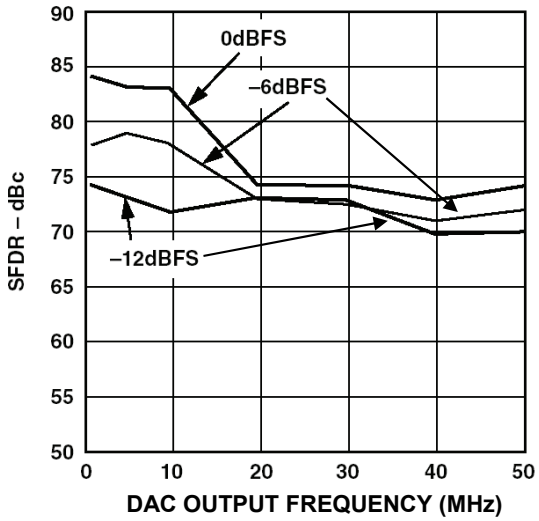


Figure 6.174: *AD9777 16-bit TxDAC SFDR, Data Update Rate = 160 MSPS*

There are nearly an infinite combination of possible clock and output frequencies for a low distortion DAC, and SFDR is generally specified for a limited number of selected combinations. For this reason, Analog Devices offers fast turnaround on customer-specified test vectors for the Transmit TxDAC family. A test vector is a combination of amplitudes, output frequencies, and update rates specified directly by the customer for SFDR data on a particular DAC.

Measuring DAC SNR with an Analog Spectrum Analyzer

Analog spectrum analyzers are used to measure the distortion and SFDR of high performance DACs. Care must be taken such that the front end of the analyzer is not overdriven by the fundamental signal. If overdrive is a problem, a band-stop filter can be used to filter out the fundamental signal such that the spurious components can be observed.

Spectrum analyzers can also be used to measure the SNR of a DAC provided attention is given to bandwidth considerations. SNR of an ADC is normally defined as the signal-to-noise ratio measured over the Nyquist bandwidth dc to $f_s/2$. However, spectrum analyzers have a resolution bandwidth which is less than $f_s/2$—this therefore lowers the analyzer noise floor by the process gain equal to $10 \log_{10}(f_s/2 \cdot BW)$, where BW is the resolution noise bandwidth of the analyzer (see Figure 6.175).

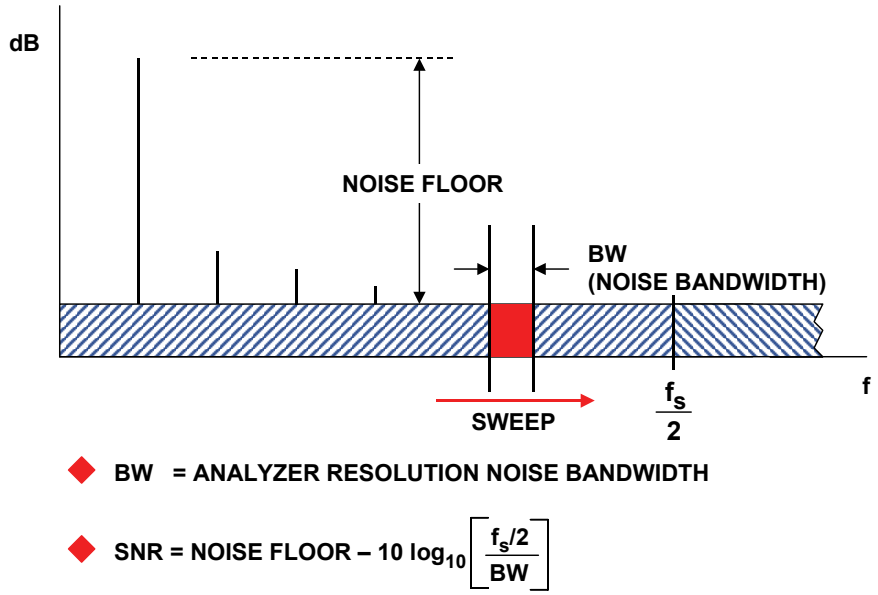


Figure 6.175: *Measuring DAC SNR with an Analog Spectrum Analyzer*

It is important that the noise bandwidth (not the 3-dB bandwidth) be used in the calculation; however from Figure 6.147 the error is small assuming that the analyzer narrowband filter is at least two poles. The ratio of the noise bandwidth to the 3-dB bandwidth of a one-pole Butterworth filter is 1.57 (causing an error of 1.96 dB in the process gain calculation). For a two-pole Butterworth filter, the ratio is 1.11 (causing an error of 0.45 dB in the process gain calculation).

Other AC Specifications

Again, there are some specifications that may be encountered that are less common and are listed below.

Acquisition Time: The acquisition time of a sample-and-hold circuit for a step change is the time required by the output to reach its final value, within a specified error band, after the track command has been given. Included are switch delay time, the slewing interval, and settling time for a specified output voltage change. This spec is less common now that the sample and hold function has largely been integrated into the ADC.

Automatic Zero: To achieve zero stability in many integrating-type converters, a time interval is provided during each conversion cycle to allow the circuitry to compensate for drift errors. The drift error in such converters is substantially zero.

Channel-to-Channel Isolation: In multiple DACs, the proportion of analog input signal from one DAC's reference input that appears at the output of the other DAC, expressed logarithmically in dB. See also *crosstalk.*

Charge Transfer (or Offset Step): the principal component of *sample-to-hold offset* (or *pedestal),* is the small charge transferred to the storage capacitor via interelectrode capacitance of the switch and stray capacitance when switching to the *hold* mode. The offset step is directly proportional to this charge, viz.,

Offset error = Incremental Charge/Capacitance = $\Delta Q/C$.

It can be reduced somewhat by lightly coupling an appropriate polarity version of the *hold* signal to the capacitor for first-order cancellation. The error can also be reduced by increasing the capacitance, but this increases *acquisition time.* Again a spec that has become less common since the sample and hold function has largely been integrated into the ADC.

Crosstalk: Leakage of signals, usually via capacitance between circuits or channels of a multichannel system or device, such as a multiplexer, multiple op amp, or multiple DAC. Crosstalk is usually determined by the impedance parameters of the physical circuit, and actual values are frequency-dependent. See also *channel-to-channel isolation.*
Multiple DACs have a *digital crosstalk* specification: the spike (sometimes called a glitch) impulse appearing at the output of one converter due to a change in the digital input code of another of the converters. It is specified in nanovolt- or picovolt-seconds and measured at V_{REF} = 0 V.

Differential Gain (ΔG): A video specification which measures the variation in the amplitude (in percent) of a small amplitude color subcarrier signal as it is swept across the video range from black to white.

Differential Phase ($\Delta\varphi$): A video specification which measures the phase variation (in degrees) of a small amplitude color subcarrier signal as it is swept across the video range from black to white.

Feedthrough: Undesirable signal-coupling around switches or other devices that are supposed to be turned off or provide isolation, *e.g., feedthrough error* in a sample-and-hold, multiplexer, or multiplying DAC. Feedthrough is variously specified in percent, dB, parts per million, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

In a multiplying *DAC, feedthrough* error is caused by capacitive coupling from an ac V_{REF} to the output, with all switches off. In a *sample-and-hold, feedthrough* is the fraction of the input signal variation or ac input waveform that appears at the output in *hold.* It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

Settling Time—ADC: The time required, following an analog input step change (usually full-scale), for the digital output of the ADC to reach and remain within a given fraction (usually ± ½LSB).

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SECTION 6.7: TIMING SPECIFICATIONS

In most cases, the digital signals of a converter are designed to operate at standard levels with standard interface specifications. Common interfaces are parallel or serial (most commonly SPI® or I^2C® compatible, but, at the high speed, LVDS is making inroads). The fact that we are compatible with defined standards means that the timing and voltage levels defined in these specifications are met.

The digital signals of a converter generally divided into one of three groups: address, data, and control.

Common timing specifications include:

Logic low level: the voltage level at which the signal is guaranteed to be seen as a logic 0. This level is generally specified at whatever power supply the converter is guaranteed to run at. This means that you will generally see different specification table for 3 V and 5 V supplies.

Logic high level: the voltage level at which the signal is guaranteed to be seen as a logic 1. Again, this will be given at the various power supply voltages.

Rise time: for a step function, the time required for a signal to change from a specified low value to a specified high value. Typically, these values are 10% and 90% of the step height (see Figure 6.176).

Fall time: for a step function, the time required for a signal to change from a specified high value to a specified low value. Typically, these values are 10% and 90% of the step height (see Figure 6.177).

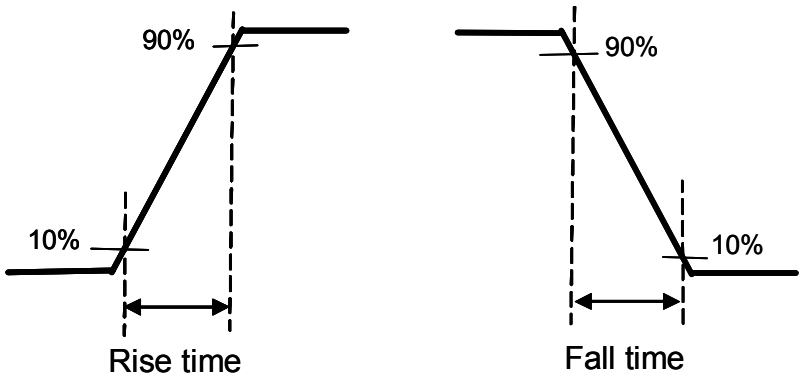


Figure 6.176: *Rise Time and Fall Time*

Setup Time: the time that the data input must be valid before the output latch samples.

Hold Time: the time that data input must be maintained valid after the output samples.

Propagation Delay: the time that takes to the sampled data input to propagate to the output.

Pulsewidth High: the minimum time a pulse must be at the logic high level

Pulsewidth Low: the minimum time a pulse must be at the logic low level

Other timing specifications are typically from one signal transition to another. These signals will be defined in the specifications. As an example see Figure 6.178.

Often the output current available is also specified. This will help determine fan out, the number of standard loads that the output can drive. But we will discuss in the circuit board considerations section why it is probably not wise to have the converter drive significant current.

Occasionally a high speed converter has a clock input that is not a standard logic signal level. This is often to make the signal easier to generate and propagate on the printed circuit board. For example, for optimum performance, the AD6645 must be clocked differentially. The encode signal is usually ac-coupled into the ENC and *ENC* pins via a transformer or capacitors. These pins are biased internally and require no additional bias. The input impedance of the input and the signal level will be specified. See Figure 6.176.

Parameter (Conditions)	Temp	Test Level	AD6645ASQ-80 Min	AD6645ASQ-80 Typ	AD6645ASQ-80 Max	AD6645ASQ-105 Min	AD6645ASQ-105 Typ	AD6645ASQ-105 Max	Unit
ENCODE INPUTS (ENC, $\overline{ENC}$)									
Differential Input Voltage[1]	Full	IV	0.4			0.4			V p-p
Differential Input Resistance	25°C	V		10			10		kΩ
Differential Input Capacitance	25°C	V		2.5			2.5		pF

Figure 6.177: *Encode Command Specifications for the AD6645*

AD6645

SWITCHING SPECIFICATIONS (continued)

(AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE, $\overline{\text{ENCODE}}$, T_{MIN} and T_{MAX} at rated speed grade, C_{LOAD} = 10 pF, unless otherwise noted.)

Parameter (Conditions)	Name	Temp	Test Level	AD6645ASQ-80 Min	AD6645ASQ-80 Typ	AD6645ASQ-80 Max	AD6645ASQ-105 Min	AD6645ASQ-105 Typ	AD6645ASQ-105 Max	Unit
ENCODE Input Parameters[1]										
Encode Period[1]	t_{ENC}	Full	V		12.5			9.5		ns
Encode Pulsewidth High[2]	t_{ENCH}	Full	V		6.25			4.75		ns
Encode Pulsewidth Low	t_{ENCL}	Full	V		6.25			4.75		ns
ENCODE/DataReady										
Encode Rising to DataReady Falling	t_{DR}	Full	V	1.0	2.0	3.1	1.0	2.0	3.1	ns
Encode Rising to DataReady Rising	t_{E_DR}	Full	V		$t_{ENCH} + t_{DR}$			$t_{ENCH} + t_{DR}$		ns
(50% Duty Cycle)		Full	V	7.3	8.3	9.4	5.7	6.75	7.9	ns
ENCODE/DATA (D13:0), OVR										
ENC to DATA Falling Low	t_{E_FL}	Full	V	2.4	4.7	7.0	2.4	4.7	7.0	ns
ENC to DATA Rising Low	t_{E_RL}	Full	V	1.4	3.0	4.7	1.4	3.0	4.7	ns
ENCODE to DATA Delay (Hold Time)	t_{H_E}	Full	V	1.4	3.0	4.7	1.4	3.0	4.7	ns
ENCODE to DATA Delay (Setup Time)	t_{S_E}	Full	V	$t_{ENC} - t_{E\_FL(max)}$			$t_{ENC} - t_{E\_FL(max)}$			ns
					$t_{ENC} - t_{E\_FL(typ)}$			$t_{ENC} - t_{E\_FL(typ)}$		ns
						$t_{ENC} - t_{E\_FL(min)}$			$t_{ENC} - t_{E\_FL(min)}$	ns
(50% Duty Cycle)		Full	V	5.3	7.6	10.0	2.3	4.8	7.0	ns
DataReady (DRY[3])/DATA, OVR										
DataReady to DATA Delay (Hold Time)	t_{H_DR}	Full	V		Note 4			Note 4		
(50% Duty Cycle)				6.6	7.2	7.9	5.1	5.7	6.4	ns
DataReady to DATA Delay (Setup Time)	t_{S_DR}	Full	V		Note 4			Note 4		
(50% Duty Cycle)				2.1	3.6	5.1	0.6	2.1	3.5	ns
APERTURE DELAY	t_A	25°C	V		–500			–500		ps
APERTURE UNCERTAINTY (Jitter)	t_j	25°C	V		0.1		0.1			ps rms

NOTES
[1]Several timing parameters are a function of t_{ENC} and t_{ENCH}.
[2]ENCODE TO DATA Delay (Hold Time) is the absolute minimum propagation delay through the analog-to-digital converter, $t_{E\_RL} = t_{H\_E}$.
[3]DRY is an inverted and delayed version of the encode clock. Any change in the duty cycle of the clock will correspondingly change the duty cycle of DRY.
[4]DataReady to DATA Delay (t_{H_DR} and t_{S_DR}) is calculated relative to rated speed grade and is dependent on t_{ENC} and duty cycle.

Specifications subject to change without notice.

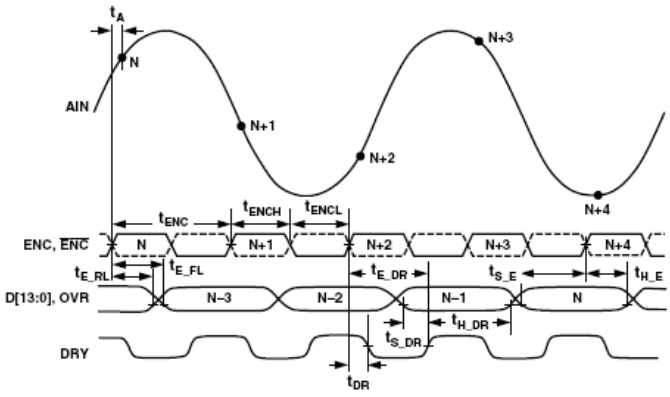


Figure 1. Timing Diagram

Figure 6.178: *Sample Timing Specifications for the AD6645*

Notes:

SECTION 6.8: HOW TO READ A DATA SHEET

While there is not an industry standard concerning data sheets (what they cover, what information is included, and where that information is located) for the most part, data sheets from various manufacturers generally are similar in construction. In this section we will take a look at several data sheets and try to give a feel for where to find certain information and how to interpret what is found.

As a demonstration we will look at 5 data sheets:

AD6645	High speed ADC
AD9777	High speed DAC (TxDAC, Interpolating DAC)
AD7678	General-Purpose ADC
AD5570	General-Purpose DAC
AD7730	Σ-Δ ADC

The part numbers chosen are arbitrarily, they were chosen only to give a range of parts.

The Front Page

This page is designed to give you the basic information you might need to choose the part. Referring to Figure 6.178. We can break this up into 3 sections.

Section 1 is the features. These bullet points are what are considered by the manufacturer to be the more important parameters of the product for its intended application. The targeted applications are typically listed as well.

The 2nd section is the product description. This typically covers some of what the manufacturer considers to be the salient features of the op amp.

The 3rd section is the functional block diagram. Many times you can get information from the block diagram. In this instance we can see that the ADC has a pipeline architecture, in this case 3 stage.

The Specification Tables

There are an unlimited number of conditions possible to measure any given specification. Obviously it is not possible to test all possible conditions. So a representative set of conditions are chosen. The test conditions are specified (1 in Figure 6.178). Occasionally if further clarification or modification of the conditions are required, they are handled as footnotes (2 in Figure 6.179).

On many converters some individual specifications may have multiple entries. This is for different performance levels. It an also be for different temperature ranges (usually commercial, industrial, or military). In this case it is for different speed grades. This can be seen in Figure 6.179 (3).

ANALOG DEVICES

14-Bit, 80/105 MSPS A/D Converter

AD6645

FEATURES
SNR = 75 dB, f_{IN} 15 MHz up to 105 MSPS
SNR = 72 dB, f_{IN} 200 MHz up to 105 MSPS
SFDR = 89 dBc, f_{IN} 70 MHz up to 105 MSPS
100 dB Multitone SFDR
IF Sampling to 200 MHz
Sampling Jitter 0.1 ps
1.5 W Power Dissipation
Differential Analog Inputs
Pin Compatible to AD6644
Twos Complement Digital Output Format
3.3 V CMOS Compatible
DataReady for Output Latching

APPLICATIONS
Multichannel, Multimode Receivers
Base Station Infrastructure
AMPS, IS-136, CDMA, GSM, WCDMA
Single Channel Digital Receivers
Antenna Array Processing
Communications Instrumentation
Radar, Infrared Imaging
Instrumentation

1

PRODUCT DESCRIPTION
The AD6645 is a high speed, high performance, monolithic 14-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on the chip to provide a complete conversion solution. The AD6645 provides CMOS compatible digital outputs. It is the fourth generation in a wideband ADC family, preceded by the AD9042 (12-bit, 41 MSPS), the AD6640 (12-bit, 65 MSPS, IF sampling), and the AD6644 (14-bit, 40 MSPS/65 MSPS).

Designed for multichannel, multimode receivers, the AD6645 is part of Analog Devices' SoftCell® transceiver chipset. The AD6645 maintains 100 dB multitone, spurious-free dynamic range (SFDR) through the second Nyquist band. This break-through performance eases the burden placed on multimode digital receivers (software radios) that are typically limited by the ADC. Noise performance is exceptional; typical signal-to-noise ratio is 74.5 dB through the first Nyquist band.

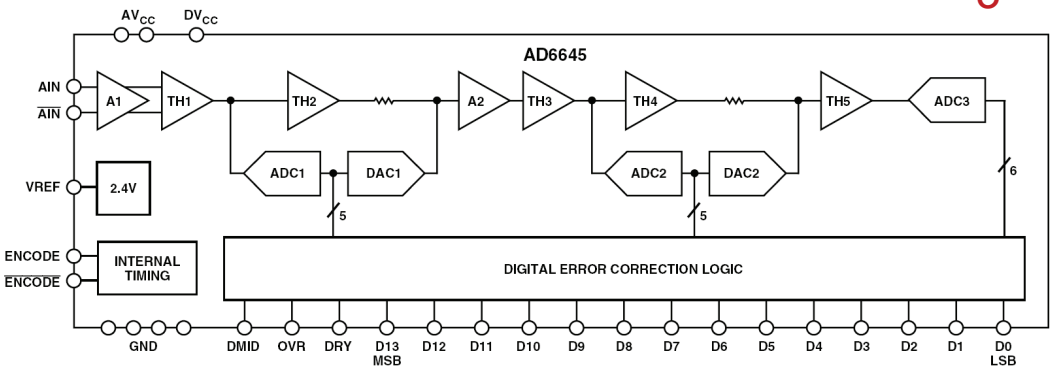
The AD6645 is built on Analog Devices' high speed complementary bipolar process (XFCB) and uses an innovative, multipass circuit architecture. Units are available in a thermally enhanced 52-lead PowerQuad 4® (LQFP_PQ4) specified from –40°C to +85°C at 80 MSPS and –10°C to +85°C at 105 MSPS.

2

PRODUCT HIGHLIGHTS
1. IF Sampling
   The AD6645 maintains outstanding ac performance up to input frequencies of 200 MHz, suitable for multicarrier 3G wideband cellular IF sampling receivers.
2. Pin Compatibility
   The ADC has the same footprint and pin layout as the AD6644, 14-Bit 40 MSPS/65 MSPS ADC.
3. SFDR Performance and Oversampling
   Multitone SFDR performance of –100 dBc can reduce the requirements of high end RF components and allows the use of receive signal processors such as the AD6620 or AD6624/AD6624A.

FUNCTIONAL BLOCK DIAGRAM

3



REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

Figure 6.179: *Example Data Sheet Front Page*

AD6645–SPECIFICATIONS

DC SPECIFICATIONS (AV_{CC} = 5 V, DV_{CC} = 3.3 V; T_{MIN} and T_{MAX} at rated speed grade, unless otherwise noted.) 1

3

Parameter	Temp	Test Level	AD6645ASQ-80 Min	AD6645ASQ-80 Typ	AD6645ASQ-80 Max	AD6645ASQ-105 Min	AD6645ASQ-105 Typ	AD6645ASQ-105 Max	Unit
RESOLUTION				14					Bits
ACCURACY									
No Missing Codes	Full	II		Guaranteed			Guaranteed		
Offset Error	Full	II	–10	+1.2	+10	–10	+1.2	+10	mV
Gain Error	Full	II	–10	0	+10	–10	0	+10	% FS
Differential Nonlinearity (DNL)	Full	II	–1.0	±0.25	+1.5	–1.0	±0.5	+1.5	LSB
Integral Nonlinearity (INL)	Full	V		±0.5			±1.5		LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		1.5			1.5		ppm/°C
Gain Error	Full	V		48			48		ppm/°C
POWER SUPPLY REJECTION (PSRR)	25°C	V		±1.0			±1.0		mV/V
REFERENCE OUT (VREF)[1]	Full	V		2.4			2.4		V
ANALOG INPUTS (AIN, $\overline{AIN}$)									
Differential Input Voltage Range	Full	V		2.2			2.2		V p-p
Differential Input Resistance	Full	V		1			1		kΩ
Differential Input Capacitance	25°C	V		1.5			1.5		pF
POWER SUPPLY									
Supply Voltages									
AV_{CC}	Full	II	4.75	5.0	5.25	4.75	5.0	5.25	V
DV_{CC}	Full	II	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Current									
I AV_{CC} (AV_{CC} = 5.0 V)	Full	II		275	320		275	320	mA
I DV_{CC} (DV_{CC} = 3.3 V)	Full	II		32	45		32	45	mA
Rise Time[2]									
AV_{CC}	Full	IV			250			250	ms
POWER CONSUMPTION	Full	II		1.5	1.75		1.5	1.75	W

NOTES
[1]VREF is provided for setting the common-mode offset of a differential amplifier such as the AD8138 when a dc-coupled analog input is required. VREF should be buffered if used to drive additional circuit functions.
[2]Specified for dc supplies with linear rise time characteristics.
Specifications subject to change without notice

2

DIGITAL SPECIFICATIONS (AV_{CC} = 5 V, DV_{CC} = 3.3 V; T_{MIN} and T_{MAX} at rated speed grade, unless otherwise noted.) 1

Parameter (Conditions)	Temp	Test Level	AD6645ASQ-80 Min	AD6645ASQ-80 Typ	AD6645ASQ-80 Max	AD6645ASQ-105 Min	AD6645ASQ-105 Typ	AD6645ASQ-105 Max	Unit
ENCODE INPUTS (ENC, $\overline{ENC}$)									
Differential Input Voltage[1]	Full	IV	0.4			0.4			V p-p
Differential Input Resistance	25°C	V		10			10		kΩ
Differential Input Capacitance	25°C	V		2.5			2.5		pF
LOGIC OUTPUTS (D13–D0, DRY, OVR[2])									
Logic Compatibility				CMOS			CMOS		
Logic 1 Voltage (DV_{CC} = 3.3 V)[3]	Full	II	2.85	DV_{CC}–2		2.85	DV_{CC}–2		V
Logic 0 Voltage (DV_{CC} = 3.3 V)[3]	Full	II		0.2	0.5		0.2	0.5	V
Output Coding				Twos Complement			Twos Complement		
DMID	Full	V		DV_{CC}/2			DV_{CC}/2		V

NOTES
[1]All ac specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially.
[2]The functionality of the Overrange bit is specified for a temperature range of 25°C to 85°C only.
[3]Digital output logic levels: DV_{CC} = 3.3 V, C_{LOAD} = 10 pF. Capacitive loads >10 pF will degrade performance.
Specifications subject to change without notice.

2

Figure 6.180: *Example Data Sheet Specification Page*

AC SPECIFICATIONS[1] (AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE, $\overline{\text{ENCODE}}$, T_{MIN} and T_{MAX} at rated speed grade, unless otherwise noted.)

Parameter (Conditions)		Temp	Test Level	AD6645ASQ-80 Min	AD6645ASQ-80 Typ	AD6645ASQ-80 Max	AD6645ASQ-105 Min	AD6645ASQ-105 Typ	AD6645ASQ-105 Max	Unit
SNR										
Analog Input	15.5 MHz	25°C	V		75.0			75.0		dB
@ –1 dBFS	30.5 MHz	Full	II	72.5	74.5					dB
	37.7 MHz	25°C	I				72.5	74.5		dB
	70.0 MHz	Full	II	72.0	73.5		72.0	73.5		dB
	150.0 MHz	25°C	V		73.0			73.0		dB
	200.0 MHz	25°C	V		72.0			72.0		dB
SINAD										
Analog Input	15.5 MHz	25°C	V		75.0			75.0		dB
@ –1 dBFS	30.5 MHz	Full	II	72.5	74.5					dB
	37.7 MHz	25°C	I				72.5	74.5		dB
	70.0 MHz	Full	V		73.0			73.0		dB
	150.0 MHz	25°C	V		68.5			67.5		dB
	200.0 MHz	25°C	V		62.5			62.5		dB
WORST HARMONIC (Second or Third)										
Analog Input	15.5 MHz	25°C	V		93.0			93.1		dBc
@ –1 dBFS	30.5 MHz	Full	II	85.0	93.0					dBc
	37.7 MHz	25°C	I				85.0	93.0		dBc
	70.0 MHz	Full	V		89.0			87.0		dBc
	150.0 MHz	25°C	V		70.0			70.0		dBc
	200.0 MHz	25°C	V		63.5			63.5		dBc
WORST HARMONIC (Fourth or Higher)										
Analog Input	15.5 MHz	25°C	V		96.0			96.0		dBc
@ –1 dBFS	30.5 MHz	Full	II	85.0	95.0					dBc
	37.7 MHz	25°C	I				86.0	95.0		dBc
	70.0 MHz	Full	V		90.0			90.0		dBc
	150.0 MHz	25°C	V		90.0			90.0		dBc
	200.0 MHz	25°C	V		88.0			88.0		dBc
TWO TONE SFDR @30.5 MHz[2, 3]		25°C	V		100			98.0		dBFS
	55.0 MHz[2, 4]	25°C	V		100			98.0		dBFS
	70.0 MHz[2, 5]	25°C	V					98.0		dBFS
TWO TONE IMD REJECTION[3, 4]										
F1, F2 @ –7 dBFS		25°C	V		90			90		dBc
ANALOG INPUT BANDWIDTH		25°C	V		270			270		MHz

NOTES
[1]All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially.
[2]Analog input signal power swept from –10 dBFS to –100 dBFS.
[3]F1 = 30.5 MHz, F2 = 31.5 MHz.
[4]F1 = 55.25 MHz, F2 = 56.25 MHz.
[5]F1 = 69.1 MHz, F2 = 71.1 MHz.

Specifications subject to change without notice.

Figure 6.181: *Typical AC Specifications*

SWITCHING SPECIFICATIONS (AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE, $\overline{ENCODE}$, T_{MIN} and T_{MAX} at rated speed grade, unless otherwise noted.)

Parameter (Conditions)	Temp	Test Level	AD6645ASQ-80 Min	AD6645ASQ-80 Typ	AD6645ASQ-80 Max	AD6645ASQ-105 Min	AD6645ASQ-105 Typ	AD6645ASQ-105 Max	Unit
Maximum Conversion Rate	Full	II	80			105			MSPS
Minimum Conversion Rate	Full	IV			30				MSPS
ENCODE Pulsewidth High (t_{ENCH})*	Full	IV	5.625			4.286		30	ns
ENCODE Pulsewidth Low (t_{ENCL})*	Full	IV	5.625			4.286			ns

*Several timing parameters are a function of t_{ENCL} and t_{ENCH}.
Specifications subject to change without notice.

AD6645

SWITCHING SPECIFICATIONS (continued) (AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE, $\overline{ENCODE}$, T_{MIN} and T_{MAX} at rated speed grade, C_{LOAD} = 10 pF, unless otherwise noted.)

Parameter (Conditions)	Name	Temp	Test Level	AD6645ASQ-80 Min	AD6645ASQ-80 Typ	AD6645ASQ-80 Max	AD6645ASQ-105 Min	AD6645ASQ-105 Typ	AD6645ASQ-105 Max	Unit
ENCODE Input Parameters[1]										
Encode Period[1]	t_{ENC}	Full	V		12.5			9.5		ns
Encode Pulsewidth High[2]	t_{ENCH}	Full	V		6.25			4.75		ns
Encode Pulsewidth Low	t_{ENCL}	Full	V		6.25			4.75		ns
ENCODE/DataReady										
Encode Rising to DataReady Falling	t_{DR}	Full	V	1.0	2.0	3.1	1.0	2.0	3.1	ns
Encode Rising to DataReady Rising	t_{E_DR}	Full	V		$t_{ENCH} + t_{DR}$			$t_{ENCH} + t_{DR}$		ns
(50% Duty Cycle)		Full	V	7.3	8.3	9.4	5.7	6.75	7.9	ns
ENCODE/DATA (D13:0), OVR										
ENC to DATA Falling Low	t_{E_FL}	Full	V	2.4	4.7	7.0	2.4	4.7	7.0	ns
ENC to DATA Rising Low	t_{E_RL}	Full	V	1.4	3.0	4.7	1.4	3.0	4.7	ns
ENCODE to DATA Delay (Hold Time)	t_{H_E}	Full	V	1.4	3.0	4.7	1.4	3.0	4.7	ns
ENCODE to DATA Delay (Setup Time)	t_{S_E}	Full	V	$t_{ENC} - t_{E\_FL(max)}$			$t_{ENC} - t_{E\_FL(max)}$			ns
					$t_{ENC} - t_{E\_FL(typ)}$			$t_{ENC} - t_{E\_FL(typ)}$		ns
						$t_{ENC} - t_{E\_FL(min)}$			$t_{ENC} - t_{E\_FL(min)}$	ns
(50% Duty Cycle)		Full	V	5.3	7.6	10.0	2.3	4.8	7.0	ns
DataReady (DRY[3])/DATA, OVR										
DataReady to DATA Delay (Hold Time)	t_{H_DR}	Full	V		Note 4			Note 4		
(50% Duty Cycle)				6.6	7.2	7.9	5.1	5.7	6.4	ns
DataReady to DATA Delay (Setup Time)	t_{S_DR}	Full	V		Note 4			Note 4		
(50% Duty Cycle)				2.1	3.6	5.1	0.6	2.1	3.5	ns
APERTURE DELAY	t_A	25°C	V		–500			–500		ps
APERTURE UNCERTAINTY (Jitter)	t_J	25°C	V		0.1		0.1			ps rms

NOTES
[1]Several timing parameters are a function of t_{ENC} and t_{ENCH}.
[2]ENCODE TO DATA Delay (Hold Time) is the absolute minimum propagation delay through the analog-to-digital converter, $t_{E\_RL} = t_{H\_E}$.
[3]DRY is an inverted and delayed version of the encode clock. Any change in the duty cycle of the clock will correspondingly change the duty cycle of DRY.
[4]DataReady to DATA Delay (t_{H_DR} and t_{S_DR}) is calculated relative to rated speed grade and is dependent on t_{ENC} and duty cycle.
Specifications subject to change without notice.

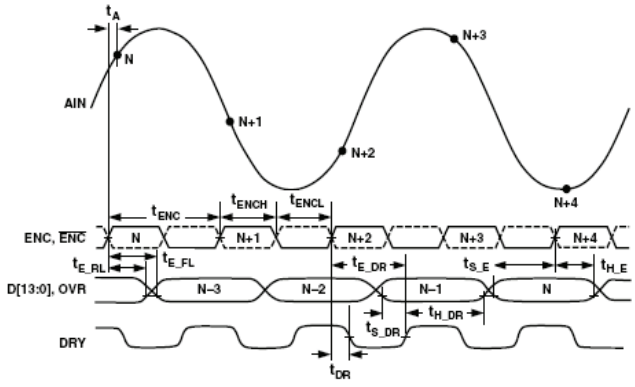


Figure 1. Timing Diagram

Figure 6.182: *Typical Timing Specification page*

DIGITAL SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS				
Logic "1" Voltage	2.1	3		V
Logic "0" Voltage		0	0.9	V
Logic "1" Current	–10		+10	µA
Logic "0" Current	–10		+10	µA
Input Capacitance		5		pF
CLOCK INPUTS				
Input Voltage Range	0		3	V
Common-Mode Voltage	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		V

Specifications subject to change without notice.

Parameter	Min	Typ	Max	Unit
SERIAL CONTROL BUS				
Maximum SCLK Frequency (f_{SLCK})	15			MHz
Mimimum Clock Pulsewidth High (t_{PWH})	30			ns
Mimimum Clock Pulsewidth Low (t_{PWL})	30			ns
Maximum Clock Rise/Fall Time			1	ms
Minimum Data/Chip Select Setup Time (t_{DS})	25			ns
Minimum Data Hold Time (t_{DH})	0			ns
Maximum Data Valid Time (t_{DV})			30	ns
RESET Pulsewidth	1.5			ns
Inputs (SDI, SDIO, SCLK, CSB)				
Logic "1" Voltage	2.1	3		V
Logic "0" Voltage		0	0.9	V
Logic "1" Current	–10		+10	µA
Logic "0" Current	–10		+10	µA
Input Capacitance		5		pF
SDIO Output				
Logic "1" Voltage	DRVDD–0.6			V
Logic "0" Voltage			0.4	V
Logic "1" Current	30	50		mA
Logic "0" Current	30	50		mA

Figure 6.183: *Typical Timing Specification page 2*

AD9777

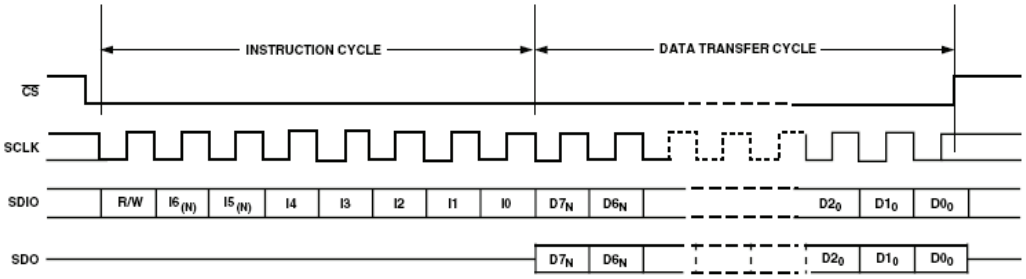


Figure 3a. Serial Register Interface Timing MSB First

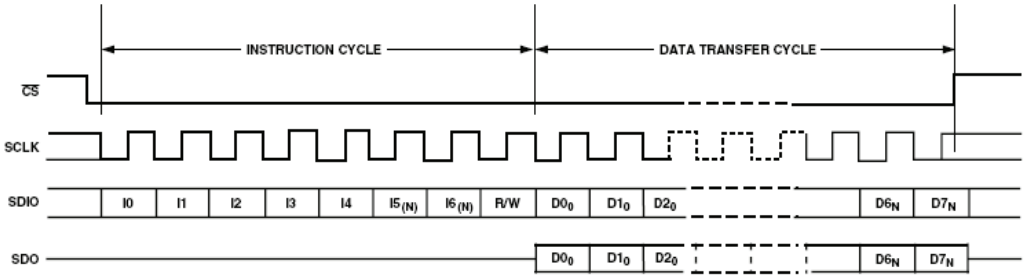


Figure 3b. Serial Register Interface Timing LSB First

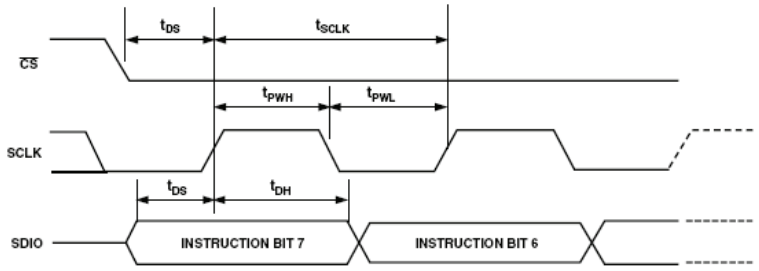


Figure 4. Timing Diagram for Register Write to AD9777

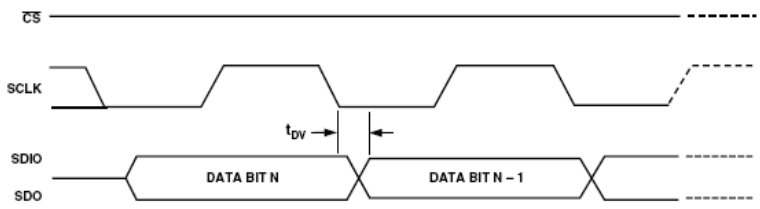


Figure 5. Timing Diagram for Register Read from AD9777

Figure 6.184: *Typical Timing Specifications page 3*

Note that there are typically 3 possibilities for the specifications, Min, Typ, and Max. See Figure 6.180 (3). At Analog Devices any specification in the min (minimum) and max (maximum) columns will be guaranteed by test. This can be a direct test, or, in some instances, testing one parameter will guarantee another. A typ (typical) specification is just that, typical. Depending on the particular specification, the deviation from the typical can be substantial. And you have no way of knowing what the range of variation on the typ specification is. Sometimes you will find a typ and a min (or max) for the same specification. This tells you that although the test limits are at a particular level (min or max) the typicals tend to run much better than the test limits. For example, in the data sheet example in Figure 6.180, the gain error is guaranteed to be ±10% (full-scale), but the error is typically 0 % (FS). When designing, using typs is risky. You are much better off using mins or maxes for error budget analysis.

Testing is one of the most expensive steps in the manufacturing of integrated circuits. Therefore a more highly specified part will typically cost more than a less completely specified part. But, in your system, the higher specified part may be required to guarantee the circuit performance.

As can be seen from the examples in Figures 6.179 to 6.182, the example used (in this case the AD6645) is specified for both dc and ac, as explain in the earlier section on converter specifications. Note that the dc specifications are in terms of absolute levels (volts, amps, etc.) while the ac specifications tend to be in terms of dB.

Also note in Figure 6.181 that the digital signal levels are also specified in terms of voltage levels. They are also specified in terms of time. These are the "switching specifications" of Figure 6.182. These specifications are for individual signals (rise and fall times, pulse width high, etc.) as well as between signals (setup and hold times, etc.).

The Absolute Maximums

There is always a section (usually just after the specification tables) with the absolute maximum ratings. These are typically voltage and temperature related.

The process used to fabricate the op amp will typically determine the maximum supply voltage. Maximum input voltages typically are limited to the supply voltages. It should be pointed out that the supply voltage is the instantaneous value, not the average, or ultimate value. So if a converter has voltages on its input but the supply voltage is not present, which could occur during power up when one section of the system is powered but others aren't, the converter is overvoltaged, even if when the converter power is applied, everything is within operational limits.

The overriding concern for semiconductor reliability is to keep the junction temperature below 150°C. There will be a θ_{ja} given for the various package options. This is the thermal resistance from the junction to free air. The units are °C/Watt. To use this information simply determine the dissipation of the package. This would be the quiescent current times the supply voltage. Then take the maximum dissipation generated by the

output stages (output current times the difference between the output voltage and the supply voltage). Add these together and you will have the total package dissipation, in watts. Multiply the thermal resistance by the dissipation and you have the temperature rise. You start with the ambient temperature (in °C, typically taken to be 25°C), take the rise calculated above and that will give you the junction temperature. Remember that the ambient temperature should be in operation. Circuits packaged in an enclosure, which is in turn placed in a rack with other equipment will have an internal ambient temperature that could be significantly above the air temperature in the room that it is located in. This must be considered.

The thermal resistance has two components θ_{jc} and θ_{ca}. θ_{jc} is the thermal resistance from the junction to the case. There is not much you can to about that. θ_{ca} is the thermal resistance from the case to the air. This we can effect relatively easily by adding a heat sink. The thermal resistance add linearly. Also note that these values are in free air. Moving air allows more cooling, especially with a heat sink.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to AGND, AGNDS, DGND	−0.3 V, +17 V
V_{SS} to AGND, AGNDS, DGND	+0.3 V, −17 V
AGND, AGNDS to DGND	−0.3 V to +0.3 V
REFGND to AGND, ADNDS	V_{SS} − 0.3 V to V_{DD} + 0.3 V
REFIN to AGND, AGNDS	V_{SS} − 0.3 V to V_{DD} + 0.3 V
REFIN to REFGND	−0.3 V to +17 V
Digital Inputs to DGND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND, AGNDS	−0.3 V to V_{DD} + 0.3 V
SDO to DGND	−0.3 V to +6.5 V
Operating Temperature Range:	−40°C to +125°C
W, Y Grades	−40°C to +125°C
A, B Grades	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (T_J Max)	150°C
16-Lead SSOP Package	
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	139°C/W
Lead Temperature (Soldering 10 s)	300°C
IR Reflow, Peak Temperature	230°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6.185: *Typical Absolute Maximum Ratings*

The Ordering Guide

Many converters are available in multiple packages and/or multiple temperature ranges. Each of the various combinations of package and temperature range requires a unique part number. This is spelled out in the ordering guide. See Figures 6.186 to 6.187.

Just as a note, in the case of general purpose ADCs and DACs, the commercial (0°C to 70°C) temperature range has mainly become obsolete. The reason for this is that most circuits yield to the industrial temperature range. It is less expensive to support less part types. Each discrete part number requires a separate test program, separate inventorying and other supporting documentation. The exception to this rule is for parts designed for a specific application which is, by definition, commercial. An example of this is consumer applications, such as audio. Wider temperature range for these parts offer no advantage.

The industrial temperature range can also mean different things. The standard industrial temperature range is −40°C to 85°C. A common variant on this is what is commonly called the automotive temperature range −55°C to 85°C. 0°C to 100°C is also common.

The military temperature range is −55°C to 125°C.

ORDERING GUIDE

Model	Maximum INL	No Missing Code	Temperature Range	Package Description	Package Option	Brand
AD7684ARM	±6 LSB	15bits	−40°C to +85°C	µSOIC-8	RM-8	C1M
AD7684ARMRL7	±6 LSB	15bits	−40°C to +85°C	µSOIC-8	RM-8 (reel)	C1M
AD7684BRM	±3 LSB	16bits	−40°C to +85°C	µSOIC-8	RM-8	C1D
AD7684BRMRL7	±3 LSB	16bits	−40°C to +85°C	µSOIC-8	RM-8 (reel)	C1D
EVAL-AD7684CB[1]				Evaluation Board		
EVAL-CONTROL BRD2[2]				Controller Board		
EVAL-CONTROL BRD3[2]				Controller Board		

NOTES
[1]This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRDx for evaluation/demonstration purposes.
[2]These boards allow a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

Figure 6.186: *Ordering Guide Example 1 (for the AD7684)*

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5570ARS	–40 °C to +85 °C	16-Lead SSOP	RS-16
AD5570ARS-REEL	–40 °C to +85 °C	16-Lead SSOP	RS-16
AD5570ARS-REEL7	–40 °C to +85 °C	16-Lead SSOP	RS-16
AD5570BRS	–40 °C to +85 °C	16-Lead SSOP	RS-16
AD5570BRS-REEL	–40 °C to +85 °C	16-Lead SSOP	RS-16
AD5570BRS-REEL7	–40 °C to +85 °C	16-Lead SSOP	RS-16
AD5570WRS	–40 °C to +125 °C	16-Lead SSOP	RS-16
AD5570WRS-REEL	–40 °C to +125 °C	16-Lead SSOP	RS-16
AD5570WRS-REEL7	–40 °C to +125 °C	16-Lead SSOP	RS-16
AD5570YRS	–40 °C to +125 °C	16-Lead SSOP	RS-16
AD5570YRS-REEL	–40 °C to +125 °C	16-Lead SSOP	RS-16
AD5570YRS-REEL7	–40 °C to +125 °C	16-Lead SSOP	RS-16
Eval-AD5570EB		Evaluation Board	

Figure 6.187: *Ordering Guides Example 2 (for the AD5570)*

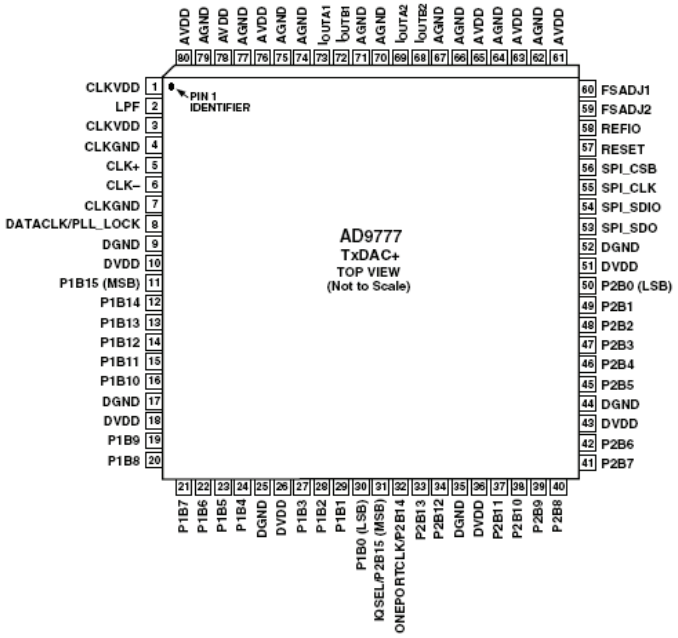
The “brand” column of the ordering guide is the package marking for small packages. The markings that are customary on the DIP package will not physically fit on the much smaller surface mount packages. For instance, DIP packages would typically include the part number, date code (when the IC was “made,” typically when it passes final test) and occasionally some other information. Obviously, the space available for marking on surface mount packages is very much limited. So the 3 character code is used instead.

Pin Description

In the pin description, information on the pin function, including optional functionality for multipurpose pins are described. Often the descriptions are expanded upon in the main body of the data sheet.

AD9777

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Description
1, 3	CLKVDD	Clock Supply Voltage
2	LPF	PLL Loop Filter
4, 7	CLKGND	Clock Supply Common
5	CLK+	Differential Clock Input
6	CLK–	Differential Clock Input
8	DATACLK/PLL_LOCK	With the PLL enabled, this pin indicates the state of the PLL. A read of a Logic "1" indicates the PLL is in the locked state. Logic "0" indicates the PLL has not achieved lock. This pin may also be programmed to act as either an input or output (Address 02h, Bit 3) DATACLK signal running at the input data rate.
9, 17, 25, 35, 44, 52	DGND	Digital Common
10, 18, 26, 36, 43, 51	DVDD	Digital Supply Voltage
11–16, 19–24, 27–30	P1B15 (MSB) to P1B0 (LSB)	Port 1 Data Inputs
31	IQSEL/P2B15 (MSB)	In one port mode, IQSEL = 1 followed by a rising edge of the differential input clock will latch the data into the I channel input register. IQSEL = 0 will latch the data into the Q channel input register. In two port mode, this pin becomes the Port 2 MSB.
32	ONEPORTCLK/P2B14	With the PLL disabled and the AD9777 in one port mode, this pin becomes a clock output that runs at twice the input data rate of the I and Q channels. This allows the AD9777 to accept and demux interleaved I and Q data to the I and Q input registers.
33, 34, 37–42, 45–50	P2B13 to P2B0 (LSB)	Port 2 Data Inputs

Figure 6.188A: *Typical Pin Description*

AD9777

PIN FUNCTION DESCRIPTIONS (continued)

Pin Number	Mnemonic	Description
53	SPI_SDO	In the case where SDIO is an input, SDO acts as an output. When SDIO becomes an output, SDO enters a High-Z state. This pin can also be used as an output for the data rate clock. For more information, see the Two Port Data Input Mode section.
54	SPI_SDIO	Bidirectional Data Pin. Data direction is controlled by Bit 7 of Register Address 00h. The default setting for this bit is "0," which sets SDIO as an input.
55	SPI_CLK	Data input to the SPI port is registered on the rising edge of SPI_CLK. Data output on the SPI port is registered on the falling edge.
56	SPI_CSB	Chip Select/SPI Data Synchronization. On momentary logic high, resets SPI port logic and initializes instruction cycle.
57	RESET	Logic "1" resets all of the SPI port registers, including Address 00h, to their default values. A software reset can also be done by writing a Logic "1" to SPI Register 00h, Bit 5. However, the software reset has no effect on the bits in Address 00h.
58	REFIO	Reference Output, 1.2 V Nominal
59	FSADJ2	Full-Scale Current Adjust, Q Channel
60	FSADJ1	Full-Scale Current Adjust, I Channel
61, 63, 65, 76, 78, 80	AVDD	Analog Supply Voltage
62, 64, 66, 67, 70, 71, 74, 75, 77, 79	AGND	Analog Common
69, 68	I_{OUTA2}, I_{OUTB2}	Differential DAC Current Outputs, Q Channel
73, 72	I_{OUTA1}, I_{OUTB1}	Differential DAC Current Outputs, I Channel

Figure 6.188B: *Typical Pin Description (cont.)*

Defining the Specifications

This section contains a brief description of the specifications. It is, in effect, a subset of the earlier section where we defined the converter specifications. The definitions will be more compact and only those specifications that apply to the particular converter will be defined.

Also in this area specialized specifications will be defined. An example of this might be differential gain and differential phase, which are definitions specific to the video industry.

Equivalent Circuits

Driving the inputs of a converter, especially at high frequencies, is not a trivial task. Loading of an output pin can also be equally as challenging. Knowing the architecture of circuit connected to that pin may be of assistance in understanding how to interface that pin.

Things that might be of interest for an input pin is the input impedance, so that the source impedance can be matched, for instance, and the dc level biasing the pin. Normally this bias is at half the supply voltage (assuming single-supply operation), but this is not always the case.

AD6645

EQUIVALENT CIRCUITS

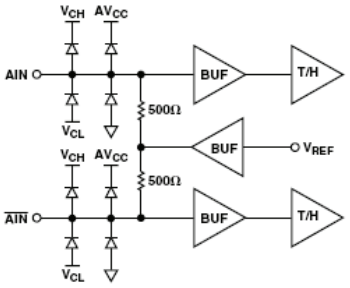


Figure 2. Analog Input Stage

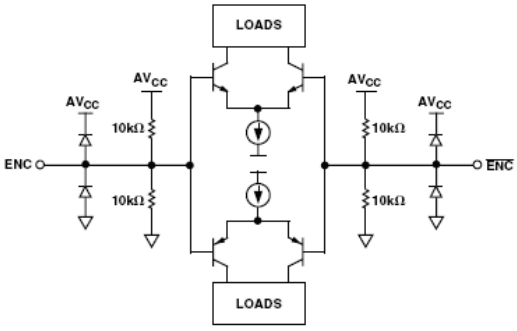


Figure 3. Encode Inputs

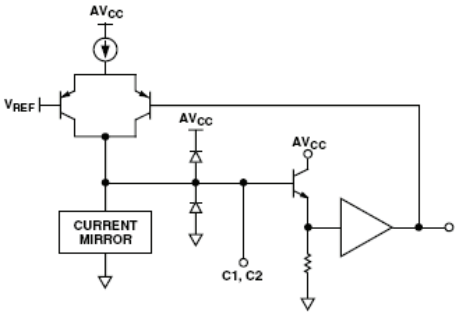


Figure 4. Compensation Pin, C1 or C2

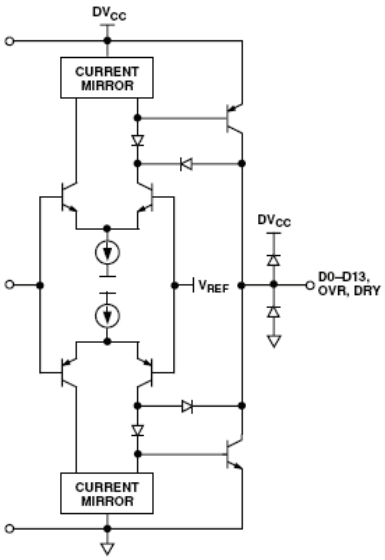


Figure 5. Digital Output Stage

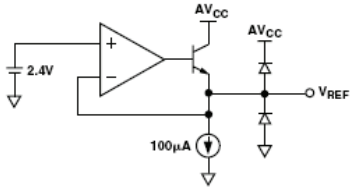


Figure 6. 2.4 V Reference

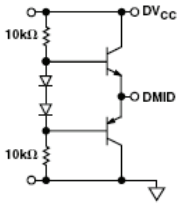


Figure 7. DMID Reference

Figure 6.189: *Typical Equivalent pin circuits*

The Graphs

Many parameters vary over the operational range of the converter. An example is the variation of spurious free dynamic range (SFDR) with frequency. See Figures 6.190 to 6.193. So to completely specify the SFDR of a part there would be a specification at particular input frequency, which typically would appear in the specification table, and graphs showing variation with input frequency, sampling rate, and level.

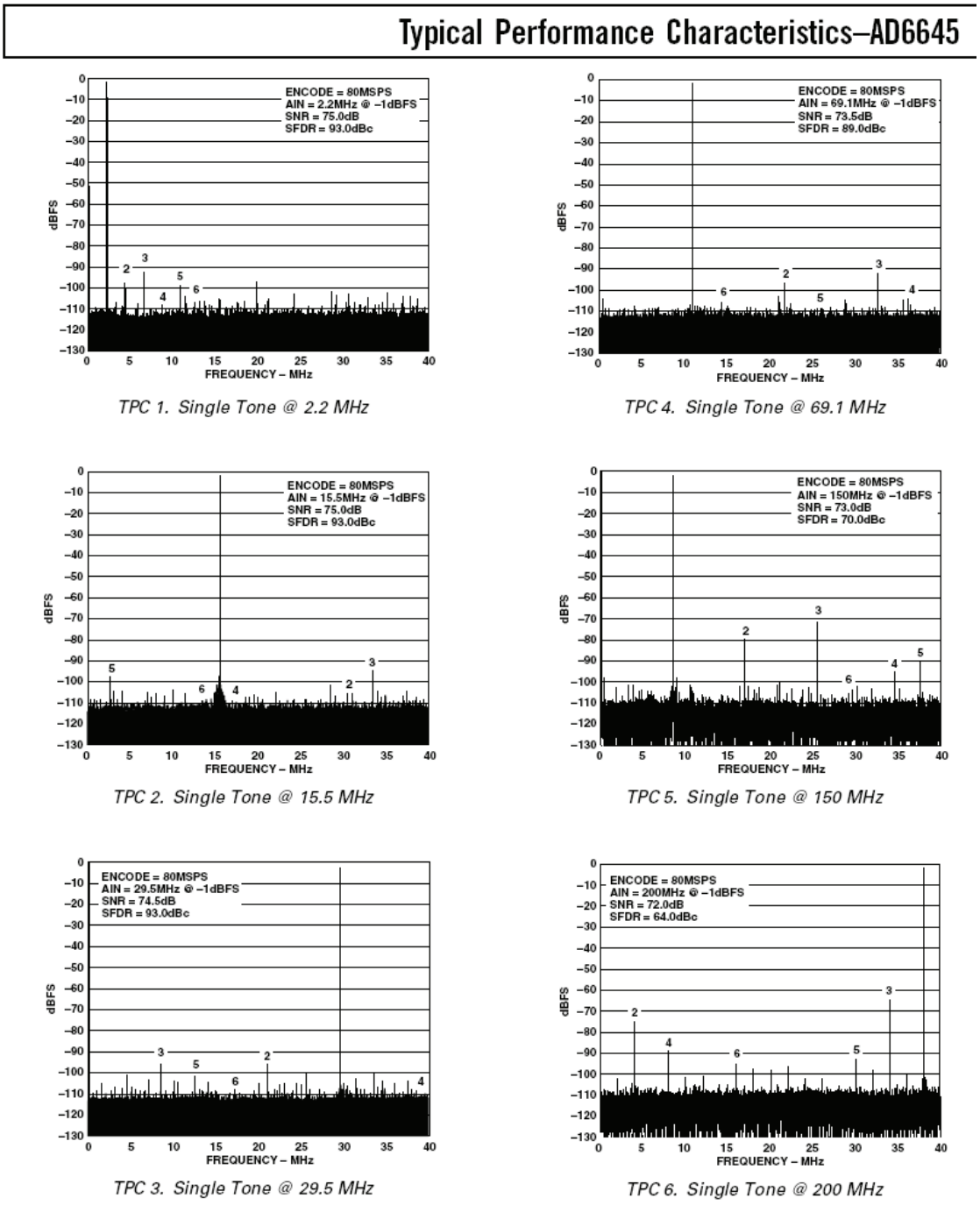
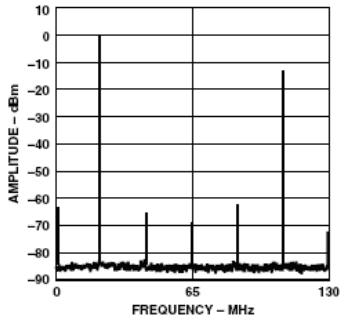


Figure 6.190: Typical performance graphs

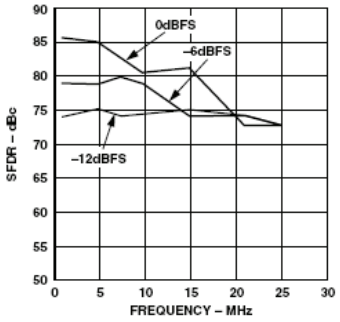
The information presented in the graphs is not uniform from vendor to vendor or even from part to part from the same manufacturer. Higher performance parts tend to be more completely specified. For the most part the graphs should be considered typical values.

Typical Performance Characteristics– AD9777

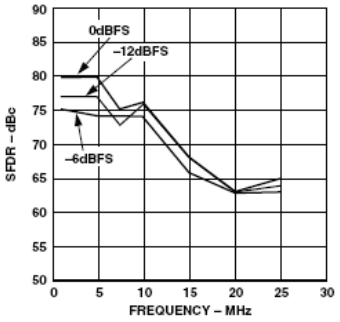
(T = 25°C, AVDD = 3.3 V, CLKVDD = 3.3 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, Interpolation = 2×, Differential Transformer-Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted.)



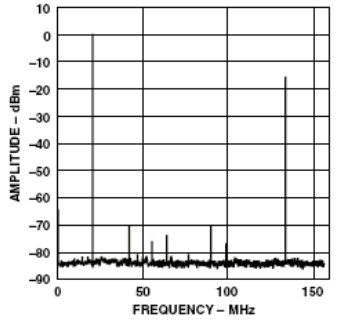
TPC 1. Single-Tone Spectrum @ f_{DATA} = 65 MSPS with $f_{OUT} = f_{DATA}/3$



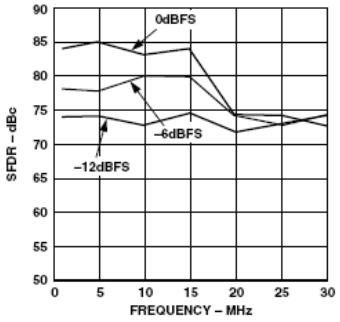
TPC 2. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 65 MSPS



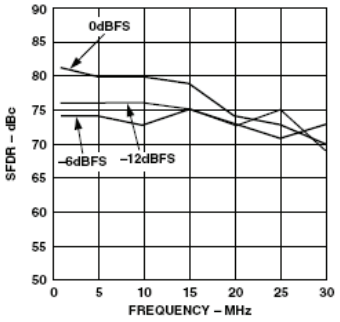
TPC 3. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 65 MSPS



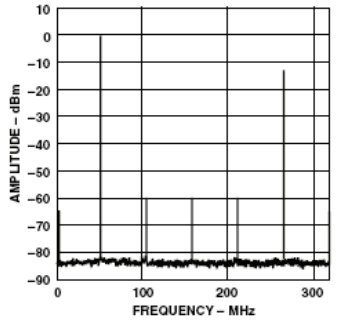
TPC 4. Single-Tone Spectrum @ f_{DATA} = 78 MSPS with $f_{OUT} = f_{DATA}/3$



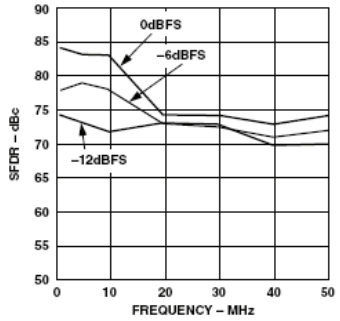
TPC 5. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 78 MSPS



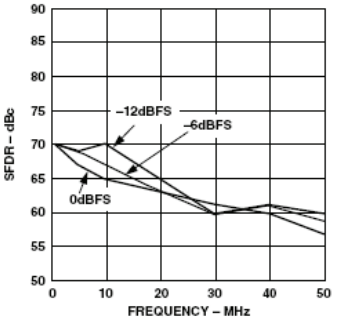
TPC 6. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 78 MSPS



TPC 7. Single-Tone Spectrum @ f_{DATA} = 160 MSPS with $f_{OUT} = f_{DATA}/3$



TPC 8. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 160 MSPS



TPC 9. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 160 MSPS

Figure 6.191: *Typical performance graphs page 2*

AD7678

TYPICAL PERFORMANCE CHARACTERISTICS

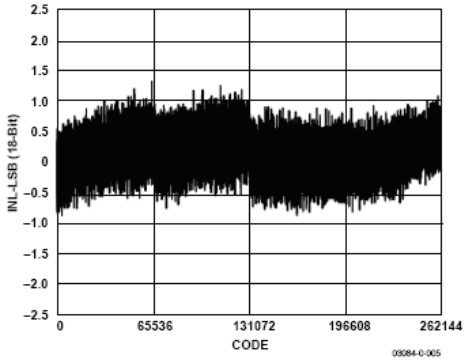


Figure 5. Integral Nonlinearity vs. Code

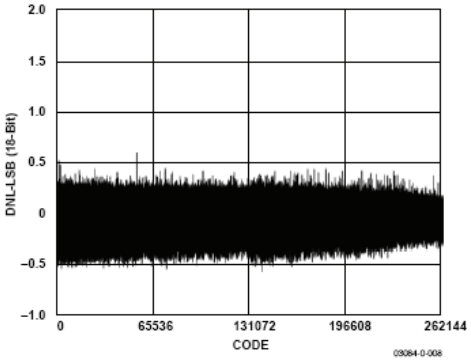


Figure 8. Differential Nonlinearity vs. Code

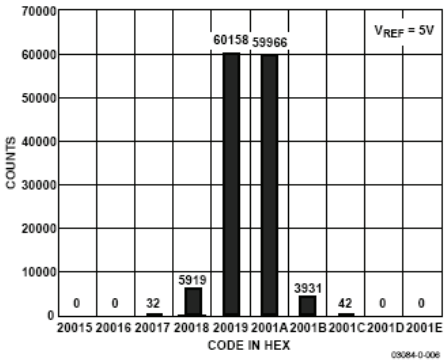


Figure 6. Histogram of 131,072 Conversions of a DC Input at the Code Transition

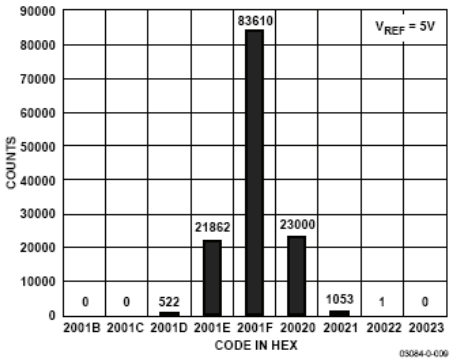


Figure 9. Histogram of 131,072 Conversions of a DC Input at the Code Center

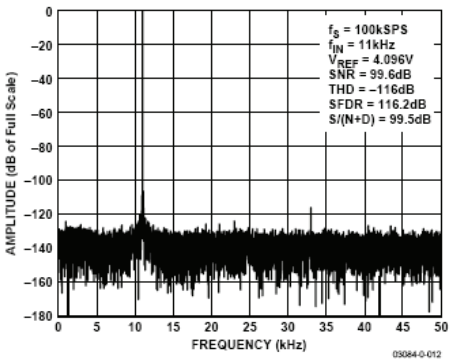


Figure 7. FFT (11 kHz Tone)

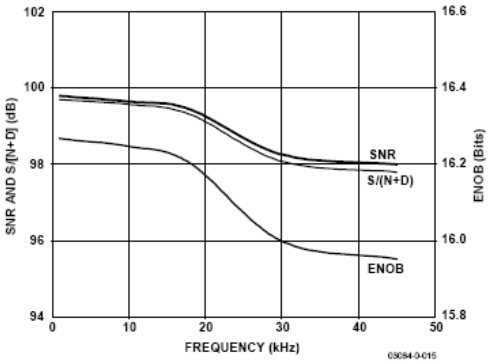


Figure 10. SNR, S/(N+D), and ENOB vs. Frequency

Figure 6.192: *Typical performance graphs page 3*

AD5570

TYPICAL PERFORMANCE CHARACTERISTICS

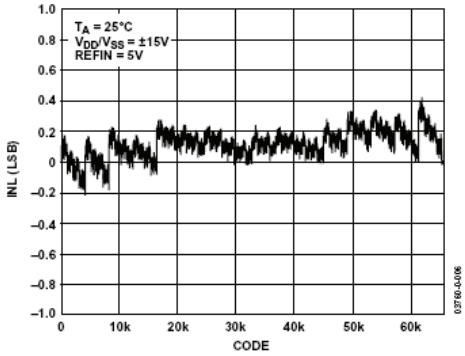


Figure 6. Integral Nonlinearity vs. Code, V_{DD}/V_{SS} = ±15 V

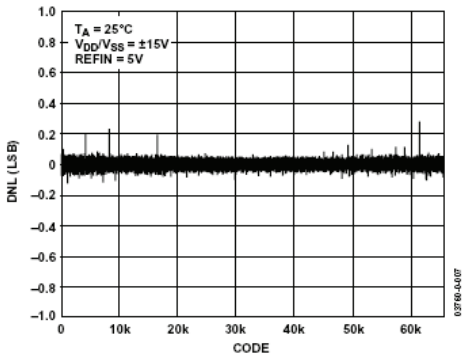


Figure 7. Differential Nonlinearity vs. Code, V_{DD}/V_{SS} = ±15 V

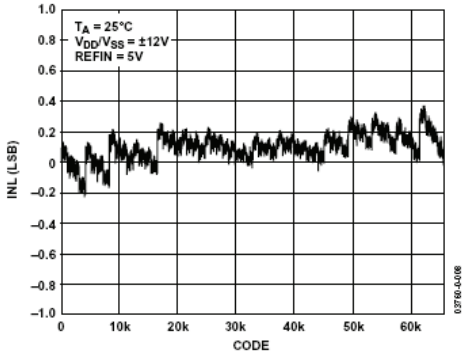


Figure 8. Integral Nonlinearity vs. Code, V_{DD}/V_{SS} = ±12 V

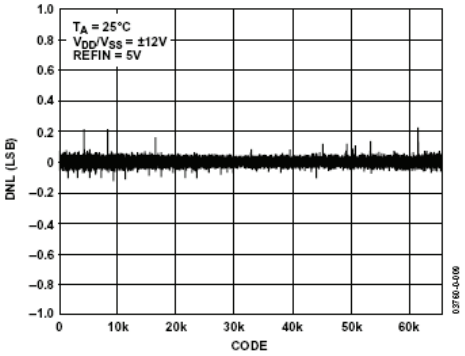


Figure 9. Differential Nonlinearity vs. Code, V_{DD}/V_{SS} = ±12 V

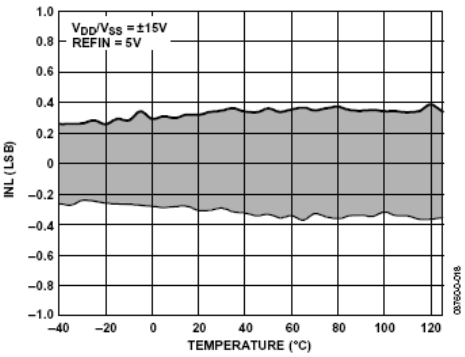


Figure 10. Integral Nonlinearity vs. Temperature, ±15 V Supplies

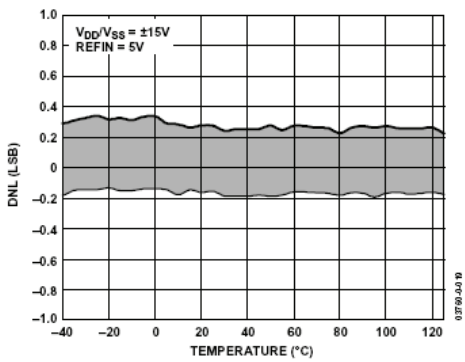


Figure 11. Differential Nonlinearity vs. Temperature, ±15 V Supplies

Figure 6.193: *Typical performance graphs page 4*

The Main Body

The main body of the data sheet contains detailed information on operations and applications of the converter. Early on at Analog Devices, it was determined that just giving someone an amplifier and letting them go off on their own to try to build whatever it is that they want to build was not the best approach. Therefore, Analog Devices includes application information with the data sheet.

Circuit Description

Typically the first part of the main body of the data sheet is the circuit description. Since the topology of the converter can determine the applicability of a particular converter in a particular design, understanding the internal operation of the converter can be very helpful. This is especially true when an understanding of the input structure of a converter may be helpful in designing the driver circuit.

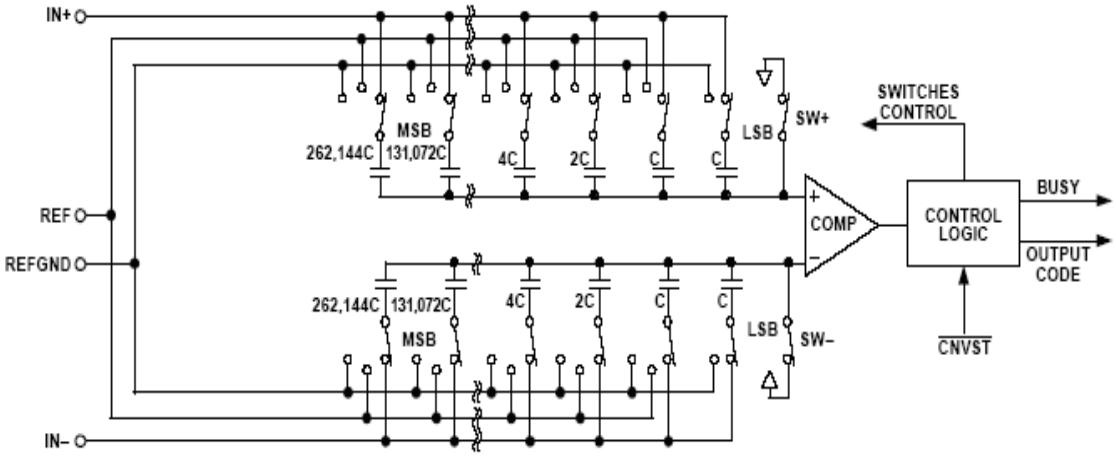


Figure 6.194: *Typical circuit diagram*

Many converters, such as the AD9777 and the AD7730 that we are using as examples in this section, are really more than just converters. They are more exactly subsystems, containing both converters and support circuitry. The operation of all of the subsections of these circuits is described.

As we said previously, driving an ADC input is not trivial at high speeds. Understanding the input configuration is essential. The same is true for the data outputs. On the DAC side the interface issues are reversed (data in/signal out), but just as important.

Interface

To use a converter we have to get the data into or out of it. There are basically two different ways to accomplish this, parallel and serial.

The parallel interface is relatively straightforward. The only timing issues that may have to be considered are set up and hold times. Obviously, with the advent of low supply voltages, signal levels of the digital interface need to be observed.

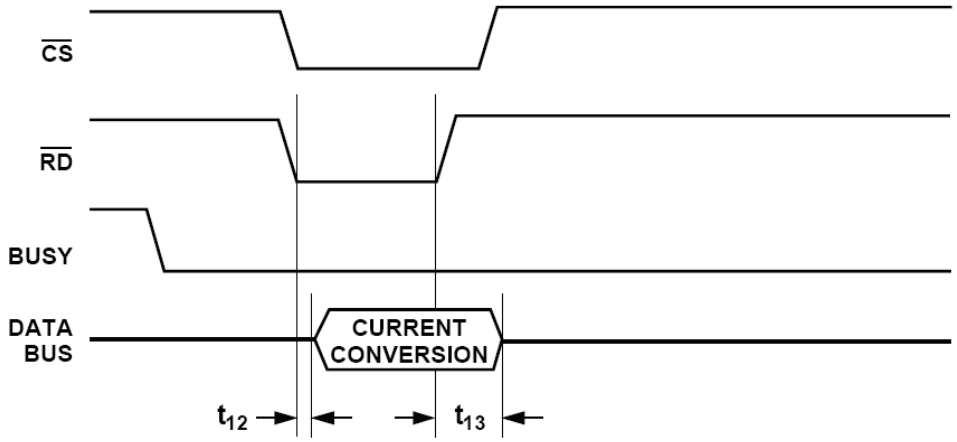


Figure 6.195: *Typical parallel interface timing diagram*

In the case of the AD7678, which is an 18-bit converter, there may be an issue interfacing with a 16 bit (or 8 bit) microprocessor bus. The output register logic is flexible enough to allow the 18-bit word to interface to these narrower data busses. See Figure 6.196.

Table 7. Data Bus Interface Definitions

MODE	MODE1	MODE0	D0/OB/$\overline{2C}$	D1/A0	D2/A1	D[3]	D[4:9]	D[10:11]	D[12:15]	D[16:17]	Description
0	0	0	R[0]	R[1]	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	18-Bit Parallel
1	0	1	OB/$\overline{2C}$	A0:0	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	16-Bit High Word
1	0	1	OB/$\overline{2C}$	A0:1	R[0]	R[1]	All Zeros				16-Bit Low Word
2	1	0	OB/$\overline{2C}$	A0:0	A1:0	All Hi-Z		R[10:11]	R[12:15]	R[16:17]	8-Bit HIGH Byte
2	1	0	OB/$\overline{2C}$	A0:0	A1:1	All Hi-Z		R[2:3]	R[4:7]	R[8:9]	8-Bit MID Byte
2	1	0	OB/$\overline{2C}$	A0:1	A1:0	All Hi-Z		R[0:1]	All Zeros		8-Bit LOW Byte
2	1	0	OB/$\overline{2C}$	A0:1	A1:1	All Hi-Z		All Zeros		R[0:1]	8-Bit LOW Byte
3	1	1	OB/$\overline{2C}$	All Hi-Z		Serial Interface					Serial Interface

R[0:17] is the 18-bit ADC value stored in its output register.

Figure 6.196: *Data bus interface example*

The case of serial interface is typically a bit more complicated. Many times the serial interface conforms to a certain interface standard. You will see that many of the serial interface converters conform to the SPI, QSPI®, MICROWIRE, or I^2C standards.

For the serial interface the converter could act as a master or a slave. The differentiation is determined by who generates the timing clock. The master typically generates the clock.

The width of the serial clock is variable. The data can be MSB first or LSB first. The time slots that line up with the data bits must be defined. Since there are multiple possibilities, each must be defined.

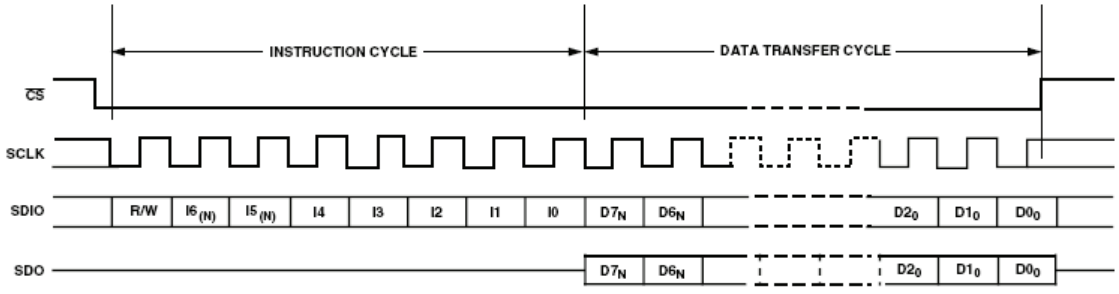


Figure 3a. Serial Register Interface Timing MSB First

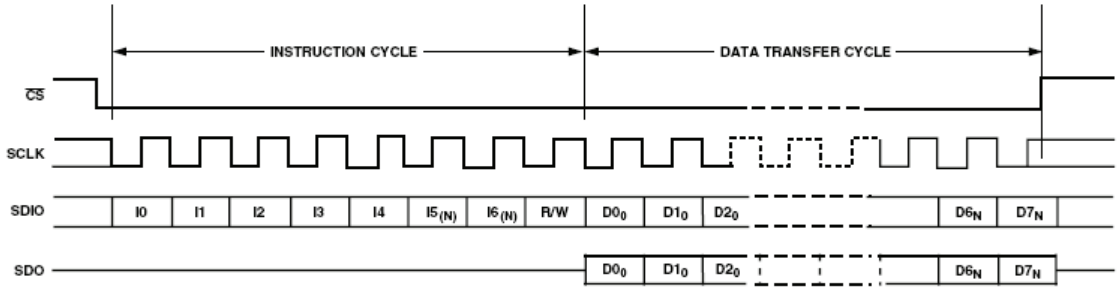


Figure 3b. Serial Register Interface Timing LSB First

Figure 6.197: *Typical DAC serial timing diagram*

Register Description

Many converters have multiple operational modes. Some have on board circuitry, such as a multiplexer or programmable amplifier (PGA) that must be configured. This requires writing to control registers. Each bit in each word must be defined.

AD7730/AD7730L

Communications Register (RS2–RS0 = 0, 0, 0)
The Communications Register is an 8-bit write-only register. All communications to the part must start with a write operation to the Communications Register. The data written to the Communications Register determines whether the next operation is a read or write operation, the type of read operation, and to which register this operation takes place. For single-shot read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications Register. This is the default state of the interface, and on power-up or after a $\overline{\text{RESET}}$, the AD7730 is in this default state waiting for a write operation to the Communications Register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high, returns the AD7730 to this default state by resetting the part. Table VI outlines the bit designations for the Communications Register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the Communications Register. CR7 denotes the first bit of the data stream.

Table VI. Communications Register

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$	ZERO	RW1	RW0	ZERO	RS2	RS1	RS0

Bit Location	Bit Mnemonic	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so the write operation to the Communications Register actually takes place. If a 1 is written to this bit, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits will be loaded to the Communications Register.
CR6	ZERO	A zero **must** be written to this bit to ensure correct operation of the AD7730.
CR5, CR4	RW1, RW0	Read/Write Mode Bits. These two bits determine the nature of the subsequent read/write operation. Table VII outlines the four options.

Table VII. Read/Write Mode

RW1	RW0	Read/Write Mode
0	0	Single Write to Specified Register
0	1	Single Read of Specified Register
1	0	Start Continuous Read of Specified Register
1	1	Stop Continuous Read Mode

With 0, 0 written to these two bits, the next operation is a write operation to the register specified by bits RS2, RS1, RS0. Once the subsequent write operation to the specified register has been completed, the part returns to where it is expecting a write operation to the Communications Register.

With 0,1 written to these two bits, the next operation is a read operation of the register specified by bits RS2, RS1, RS0. Once the subsequent read operation to the specified register has been completed, the part returns to where it is expecting a write operation to the Communications Register.

Writing 1,0 to these bits, sets the part into a mode of continuous reads from the register specified by bits RS2, RS1, RS0. The most likely registers with which the user will want to use this function are the Data Register and the Status Register. Subsequent operations to the part will consist of read operations to the specified register without any intermediate writes to the Communications Register. This means that once the next read operation to the specified register has taken place, the part will be in a mode where it is expecting another read from that specified register. The part will remain in this continuous read mode until 30 Hex has been written to the Communications Register.

When 1,1 is written to these bits (and 0 written to bits CR3 through CR0), the continuous read mode is stopped and the part returns to where it is expecting a write operation to the Communications Register. Note, the part continues to look at the DIN line on each SCLK edge during continuous read mode to determine when to stop the continuous read mode. Therefore, the user must be careful not to inadvertently exit the continuous read mode or reset the AD7730 by writing a series of 1s to the part. The easiest way to avoid this is to place a logic 0 on the DIN line while the part is in continuous read mode. Once the part is in continuous read mode, the user should ensure that an integer multiple of 8 serial clocks should have taken place before attempting to take the part out of continuous read mode.

Figure 6.198: *Typical register description (partial)*

Application Circuits

Often some typical application circuits are provided to assist in applying the converters.

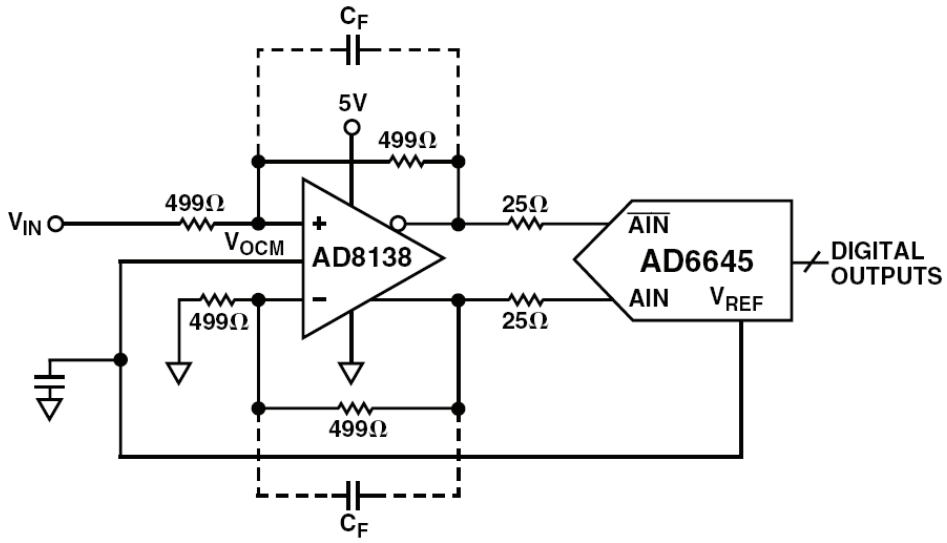


Figure 6.199: *AD6645 Typical Application Circuit*

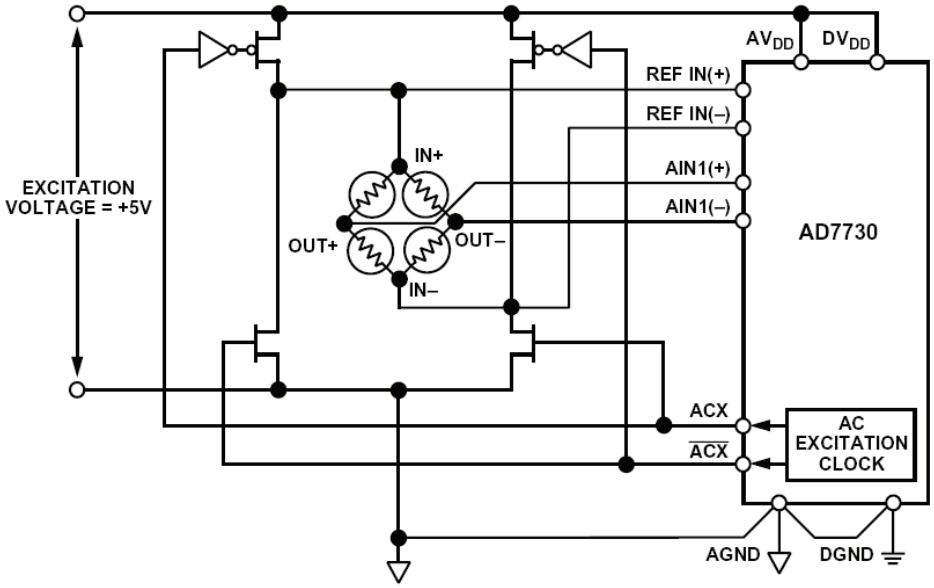


Figure 6.200: *AD7730 Typical Application Circuit*

When looking at the applications circuits, note that the recommended support part numbers, while still valid, may no longer be the best choices. This is because newer parts may have been released since the data sheet was written. Always look to see if a newer part may be better.

Evaluation Boards

The only way to be sure that your design works is to actually build it. But as has been mentioned several times, the layout of a printed circuit board is as critical as any other part of the design. To that end, manufacturers often make evaluation boards available. This is an advantage for the design engineer, since it relieves him of the responsibility of developing and manufacturing an evaluation board. It also allows him to test a portion of the design before committing to the prototype run.

But the evaluation board serves the manufacturer as well. Since the manufacturer controls the design of the board, he can insure that the evaluation system shows off the part in it best light. The manufacturer will ensure that the performance of the board will not limit the performance of the part. This means a more fair evaluation, since many variables are removed.

The schematic and board layouts are typically presented in the data sheet. Often the Gerber files for the evaluation board are available as well from the manufacturer. A word of warning is in order though. Just cut and pasting the Gerber files into your design is not enough to ensure optimum performance. Integrating the evaluation board section into the rest of the system is important as well. For instance, what if there is more than one converter in the system? The grounding scheme of the evaluation board, which worked in the instance of the one converter evaluation system, may be inadequate for larger systems.

Evaluation boards are typically part of larger systems for evaluation of a converter. Typically software is included to interface to the part. This software typically runs on a PC and includes a human interface. Evaluation systems are covered in more detail in the chapter on design aids.

Summary

Not all data sheets for converters (or any other classification of part, for that matter) are the same, not from different manufacturers or even from the same manufacturer. But there are some features which are more or less standard. Knowing what the look for and where to look for it can make the daunting task of part selection a bit easier and possibly more exact.

Notes:

SECTION 6.9: CHOOSING A DATA CONVERTER

Often the choice of the data converter is the cornerstone of the entire design. As we have seen in the previous sections, a converter can have many specifications. Now that we have gone over what those specifications mean and how to read a data sheet we are ready to proceed to the next step. How, then, do you determine which converter best suits your needs?

Determine the Parameters

The most obvious parameters that we may need to specify the converter are the resolution and sample rate. Remember that the resolution of converter and the accuracy may not be the same. Quite often it is really the accuracy that is required.

For ADCs, when we think of sample rate, we generally mean the maximum frequency. However, when the sample rate is reduced, the hold time requirements of the hold capacitors in the sample-and-hold section of the ADC increase proportionally. This can lead to errors if the sample rate is slow enough for the droop rate of the sample-and-hold to allow the sampled voltage to decay till it is out of the error band before the next sample period. While the droop rate of ADCs with internal SHAs is typically not specified, a minimum sample rate will be. This effect is dependant on the architecture of the ADC. Successive approximation ADCs rarely have this problem but pipelined architectures often do.

How the ADC is to be used may also effect the part selection. Pipelined ADCs and Σ-Δ converters typically don't have a control signal for starting the conversion. They are designed to convert continuously. This makes them a bit more difficult to use in applications in which the sample must be synchronous. This would include multiplexed applications and those where the sample is to be triggered by an external stimulus. Flash or successive approximation type converters are probably a better choice in these type of applications.

We stated in the specifications section that there are two ways to specify the converter, ac specifications and dc specifications. In general ac specifications tend to be important with continuous sampling, higher speed. DC specifications tend to be more important with single conversion or multiplexed applications, which tend to be lower speed.

What is the frequency range of the input signal? For high frequency applications, is the input frequency band in the first Nyquist zone, or is undersampling to be employed?

Another point: Nyquist says that the input frequency can be up to half of the sample rate (for baseband sampling), but the antialiasing filter complexity increases sharply as the upper end of the input frequency band approaches the Nyquist frequency (Fs/2). By using oversampling, moving the sample rate out so that the input frequency band is proportionally smaller, system cost and complexity can be reduced.

The analog considerations for interfacing DACs are typically much less involved. In general, the decisions are whether the DAC should be current out or voltage out. If current out, the DAC will typically dictate the use of a current to voltage (I/V) converter. One possible exception is whether the DAC is multiplying, in which case you need to specify the input signal.

On the digital side, the primary consideration is whether the data bus is parallel or serial. With the proliferation of low voltage circuits, the voltage level of the interface also needs to be defined. In many cases the data output level is the same as the power supply, but some converters have a separate power pin which sets the voltage level of the digital interface. While the parallel interface is fairly simple, there are some added questions concerning the serial interface. Does it need to support a standard such as SPI, I^2C, or LVDS?

If the resolution of the converter is not the same as the data bus width (interfacing a 12 bit converter to an 8 bit parallel bus for instance) the converter will require multiple read/write cycles. Similarly, in a serial interface you may have to specify right or left justified data.

In some converters control words must be written to the converter as well.

As always, what the physical environment the converter must operate in is a concern. What is the temperature that the system must operate in? Is there a size limitation? What power supplies are available? Also, high speed converters tend to be relatively high power dissipation devices. Thermal considerations must also be considered.

Part of this process is determining the values for the various parameters. In doing this you should determine an optimum value and an acceptable range. For example, you may have a target value of full 16 bits for the accuracy, but you may be able to live with 2 LSBs of differential nonlinearity and by loosening this spec, a better overall fit could be made. The temperature range over which that the circuit will be required to operate will affect this as well. The physical size of the package and the cost, as always, should be considered. It is good practice to allow a little margin on the specs, if possible, so that aging effects, etc., don't cause the circuit to go out of spec.

Prioritizing the Parameters

As can be seen from the discussion above, there can be a number of considerations involved in selecting a part. Typically, however, there are one or two that are more important than the rest. It is always a good idea not to overspecify a part. The more specifications that have to be met, the harder it will be to meet all of them.

Selecting the Part

The last step is to finally select the part. The "brute force" method would be to gather data books and randomly start looking at the specs for each of the parts individually. This would quickly get out of hand. There are several tools that make the job much easier.

One such tool is a selection guide. These appear frequently in magazine ads and promotional mailers. The main difficulty with using these guides is that, in many instances, the lists are not all inclusive, but instead are usually focused on specific sub groups such as new products, single-supply, low power, etc. The narrow focus may cause you to miss some otherwise acceptable options. An example of a selection guide, in this case called a solutions bulletin is given in Figure 6.201.

ADI provides a piece of literature called "The Short Form Designers Guide" which is much better suited to the purpose. It contains all of ADI's current product offering, sorted by function and performance. Two of the main parts of the short form are the product trees and selection guides.

Using the converter section as an example, we can choose between several possibilities, each of which are expanded further in subsequent trees. This allows the designer to drill down to a particular converter which will be acceptable in his application. Figures 6. 202 through 6.205 shows part of the ADC selection tree.

The selection trees only give one, maybe two, specs. It is designed to be the start of the selection process. More detailed specs are given in the selection guides, which will take a category corresponding the one of the sections of the selection trees, and then sort the parts by the relevant parameter. For example, for converters, they would be sorted by resolution, lowest resolution first. The converters are then sorted by the next parameter, in this case sampling rate.

In addition to the specs used to sort the parts, there are several other specs given. These include package size and cost. The cost quoted is generally the 1000 piece price for the base grade of the converter. It should be used for comparison purposes. Small quantities will typically be priced higher, higher quantities will generally be lower.

An alternative is the parametric search engine. Here you enter the relevant parameters for your design. The converter search is shown in Figures 6.206 through 6.207. You can also prioritize the selection by clicking on the "priority" box. The search will then search the database of parts and it will come up with 10 alternatives.

A particularly nice feature of the search engine is that if it can't meet your selection criteria exactly, it will come back with a selection of parts that come close to matching your criteria. Where there is not a match, the parameter is presented in red. This allows the designer the chance to evaluate how well his application lines up with available components.

High Speed Converters

April 2004 THE ANALOG DEVICES SOLUTIONS BULLETIN

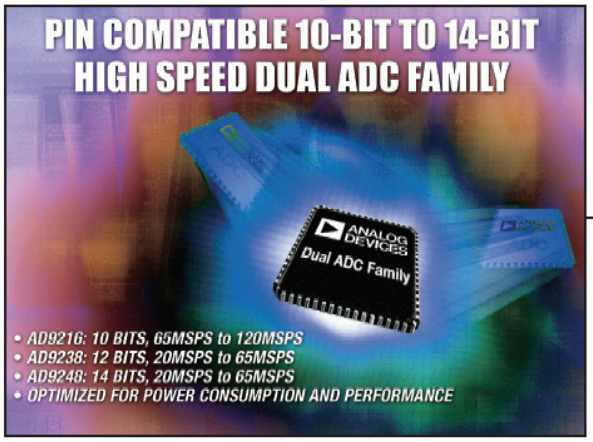
IN THIS ISSUE

Next-Generation, Dual, High Speed ADCs

Whether you're designing a next-generation wireless communications receiver or a low power data acquisition subsystem, your choice of an A/D converter solution can be a key element in meeting end system requirements for performance, power, size, and cost.

Analog Devices has developed the next-generation family of dual, high speed ADCs, meeting the most stringent design requirements. Ranging from 10 bits to 14 bits, and from 20 MSPS to 65 MSPS (up to 120 MSPS for 10 bits), this pin compatible family allows for flexibility in design, depending on the ADC signal chain requirements, while assuring that performance and power have been optimized.

This dual family builds off the feature-rich AD9238, 12-bit, 20, 40, and 65 MSPS ADCs that includes optimized power consumption, IF sampling capability, and flexible output interface configurations—all in a very space-efficient 9 × 9 LFCSP. The AD9216 is the 10-bit companion device that supports speeds from 65 MSPS to 120 MSPS. It is suitable for direct conversion applications, such as in broadband wireless and satellite communications. Extending the family to 14 bits is the AD9248, offered in three speed grades of 20, 40, and 65 MSPS, respectively. The AD9248 gives system designers a low cost converter alternative to today's wide-ranging choice of receivers.



Part Number	Resolution (Bits)	Sample Rate (MSPS)	SNR (dB @ 39 MHz)	SFDR (dBc @ 39 MHz)	Power per Channel (mW)[1]	Price per Channel ($U.S.)
AD9216	10 × 2	65/80/105/120	58.0	75.0	90	5.49
AD9238[2]	12 × 2	20/40/65	70.0	85.0	90	6.57
AD9248[2]	14 × 2	20/40/65	73.5	85.0	90	14.69

[1]Low speed grade.
[2]Also available in LQFP-64.

Visit our website for samples, data sheets, and additional product information.
www.analog.com/bulletins/converter

All prices in this bulletin are in USD in quantities greater than 1,000 (unless otherwise noted), recommended lowest grade resale, FOB U.S.A.

ANALOG DEVICES

Figure 6.201: *Typical Solutions Bulletin Front Page*

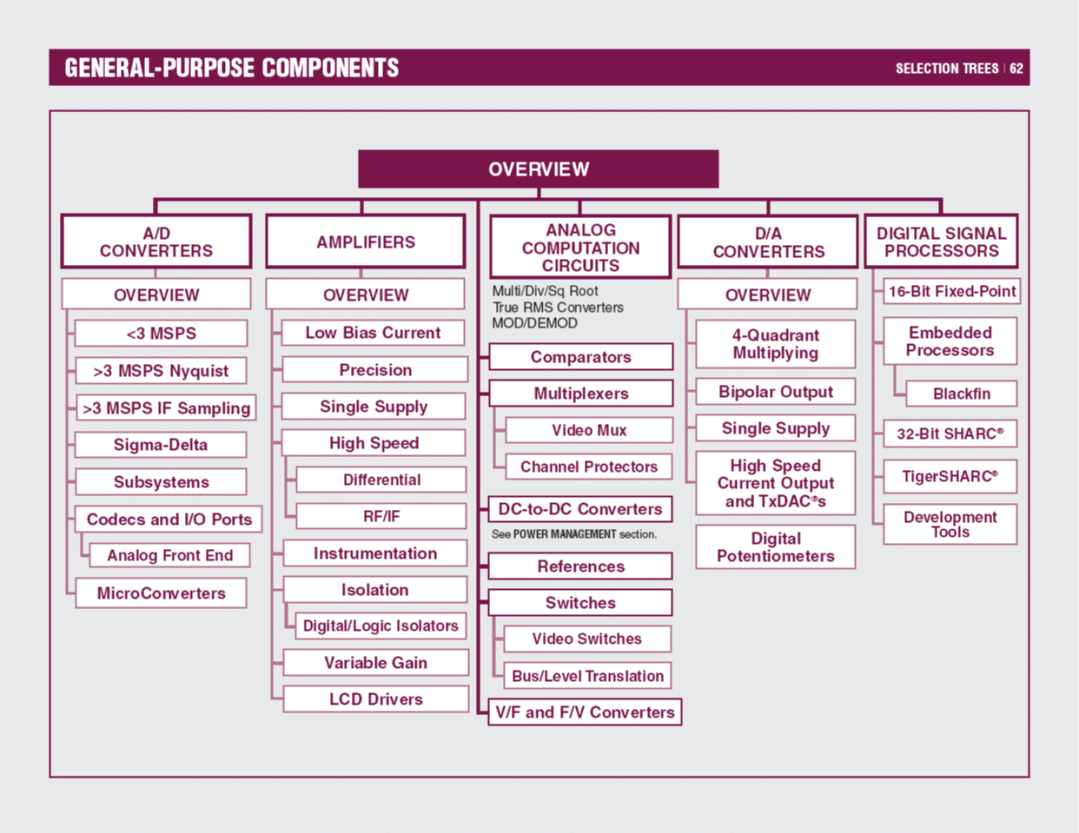


Figure 6.202: *Short Form Selection Guide Top Level*

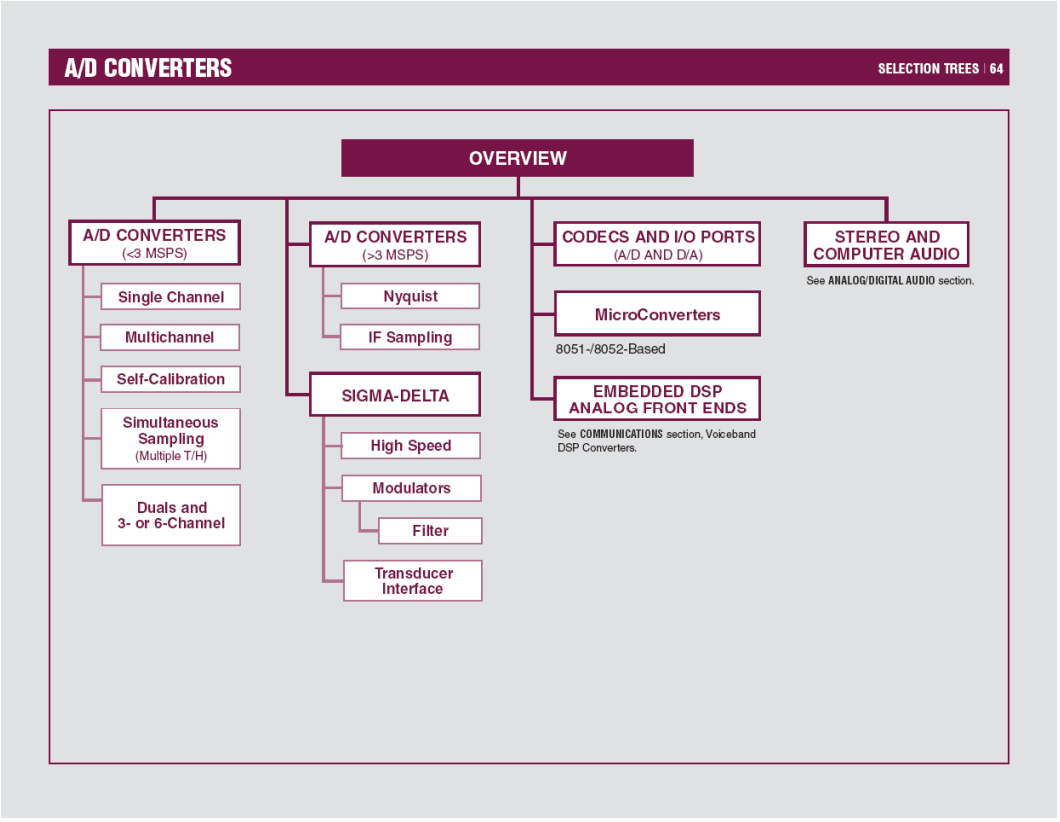


Figure 6.203: *Short Form ADC Selection Table, Front Page*

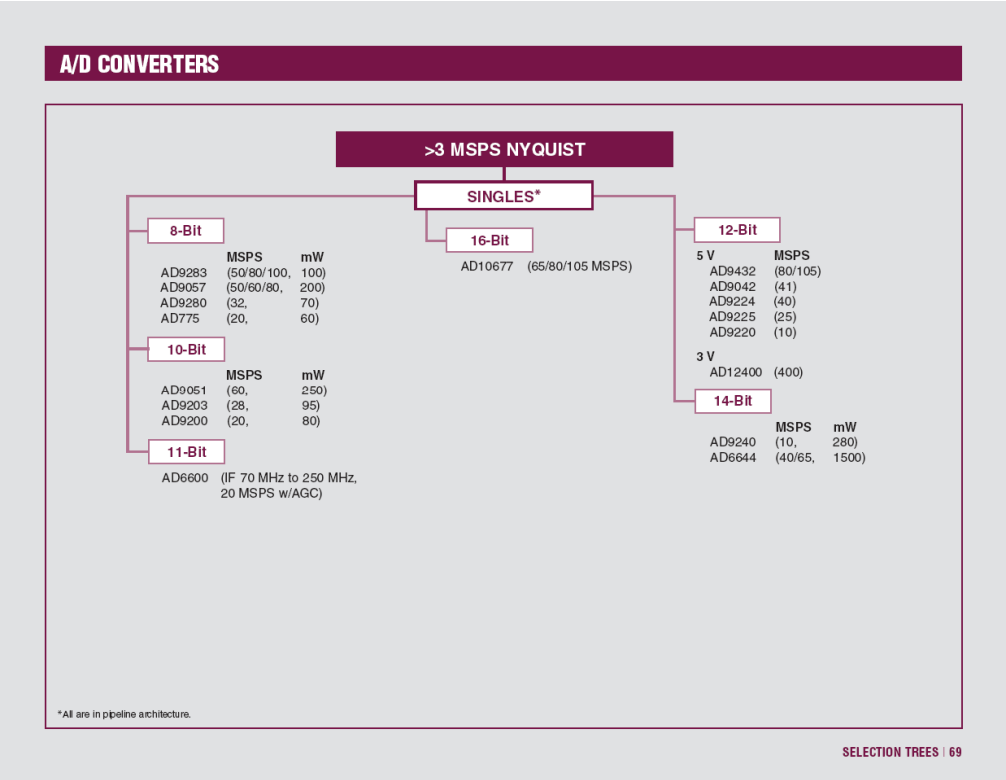
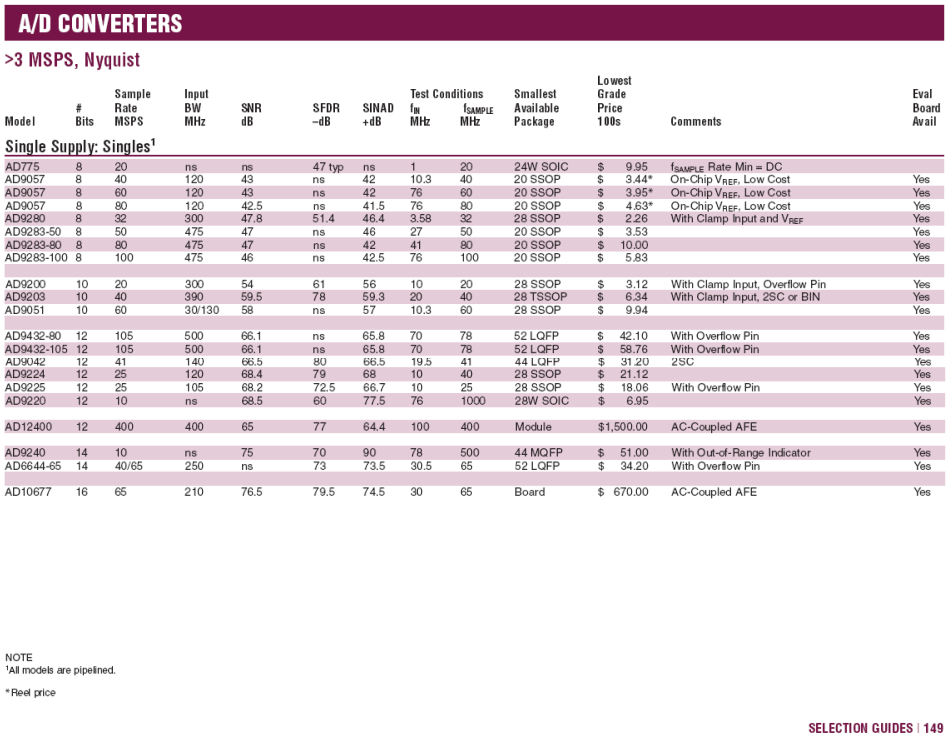


Figure 6.204: *Short Form Selection Guide 2nd Level*



A/D CONVERTERS

>3 MSPS, Nyquist

Model	# Bits	Sample Rate MSPS	Input BW MHz	SNR dB	SFDR –dB	SINAD +dB	Test Conditions f_{IN} MHz	Test Conditions f_{SAMPLE} MHz	Smallest Available Package	Lowest Grade Price 100s	Comments	Eval Board Avail
Single Supply: Singles[1]												
AD775	8	20	ns	ns	47 typ	ns	1	20	24W SOIC	$ 9.95	f_{SAMPLE} Rate Min = DC	
AD9057	8	40	120	43	ns	42	10.3	40	20 SSOP	$ 3.44*	On-Chip V_{REF}, Low Cost	Yes
AD9057	8	60	120	43	ns	42	76	60	20 SSOP	$ 3.95*	On-Chip V_{REF}, Low Cost	Yes
AD9057	8	80	120	42.5	ns	41.5	76	80	20 SSOP	$ 4.63*	On-Chip V_{REF}, Low Cost	Yes
AD9280	8	32	300	47.8	51.4	46.4	3.58	32	28 SSOP	$ 2.26	With Clamp Input and V_{REF}	Yes
AD9283-50	8	50	475	47	ns	46	27	50	20 SSOP	$ 3.53		Yes
AD9283-80	8	80	475	47	ns	42	41	80	20 SSOP	$ 10.00		Yes
AD9283-100	8	100	475	46	ns	42.5	76	100	20 SSOP	$ 5.83		Yes
AD9200	10	20	300	54	61	56	10	20	28 SSOP	$ 3.12	With Clamp Input, Overflow Pin	Yes
AD9203	10	40	390	59.5	78	59.3	20	40	28 TSSOP	$ 6.34	With Clamp Input, 2SC or BIN	Yes
AD9051	10	60	30/130	58	ns	57	10.3	60	28 SSOP	$ 9.94		Yes
AD9432-80	12	105	500	66.1	ns	65.8	70	78	52 LQFP	$ 42.10	With Overflow Pin	Yes
AD9432-105	12	105	500	66.1	ns	65.8	70	78	52 LQFP	$ 58.76	With Overflow Pin	Yes
AD9042	12	41	140	66.5	80	66.5	19.5	41	44 LQFP	$ 31.20	2SC	Yes
AD9224	12	25	120	68.4	79	68	10	40	28 SSOP	$ 21.12		Yes
AD9225	12	25	105	68.2	72.5	66.7	10	25	28 SSOP	$ 18.06	With Overflow Pin	Yes
AD9220	12	10	ns	68.5	60	77.5	76	1000	28W SOIC	$ 6.95		Yes
AD12400	12	400	400	65	77	64.4	100	400	Module	$1,500.00	AC-Coupled AFE	Yes
AD9240	14	10	ns	75	70	90	78	500	44 MQFP	$ 51.00	With Out-of-Range Indicator	Yes
AD6644-65	14	40/65	250	ns	73	73.5	30.5	65	52 LQFP	$ 34.20	With Overflow Pin	Yes
AD10677	16	65	210	76.5	79.5	74.5	30	65	Board	$ 670.00	AC-Coupled AFE	Yes

NOTE
[1]All models are pipelined.

*Reel price

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Figure 6.205: *Short Form Selection Guide ADC Page*

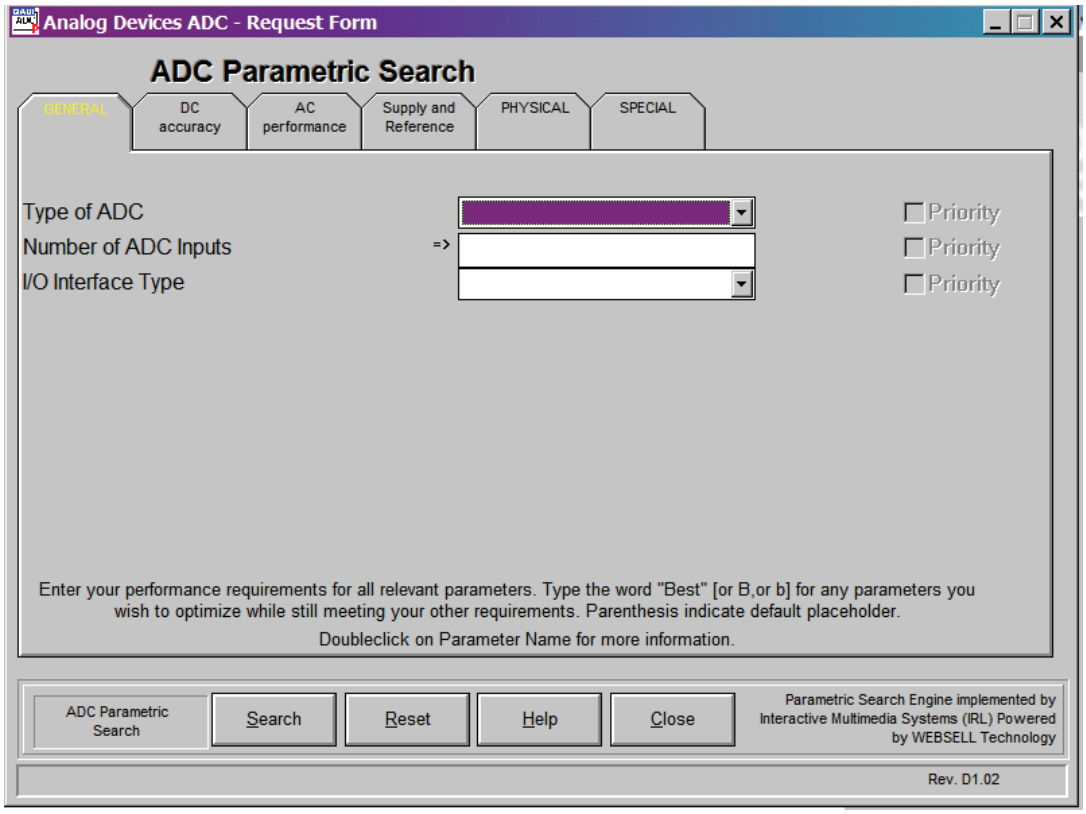

Figure 6.206: *Parametric Search General Page*

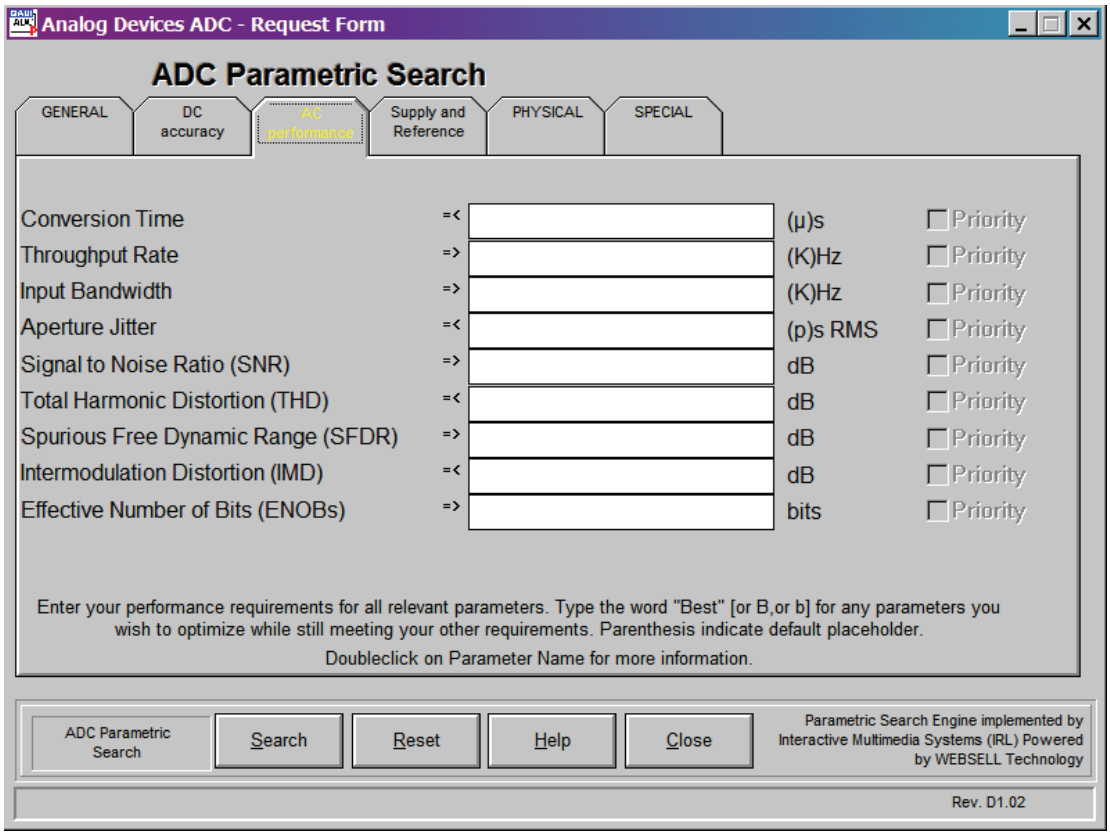

Figure 6.207: *Parametric Search AC Specs Page*