

Daisy-chaining Decoder Chips – A Thorny Problem

THE JOHNSON counter with fully decoded outputs can be a very useful device indeed. However, as far as I can discover, the only readily available CMOS chips are the CD4022, with eight fully decoded outputs, and the CD4017, with ten.

A recent project involved the generation of three-phase signals using digital techniques, based upon the synthesis of sinewaves as a series of voltage levels. This was accomplished using a Johnson counter with a set of “weighted” resistors to create an artificial sine wave. To improve the resolution of the sinewave, I wanted to “daisy chain” several counters and after much consideration arrived at the circuit of Fig. 5.

If we consider the state after reset, both counters will have a logic high on their 0 output. Since the 9 output of counter “A” will be low and this is wired to its Count Inhibit pin, counter “A” is enabled, and the inverter “A” causes counter “B” to be disabled.

As the clock cycles, a logic High ripples along the outputs of counter “A” until it reaches 9. At this point, several things happen very rapidly! Counter “A” is disabled, and conversely counter “B” is enabled via

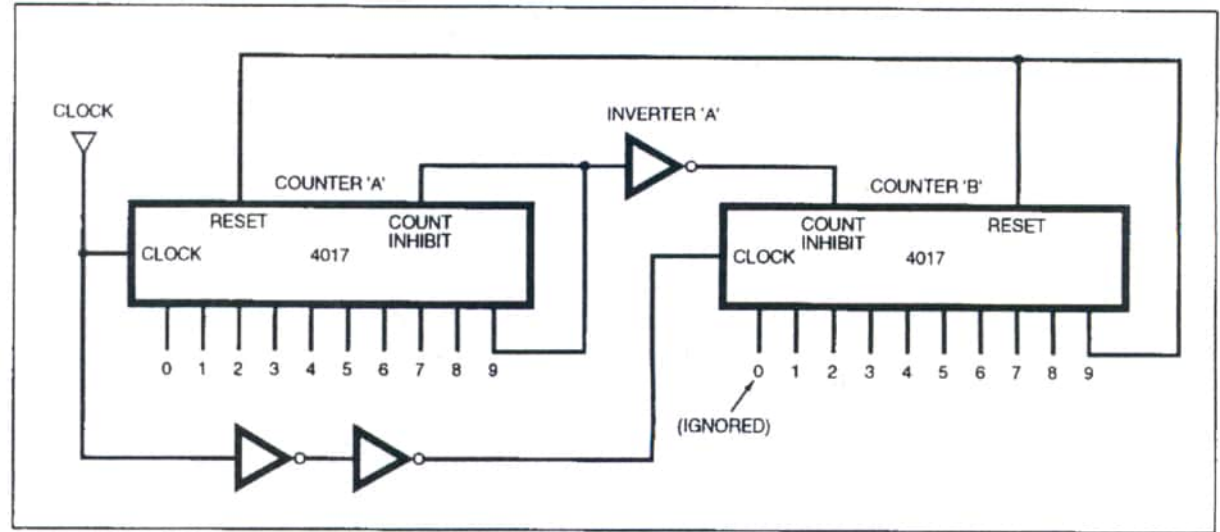


Fig.5. Circuit diagram for cascading decoders to improve the resolution of an artificial sine wave signal.

the inverter “A”. The clock pulse, which is very slightly delayed by the two inverters in series, clocks the high from the 0 output to the 1 output in counter “B”.

Subsequent clock pulses ripple the logic-high along counter “B” until it reaches the 9 output, when the system will reset and we are back to 0. Consequently a fully-decoded ring counter with up to 17 outputs (nine in counter “A”, eight in counter “B”) is

produced. The system could be extended further if necessary.

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● See also *Circuit Surgery*, November 1997 in which Ian Bell of the University of Hull discusses further techniques for cascading digital counters. A.R.W.