Up/down latching sequencer keeps order

by Marc D. Williams
Standard Telephone Co., Cornelia, Ga.

Circuits sometimes need energizing in a prescribed order and de-energizing in the reverse order, on a first-on, last-off basis. At a high-power radio station, for instance. the antennas are switched for transmitting and receiving, and the linear amplifier must be turned off before the switching and on afterwards if its output section is not to be destroyed. A sequencer that performs this task can be built with transistor-transistor-logic circuits, having a sequence rate controlled by an external TTL clock and a completely expandable number of outputs.

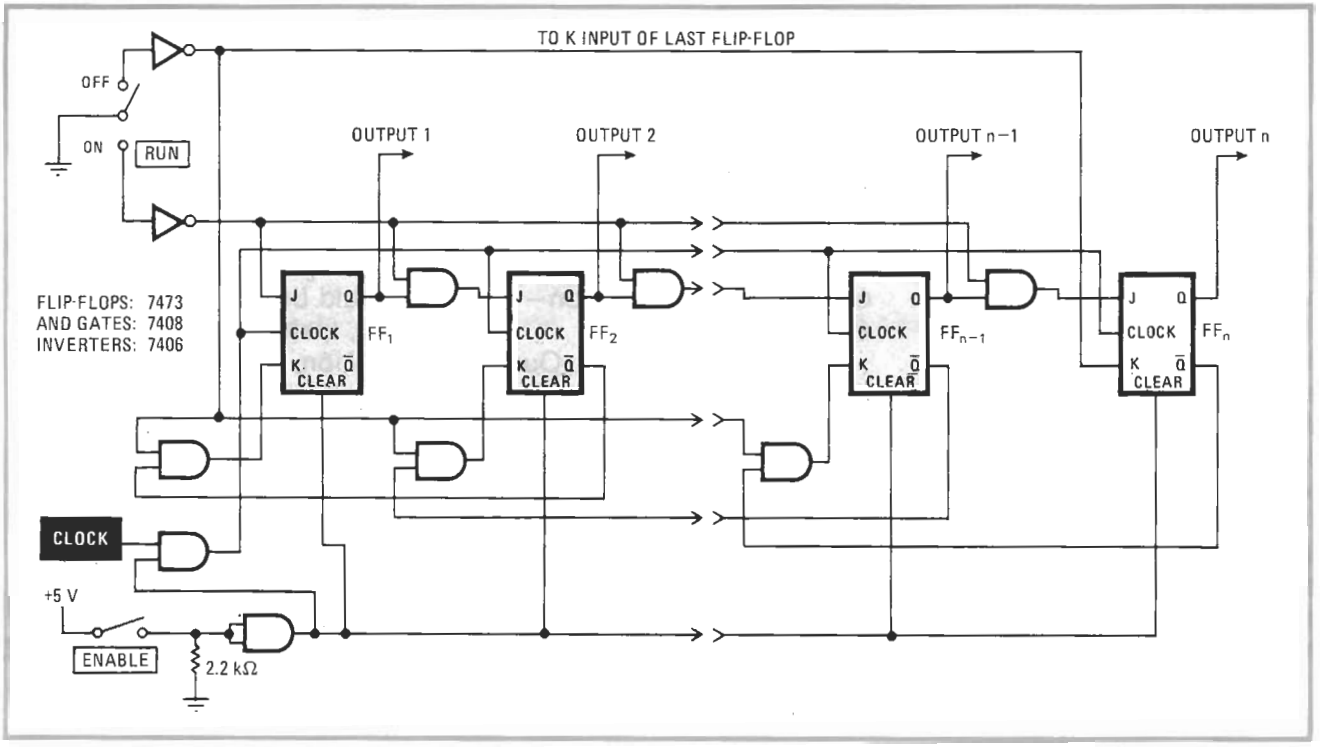
The circuit uses AND gating and inhibiting inputs on the control flip-flops to execute the proper sequence. As shown in the schematic, closing the ENABLE switch allows clock pulses to pass to the flip-flops, which are inhibited by the low level at their J inputs. Turning on the RUN switch allows the first flip-flop, FF_1, to toggle upon receipt of the next clock pulse, and the Q output of FF_1 enables FF_2 to toggle with the following clock pulse. The $\overline{Q}$ output of FF_2 inhibits FF_1, while the Q output of FF_2 allows FF_3 to toggle, and so on down the line to the last flip-flop, FF_n, as long as the RUN switch remains on. The circuit now is stable with all the Q outputs high.

Turning the RUN switch off starts the unlatch sequence by enabling FF_n to return to its off state due to the high K and low J input levels. The $\overline{Q}$ output of FF_n enables the preceding flip flop FF_{n-1} to return to its low state, and so on back to FF_1. Opening the ENABLE switch simultaneously resets all the flip-flops and prevents further toggling.

A three-stage sequencer will require five TTL packages, excluding the clock circuit. Driving displays or relays requires buffering of the Q outputs on the flip-flops.

Although the sequencing may be extended to many stages, the inverters may have to be buffered to drive the AND gates for many stages. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published



First on, last off. With ENABLE switch on, turning RUN switch on starts the latching sequence: with each clock pulse Q output of each flip-flop goes high in ascending order, until all are high. Turning RUN switch off unlatches outputs in descending order. The circuit was designed to permit switching of antenna couplers only after removing power from radio transmitter, and RUN function was performed by keying.