Analog Applications Journal

DESIGN BRIEF

Simultaneous Power-Down Sequencing with Linear Regulators

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Introduction

In the past, ensuring successful power up for DSPs and FPGAs in electronic equipment was a challenge. The most recent DSPs and FPGAs have more relaxed requirements for core and I/O power up/down. However, a few still specify power-up ramp rates and recommend sequential sequencing for predictable and repeatable startup. Even fewer specify power-down requirements, including ramp rates and/or sequences. In most cases, the ultimate goal of these requirements is to ensure that the DSP and FPGA power rails do not have a larger differential voltage than that for which they were designed, even during the brief periods at power up/down. Otherwise, immediate or cumulative damage to internal circuits, which reduces long-term reliability, can occur. Therefore, the ideal method for DSP and FPGA power up/down is for all rails to rise and fall at the same time and rate.

Two or more power-rail ICs are said to have been simultaneously sequenced on power up when they track one another with the same rising dv/dt, and the lower rail stops at its regulated voltage while the upper rail continues to its higher regulated voltage. Various devices, including the TPS74301 linear regulator, have a tracking input to provide simultaneous power-up sequencing. Simultaneous sequencing on power up/down is implemented by replacing the converter's error-amplifier reference voltage with the tracking input signal while the signal is less than the reference voltage. However, for power-down sequencing to work, the converter must have circuitry to pull down the output under light load. Switching converters such as the TPS54x80 family can easily pull down the output by modulating the duty cycle. Most linear regulators do not have pull-down circuitry; so, even though the linear regulator tries to lower the output voltage, it must wait for the output capacitor to discharge through the load resistance. Figure 1 shows a block diagram of the TPS74301 configured to track the 3.3-V rail from a TPS54610. See Reference 1 for a complete schematic of TPS54xxx devices.

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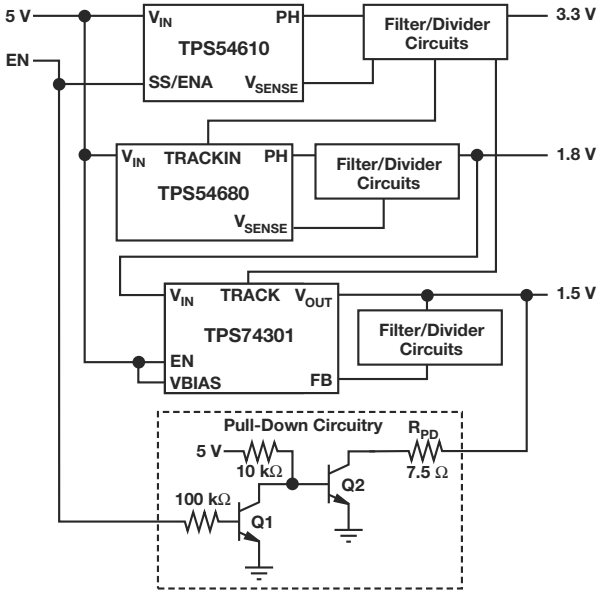

Figure 1. Block diagram of TPS74301 providing power-up/down sequencing

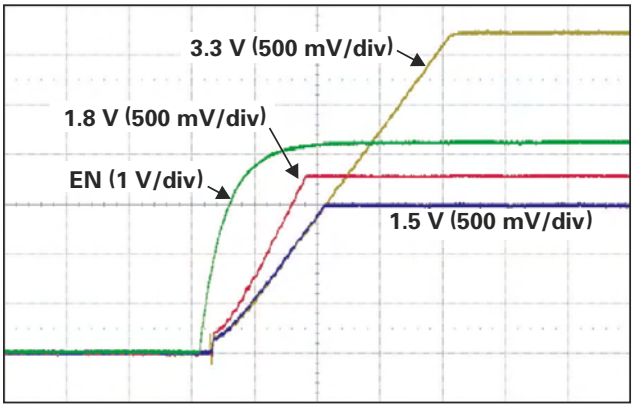

Figure 2. TPS74301 1.5-V output with power-up sequencing

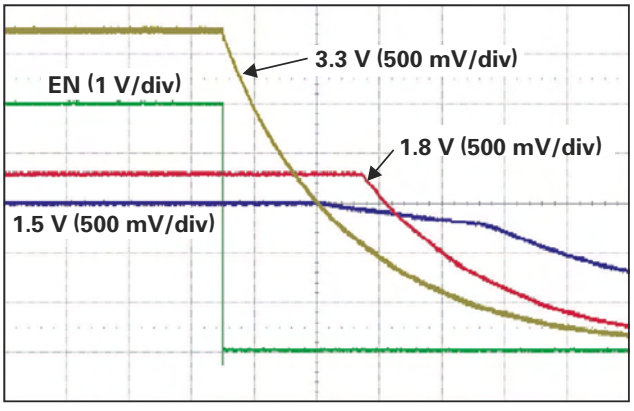

Figure 3. TPS74301 1.5-V output without power-down sequencing

Figure 2 shows simultaneous power up of the 3.3-V and 1.5-V rails. Figure 3 shows that, with the pull-down circuitry (low-cost, bipolar transistors Q1 and Q2 and their supporting components) removed, the TPS74301 output voltage does not track down because the power-down load resistance is too high. The pull-down circuitry shown in Figure 1 adds the pull-down resistor, R_{PD}, in parallel with R_{L2}, which lowers the regulator's load resistance and its RC time constant ($R_{L2} \times C_{O2}$) during power down. This means that the TPS74301 output will track down as shown in Figure 4, since the $R_{PD} \parallel (R_{L2} \times C_{O2})$ time constant is less than the $R_{L1} \times C_{O1}$ time constant.

The circuit in Figure 5 shows how to make all versions of the TPS74x01 family achieve "pseudo" simultaneous power-up/down sequencing by having V_{OUT} follow V_{IN}. When V_{IN} is less than the sum of the output voltage and the regulator's dropout voltage (V_{DO}) for a given output load, the regulator's pass element is operating in dropout. Therefore, if the load during power up/down is heavy enough, the regulator's output voltage could be below the voltage being tracked by $V_{DO(max)}$. Note that the soft-start capacitor, C_{SS}, must be set so that the TPS74x01 output ramps up faster than V_{IN}.

Please see Reference 2 for the complete version of this article, which shows waveform examples for two TPS74x01 devices with a 1-Ω load and one device with no load.

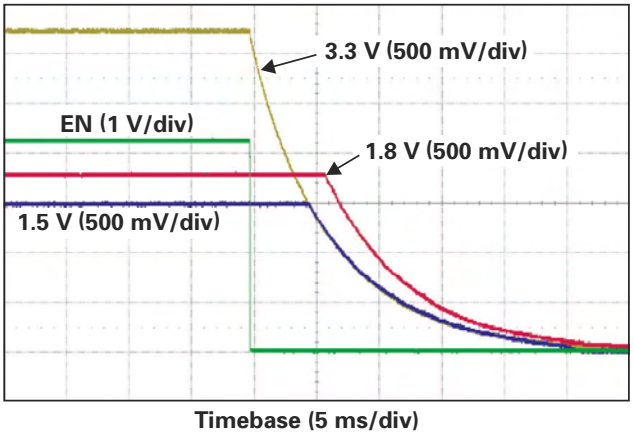

Figure 4. TPS74301 1.5-V output with power-down sequencing

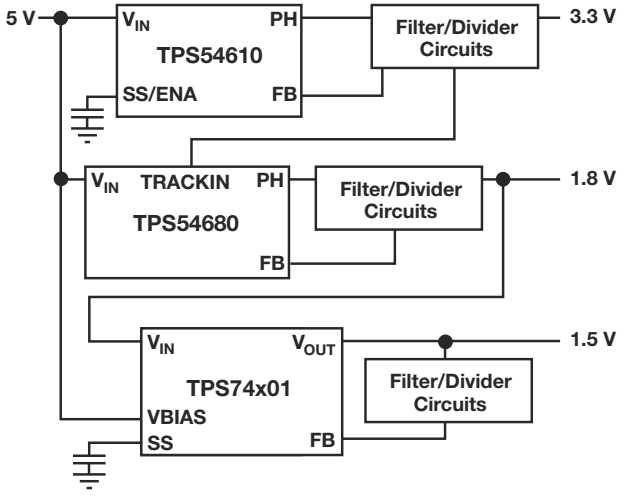

Figure 5. Block diagram of TPS74x01 providing pseudo power-up/down sequencing

Conclusion

The TPS74x01 family of linear regulators easily provides simultaneous power-up sequencing and, with the assistance of simple pull-down circuitry and/or careful sizing of the load resistance at power down, provides two different methods for achieving simultaneous power-down sequencing.

References

1. "TPS54680EVM-228 6-Amp, TPS54880EVM-228 8-Amp, SWIFT™ Regulator Evaluation Module," User's Guide, Literature number: slvu077
2. View the complete article at http://www-s.ti.com/sc/techlit/slyt281