NEW PULSE WIDTH MODULATOR CHIP CONTROLS 1 MHz SWITCHERS

ABSTRACT

Controversy prevails as to the benefits of pushing switched mode pulse width modulated power supplies higher and higher in frequency. Two facts are undisputed though: the industry is pushing switching frequencies up daily and no PWM control IC has been available to optimally control circuits running above several hundred kilohertz. A new IC, the UC3825, has been developed with the top end of the PWM frequency spectrum in mind to simplify high speed control problems. This chip, suitable to either voltage or current mode control, addresses the speed critical parameters that have been glossed over in the past: error amp bandwidth, output drive capability, oscillator frequency range, and propagation delay. A one megahertz, 50 watt supply has been built to demonstrate the chip.

PWM CONTROLLER REVIEW

Briefly reviewing popular control IC's on the market today should serve to illustrate one source of the headaches belonging to designers of high frequency switching power supplies. The snaggle-toothed appearance of the table illustrates the fact that high speed parameters have generally been ignored. The entries in this table represent the tried and true first and second generation standbys (1524, 1525, 494), dedicated off line control (1840), and current mode (1846). All these architectural approaches have certainly proven sufficient for numerous converter designs, but all lack the processing speed required to keep track of a 1 MHz switcher, or even 200 kHz for that matter. Many specifications in the table are missing completely, some are only typical, and the few guaranteed limits leave much room for improvement.

Of prime importance here is the delay time between fault detection and turning off the power switch – the speed critical path. When a fault occurs, either the on chip over-current sense section or an off chip fault detector plus the shutdown section of the chip must work fast enough to turn off the power switch before destructive current levels introduce an automatic (and permanent) power down feature to the supply. This feature, of course, is manifested in blown power devices. The problem is aggravated at the onset of core saturation, since switch currents then rise at much faster rates.

Also important is the drive capability of the output stage of the control chip chosen. Rise and fall times must be consistent with switching speeds or else an output buffer will have to be added. This, of course, adds delay to the speed critical path placing tighter demands on the delays through the chip or forcing the designer to over-specify the power elements to insure fault survival. Over-specifying, however, adds cost, weight and volume as transistors, heat-sinks, and transformers are beefed-up. These consequences are in direct opposition to the very motives for going to higher frequencies in the first place – reduced volume and lower cost.

On-chip error amplifiers have also been a design obstacle in the past. Why build a high frequency switcher and then over compensate the loop due to lack of error amp bandwidth? Designers have been forced to conser-

SPEED COMPARISON OF PWM CONTROLLER IC'S

	SHUT DOWN DELAY (ns)		OVER-CURRENT SENSE DELAY (ns)		ERROR AMP BANDWIDTH (MHz)		ERROR AMP SLEW RATE (V/ s)		OUTPUT RISE/FALL TIME (ns)	
	TYP	MAX	TYP	MAX	TYP	MIN	TYP	MIN	TYP	MAX
SG3524	–	–	–	–	3	–	–	–	200	–
UC3524A	200	–	600	–	3	–	–	–	200	–
UC3525A	200	500	–	–	2	1	–	–	100	600
TL494	–	–	–	–	0.8	–	–	–	200	400
UC3840	–	–	200	400	2	1	0.8	–	–	–
UC3846	300	600	200	500	1	0.7	–	–	50	300
UC3825	50	80	50	80	5.5	3	12	6	30	60

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vatively use the bandwidth available simply due to a lack of guaranteed specifications in many cases. Also, some characteristics which would prove useful haven't been specified at all. Slew rate is such a specification that has great bearing on the large signal response of the supply.

By comparison, the 3825 specifically addresses the speed critical parameters. Maximum propagation delays of 80 ns nearly belong in the "order of magnitude" improvement catagory. Slicing delays yielded a hefty output stage capable of 1.5 Amp peak currents. The guaranteed rise time is, in fact, more a function of internal slew rates than external loading in the 1000 pF range. The error amp guaranteed to 3 MHz and 6 V/μs promises ease of use when controlling wide-band loops.

UC3825 BLOCK DIAGRAM

The design philosophy for the 3825 was to build a chip faster than any other available and tailor it to fit neatly into high frequency converter designs. It includes a dual totem-pole output stage capable of driving most power mosfet gates stand-alone, and the versatility to be useful for DC to DC, off-line, bridge, flyback, push-pull, and even resonant mode converter topologies. The member of a family covering the conventional temperature ranges, the UC3825 is specified for zero to 70 degrees centigrade while the UC2825 spans −25 to 85, and the UC1825, −55 to 125.

The block diagram of the 3825 (figure 1) is architecturally similar in many respects to a number of previous PWM controllers. It includes an oscillator, undervoltage-lock-out circuit, trimmed bandgap voltage reference, wideband error amplifier, PWM comparator PWM latch, toggle flip-flop, soft start section, comparators for over-current sensing and reinitializing soft start, and dual totem-pole outputs. The input to the PWM comparator is brought out to a separate pin so that it can be connected either to the timing capacitor for conventional PWM designs or a current sensing network for current mode control schemes.

In normal operation, the oscillator establishes a fixed clock frequency issuing blanking pulses to terminate one period and begin the next. These pulses serve to reset the PWM comparator while blanking the outputs off. After the blanking pulse, one output turns on until the ramp input (level shifted 1.25 Volts) exceeds the error amp output voltage. This sets the PWM latch which turns the output off and triggers the toggle flip-flop, selecting the other output for the next period.

THE SPEED CRITICAL PATH

The blocks that set the 3825 aside as the controller best suited for frequencies over several hundred kilohertz are those in the speed critical path (high-lighted blocks in figure 1.): the PWM comparator and current limit comparator in the front end; the PWM latch and associated internal logic; and the ouput stage. Signal

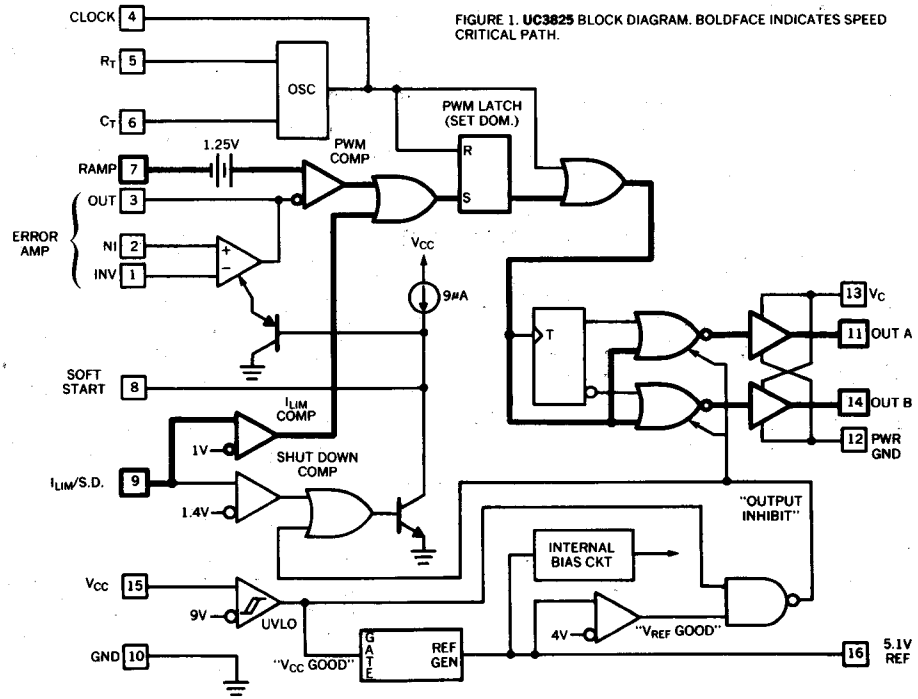


FIGURE 1. **UC3825** BLOCK DIAGRAM. BOLDFACE INDICATES SPEED CRITICAL PATH.

propagation through these subcircuits makes or breaks a design during a fault condition. In the 3825, the propagation delay from either the Ramp input or the Current-limit sense input to the output pins is typically 50ns, very much faster than any chip available today.

Comparators

The PWM comparator is basically an npn differential pair with an emitter follower output (figure 2a). The pair is biased so that the output swing is one Vbe. This guarantees none of the transistors in the comparator will saturate while providing output voltage levels compatible with the internal logic. In order to assure that the input common mode range of the comparator is not exceeded (the range of an npn input pair cannot go below approximately one Volt), a 1.25 Volt level shift is included between the non-inverting input of the comparator and the input pin of the chip. This allows the ramp input to swing from zero to approximately three Volts. The inverting input is tied directly to the output of the error amplifier.

The benefit of this approach is ease of use both in current mode and conventional PWM applications. For the older PWM circuit approach, the ramp input pin can be tied directly to the oscillator Ct pin while current mode users can simply tie a ground referenced current sense network directly to the Ramp pin.

The current limit comparator is very similar in design to the PWM comparator. Its inverting input is referenced internally to a one Volt level derived from the 5.1 Volt reference allowing the non-inverting input to be brought directly to the current limit pin. Functionally, when a fault causes the Current-limit pin to exceed one Volt, it acts just like the PWM comparator, setting the PWM latch and causing the outputs to remain off for the duration of the clock cycle.

The current-limit comparator can also be combined with the 3825 outputs and a few external components to form a constant volt-second product clamp (figure 2b). This clamp is useful in current mode systems to prevent core saturation during load transients. When either output turns on (goes high), capacitor, C, is charged from Vin through resistor, R. Normal circuit operation would turn off the outputs causing C to be discharged before it reaches one Volt. If, however, it does reach one Volt, the current-limit comparator terminates the output pulse. Since the charge rate is proportional to Vin (assuming Vin is much greater than one Volt), then a constant Volt-second product clamp of one Volt times RC is achieved.

Logic

All of the speed critical logic, including the PWM latch, the toggle flip-flop, and various gates are a cross between emitter coupled logic and emitter function logic. In either case, their speed relies on emitter coupled pairs and emitter follower buffers biased to insure that no transistor saturates. Although two OR's, a NOR and the PWM latch are directly in the critical path between the input comparators and the output drivers, they account for only twenty percent of the total delay, the remainder being shared between the comparators and the output stage.

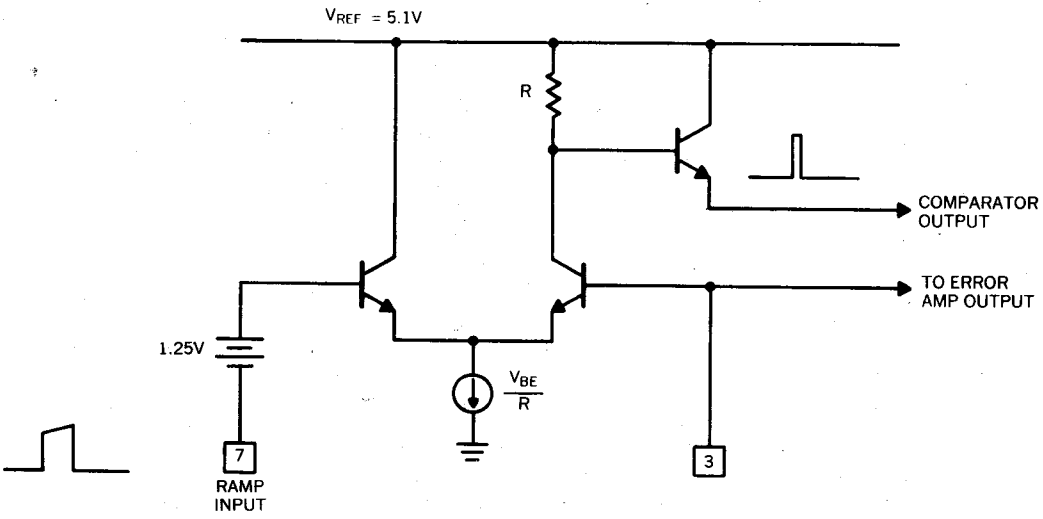


FIGURE 2a. PWM COMPARATOR SCHEMATIC.

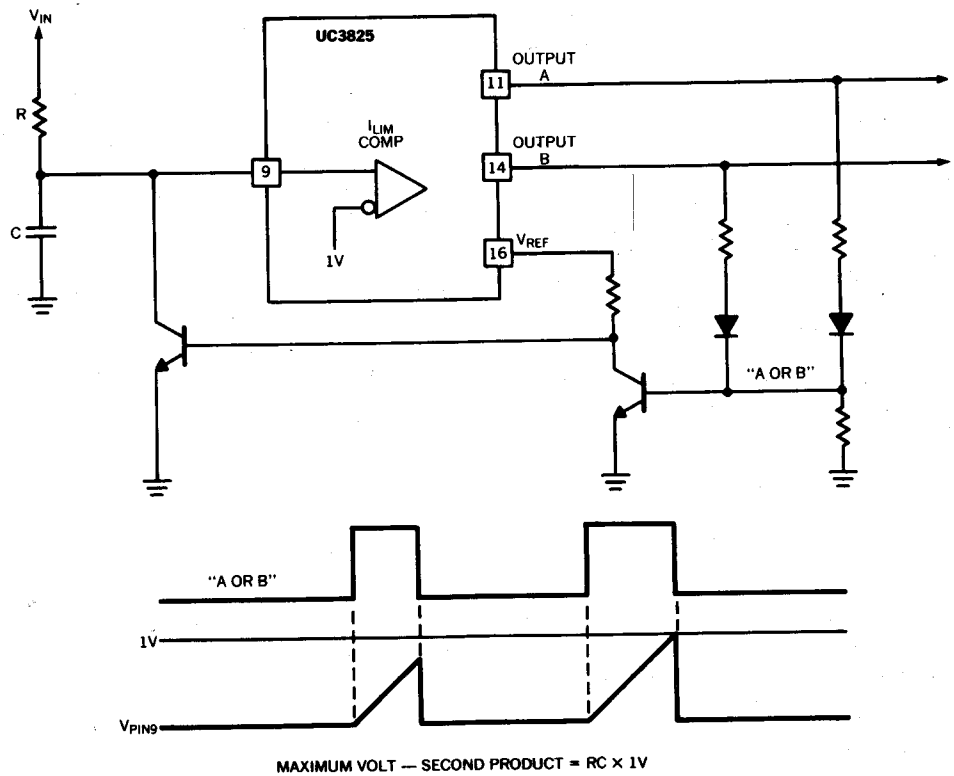


FIGURE 2b. CONSTANT VOLT-SECOND PRODUCT CLAMP IMPLEMENTED USING THE CURRENT LIMIT COMPARATOR.

Outputs

Speed from one pin to another does little or no good unless the signal coming out of the chip has the strength to do its job. The dual totem-pole drivers of the 3825 are capable of driving 1000 picofarads from one rail to the other in a mere 30 nanoseconds. In fact the peak current avilable is in excess of 1.5 Amps. This kind of brute strength is sufficient for driving a wide range of power mosfet's in a variety of applications.

Some older PWM controllers with totem-pole output stages are plagued with hefty amounts of cross conducted charge during output transitions. This can result in major self heating problems especially at higher clock rates. The 3825 output stage (figure 3a) has been modeled after the successful designs of the UC3846 and UC3842. The differences are in bias values and the addition of Schottky diodes. This circuit guarantees the output transistors, Q1 and Q2, are driven with complementary signals to keep cross conducted charge under control. This approach necessarily involves a compromise since speed is of the utmost concern. Delays could be inserted to guarantee zero cross conducted charge, but that would be contrary to the required propagation delays for high speed operation. The outputs have been adjusted to yield these rise and fall times at a penalty of only 20 nanocoulombs of cross conducted charge per transition. At a clock frequency of 500 kHz, this only adds an additional 10 mA to the supply current.

Rather than dwell on cross conducted charge, which is measured with no load on the outputs, it is more appropriate to examine the performance with typical loads. The most anticipated load is a power mosfet. The impedence presented by the gate of the fet is application dependent, but is primarily capacitive. Therefore, consider the requirements of driving a capacitor with a square wave voltage. The charge required for one cycle is equal to the capacitance times the voltage. The average current taken from the supply is that charge times the switching frequency. This determines the power required from the supply to drive the cap. Since the cap is an energy storage element, all the power

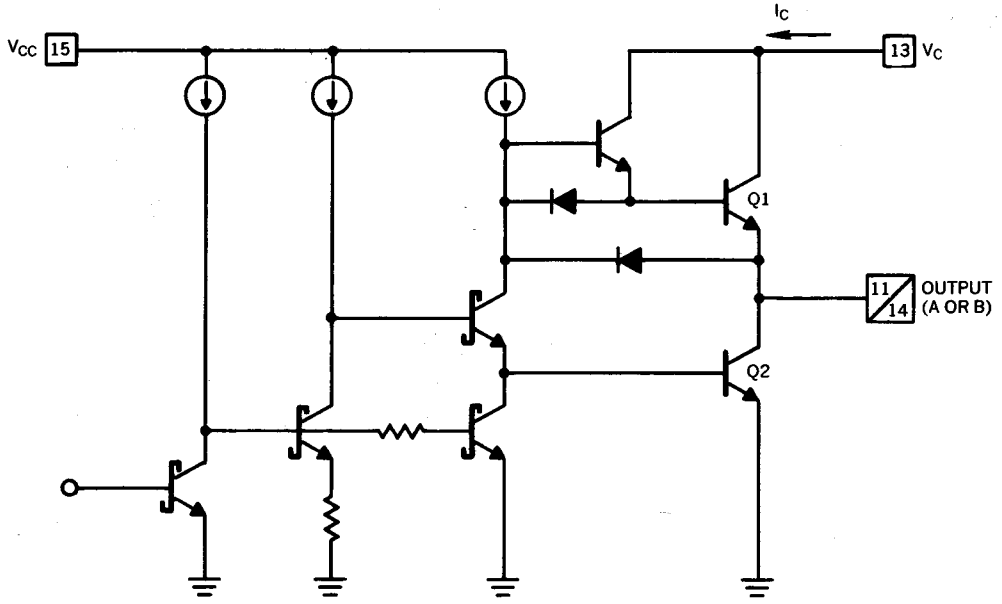
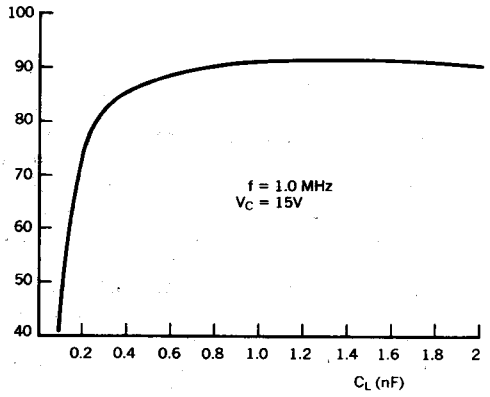


FIGURE 3a. OUTPUT STAGE SIMPLIFIED SCHEMATIC.

taken from the supply is dissipated by the chip. An efficiency figure for the chip can be defined as the ratio of the theoretical power dissipation to the actual power dissipated by the chip. This can be determined for a given frequency and supply voltage by measuring the average supply current into the Vc pin (assuming the peak output voltage is approximately equal to the supply voltage). The figure of efficiency, then, is: (CVf)/Ic. The graph of figure 3b shows the 3825 optimized to drive capacitances above 200pF. Care should always be taken when driving high capacitive loads to make sure the maximum power dissipation level of the chip is not exceeded.

FIGURE 3b

$$\text{EFFICIENCY} = \frac{cvf}{I_C} \ (\%)$$



Another side effect of the output stage should be considered. Any node in a circuit capable of driving large capacitances at these rates begins quickly to resemble an LC tank. Transmission lines, even one inch in length, can become troublesome. The trouble occurs when, on the falling edge at an output, the load rings and actually pulls the output pin below ground. For years IC manufacturers have been warning users not to allow certain pins to go below ground and the 3825 output pins carry the same warning. The collector of the pull down transistor becomes a parasitic npn emitter when pulled below the chip's substrate, which is grounded (figure 4). The collector, or collectors as the case is, are every other npn collector and pnp base on the chip. The ones that are closer to the parasitic emitter collect proportionally more current than ones further away. Physical size of the parasitic collectors also plays a similar role. The results of this phenomenon can range from nonobservable to severe. Resembling leakage current internally, reference voltages can be altered, oscillator frequency can jitter, or chip temperature can be elevated. Dummy collectors tied to ground are inserted into the 3825 chip which help to attenuate this problem but the designer still needs to be aware of it. The problem's potential is not a horror story, though. Among the easiest of solutions is some form of damping in the load circuit (for example ten ohms series resistance) and a good high speed diode, Schottky if possible, to clamp the output pin's negative going excursion.

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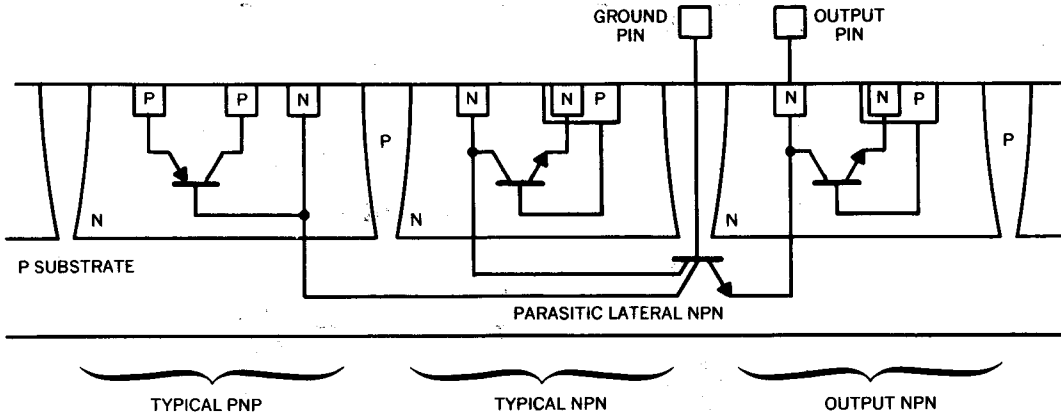

FIGURE 4. PARASITIC NPN TURNS ON WHEN SUBSTRATE – EPI JUNCTION IS FORWARD BIASED.

HIGH SPEED COMPLEMENTARY BLOCKS

An integrated circuit controller with delays of 50ns through its speed critical path is certainly a leading candidate for high frequency switcher applications. There are a few blocks just off the race path that need also to be fast in order to fully qualify the chip for such applications. The oscillator and error amplifier are two such blocks.

Oscillator

From the users point of view, the oscillator looks identical to many that have gone before it (figure 5a). Composed of an all npn comparator, this oscillator has dual thresholds – the upper at 2.8 Volts and the lower at one Volt. Charging current for the timing capacitor, Ct, is mirrored from the timing resistor, Rt. The Rt pin is held at a temperature stable 3 Volts. Temperature stability of the oscillator, then, is achieved by maintaining stable thresholds at the comparator. When Ct has charged to the upper threshold, Q3 turns on to sink a controlled current of approximately 10 mA. The effect of this action is that the discharge of Ct is done in an orderly manner allowing the comparator to reliably catch it when crossing the lower threshold. This also prevents Q3 from saturating, reducing delays in the oscillator and enabling it to operate at higher frequencies. The 3825 oscillator is nominally specified at 400kHz with an initial guaranteed accuracy of 10%. Temperature stability is typically better than 5% while voltage stability (frequency shift over supply voltage) is 0.2%. Oscillator dead time, which effects controller dynamic range, can typically be held to 100ns at 1MHz, allowing 90% duty cycles.

In applications where two 3825's are used in close proximity and synchronization is desired (figure 5b), the oscillator in one chip can be disabled by tying Rt to the reference Voltage. That chip, then, must be clocked by joining the clock pins of both chips. Multiple 3825's also can be synchronized from a master 3825 or other external sync signal. The slave chips are programmed to run at a frequency somewhat lower than the master chip. The master then inserts a sync pulse forcing each slave's Ct over the top threshold and causing discharge action to occur. This way, each chip generates its own clock pulses synchronized to a master clock.

Error Amplifier

The 3825 error amplifier is a voltage gain amp with premium bandwidth and slew rate. Again using only npn's in the signal path, a compensated unity gain bandwidth of 5.5 MHz is achieved. The simplified schematic (figure 6) shows the signal path of the amplifier. Note that while the compensation scheme is not extremely complex or brand new in nature, neither is it the simple dominant pole approach. Included are two zeros located beyond the unity gain frequency to enhance phase margin. One is created by a capacitor across the emitter degeneration resistors in the first stage and the second is formed by a resistor in series with the dominant pole capacitor.

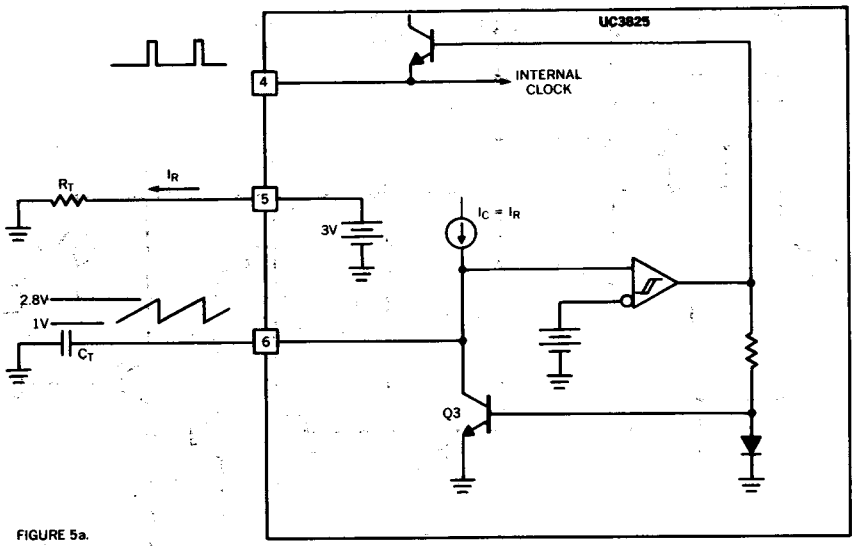

FIGURE 5a.

FIGURE 5b.

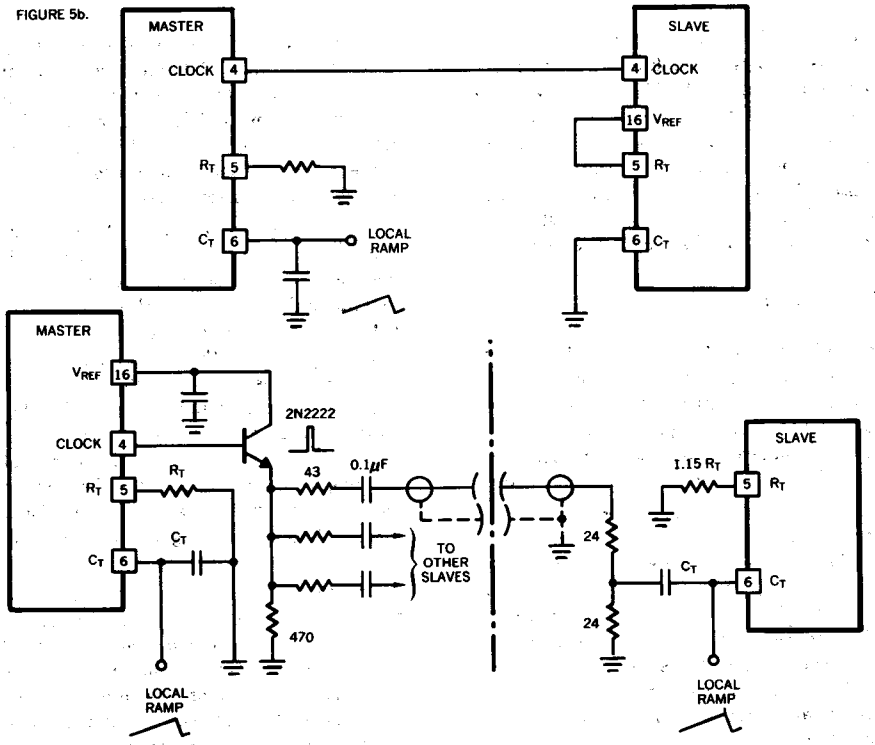

FIGURE 5. OSCILLATOR SIMPLIFIED SCHEMATIC (a) AND TWO SYNCHRONIZATION METHODS (b).

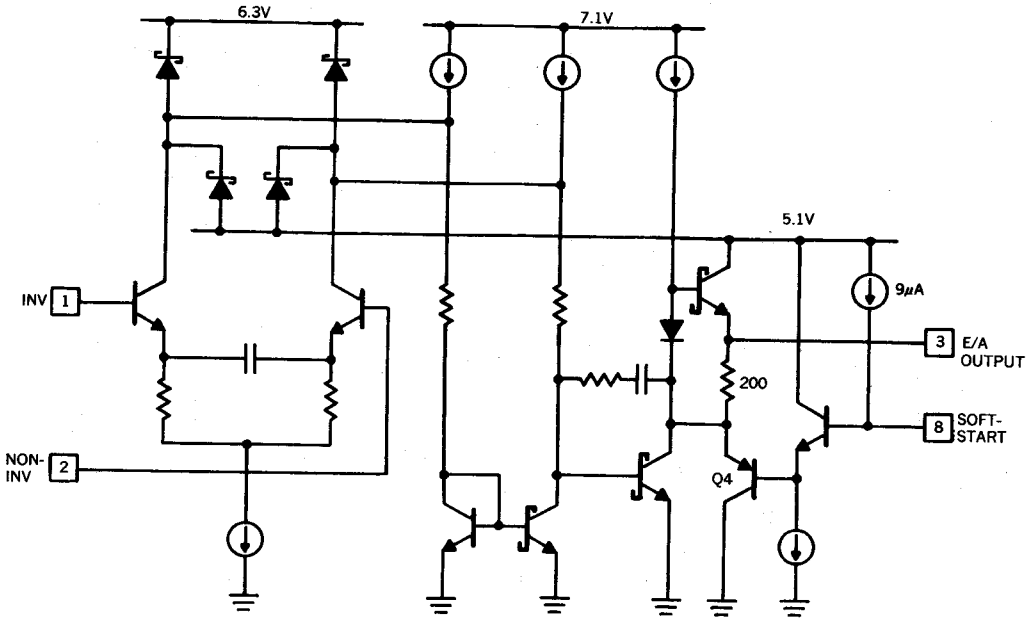

FIGURE 6. SIMPLIFIED SCHEMATIC OF WIDE BAND ERROR AMPLIFIER SHOWING SOFT START CLAMP SCHEME.

By degenerating Gm, the emitter resistors allow an increased first stage bias current level. This contributes to a 12 V/μs typical slew rate. High slew rate, while desirable for good large signal transient response, is not enough to guarantee minimal response time. Often an amplifier may have high slew rates yet exhibit long delay times coming out of saturation when it has been driven to a rail. To defeat this problem, all critical nodes within the amp have been Schottky clamped.

GLUE BLOCKS

The remaining blocks, while not speed critical, mold the 3825 into a more complete PWM controller. The reference, a time proven design, is trimmed to guarantee 5.1 Volts at better than one percent tolerance. This voltage is then held over conditions of line, load, and temperature changes to a two percent total spread.

Soft-start is very simply implemented by a pnp clamp transistor merged into the output stage of the error amp (figure 6). During soft start, while the 9 μA current source is charging the external capacitance on pin 8, Q4 actively forces pin 3 to follow pin 8. In this manner a controlled slow start can be achieved for either voltage or current mode systems. When the error amp comes into regulation, Q4's emitter-base junction is reverse biased and offers no further interference to the normal operation of the amp.

In addition to slow starts, the soft-start pin can be used to other ends. Clamping the maximum voltage this pin is allowed to rise to will then effectively clamp the maximum swing of the error amplifier. In a conventional PWM scheme this results in a duty cycle clamp while in a current mode application, it establishes the maximum peak current level.

Fault conditions are sensed by the 3825 at pin 9 which is shared by the inputs of the current limit comparator and the shut down comparator. When this pin exceeds one Volt, the current limit comparator sets the PWM latch, terminating the output for the remainder of that cycle. As with normal operation, setting the PWM latch causes the toggle flip-flop to switch states. If the pin is further raised to exceed 1.4 Volts, the shut-down comparator forces the soft-start pin to sink a guaranteed minimum of one milliampere rather than sourcing 9 microamperes. Thus the shut down comparator causes the soft start capacitor to be discharged rapidly. After the fault signal is removed the 3825 will then execute a normal soft-start sequence.

One method of combining current-limit and shut-down signals is shown in figure 7. Here, in a current mode control example, a current sense transformer is used to translate switch current to proper voltage analogs for optimal control at both the Ramp and Current-limit sense pins while the shut-down signal is inserted with a resistive summing technique.

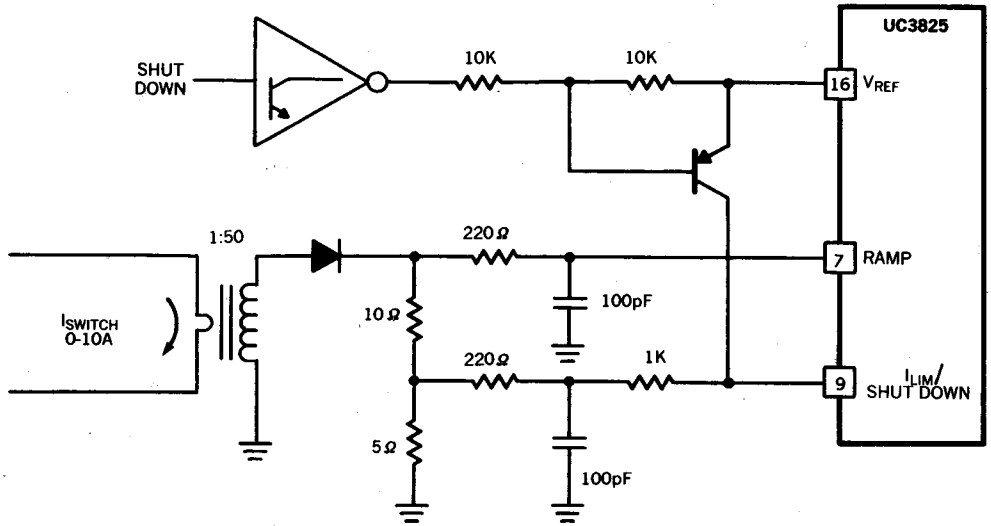

FIGURE 7. CURRENT LIMIT SENSE AND SHUT DOWN SIGNALS ARE COMBINED AT PIN 9 IN THIS CURRENT MODE EXAMPLE.

Starting the 3825 involves the Under-voltage lockout portion of the chip. This block acts like a comparator with it's inverting input biased to 9 Volts and having 0.8 Volts of hysteresis. If Vcc is below the UVLO threshold, the reference generator and the internal bias are turned off, Keeping Icc at a typical 1.1 mA and the outputs in a high impedence state. When Vcc exceeds the UVLO threshold, the reference is turned on and the chip comes alive. Bedlam is avoided, however, as a second comparator monitors the reference voltage and inhibits the outputs until the reference is high enough to ensure intelligent operation. This inhibit signal also holds the soft start pin at a low voltage. After the reference is sufficiently high, the chip begins a soft start sequence.

50 WATT DC-DC PUSH-PULL CONVERTER

A 48 to 5 Volt, 50 Watt converter has been built as a test vehicle for the chip (U-110). Designed around a push pull, current mode controlled topology, the circuit runs from a 1.5 MHz clock. In the interest of simplicity, the ramp input and current limit pins were tied together underutilizing the available dynamic range of the Ramp pin by a factor of 3. A ground plane, judicious bypass capacitors and tight layout technique yielded a circuit that could be easily interrogated without significant noise interference problems.

In this simple application, the 3825 performs all the tasks required to regulate the 50 W power stage. The gate drive for the two power mosfets comes directly from the chip. Current loop slope compensation is resistively summed with the current sense signal at pin 7. Overall loop compensation is implemented with two resistors and a capacitor on the error amplifier. Taking advantage of the 1.5 MHz switching frequency and the wide bandwidth characteristics of the error amp, the control loop was compensated to zero dB at 300kHz.

CONCLUSION

Presenting an easy to use PWM architecture, the UC3825 possesses the necessary high speed characteristics to control switchers in the higher frequency ranges. This fills a void that has hindered high frequency applications in the past. A simple example running at 1.5 MHz points to a future of faster switching supplies.

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