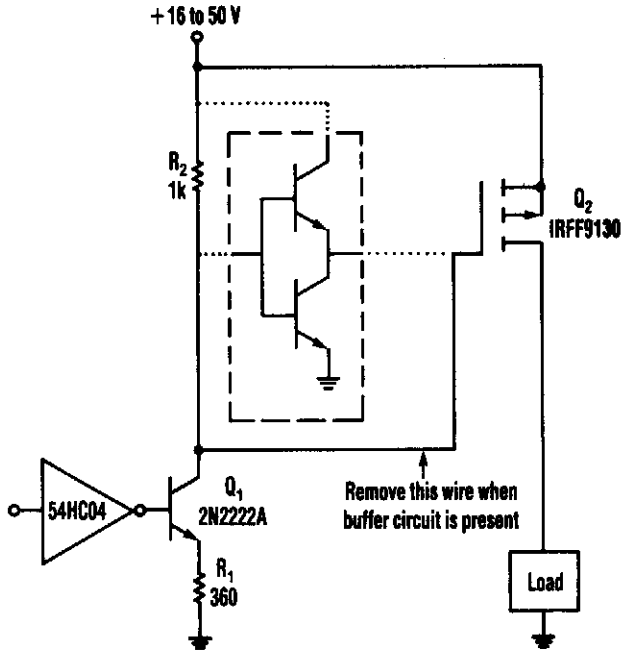
LOW-LEVEL POWER FET DRIVER METHOD



ELECTRONIC DESIGN

Fig. 41-3

This circuit operates from a 16- to 50-V supply. Adding the buffer circuit (within the dashed lines) offers 100-ns switching times. Otherwise, the circuit switches in 1 μs.

Q1 and R1 form a switched current source of about 12 mA. The current flows through R2, which supplies 12 V to the FET. The circuit works well over a wide range of supply voltages. Furthermore, it switches smoothly in the presence of large ripple and noise on the supply. The switching time (about 1 μs) can be reduced considerably by lowering the values of R_1 and R_2 at the expense of higher power dissipations in the resistors and Q1. Alternatively, a buffer circuit can be added to produce switching times of 100 ns without generating significant power dissipation.