Fewer parts resolve shaft encoder data

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This circuit achieves the same resolution as the circuit proposed by Amthor [*Electronics*, Sept. 11, 1980, p. 139] but requires only one integrated circuit, instead of seven, and half the number of discrete components.

A standard shaft encoder has two ports, A and B, each generating a square wave as the shaft encoder is turned. The square wave from port A will either lead or follow port B's square wave by 90°, depending on the direction of the rotation of the encoder (a).

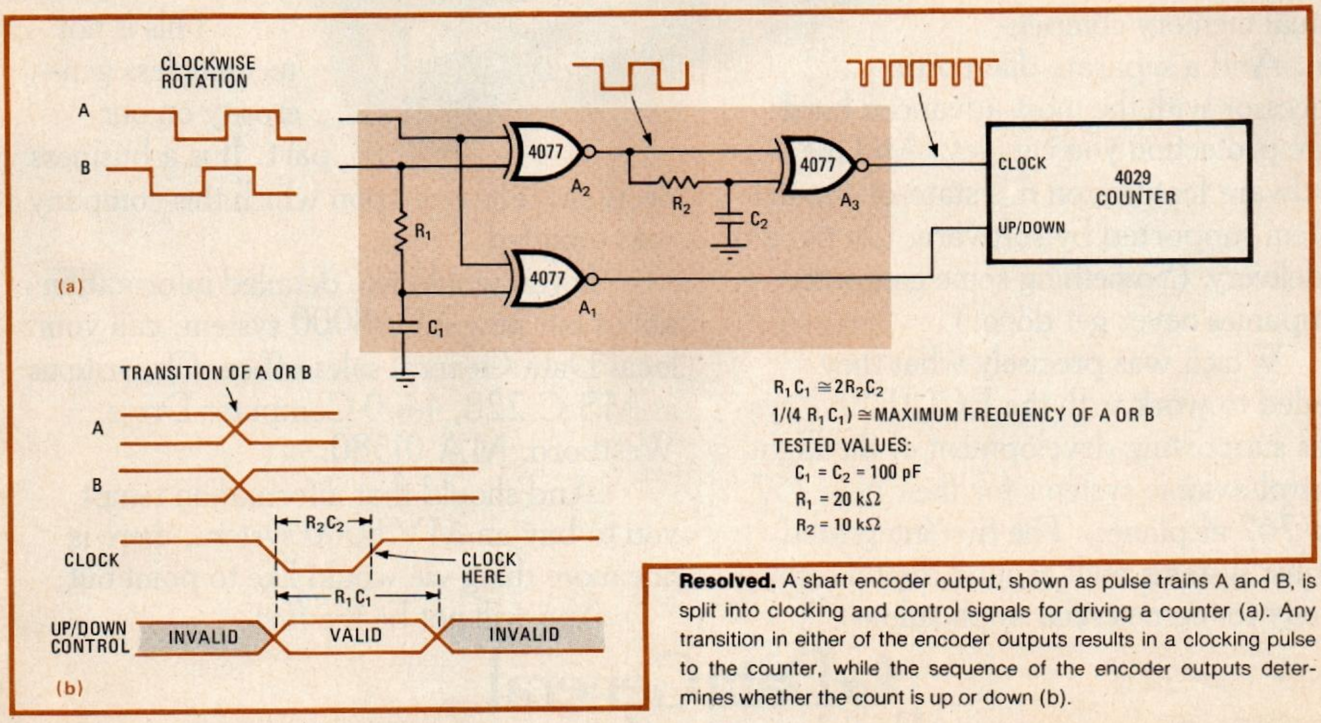
To get the maximum resolution out of the shaft encoder, every change of state for both A and B must be counted. Depending on the direction of rotation of the shaft encoder, the counter will count up or down. By exclusive-NOR-ing square waves A and B at gate A_2, a square wave that changes state whenever there is a change of state of either A or B can be obtained. The output of exclusive-NOR gate A_3 is high except when a change of state at gate A_2 occurs. Whenever the output of gate A_2 changes state, the two inputs of gate A_3 will be of opposite state for a time determined by R_2 and C_2, generating a short, low-going pulse. By using complementary-MOS exclusive-NOR gates, the pulse at the output of gate A_3 will have about the same duration for both the positive and negative transitions of gate A_2. The trailing edge of this pulse is used to clock the counter, allowing setup time for the up-down control (b).

The up-down control is generated by R_1, C_1, and gate A_1. R_1 and C_1 act as a latch, holding the value of B prior to a change of state of A or B during the clock pulse at gate A_3. Exclusive-NOR-ing the value of A just after a change of state in A or B, with the value of B set just prior to a change of state of A or B, achieves the proper up-down control.

The operation of gate 1 can be demonstrated as follows: square waves A and B are out of phase with each other by 90°. Adding −90° to B would change the phase shift to 0° or −180°, depending on the direction of rotation of the shaft encoder.

As a result, the output of exclusive-NOR gate A_1 would be high when A and B are in phase and low when A and B are 180° out of phase. Since the only concern is the output of gate A_1 when the counter is clocked, R_1 and C_1 give enough time lag to phase-shift B for the duration of the clock pulse at gate A_3. For this reason the time constant R_1C_1 is greater than R_2C_2.

The polarity of the up-down control may be inverted by swapping the A and B wires or by using the fourth exclusive-NOR gate in the 4077 integrated circuit as a selectable inverter-buffer. If the clock signal needs to be inverted for another type of counter, the entire 4077 exclusive-NOR–gate package can be changed to a 4070 exclusive-OR package. If standard C-MOS rise and fall times at the A and B inputs cannot be guaranteed, it becomes necessary to buffer the A and B inputs with a Schmitt trigger, such as a 74C914. □



Resolved. A shaft encoder output, shown as pulse trains A and B, is split into clocking and control signals for driving a counter (a). Any transition in either of the encoder outputs results in a clocking pulse to the counter, while the sequence of the encoder outputs determines whether the count is up or down (b).