Power Management in RF Circuits

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Abstract

RF circuits have very specific requirements that they impose on the power supply. This paper discusses these requirements. The different ways of generating such power supply in a suited way for RF circuits is also discussed. A large section of this paper is taken up by an example RF circuit that has ultra-low power and miniature size requirements. This makes that this circuit needs to run directly from a single cell battery. The large impact his has on design choices is discussed.

1. Introduction

A little more than one decade ago wireless communication did start its strong uprise. The cellular mobile phone system GSM is of course the clearest example of this, but since then many other wireless applications and standards, such as WLAN and BlueTooth, have emerged. In all these applications battery lifetime is a most critical property for the mobile stations and a search for its constant improvement is always ongoing. The power profile of a wireless circuit or system is however much more than the sum of the active currents of all its subcircuits multiplied with the batteries voltage level. The first part of this paper will discuss the different issues involved with the selection of the power supply voltage for the different parts in wireless system. The second part describes the different circuits techniques that can bridge the difference between the battery properties and the power supply needs. The following section goes briefly into the dynamic behavior of the power consumption in a wireless system. Finally, an example of a wireless system is presented that requires an ultra low power consumption in a minimum space. One of the consequences of these extreme requirements is that this RF chip does need to run directly from the battery. The impact of this on the power profile of the chip is discussed.

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2. Choosing the power supply voltage

The properties of analog and RF circuits will vary widely with a variable power supply voltage. In fact, this is maybe even more so for digital circuits, where the power consumption and speed performance roughly vary with the square of the power supply voltage. The difference will be however that for some analog circuits you may see degradation in both directions when deviating from the optimum power supply level. The result is that in general a good quality RF circuit cannot run directly from the battery. A voltage regulator will be needed that keeps the power supply constant within a small range. This section will discuss the issues related to power supply regulation and the optimum choice of the power supply level.

2.1. Battery properties

Fig. 1 illustrates the large variations in voltage level over the battery life time that can be expected [1]. These example discharge curves are given for a number of the most common used battery types for wireless applications. Although these curves show a rather flat response for most of the time, the designer has to take into the peak voltage that will be present at start. There is some more flexibility on which point will be defined as fully discharged, but even so the ratio between the highest and lowest possible voltage level can be a factor 1.5 to almost 2. This is an enormous variation for analog and RF circuits to cope with.

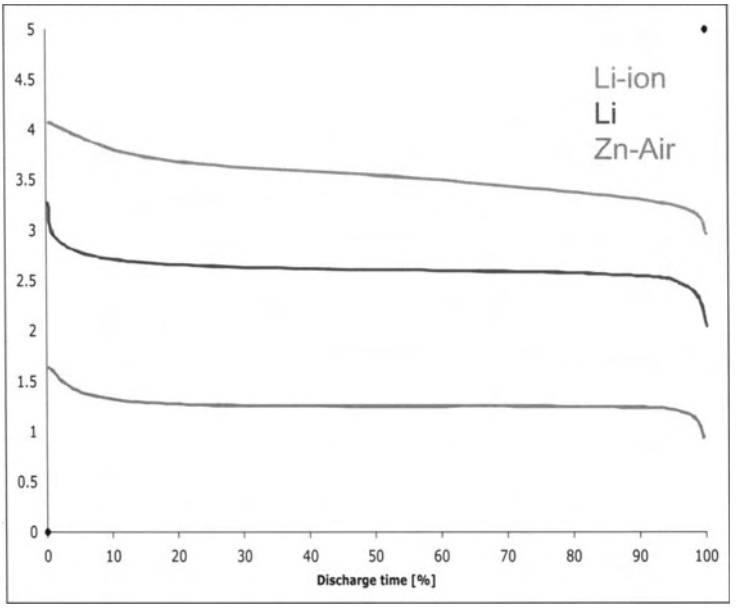

Fig.1. Example discharge curves of commonly used battery types.

An equally important aspect that will prevent direct operation from the battery is its internal resistance. The battery's internal resistance makes that variable currents that are drawn by the wireless device will be converted in a ripple on the battery level. The consequence is that very strong power supply rejection ratio requirements need to be imposed on those circuits that would operate directly from the battery.

2.2. Circuit requirements

Different RF circuits have different power supply needs. A specific example is for instance an LC VCO. Although the VCO's varicap uses preferable a rather large voltage range in order to keep its sensitivity low, the VCO core itself is a block that does not require a large power supply voltage [2]. Fig. 2 shows the basic outline of a LC VCO circuit. As power supply voltage it requires only the V_{GS} values for the cross-coupled negative g_m plus the V_{Dsat} of the current source. Large signal swings will be generated in the oscillator, but this has no influence on the power level requirement. The consequence is that in today's mainstream technologies an LC VCO will only require a 1 V to 1.5 V power supply. Anything in excess of that will result in a loss of power in its current source. As an alternative, LC VCO topologies can be used that take into account the available voltage headroom by placing both and nMOS and pMOS negative g_m pair [3],[4]. The pMOS pair will however not achieve the same efficiency for the power supply drop it uses as the nMOS pair.

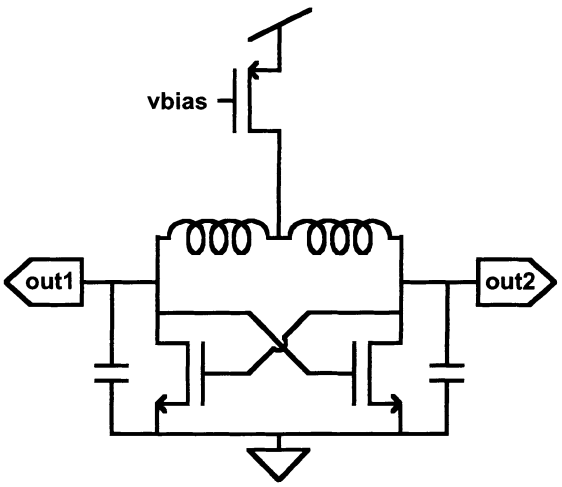

Fig.2. Basic topology of a differential LC oscillator.

A similar story goes for the LNA. An LNA is basically designed to pick up very small signals and amplify these. Even after amplification its output swing will remain limited even for the highest input signal level that must be tolerated. Especially when an inductive load is used, a 1 to 2 V power supply may be sufficient for the LNA [5]. In some cases this property has been used to save power by stacking different stages on top of each other. Fig. 3 gives an example of an LNA circuit that uses this property. A source follower buffers the load capacitance in this topology such that a high bandwidth can be obtained, even without inductive load.

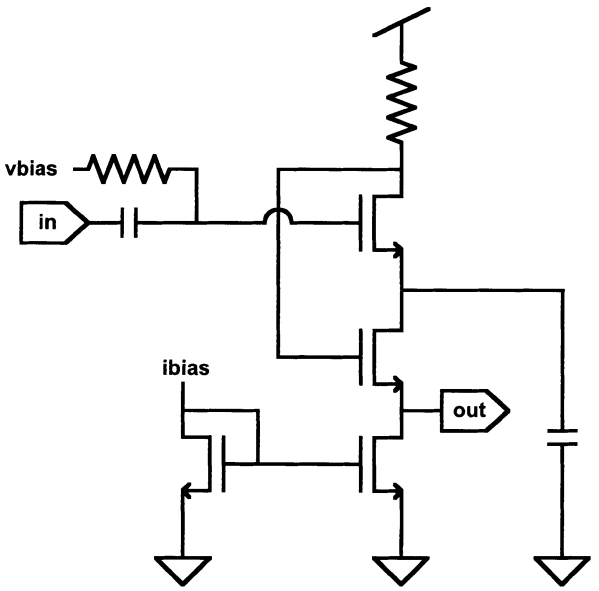

Fig.3. LNA topology that re-uses the current.

A downconversion mixer and its succeeding IF filters have a different dependency on the power supply. In this case it is the achievable signal swing that must be maximized and at low frequencies this implies using the largest possible power supply level [6]. A larger signal swing will allow for equally larger noise levels in these blocks and thus directly for a lower area and power consumption. Without going into much detail on specific types of circuits in RF chips, it is clear that different part may have different power supply requirements.

3. Generating the power supply for RF circuits

Most wireless circuits will require some extra circuitry to manage the power supply level [1],[7]. The main function of such circuit will be to regulate the voltage that is provided to the wireless chip such that is kept within small boundaries. Maximum variations of ± 5 % or ± 10 % are common. A second function of a power management circuit is making sure that the power supply signal is a clean signal. This means it needs to have a low internal impedance over a wide frequency range such that current variations are not translated into voltage variations. It also means removing noise that is present on the unregulated power supply level. The use of different regulators for different parts of the system allows for an isolation between them.

3.1. Linear regulators

Linear regulators are the most easy to implement type of regulators. In many cases, depending on the current they have been designed for, they can be implemented onto the same chip as the RF circuitry, which makes them also the cheapest implementation of a regulator.

There are two major drawbacks for a linear regulator: its efficiency and the fact that the supply level at its output can only be lower than the lowest possible input level. The latter means that a battery that can go as low as 0.9 V in an almost discharged configuration will only yield a linear regulated power supply of 0.8 V for the complete operation time. The efficiency of the regulator is already reduced due to the variable voltage drop over the regulator that needs to carry the current that is consumed by the active circuit, but on top of that there is the increased current that will be needed for an analog and RF circuit in order to give it the same speed and accuracy performance on the low power supply level of e.g. 0.8 V [6], compared to a possible much higher voltage that is tolerable by the technology. For this reason, linear regulators are in power consumption critical wireless systems mostly only used for specific blocks that require an improvement of their PSRR. The clearest example is the regulation of an LC VCO. As indicated before, an LC VCO does not require a large power supply voltage, while it is most critical to picking up power supply noise since this directly translates into spurii on the LO signal and thus a reduction of the bit-error-rate or the selectivity.

Part of the previous efficiency argument disappears when the power supply level that is tolerable by the technology is close to the low power supply level that the regulator generates. For the example of 0.8 V given above, this becomes true for e.g. a 0.13 μm and certainly a 90 nm CMOS technology. For very cost

sensitive high-volume applications in which a full single chip implementation is a necessity, like e.g. BlueTooth [8], the use of an on-chip regulator built with thicker oxide devices for the complete RF part becomes an option. For the digital part of such a chip a switching regulator is more suited since its switching noise is in that case no problem, such that the higher efficiency can be fully exploited. It remains however doubtful that there is fact a business case for many single chip wireless systems in a 90 nm technology. The chip area taken up by the digital part may in such a technology become only a fraction of the RF and analog chip area and since the latter do not scale well between technology generations, there is not a large cost advantage to be expected from moving to the more fine line technology, while development cost rise of course sharply.

3.2. Switching regulators

An alternative to linear regulators are switching regulators. In a switching regulator a power transistor will in combination with an inductor, convert an input voltage level into a different output voltage. Pulse width modulation allows to make the ratio between input and output variable and thus to regulate the output level. The main advantage of the switching regulator is its efficiency. Values better than 90 % are commonly achieved. The drawbacks of the switching regulator are twofold: cost and switching noise. The switching regulator will require the use of a good quality inductor, a large decoupling capacitor and likely an off-chip power transistor. The switching process generates spurii onto the regulated power supply that cannot be removed completely. Higher switching speeds reduce the size of inductor and capacitor that is needed, but due to a reduction of the efficiency this remains limited to values of around 1 MHz, a frequency that is still too low to remove efficiently with proper filter choices in the RF part. RF blocks that have a rather large power consumption requirement will be the preferred parts to be powered from an inductive switching regulator. A power amplifier for long distance wireless systems, like GSM, that can transmit up to 2 W, is a good example.

Lower cost implementations may use a capacitive switching regulator [1]. They are limited to lower current levels, have a more worse efficiency and they will also generate switching noise, although less than an inductive regulator.

4. Dynamic power consumption

Different from many other applications, wireless systems have in general a very dynamic power consumption behavior. First of all there is the difference between an active communication mode and a stand-by mode. In the stand-by mode a channel is only check from time to time to verify if any relevant

information is present for the receiver. Even in an active mode digital wireless communication will in most case use some form of time division multiplexing in which communication is only performed during certain time slots.

The difference in current consumption between a 'communicating' mode and a 'non-communicating' mode can be as high as a factor 1000. In fact, in complex wireless systems there may be a wide number of different operating modes, each with their own current consumption requirement and timing profile. An example is for instance the fact that a synthesizer must be started up first and must be locked before a power amplifier can be switched on in order not to pollute the transmitted spectrum. Power supply regulation circuits for wireless systems must be specifically designed for this task. The efficiency of a basic supply regulator varies highly with a variation of its load. The efficiency in both a high current consumption and low current consumption mode may however be equally important for the battery life time since the low current consumption mode may for instance be a power preservation mode that takes up 99 % of the total operation time. Advanced power regulators must thus be used that are able to detect the current consumption of their load and that can change to a different operation mode, like e.g. from switching regulation to linear regulation, in order to keep the efficiency high over a wide range of several decades. This has however its limitations. The reaction speed of the regulator that can be achieved will make that there is each time some transition period that will need to be taken into account. More advanced power supply regulation systems will therefore start to use a communication protocol with the controller of the wireless system such that the regulator can be warned or even pre-warned for a change in operation state with a digital command.

5. Example implementation

As example, the power management profile of an ultra low power FM receiver will be analyzed here. The discussion start by a presentation of the application and its requirements [9]. In the following sections it is further reviewed how these requirements impact different choices concerning power supply and power consumption issues.

5.1. Miniature FM receiver for hearing aid applications

Fig. 4 shows the selected architecture for the miniature FM receiver. This FM receiver has been developed as an add-on module for hearing aids. With this module clicked on to their hearing aid, hearing impaired persons can now not only use the built-in microphone of the hearing aid. They can also use a second, wireless, microphone that can be placed far away from the hearing aid, close to the audio source. In many difficult circumstances with a high background noise,

this can give a significant improvement of the audio signal-to-noise ratio. For this application worldwide different frequency bands have been allocated. These bands range from 72 MHz to 225 MHz. In these bands smallband FM modulation is used with a 25 kHz channel spacing.

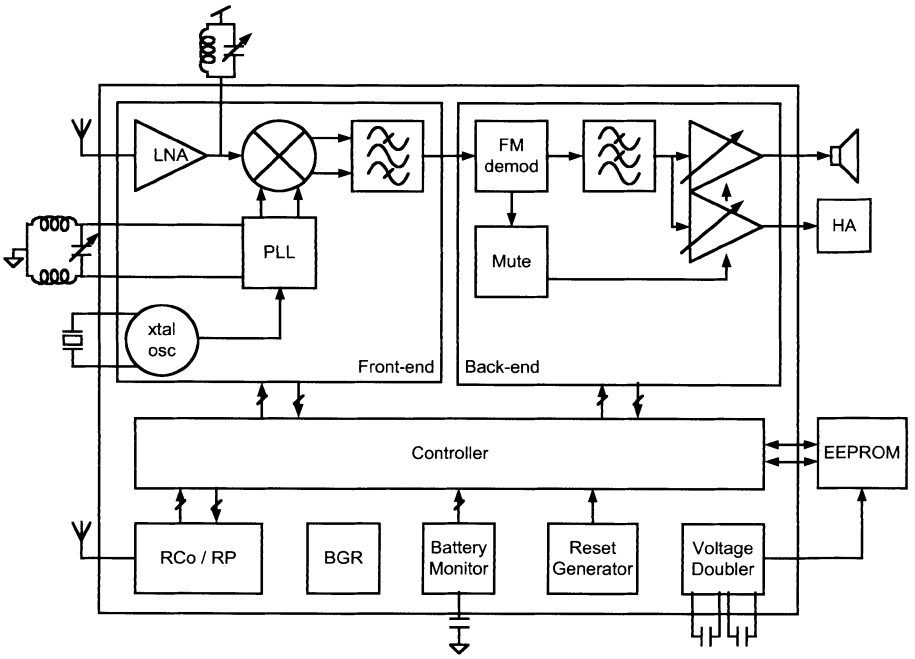

Fig.4. Architecture of the low voltage FM receiver.

The application as an add-on module brings some specific requirements. The first one is that it must be able to run from the hearing aids battery. This is typically a zinc-air battery, which has a working range of 0.9 V to 1.6 V. This also means that its full active power consumption must be limited to a few milliamps in order not to become dominant on the hearing aids battery lifetime. This must be extended with a number of power preservation modes in order to further save power whenever possible.

A main requirement in this application is also that the FM receiver must have a programmable PLL on board. It will be discussed later on how this puts extra specific requirements on the technology choice and power supply selection strategy. If direct operation from the battery cannot be avoided, this brings specific stringent PSRR requirements to the synthesizer.

Finally, the application as an add-on module for hearing-aid applications also brings in the requirements that the FM receiver must have a miniature size. In

some applications it will even be worn directly into the ear. In that case only an earphone is connected directly to the FM receiver and no additional hearing aid is used to perform further advanced signal processing on the audio signal. Fig. 5 shows the FM receiver module and gives an impression of its size. It fits within 1 cm^3. This is realized by having as many components as possible integrated on to the chip.

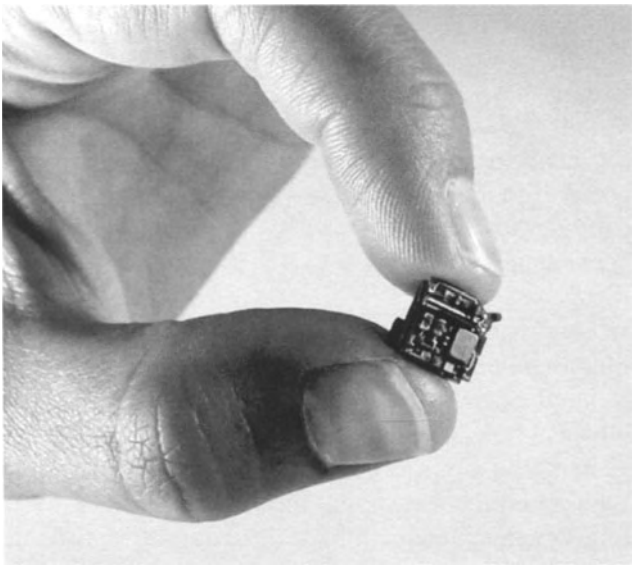

Fig.5. The complete miniature FM receiver module.

5.2. Direct battery operation

The available options for the implementation of the power supply are in the case of this FM receiver highly limited. The most flexible solution would be the use of an inductive supply converter. As discussed in section 3 this can have the advantage of an optimum supply level choice, most suited for the selected technology, while offering also the benefit of giving only a small variation on the power supply level. Power consumption is very critical in this application, but an inductive converter can also offer an efficiency of more than 90 %, although generally realized at higher power levels. There are however two main reasons why inductive conversion is not an option here. First of all there is the miniature size requirement. It does require at least a low loss inductor and capacitor. Their size is directly related with how much the switching ripple must be reduced. In this case this is highly important since a ripple on the power supply will be picked up by the synthesizer and will result in spurii being generated on the local oscillator, thus reducing directly the sensitivity. Increasing the switching speed will reduce the size of the components that are required, but this comes at the cost of a reduction of the efficiency. The

maximum usable switching speed is 1 to 2 MHz and this is too low to make that the generated spurii would fall far out of band such that the antenna filter would still make the sensitivity OK.

The alternative solution to generate a highly stable power supply voltage is the use for a low drop out linear voltage regulator. Since the power consumption is only a few milliamps such regulator could be placed on chip at a limited area cost. The problem is that the regulator generates a voltage drop. The output voltage of the regulator will thus be smaller than the smallest possible input voltage. In this case this would mean for a power supply level that varies from 0.9 V to 1.6 V that the regulated voltage would be close to 0.8 V. This extra drop of 100 mV has a significant impact on the still achievable performance of the RF, analog and digital circuitry. The speed performance of e.g. a D-flip-flop configured as divide-by-2 block decreases for instance with a factor 2 for a power supply level change from 0.9 V to 0.8 V.

The consequences of not being able to use a switching power supply converter or a linear regulator is that the only remaining alternative is to work directly from an unregulated power supply. This is a situation that is in general not commonly used for wireless systems. It are however the extreme requirements of ultra-low power consumption, and miniature size that dictate this only alternative remaining option of running the RF circuits directly from the battery voltage. The consequences for the circuit designer are significant and two-fold. One is the fact that all circuits will now have to cope with a power supply level variation that is a factor 1.8 between the lowest and highest value, while the circuit properties like e.g. gain or bandwidth should not change much over this range. Second is the fact that any ripple which will be induced on to the power supply by any block that draws some peak current at a certain frequency will directly be picked up by the RF circuits. In this application such ripple can be quite significant. Hearing aids with a high audio gain can draw a significant peak current from the battery. The battery is not capable of instantaneously delivering this peak current and an immediate voltage drop on the battery level will be the result, especially since there is not much room to place a large good quality decoupling capacitor that can level out these variations. A good PSRR will thus be a main requirement for the RF circuits that run here directly from the battery.

5.3. Technology choice

The fact that this FM receiver needs to operate directly from a single cell battery has a strong influence on the technology selection. The first main choice is between a bipolar, BiCMOS technology and a pure CMOS technology. A pure bipolar technology is actually no option since we also need a digital controller

on board and a lot of analog features need to be digitally programmable which is best implemented with MOS switches. The trade-off between using a BiCMOS or CMOS technology is mainly determined by the V_T values of the MOS transistors under consideration. As soon as the V_T of both the nMOS and pMOS is significantly under the V_{BE} of a bipolar transistor, it will be easier to realize the operation at 0.9 V in the CMOS technology. In this case a 0.25 μm CMOS technology has been selected with a medium V_T transistor option. The latter makes that transistor with a V_T of 300 to 400 mV are available. This gives the possibility to generate just enough overdrive at 0.9 V to achieve the operation at 225 MHz. The drawback is that these device show more leakage, but in combination with the standard transistors that have 500 to 600 mV V_T the circuits leakage can be optimized.

A 0.18 μm CMOS technology would have these lower V_T transistors standard available. Since it is capable of handling 1.8 V power supplies it is also suited to work directly from the zinc-air battery. There is however not a lot of added advantage compared to a 0.25 μm CMOS with medium V_T option. Since we have to work with smallband FM modulation in this application 1/f noise is a critical factor in all circuits blocks and minimum length transistors are seldom used, even in such a critical circuit as the RF mixer. The blocks that would benefit directly in power consumption are high speed digital circuits, mainly the prescaler in the PLL. The drawback of using a 0.18 μm CMOS is of course a higher cost, while the chip area would remain the same since more than 70 % of the area is occupied by linear capacitors anyway and these do not really scale down in succeeding technology generations.

Going further down in technology feature size is in this case not really an option. There is of course the further increasing cost, but additionally there is the power supply level of 1.6 V that cannot be handled by a 0.13 um CMOS technology. An extra on-chip regulator would be needed using thicker oxide transistors to come to the allowed 1.2 V power level. For the 225 MHz smallband application discussed here there is no need for this. More broadband higher frequency applications, working e.g. at 2.4 GHz, could benefit from the faster devices.

A final note on the technology is on the variations to be expected over the processing conditions. The relative wide power supply level variation, almost a factor 2, will already result in enormous variations of analog properties if no appropriate circuits techniques are used. The low power supply level adds to this fact that the used overdrive voltages will be small and thus the relative variations become larger for the same variation on the V_T's over the processing conditions.

5.4. Low power consumption

The front-end of this FM receiver is a low-IF topology without mirror signal suppression. The main reason for not doing any mirror signal suppression is to save power. This comes at the cost of a 3 dB higher noise level. An occupied mirror channel is treated the same as when the selected channel is occupied. The user will have to switch channel. The IF filter is an 8th order low noise bandpass filter with 25 kHz center frequency.

The back-end contains an FM demodulator followed by an audio filter and both a hearing aid and earphone output driver. The FM demodulator uses an analog delay line specifically designed for its low noise operation. An automatic frequency control loop sets the delay time and thus tracks the deviations on the 25 kHz IF frequency by checking that no DC level remains present after FM demodulation. The core of the audio filter uses a programmable switched-cap implementation, preceded by an continuous time passive anti-aliasing filter and followed by a continuous time active smoothing filter and highpass filter. The hearing aid driver generates a signal that can be further amplified and processed by the hearing aid itself, while the earphone output allows to drive 1.5 mA directly into an earphone without the need of using a hearing aid. A squelch circuit is also present in the back-end. This shuts off the audio output when the signal quality becomes too low.

A dedicated digital controller is on board. After a power on reset this controller temporarily switches on a voltage doubler to download the content of an external EEPROM that is 3D mounted on this chip as bare die. After this data download the voltage doubler is switched-off again to preserve power and prevent the addition of a switching ripple on the power supply. A two-way inductive link is also present. This is a short range low data rate wireless digital interface that is used to allow for remote control of the device by the user. Actions that can be performed by the user are for instance switch to the next available channel or scan all available channels. The same inductive link can also be used in a two-way mode for servicing and optimization of the settings by an audiologist. In this mode commands can be given that switch on the voltage doubler. Reading from and writing to the EEPROM via the wireless link becomes then possible.

In order to obtain an ultra low power consumption, specific design techniques have been used in the LNA, VCO and synthesizer. The schematic of the implemented LNA with the antenna and its matching network is given in Fig. 6. The antenna is a high Q inductor wounded on a ferrite core. The Q of the antenna is about 100 giving a significant increase of the voltage level that is applied to the LNA's input transistor. The resonance frequency is set by laser

trimming an external capacitor. The Q-factor of the input circuitry is so high that only a frequency band of 1 MHz is selected. In order to extend the frequency band of operating an on-chip capacitor bank is used to dynamically track the channel frequency by changing each time this bank setting together with changing the synthesizer frequency setting.

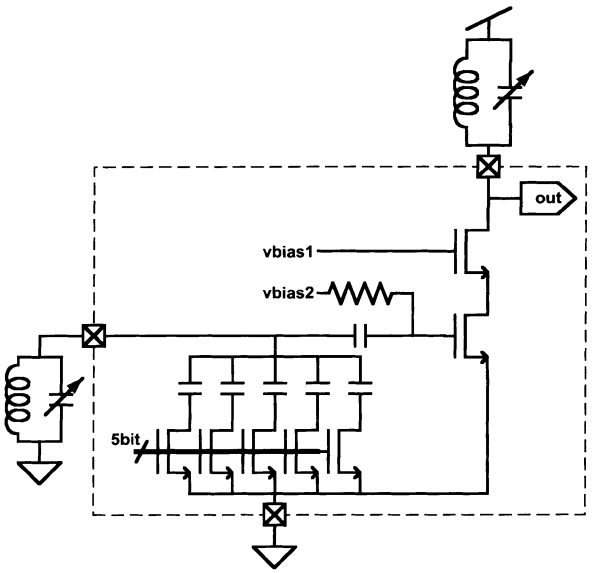

Fig.6. Schematic of the LNA.

For the VCO an LC VCO is used with external inductors to have a sufficiently high Q factor. Its schematic is shown in Fig. 7. The use of high Q external inductors is the only way to keep the power consumption low. The 0.9 V power supply makes that we can only use a small tuning range. Taking into account the charge pumps limitations, the useful range is from 300 mV to 650 mV. This small range makes that we need to use a relative high K_{VCO} of 50 MHz/V. An external laser trimmed capacitor is used to set the band of operation and makes that the varicaps can remain small. The varicap that is used is a pMOS operating in inversion mode. The relative large K_{VCO} makes this VCO sensitive to power supply variations. This is reduced as much as possible by using the cascoded current source. The 0 volt DC biasing of the resonance tank makes it also less dependent on power supply variation and by having the loop filters ground not connected to the on-chip ground and substrate, but via an extra bondpad to the external ground of the VCO we further ensure that the PSRR is good.

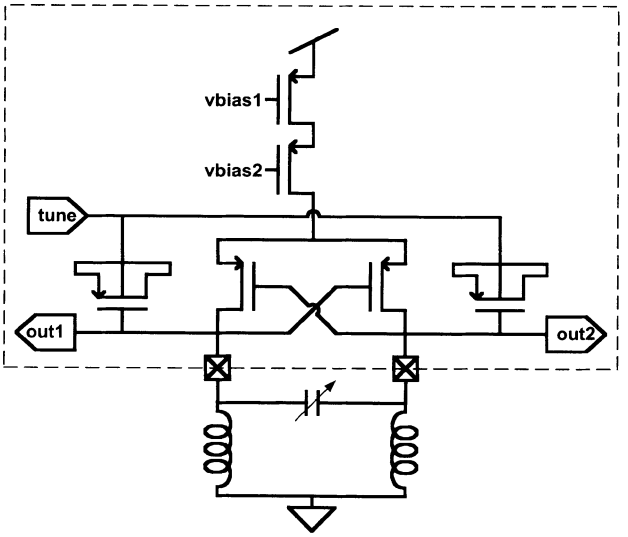

Fig.7. Schematic of the LC VCO.

5.5. Alternatives to direct battery operation

To run directly from the single cell zinc-air battery is not for all blocks in this application the most suited solution. The low frequency audio signal processing blocks in the back-end could run from a regulator that keeps the voltage constant between 0.8 V and 0.9 V. This would give these blocks an improved PSRR, but since this is far less critical than the PSRR of the synthesizer, this option has not been taken.

A block that needs a higher power supply level than 0.9 V is the EEPROM that stores a number of programmable settings. In this case an external EEPROM is used that is 3D mounted onto the FM receiver chip. This EEPROM requires at least 1.8 V power supply, its current consumption is limited to 1 mA. This can be easiest realized with a capacitive voltage doubler if transistors are available that can withstand 3.2 V. 3.2 V can occur since the highest possible battery level will also be doubled. A capacitive voltage conversion circuit is, unless specifically designed for it, not a regulated system and the output will be an integer multiple or a fraction of integers of the input. In this case this is no problem for the EEPROM that can handle a wide range of power supply variation. Such a capacitive voltage doubler has been implemented here, using 2 external capacitors. The main problem of this voltage doubler is that it generates a switching ripple on the power supply. This is solved here by having the EEPROM and the voltage doubler only switched on directly after a power-on reset. The dedicated controller initiates at that moment a full download of the EEPROM contents into its RAM and directly after that the EEPROM and the

voltage doubler is switched off again. Only after the voltage doubler has been switched off, audio reception is switches on.

A second block that uses voltage doublers is the switched-cap programmable audio filter. The block itself is not fed from a doubled power supply, but the clock signals to the switches are doubled. The main difference is that these signals do not draw a lot of power since these are small capacitive loads. The consequence is that clock doublers do not really introduce a significant switching ripple on the power supply, while they can allow for a significant increase of the signal swing that can be used in the switched cap circuits. An increased signal swing results directly in a scaling down of area and power for a given signal-to-noise requirement [6]. The condition is again that transistors must be available that can handle 3.2 V. If not, alternative techniques, like switched-opamp can be used to increase to usable signal swing [10].

There are a number of switches for which it is not preferable to use a thicker oxide transistor such that they are able to handle the double power supply. These are RF switches; switches that are used in RF circuits that need to handle high frequency signals and for which their Q-factor is of high importance. Examples are a switched capacitor bank to trim the center frequency of a resonance tank in e.g. an LNA or VCO. In order to achieve the highest possible Q-factor, these switches do need to get the highest overdrive voltage possible all the time. In the case of this 0.25 μm CMOS technology, the highest possible allowed voltage with the standard transistors is 2.5 V. This situation can be solved by applying the voltage doubling on a signal that has been regulated first. Again, the current requirement for driving these switches is low. In this case the regulated voltage can be the bandgap reference signal. A 1.2 V bandgap reference signal is highly stable over power supply and temperature and in a doubled version it will result in a 2.4 V drive signal for the RF switches that is close to the maximum overdrive possible, while it does not vary much with power supply variations.

5.6. PSRR requirements due to direct battery operation

For the LNA and mixer the interference of power supply signals is only a second order problem. It is only in combination with a limited linearity that low frequency power supply noise can be mixed up to the high operating frequencies of the RF carrier. In most cases the received signals will be rather small and no effect will be present. When large signals would be received, the relative impact of the interfering power supply signals would be small.

The synthesizer is far more critical towards the rejection of power supply noise that is picked up. Power supply noise can generate jitter on the local oscillator

signal, visible as spurii. Depending on their frequency these spurii will either introduce a distortion of the received audio signal or a reduction of the selectivity of the receiver. These effects will be present for both small and large received input signal levels.

The synthesizer architecture is shown in Fig. 8. The synthesizer is a fractional-N synthesizer that uses a relative high comparison frequency of about 8 MHz. This allows for the use of a high PLL loop bandwidth of 30 kHz. This high loop bandwidth works as an advantage to keep the close-in phase noise low. This is a critical issue since we use smallband operation here. Smallband operation needs a low close-in phase noise, but the MOS transistors 1/f noise makes it more difficult to achieve this. The high loop bandwidth gives extra suppression to this 1/f noise. The high loop bandwidth makes it also possible to integrate the loop filter on chip. This is critical since 5 extra external components would compromise the miniaturization possibilities. The LC VCO operates at the double frequency. It is followed by two CML logic dividers. A MUX makes it possible to receive frequencies in a range from 72 MHz to 225 MHz. The values of the external components determine which frequency band is actually selected.

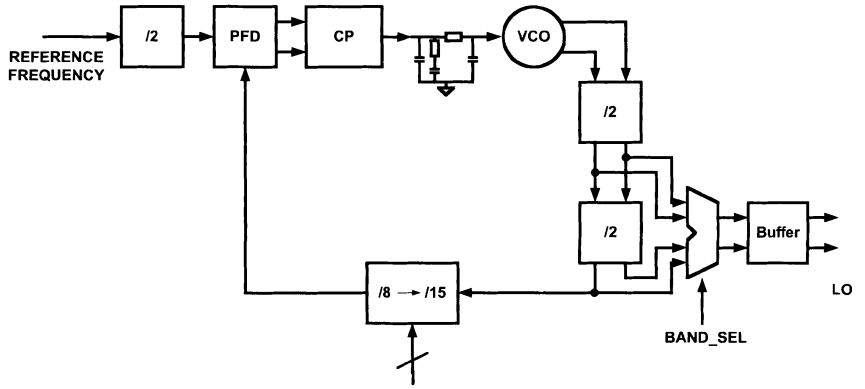

Fig.8. Architecture of the synthesizer.

How the PSRR of the VCO is kept high was already described in section 5.4. Other blocks that are critical for the PSRR of the synthesizer are the logic gates in the reference and PLL feedback path. Different from the VCO, the spurii they introduce are not suppressed within the PLLs loop bandwidth. Fig. 9 shows the delay times of a NAND and a D-flipflop used as divider. The delay time is given in function of the power supply level for the 0.25 μm technology that we use here. At 1 V and below you can see a dramatic increase in delay time since the power supply level is coming close to the sum of the nMOS and pMOS V_T threshold values. This does imply that at 1 V and below variations on the power

supply will create significant timing jitter on the digital signals. In the synthesizer such jitter translates itself into an FM modulation of the carrier frequency according the following expression:

$$\ddot{A}f_{dev} = 2\partial \cdot \ddot{A}t_d \cdot f_{LO} \cdot f_{mod} \quad (1)$$

Remark that this means that the sensitivity of the divide-by-2 block towards power supply noise is independent of the frequency it operates on. A divider in the reference path working at 8 MHz has the same impact on PSRR as for instance a divider that works in the PLLs feedback path at 60 MHz. Careful design, scaling and optimisation of the logic used in the synthesizer is thus important.

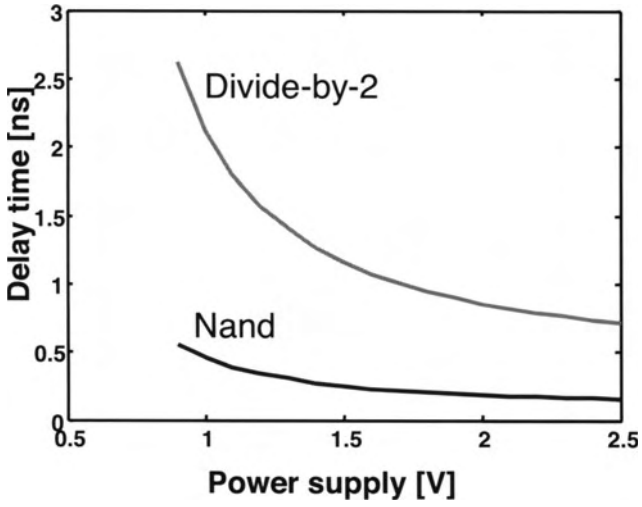

Fig.9. Delay time of digital cells i.f.o. the power supply.

Fig. 10 shows for instance how the PSRR of the divide-by-2 block used in the synthesizers reference frequency path can be significantly improved. The output of the divider is recombined with the input signal in a NAND gate, such that the transition of the output signals falling edge is now determined directly by the input signal and delayed only by the NAND. The succeeding block is a phase-frequency detector that is only sensitive to falling edges. The function of the divider is now only to generate a signal that can be used to suppress half of the edges of the input signal. The smaller delay time and delay time variation of the NAND results in an improved PSRR. The same goes for the prescaler that is used. The bottom part in Fig. 11 is a traditional prescaler topology. The classical output of this prescaler is now used in combination with other internal states of

the prescaler to generate signals that can be used to suppress a selected number of the input signals edges. An actual transition of the output signal will be triggered through the critical path that is shown at the top. This limits the delay time and the delay time variation to that of only 3 NANDs and an inverter.

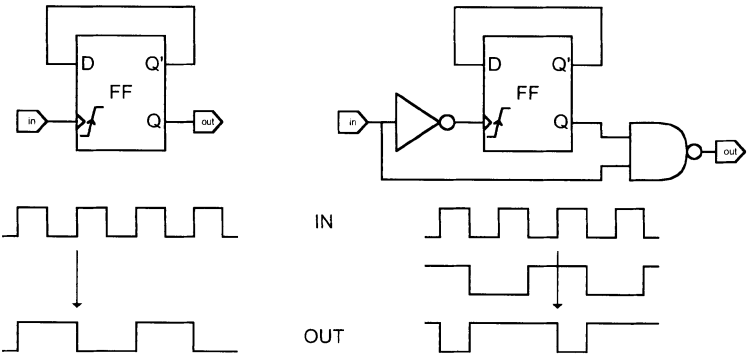

Fig.10. Improved PSRR design of a divide-by-2 block.

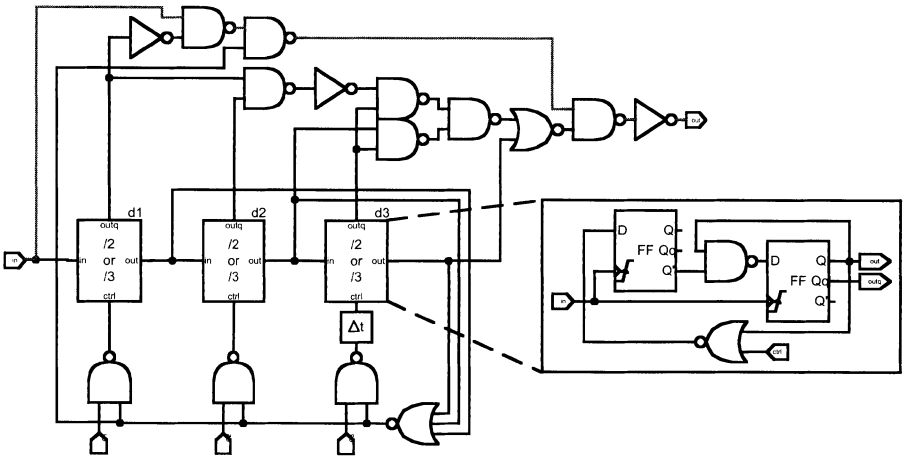

Fig.11. Improved PSRR design of a prescaler.

5.7. Results of the realization

Fig. 12 shows a microphotograph of the chip. The RF front-end with the LNA, mixer and synthesizer, including the loop filter, is located on the left side. The chip is realized in a 0.25 µm CMOS technology and is 22.7 mm^2 large. What is clearly visible here is that a large part of the chip area, in fact more than 70 %,

is taken up by capacitors. Main area consumers are the loop filter, the IF filter which needs the capacitor area for low noise and the back-end that contains a continuous time 100 Hz AFC loop filter and a 30 Hz audio highpass filter.

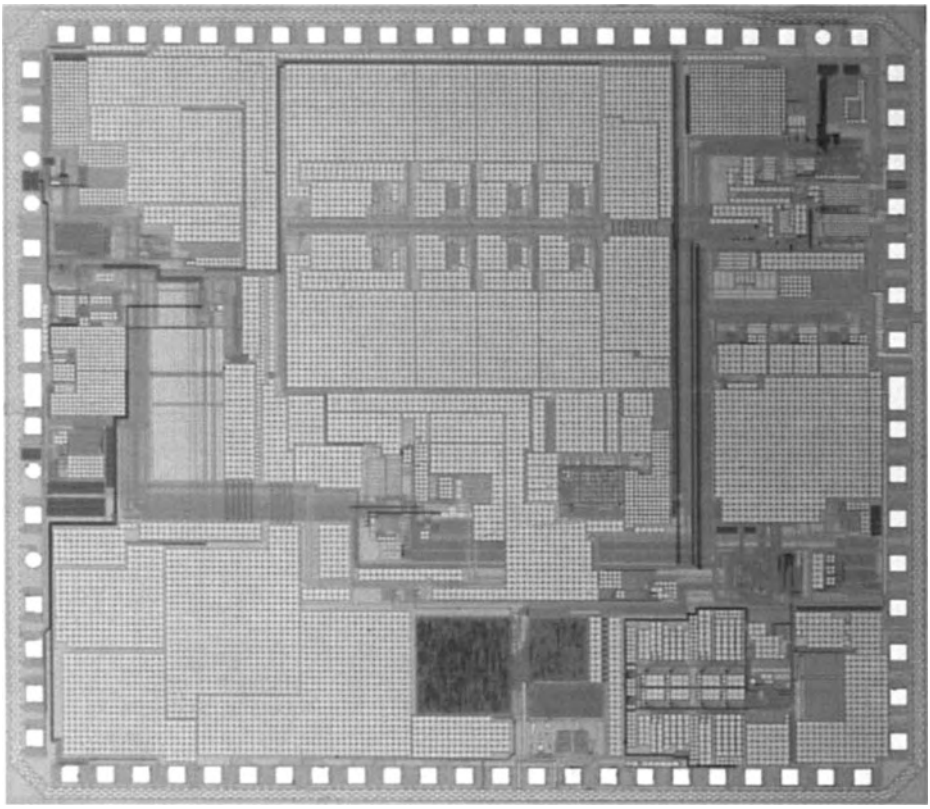

Fig.12. Microphotograph of the FM receiver.

Table 1 gives an overview of the chips main properties and measurement results. The chip operates from 0.9 V to 1.6 V. Off-mode current is 1.5 μA. Active-mode current including front-end and back-end signal processing is 2.2 mA. The carrier frequency can vary from 72 MHz to 225 MHz. The actual band of operation is selected with the external component values and synthesizer settings. Fig. 13 shows the audio output signal to noise ratio in function of the input signal power for an audio bandwidth of 7.5 kHz. At high levels the SNR is limited to 43 dB. This is determined by the close-in phase noise of the synthesizer. At small input signal levels a 10 dB SNR is achieved at –103 dBm. The RF bandwidth is at least 7 MHz. The audio bandwidth is programmable between 5.5 kHz and 7.5 kHz. The measured total harmonic distortion is 2 % for an input signal with a 5 kHz FM deviation. The remote controls sensitivity is 50 $\mu V_{pp,diff}$.

Supply voltage	0.9 V - 1.6 V
Off-mode current	1.5 µA
Active-mode current	2.2 mA
Carrier frequency	72 MHz - 225 MHz
SNR	43 dB
Sensitivity	-103 dBm
RF bandwidth	7 MHz
Audio bandwidth	5.5 kHz - 7.5 kHz
THD	2 %
RCo/RP sensitivity	50 µVpp, diff
Chip size	22.7 mm^2

Table 1. Main properties of the FM receiver.

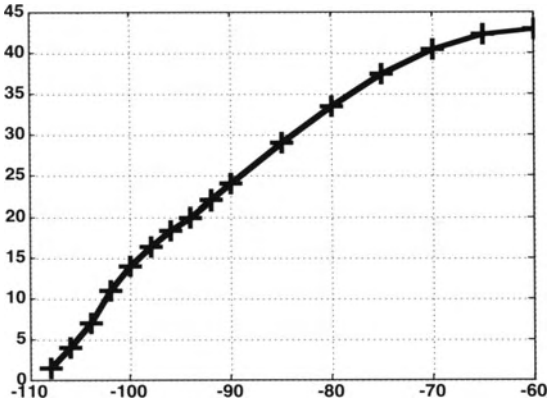

Fig.13. SNR in function of the input signal power.

6. Conclusions

Power management is an essential part of the design of any wireless system. In this paper the importance of selecting the most suited power supply level has been discussed in combination with how this power supply level can be generated with a regulator that is suited for RF circuitry. With an example of a miniature ultra low power FM receiver it has been demonstrated how running directly from the battery without any regulation has an enormous impact on the choices to be made for the wireless system. Especially the PSRR of the synthesizer is a most critical parameter, even influenced by the digital circuitry used in the PLL loop. Circuit design techniques have been introduced that improve the PSRR of the synthesizer significantly.

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