USING AN INTEGRATED CONTROLLER IN THE DESIGN OF MAG-AMP OUTPUT REGULATORS

By
Robert A. Mammano, Unitrode IC Corp.
Charles E. Mullett, Mullet Associates, Inc.

Magnetic amplifier technology dates back considerably further than transistors but its wide-spread use has been slow in developing. While many factors may have been responsible for this, at least one — the high cost of tape-wound magnetic cores — has been alleviated with significant recent price reductions and the introduction of less expensive materials. And now, another one — the problems in designing effective control loops utilizing mag amps as voltage regulators — has fallen with the introduction of an IC dedicated to mag amp control — the UC1838.

While there are many types of power supply applications where mag amps may effectively be used, one of the most popular current uses is as a secondary regulator in multiple output power supplies configured as shown in Figure 1. The problem with multiple outputs stems from the fact that the open-loop output impedance of each winding, rectifier, and filter is not zero. Thus, if one assumes that the overall feedback loop holds the output of V_{01} constant, then increasing the loading on V_{01} will cause the other outputs to rise as the primary circuit compensates; similarly; increasing the loading on any of the other outputs will cause that output to droop as the feedback is not sensing those outputs. While these problems are minimized by closing the feedback loop on the highest power output, they aren't eliminated and auxiliary, or secondary regulators are the usual solution. A side benefit of secondary regulators, particularly as higher frequencies reduce the transformer turns, is to compensate for the fact that practical turns ratio may not match the ratio of output voltages. Clearly, adding any form of regulator in series with an output adds additional complexity and power loss. Mag amps are a hands down winner in both areas.

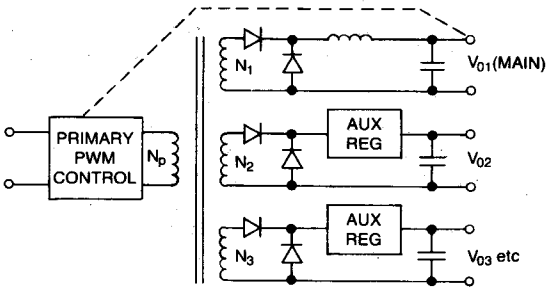

Figure 1. A typical multiple output power supply architecture with overall control from one output.

MAG AMP VOLTAGE REGULATORS

Although called a magnetic amplifier, this application really uses an inductive element as a controlled switch. A mag amp is a coil of wire wound on a core with a relatively square B-H characteristic. This gives the coil two operating modes: when unsaturated, the core causes the coil to act as a high inductance capable of supporting a large voltage with little or no current flow. When the core saturates, the impedance of the coil drops to near zero, allowing current to flow with negligible voltage drop. Thus a mag amp comes the closest yet to a true "ideal switch" with significant benefits to switching regulators.

Before discussing the details of mag amp design, there are a few overview statements to be made. First, this type of regulator is a pulse-width modulated down-switcher implemented with a magnetic switch rather than a transistor. It's a member of the buck regulator family and requires an output LC filter to convert its PWM output to DC. Instead of DC for an input, however, a mag amp works right off the rectangular waveform from the secondary winding of the power transformer. Its action is to delay the leading edge of this power pulse until the remainder of the pulse width is just that required to maintain the correct output voltage level. Like all buck regulators, it can only subtract from the incoming waveform, or, in other words, it can only lower the output voltage from what it would be with the regulator bypassed. As a leading-edge modulator, a mag amp is particularly beneficial in current mode regulated power supplied as it insures that no matter how the individual output loading varies, the maximum peak current, as seen in the primary, always occurs as the pulse is terminated.

MAG AMP OPERATION

Figure 2 shows a simplified schematic of a mag amp regulator and the corresponding waveforms. For this example, we will assume that N_S is a secondary winding driven from a square wave such that it provides a ± 10 volt waveform at v_t. At time $t = 0$, v_t switches negative. Since the mag amp, L1, had been saturated, it had been delivering $+10V$ to v_3 prior to $t = 0$ (ignoring diode drops). If we assume $v_c = -6V$, as defined by the control circuitry, when v_t goes to $-10V$, the mag amp now has four volts across it and reset current from v_c flows through D1 and the mag amp for the 10 μS that v_t is negative. This net four volts for 10 μS drives the mag amp core out of saturation and resets it by an amount equal to 40V-μS.

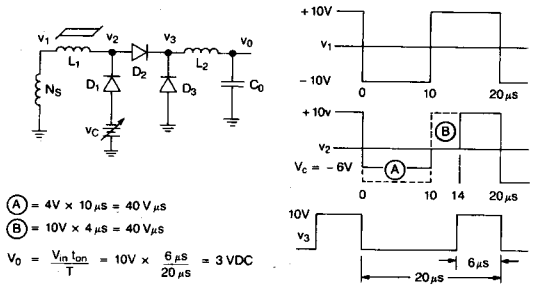

Figure 2. A simplified mag amp regulator and characteristic waveforms.

When t = 10 μS and v_1 switches back to +10V, the mag amp now acts as an inductor and prevents current from flowing, holding v_2 at 0V. This condition remains until the voltage across the core — now 10 volts — drives the core back into saturation. The important fact is that this takes the same 40 volt-μS that was put into the core during reset.

When the core saturates, its impedance drops to zero and v_1 is applied to v_2 delivering an output pulse but with the leading edge delayed by 4 μS.

Figure 3 shows the operation of the mag amp core as it switches from saturation (point 1) to reset (point 2) and back to saturation. The equations are given in cgs units as:

N = mag amp coil turns
Ae = core cross-section area, cm^2
ℓe = core magnetic path length, cm
B = flux density, gauss
H = magnetizing force, oersteads

The significance of a mag amp is that reset is determined by the core and number of turns and not by the load current. Thus a few milliamps can control many amps and the total power losses as a regulator are equal to the sum of the control energy, the core losses, and the winding I^2R loss — each term very close to zero relative to the output power.

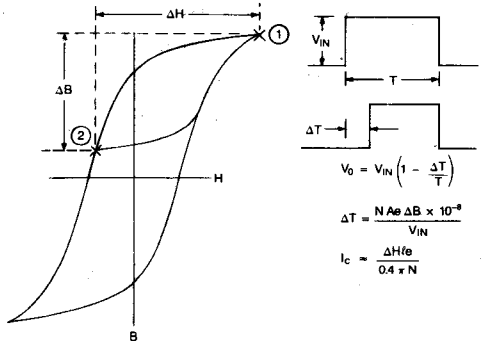

Figure 3. Operating on the B-H curve of the magnetic core.

Figure 4 shows how a mag amp interrelates in a two-output forward converter illustrating the contribution of each output to primary current. Also shown is the use of the UC1838 as the mag amp control element.

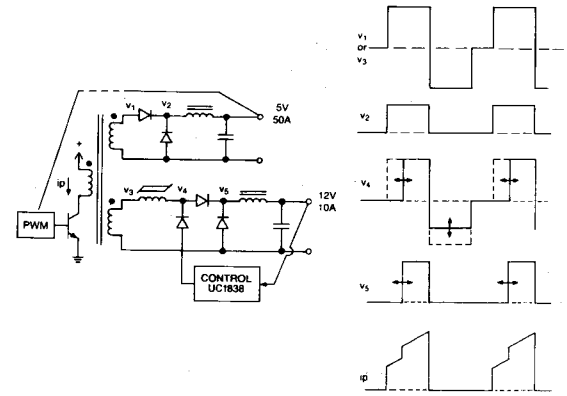

Figure 4. Control waveforms for a typical two-output, secondary regulated, forward converter.

THE UC1838 MAG AMP CONTROLLER

While bringing no major breakthroughs in either integrated circuit or power supply technology, the UC1838 provides a low-cost, easy-to-use, single-chip solution to mag amp control. The block diagrams of this device, as shown in Figure 5, includes three basic functions:

1. An independent, precise, 2.5V reference
2. Two identical, high-gain operational amplifiers
3. A high-voltage PNP reset current driver.

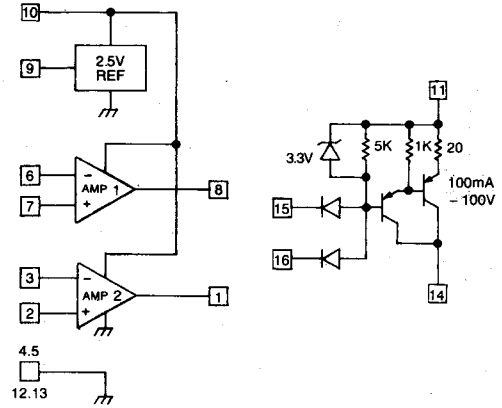

Figure 5. The block diagram of the UC1838 mag-amp control integrated circuit.

The reference is a common band-gap design, internally trimmed to 1%, and capable of operating with a supply voltage of 4.5 to 40 volts. The two op amps are identical with a structure as shown simplified in Figure 6. These amplifiers have PNP inputs for a common mode input range down to slightly below ground and have class A outputs with a 1.5 MA current sink pull down. The open loop voltage gain response, as shown in Figure 7, has a nominal 120 dB of gain at DC with a single pole roll-off to unity at 800 KHz. These amplifiers are unity-gain stable and have a slew rate of 0.3 V/μS.

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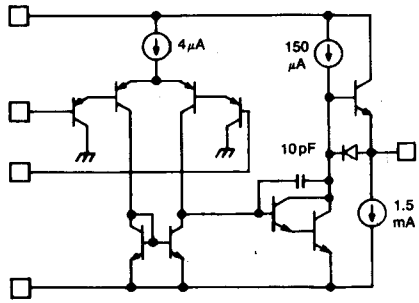

Figure 6. Simplified schematic of each of the operational amplifiers contained within the UC1838.

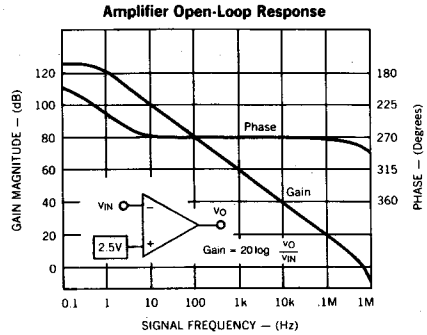

Figure 7. Open-loop gain and phase response for the UC1838 op amps.

Two op amps are included to provide several design options. For example, if one is used to close the voltage feedback loop, the other could be dedicated to some protective function such as current limiting or over-voltage shutdown. Alternatively, if greater loop gain is required, the two amplifiers could be cascaded.

The PNP output driver can deliver up to 100 MA of reset current with a collector voltage swing of as much as 80 volts negative (within the limits of package power dissipation). Remembering that the mag amp will block more volt-seconds with greater reset, pulling the input of the driver low will attempt to reduce the output voltage of the regulator. Thus, there are two inputs, diode "OR" ed to turn on the driver, turning off the supply output.

With internal emitter degeneration, this reset driver operates as a transconductance amplifier providing a reset current as a function of input voltage as shown in Figure 8. The frequency response of this circuit is plotted in Figure 9 showing flat performance out to one megahertz.

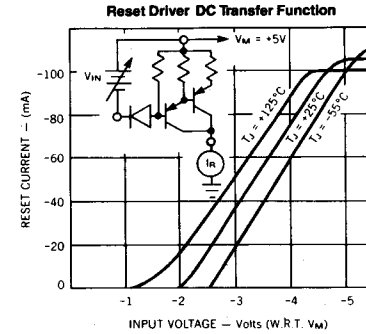

Figure 8. Transconductance characteristics of the UC1838 reset current generator.

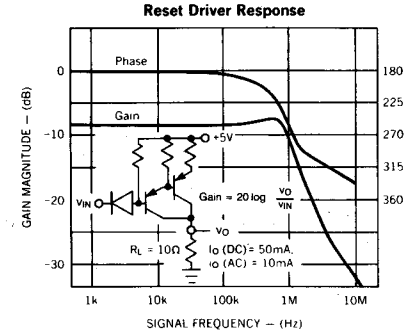

Figure 9. Reset driver frequency response.

Current limiting to protect the output driver is achieved by means of the 3.5 V Zener clamp (which is temperature compensated to match two VBE's) in conjunction with the 20Ω emitter resistor. It should be noted that thermal shutdown is purposely not included since protecting the driver by turning it off would mean losing control of the power supply output. Pin 11 — the emitter of the driver — can be connected to any convenient voltage source from 5VDC to the level used to supply the op amps. Note that the op amp supply must be at least 2 volts higher than the DC level on the inputs, a point to remember when selecting a location for current sensing. One possible configuration for a complete secondary regulator with shutdown control is shown in Figure 10.

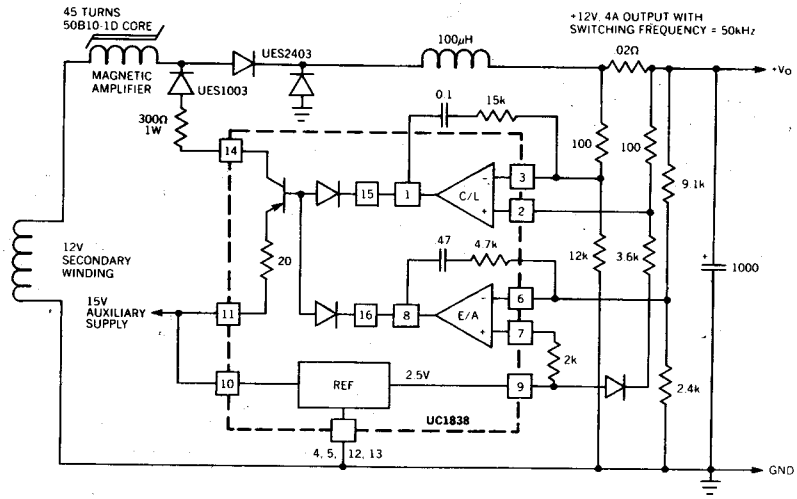

Figure 10. Using the UC1838 to provide both voltage control and over-current shutdown in a typical 12V, 4A regulator.

MAG AMP DESIGN PRINCIPLES

One of the first tasks in a mag amp design is the selection of a core material. Technology enhancements in the field of magnetic materials have given the designer many choices while at the same time, have reduced the costs of what might have been ruled out as too expensive in the past. A comparison of several possible materials is given in Figure 11. Some considerations affecting the choices could be:

1. A lower Bmax requires more turns — less important at higher frequencies since fewer turns are required.
2. Higher squareness ratios make better switches
3. Higher I_M requires more power from the control circuit
4. Ferrites are still the least expensive
5. Less is required of the mag amp if it only has to regulate and not shut down the output completely

MATERIALS

Example: Similar Toroids, 1" O.D., 0.75" I.D., 0.25" High, 25KHz, 20V.

Trade Name	Composition	Bmax (kG)	Core Loss @ Bmax	Squareness Ratio	Turns Req'd	I_M (A)
Sq. Permalloy 80	79% Ni, 17% Fe	7	1.2W	0.9	19	0.04
Supermalloy	78% Ni, 17% Fe, 5% Mo	7	1.0W	0.55	19	0.03
Orthonol	50% Ni 50% Fe	14	7.2W	0.97	10	0.39
Sq. Metglass	Fe, B	16	7.6W	0.5	9	0.06
Power Ferrites	Mn, Zn	4.7	1.8W	0.4	11	0.1
Sq. Ferrite (Fair-Rite #83)	Mn	3.9	2.8W	0.9	13	0.4

Figure 11. A comparison of several types of core materials available for mag amp usage.

In addition to selecting the core material, there are additional requirements to define, such as:

1. Regulator output voltage
2. Maximum output current
3. Input voltage waveform including limits for both voltage amplitude and pulse width
4. The maximum volt-seconds — called the "withstand area," Λ — which the mag amp will be expected to support

With these basic facts, a designer can proceed as follows:

1. Select wire size based on output current. 400 amp/cm² is a common design rule.
2. Determine core size based upon the area product:

$$AwAe = \frac{Ax \times \Lambda \times 10^8}{\Delta B \times K} \quad \text{where}$$

Aw = Window area, cm²
Ae = Effective core area, cm²
Ax = Wire area, (one conductor) cm²
Λ = Required withstand area, V-sec
ΔB = Flux excursion, gauss
K = Fill factors ≈ 0.1 to 0.3

3. Calculate number of turns from

$$N = \frac{\Lambda \times 10^8}{\Delta B \times Ae}$$

4. Estimate control current from

$$Ic \approx \frac{Hle}{0.4\,\pi\,N} \quad \text{where}$$

l_e = core path length, cm
H is taken from manufacturer's curves. Note that it increases with frequency.

5. Check the temperature rise by calculating the sum of the core loss and winding loss and using

$$\Delta T \approx \frac{P \text{ watts}^{0.8}}{A \text{ (surface) cm}^2} \times 444°C$$

6. Once the mag amp is defined, it can be used in the power supply to verify I_C and to determine the modulator gain so that the control requirements may be determined.

9

COMPENSATING THE MAG AMP CONTROL LOOP

The mag amp output regulator is a buck-derived topology, and behaves exactly the same way with a simple exception. Its transfer function contains a delay function which results in additional phase delay which is proportional to frequency.

Figure 12 shows the entire regulator circuit, with the modulator, filter, and amplifier blocks identified. The amplifier, with its lead-lag network, is composed of the op-amp plus R1, R2, R3, C1, C2, and C3. The modulator, for the purpose of this discussion, includes the mag amp, the two rectifier diodes, plus the reset driver circuit which is composed of D1, Q1, and R7.

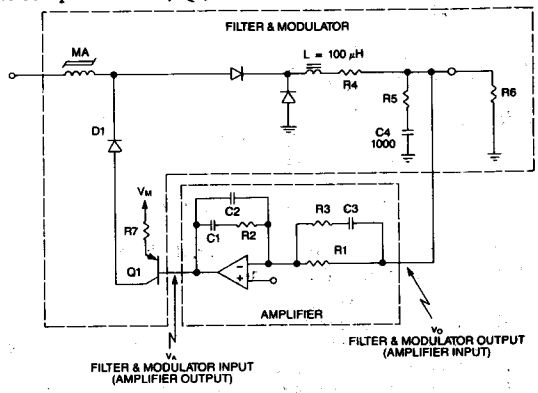

Figure 12. Schematic diagram of a typical regulator control loop.

The basic filter components are the output inductor (L) and filter capacitor (C4) and their parasitic resistances R4 and R5. For this discussion, a 20 KHz, 10 Volt, 10 Amp regulator is used. The output inductor has been chosen to be 100 μH, the capacitor is 1000 μF and each has .01 ohms of parasitic resistance. The load resistor (R6) of 1 ohm is included since it determines the damping of the filter.

The purpose of proper design of the control loop is to provide good regulation of the output voltage, not only from a dc standpoint, but in the transient case as well. This requires that the loop have adequate gain over as wide a bandwidth as practical, within reasonable economic constraints. These are the same objectives we find in all regulator designs, and the approach is also the same.

A straightforward method is to begin with the magnitude and phase response of the filter and modulator, usually by examining its Bode plot. Then we can choose a desired crossover frequency (the frequency at which the magnitude of the transfer function will cross unity gain), and design the amplifier network to provide adequate phase margin for stable operation.

Figure 13 shows a straight-line approximation of the filter response, ignoring parasitics. Note that the corner frequency is $1/(2\pi\sqrt{LC})$, or 316 Hz, and that the magnitude of the response "rolls off" at the slope of -40 dB per decade above the corner frequency. Note also that the phase lag asymptomatically approaches 180 degrees above the corner frequency.

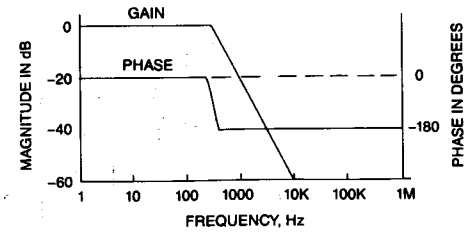

Figure 13. Output filter response.

To include the effects of the mag amp modulator, we must consider the additional phase shift inherent in its transfer function. This phase delay has two causes:

1. The output is produced after the reset is accomplished. We apply the reset during the "backswing" of the secondary voltage, and then the leading edge of the power pulse is delayed in accordance with the amount of reset which was applied.
2. The application of reset to the core is a function of the impedance of the reset circuit. In simple terms, the core has inductance during reset which, when combined with the impedance of the reset circuit, exhibits an L-R time constant. This contributes to a delay in the control function.

The sum of these two effects can be expressed as:

$$\varnothing m = -(2D + \alpha)\frac{\omega}{\omega_S}, \text{ where}$$

$\varnothing_M$ = Modulator phase shift
D = Duty ratio of the "off" time
α = resetting impedance factor: = 0 for a current source; = 1 when resetting from a low-impedance source; and somewhere in between for an imperfect current source.
ω_S = $2\pi f_S$, where f_S = the switching frequency.

When the unity-gain crossover frequency is placed at or above a significant fraction (10%) of the switching frequency, the resultant phase shift should not be neglected. Figure 14 illustrates this point. With $\alpha = 0$, we insert no phase delay, and with $\alpha = 1$ we insert maximum phase delay, which results from resetting from a voltage source (low impedance). The phase delay is minimized in the UC1838 by using a collector output to reset the mag amp.

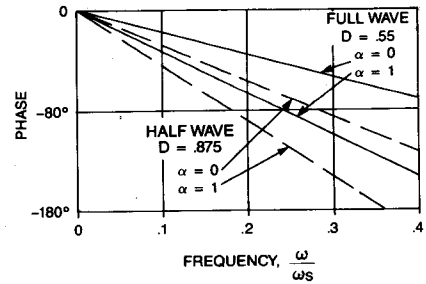

Figure 14. Mag amp phase shift.

It is difficult to include this delay function in the transfer function of the filter and modulator. A simple way to handle the problem is to calculate the Bode plot of the

filter/modulator transfer function without the delay function, and then modify the phase plot according to the modulator's phase shift.

Using this technique, the Bode plot for the modulator and output filter of this example has been calculated assuming $\alpha = 0.2$ and $D = 0.6$ yielding the graph of Figure 15.

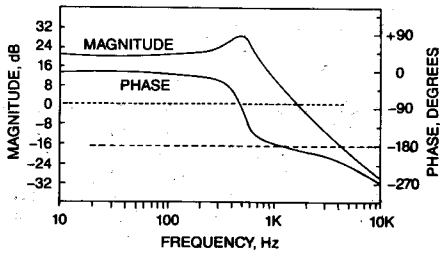

Figure 15. Filter-modulator response including the effects of mag amp phase delay.

If we now close the loop with an inverting error amplifier, introducing another 180 degrees of phase shift, and cross the unity gain axis above the corner frequency, we will have built an oscillator — unity gain and 360 degrees of phase shift.

An alternative, of course, is to close the loop in such a way as to cross the unity-gain axis at some frequency well below the corner frequency of the filter, before its phase lag has come into play. This is called "dominant pole" compensation. It will result in a stable system, but the transient response (the settling time after an abrupt change in the input or load) will be quite slow.

The amplifier network included in Figure 12 allows us to do a much better job, by adding a few inexpensive passive parts. It has the simplified response shown in Figure 16. The phase shift is shown without the lag of 180 degrees inherent in the inversion. This is a legitimate simplification, provided that we use an overall lag of 180 degrees (not 360 degrees) as our criterion for loop oscillation.

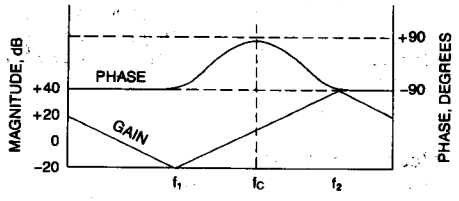

Figure 16. Compensated amplifier frequency and phase response.

The important point is that this circuit provides a phase "bump" — it can have nearly 90° of phase boost at a chosen frequency, if we provide enough separation between the corner frequencies, f1 and f2. This benefit is not free, however. As we ask for more boost (by increasing the separation between f1 and f2) we demand more gain-bandwidth of the amplifier.

DESIGN EXAMPLE

An 8V, 8A Output Derived from a 12V Output — 20 KHz Push-Pull Converter

This example uses the UC1838 to control a full-wave mag amp output regulator, with independent shutdown current limiting. Capsule specifications are as follows:

INPUT: PWM quasi-square wave which, without the magamp, produces 12 Vdc.

OUTPUT: 8.0 Vdc ±1% at load currents from 1 to 8A.

OUTPUT RIPPLE: Less than 50 mV p-p.

TRANSIENT RESPONSE: For load changes of 6 to 8 and 8 to 6A, peak excursion of the output shall be less than ±2% and settle to within 1% of the final value within 500 μS.

OUTPUT PROTECTION: The 8V output shall have independent current limiting, so as not to shut down the 12V output when the 8V output is overloaded or short-circuited. It shall recover from the overload automatically when the overload is removed.

Figure 17 shows the proposed circuit approach. A current transformer has been used to sense the overload, simply to illustrate this approach. A simple series resistor of perhaps .01 or .02 ohms would do as well here, but the current transformer is preferred for high-current outputs.

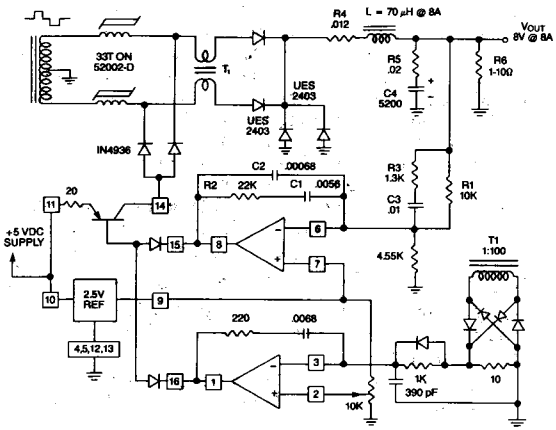

Figure 17. Control and current limiting for a 8V, 8 amp, 20 KHz push-pull converter.

DESIGN APPROACH

With the input waveform already set by the converter design, and the above specifications to define the desired output, the new output circuit will be approached as follows:

1. Draw the preliminary schematic.
2. Design the mag amp.
3. Design the feedback loop.
4. Design the current limiter.
5. Build the breadboard and test it.

PRELIMINARY SCHEMATIC

Figure 17 shows the preliminary circuit diagram. Parasitic resistance of the output filter inductor and capacitor (R4 and R5) are shown, along with the expected feedback com-

pensation elements (R1, R2, R3, C1, C2, and C3). These will be referenced in the mag amp design.

MAG AMP DESIGN

The information necessary to the design is as follows:

1. Input pulse: nominally 32V × 9 μS, = 288 volt-microseconds.
2. Duty ratio of the "off" time: nominally (25 - 9 μS)/ 25 μS = .76, since the frequency at the output is 40 KHz.
3. Output current: 8A.
4. Regulation only, or complete shutdown required? Shutdown.

Comments on the output filter

Design of the output filter is not complicated by the presence of the mag amp. In this case, it was designed with output ripple specs, and capacitor ripple current in mind. Although this design has adequate inductance for continuous conduction of the inductor at minimum load, this is not mandatory. The mag amp, when designed for shutdown, is capable of regulating the output in the discontinuous conduction mode.

Mag amp core selection

1. Wire size: The current waveform in the magamp can be analyzed as follows: During the power pulse, the current is approximately 8A (inaccurate only due to the "tilt" of the top of the current pulse); the duty ratio of this pulse is half the ratio of the output voltage to the pulse height, or .5 × 8/30 = .12. During the dead time between pulses, the inductor current is shared by the rectifier diodes and the "catch" diode. The duty ratio is 1 - 2 × .12 = .76, and the current during this interval is 8/3A. During the remaining interval the current is zero, because the entire 8A is flowing in the other mag amp.

   The rms value of the current can now be computed:

   $$\text{Irms} = \sqrt{8^2 \times .12 + (8/3)^2 \times .76} = 3.62 \text{ A.}$$

   At 400 Amp/cm², a wire area of approx. .0091 cm² is required. 16 gauge wire has an area of .0131 and is chosen for the mag amp.

2. Core selection: An appropriate material at this frequency is square-loop 80% nickel (Square Permalloy 80 or eq.) with a tape thickness of 1 mil. The saturation flux density if this material is 7000 gauss. A fill factor of 0.2 is chosen for the winding. The required area product is:

   $$\text{AwAe} = \frac{\text{Ax} \times \Lambda \times 10^8}{\Delta B \times K} = \frac{.0131 \times 288 \times 10^{-6} \times 10^8}{2 \times 7000 \times 0.2} = .135 \text{ cm}^4$$

   which can be divided by 5.07 × 10^{-6} cm²/C.M. in order to refer to core manufacturer's tables.

   An appropriate core is the Magnetics 52002-10, which (with 1 mil tape thickness) has an area product of .026 × 10^6 C.M. cm². The core area of this core is 0.076 cm².

3. Determine the number of turns: The mag amp must be able to withstand the entire area of the input pulse, which is 288 volt-microseconds.

   $$N = \frac{\Lambda \times 10^8}{2 \times Bm \times Ac} = \frac{288 \times 10^{-6} \times 10^8}{2 \times 7000 \times .076} = 27 \text{ turns.}$$

   Allowing an extra 20% for variations in Bm, pulse dimensions, etc., the winding is chosen to be 33 turns.

FEEDBACK LOOP DESIGN

The key steps in the design of the feedback loop are as follows:

1. Determine the modulator's dc transfer function.
2. Plot the transfer function of the modulator and filter, to determine the gain and phase boost required of the feedback amplifier.
3. Design the feedback amplifier.
4. Plot the results in the form of the closed-loop transfer function.

Plotting the modulator's transfer function can be easily done experimentally with the UC1838 by opening the feedback loop at the input to the Reset Driver and driving this point (pin 15 or 16) directly. For interest, the reset current is also measured with the help of a 1 ohm resistor placed in series with the emitter of the reset transistor (pin 11 of the UC1838). The results are shown in Figure 18, with load resistors of 1 ohm and 10 ohms.

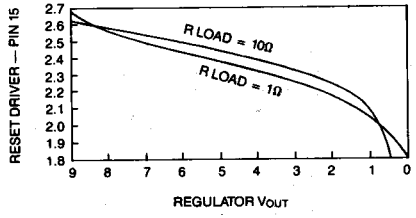

Figure 18. DC gain of the mag amp modulator.

Note that the results are practically the same at both load values. This is to be expected, since the output inductor is still in the continuous conduction mode at the minimum load.

In the region of the desired output (8V and 8A load), the modulator dc gain is approximately 12.5, or 22 dB. In addition to the phase shift of the filter, the modulator contributes additional phase lag! Assuming that we will not attempt to cross unity-gain at a frequency above one-tenth the switching frequency, we can neglect the phase lag due to the impedance of the core and the reset circuit. But we cannot neglect the phase lag resulting from the delay between the time of resetting the core and the time when the core delivers its output:

$$\varnothing_M = 2D \frac{\omega}{\omega_S}, \text{ where}$$

$\varnothing_M$ = Modulator phase shift
D = Duty ratio of the "off" time (.76 in this example)
ω_S = 2 D f_a, where f_a = the switching frequency (40 KHz)

We can use any one of the common circuit analysis programs for analyzing the filter-modulator, neglecting the modulator phase lag when running the program, and then adding it later. Or, the lag may be included in a more sophisticated analysis program. The resultant response prediction is shown in Figure 19.

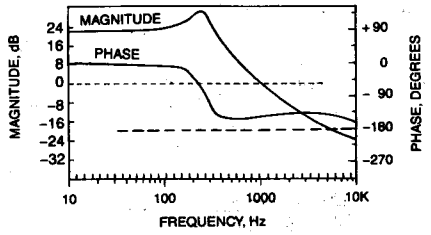

Figure 19. Calculated response plot for the modulator and filter.

Note the shape of the phase response. In the region of 2 KHz the phase lag is decreasing, due to the ESR of the output capacitor. Above 6 KHz the modulator's phase lag becomes important, and the phase lag increases.

Choosing one-tenth the switching frequency for the unity-gain crossover frequency (4 KHz), we can determine the desired gain and phase boost of the feedback amplifier. At 4 KHz, the gain of the modulator is -15 dB (a factor of .179) and the phase shift is -135 degrees. It is generally recommended that there be at least 60 degrees of phase margin at the crossover frequency. This will require reduction of the phase lag to -120 degrees.

In accordance with the design procedure of Venable[2], the required boost is:

Bc = M - P - 90, where

M = desired phase margin, and P = filter & modulator phase shift.

In this case, Bc = 60 - (-135) -90 = 105 degrees. This is comfortably within the theoretical limit of 180 degrees, inherent in the amplifier configuration shown in Figure 17. The gain required at the crossover frequency is the reciprocal of the modulator's gain, or +15dB = a gain of 5.6.

Continuing with the procedure, we can now compute the amplifier components:

$K = (\text{Tan}\ [\ (Bc/4) + 45]\ )^2 = 8.65$
$C2 = 1/(2\pi f G R1) = .00071\ \mu F$
$C1 = C2\ (K - 1) = .0055\ \mu F$
$R2 = \sqrt{K}/(2\pi f C1) = 21{,}485$ ohms
$R3 = R1/(K - 1) = 1{,}302$ ohms
$C3 = 1/(2\pi f \sqrt{K} R3) = .01\ \mu F$

where f = crossover frequency in Hz, G = amplifier gain at crossover (expressed as a ratio, not as dB), and K is a factor which describes the required separation of double poles and zeroes to accomplish the desired phase boost. These frequencies are:

$f1 = f/\sqrt{K}$ (double zero), and $f2 = f\sqrt{K}$ (double pole),

In this example, f1 = 1361 Hz and f2 = 11.76 KHz. With this information at hand, it is wise to check the gain-bandwidth required of the feedback amplifier to see that the circuit's needs can be met with one of the amplifers in the UC1838. Knowing that the amplifier rolloff is 20 dB per decade, we can simply calculate the required gain-bandwidth at f2 and see that it is well below the gain-bandwidth of the amplifier.

The gain at f2 is:

$Gf_2 = \sqrt{K}\ G$, and hence the required gain-bandwidth is:

$GBW = \sqrt{K}\ G\ f2 = K\ G\ f$, where G is the desired gain at crossover.

In this example, GBW = 8.65 × 5.6 × 4000 = 194 KHz. This is comfortably below the gain-bandwidth of the amplifier, which is 800 KHz.

For interest, the response of the amplifier is plotted in Figure 20. Note that the gain reaches a minimum at 1.3 KHz, and that the phase boost peaks at 4 KHz, as intended.

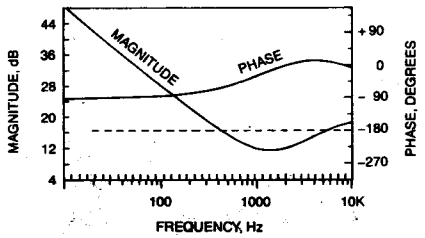

Figure 20. Compensated amplifier response.

Figure 21 shows the overall response, combining the filter-modulator's response with that of the feedback amplifier. Note the 60 degrees of phase margin at the crossover frequency.

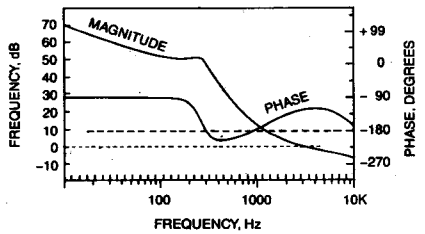

Figure 21. Total loop response with 60 degrees of phase margin at crossover.

CURRENT LIMITER DESIGN

Although a series sensing resistor might have been acceptable at this level of output current, a current transformer, T1 in Figure 17, has been used for the sake of interest. The secondary has 100 turns, and each primary winding is simply one pass through the toroid.

The amplifier performs as an integrator rather than as a comparator, the form found in many primary current limiters of switched-mode controllers. This is not an arbitrary choice. Since the current pulse occurs during the time that the core is obviously not being reset, the circuit must have "memory" — it must apply a shutdown command to the reset transistor during the next reset interval. Although many sophisticated schemes can be devised, the integrator is attractive because of its simplicity.

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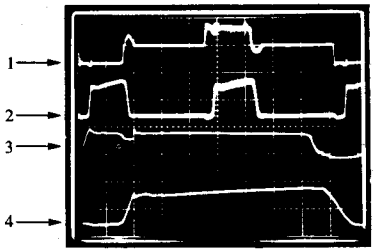
A diode is placed across the input resistor of the integrator, to force its output down quickly when receiving the narrow pulses which occur when the circuit is in current limit. The circuit of this example was developed experimentally. A future goal is to explore this in detail and develop a more rigorous approach. The performance of this circuit is illustrated with waveform photos later in the paper.

BREADBOARD TEST RESULTS

Figure 22 shows the waveform of the input voltage which is applied to the mag amp core, and the current of the two mag amps combined (by placing a current probe on the return leg of the secondary of the converter's transformer). The lower two traces are expanded versions of the top ones, and one can see clearly the effect of the transformer's leakage inductance: the voltage pulse has a "dent" in it during the rise of the current in the mag amp.

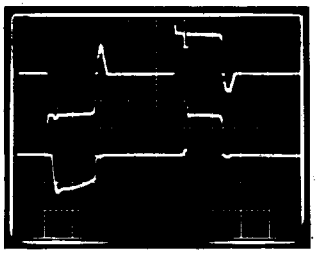


1. Secondary voltage, 50V, 5 μs/div.
2. Current in return (center tap) of secondary. 5A, 5 μs/div.
3. Secondary voltage, 50V, 1 μs/div.
4. Current in return (center tap) of secondary. 5A, 5 μs/div.

Figure 22. Input voltage and current to the mag amp.

Also note the "backswing" at the end of each voltage pulse. This is the discharge of the energy stored in the saturated inductance of the mag amp core. Finally, note the rate of rise of the current pulse, which is determined by the saturated inductance of the mag amp, in series with the leakage inductance of the transformer.

Figure 23 illustrates the operation of the mag amp in more detail. The upper trace is the input voltage of the mag amp, and the lower trace is its output. The reset volt-second product is the difference between the negative pulses of the two traces. The shape of the negative pulse in the lower trace is due to the changing impedance of the mag amp core during reset.

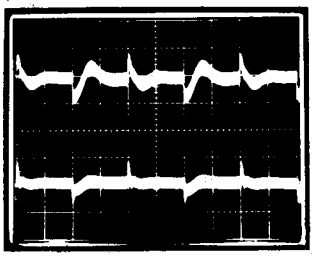


Top: Secondary voltage (into mag amp), 20V × 5 μs/div.
Bot: V_{OUT} of mag amp, 20V × 5 μs/div.

Figure 23. Mag amp operation.

Control loop transient response

To test the response of the regulator to step changes in load, an electronic load was square-wave modulated at 500 Hz, between the values of 6A and 8A. The results are shown in Figure 24. The upper trace is the regulator's output voltage, showing peak excursions of less than 50 mV, and recovery time of .5 ms. The lower trace is the reset current, measured with a current probe at the collector of the reset transistor in the IC.

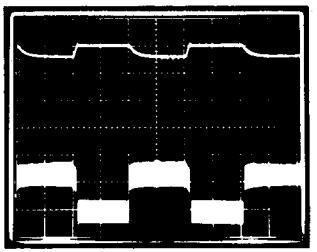


Output transient response 6-8A ΔI_{LOAD}
Top: Output voltage, 50mV × .5 ms/div.
Bot: Reset current, 20mA × .5 ms/div.
(Measured at collector of UC1838 transistor)

Figure 24. Dynamic regulator response to step change in load between 6 and 8 amps.

Response of the current limiter

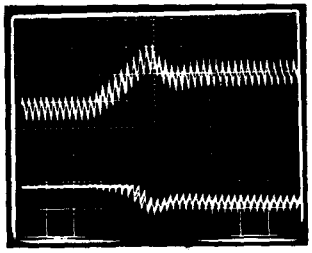
To illustrate the dynamic operation of the limiter, the current limit was set at 7A, and then the electronic load was modulated between 5.7A and 8.7A at a rate of approximately 25 Hz. Figure 25 shows the output voltage in the top trace. The lower trace is the current in the output inductor. Note that the output voltage is well-behaved and that there is no overshoot of the inductor current.



Top: V_{OUT}, 2V × 20 ms/div.
Bot: Inductor current, 2A × 20 ms/div.

Figure 25. Response of current limiter with load switched between 5.7 and 8.5A; with current limit set at 7.5A.

Finally, Figure 26 shows the operation of the current-limiting amplifier. The upper trace is the inductor current, and the lower trace is the output voltage of the current-detecting amplifier. Note the output waveform of the amplifier. Although the amplifier performs as an integrator, it slews fast enough to keep up with the rate of rise of the inductor current, thus adequately protecting the converter and output rectifiers.



Top: Inductor current, 2A × .1 ms/div.
Bot: V_{OUT} of C.L. amp (pin 1), 2V × .1 ms/div.

Figure 26. Response time of current limit amplifier.

APPLICATIONS AT HIGHER SWITCHING FREQUENCIES

As mag amp output regulators are applied at higher and higher switching frequencies, the second-order effects, of course, become more significant.[3] Leakage inductance of the transformer and saturated inductance of the mag amp rob the circuit of its control range, since these produce additional dead time at the leading edge of the output pulse. Even without the mag amp output regulator, this can be a problem in high-frequency switched-mode converters.

Diode storage time has the same result. If the output side of the mag amp "sticks" at ground (during reverse recovery of the rectifier) while its input voltage swings negative, some unwanted reset will be applied to the mag amp. There are techniques to deal with this problem, by providing a shunt recovery path around the mag amp to remove the stored charge in the diode.[4]

The control circuit of the mag amp regulator is not involved in the cycle-by-cycle operation of the circuit; hence, the control IC is not a major barrier to raising the operating frequency. It does affect the situation in an indirect way, however. Its gain-bandwidth may limit the speed of transient response such that the loop crossover frequency cannot be raised in proportion to the switching frequency. In most applications this will not be objectionable. If it is, an outboard op amp can provide the additional gain-bandwidth. If the regulator is not required to have its own current limiter, then the second amplifier can be used in cascade with the first, to provide additional gain-bandwidth.

The integration of the circuit blocks required to implement mag amp output regulators is an important contribution. It is especially beneficial to have the reset transistor included, as this can even eliminate a small heat sink. Finally, it is helpful not only in the design process but also in production to have a single component which encompasses all of the active control functions. As more and more designers are working with the same component, the development of the technology will be more focused, and this will be universally beneficial.

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5. Unitrode IC Corp. acknowledges and appreciates the support and guidance given by the Power Systems Group of the NCR Corporation, Lake Mary, FL in the development of the UC1838.

Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Merrimack, New Hampshire • 03054-0399
Telephone 603-424-2410 • FAX 603-424-3460