DRIVING THREE-PHASE BRUSHLESS DC MOTORS — A NEW LOW LOSS LINEAR SOLUTION

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ABSTRACT

A new linear driver for small Brushless DC motors has been developed which has the capability of maximizing the voltage delivered to the motor while additionally providing commutation logic and full control. By using discrete PNP high-side transistor switches in conjunction with integrated saturable NPN low-side drivers, less than one volt total loss can be achieved at currents up to two amps, and complete motor control can be derived from only a five volt power source.

BRUSHLESS DC MOTORS

Although the world has long known of the myriad problems with brush-type DC motors, the development of electronically commutated, or "Brushless" (BDC), motors has not been a simple transition. While Hall Effect sensors have developed to the point where accurate and reliable armature position information can now be readily derived, the problems of amplifying these low-level signals, applying them to the appropriate winding, and then driving that winding with an efficient power transfer still represent a significant challenge. Particularly when this intervening circuitry - none of which was required with brush-type motors - also has to be reliable, very low cost, noise free, and take up minimal space. The problem is further compounded by the need to provide three-phase drive for all but the simplest, specialized motors in order to accommodate bidirectional rotation and wide variations in speed and load.

For complete control of a brushless DC motor, the circuitry must provide at least three functions:

1. Commutation logic to generate the correct phase timing from the Hall sensors. In most cases, this is implemented as a digital decoding function.

2. Power drivers for each of the three output phases. The challenge here is finding a solid state switch as efficient as the old commutator brush.

3. Control circuitry to give the motor some intelligence. This usually means controlling motor current in response to commands based on speed, position, torque, or some other measurable output.

THE SPINDLE DRIVE PROBLEM

Providing the above functions as a spindle driver for rotating memories represents an additional challenge as disk drive users have come to expect the package density and low costs of an integrated driver while at the same time demanding ever higher operating efficiencies to minimize the requirements on power supplies and heat sinks.

While discussing drive efficiency, it is worth noting that disk drives add a further restriction due to the magnetic media and low signal levels involved. This is that the use of switch-mode technology to increase power control efficiency is usually forbidden out of concerns for possible high-frequency EMI noise. Ruling out switch-mode techniques leaves the designer faced with the problem of providing maximum efficiency with linear current control, and thus his quest for power savings can only be directed toward minimizing the drop across the output switches in order to use the highest efficiency motor.

THREE PHASE MOTOR DRIVE

The drive stage for a typical brushless DC motor is shown in Figure 1 where the motor is shown wound in the "Y" configuration. A "delta" form is equally applicable and would make no difference to the switches. The driving problem is immeadiatly apparent in that there are six separate switches required and two are in series with any current path through the motor. With a 12 volt supply and typical bipolar darlington switches - each with a probable 1.5 volt drop - the maximum voltage to the motor is nine volts and one fourth of the input power is lost in the switches.

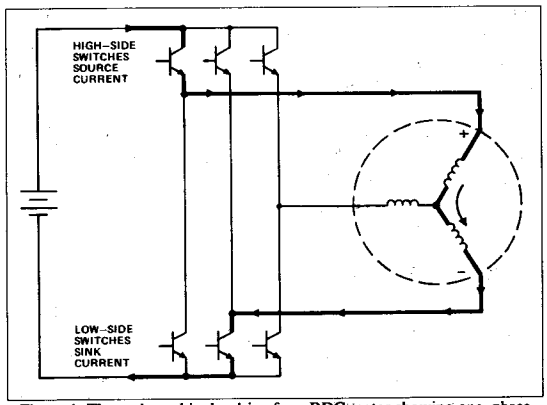

Figure 1: Three phase, bipolar drive for a BDC motor showing one phase of current flow.

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These switch voltage drops have added significance in terms of optimizing the motor design since the maximum current through a given motor is defined by the difference between the voltage applied to the motor and the back EMF generated while it is running. Reducing the voltage drop across the switches allows the use of a motor with a higher torque constant and correspondingly higher back EMF which results in a lower motor current for the same load. Since the power loss in the motor is equal to I^2 times the wire resistance, the gain in overall efficiency is more than proportional. For example, with a three volt switch drop from a 12 V supply, an optimum motor choice might have a back EMF of 8 V and require 4 W of power from the supply to do 2.7 W of work. Reducing the switch drop to one volt would now allow a motor with a back EMF of 10.2 V to be used which, with all other factors remaining unchanged, would require only 3.16 W to do the same work. In other words, a 22% increase in the voltage applied to the motor can result in a 27% increase in motor efficiency. This is in addition to saving 2/3 of the power lost in the switches.

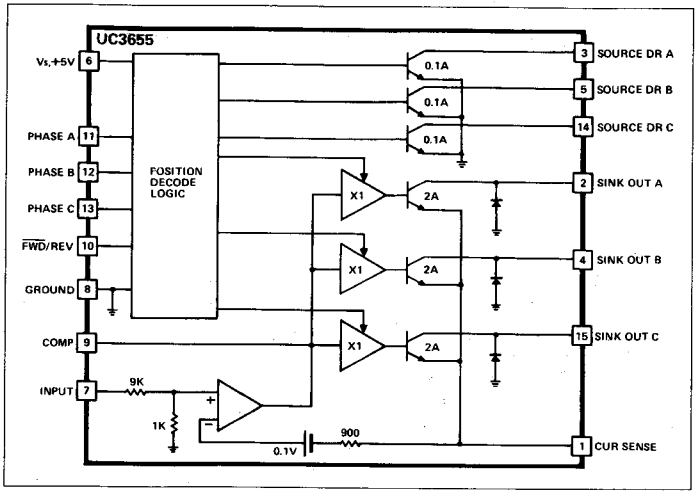

Figure 2: The UC3655 IC provides decode logic, high-current low-side linear drivers under the control of an internal amplifier, and switches to activate high-side, external PNP transistors.

While power MOSFET technology has the potential of offering lower switch losses in discrete form, an integrated monolithic FET structure, while technically feasable, may well be economically impractical. An integrated bipolar transistor scaled for a Vsat of 0.4 V at one amp requires approximately 2000 square mils of silicon, while an integrated DMOS transistor with an Rds(on) value of 0.4 ohms would be closer to 5000 square mils. And it takes six transistors to build a three phase driver. Therefore, a more cost-effective solution would indicate the use of bipolar transistors, but as single saturating switches - not darlingtons.

The low-side switches of Figure 1 are easily integrated in this form as power NPN transistors with their base currents derived efficiently from a five volt power supply. The high-side devices are more of a problem, however, as these need to be PNP transistors to achieve the same low-sat performance, and isolated power PNP transistors are still not compatible with an integrated bipolar process. Thus the decision made for the motor driver described herein was to supply the PNP's as external, discrete saturating switches while the rest of the control circuitry was integrated into a single power IC. The result is the UC3655 illustrated in the block diagram of Figure 2.

THE UC3655 LINEAR BDC MOTOR DRIVER

This device achieves efficient operation by allowing the external PNP's to be selected for the specific application, while internally generating a switched base drive of up to 100 mA - adequate for motor load currents of at least 3 Amps. Because the PNP's are always driven into saturation, their power dissipation will usually be low enough to require no special heat sinking and, in many cases, they may not even need power packages. The only specification of significance for these devices is their saturation voltage for a given base drive. While bipolar PNP transistors are used throughout in this paper, it should be clear that this is a cost consideration and P-channel FET devices could be used as well with the benefit of reduced drive power losses.

The current-limited darlington circuit used for each of the three PNP drivers is shown in the upper portion of Figure 3. This driver is activated by the digital signal from the Channel Select Logic which is defined to allow only one PNP to be on at a time. Note that the total supply current for this stage is a constant 100 uA from the five volt supply for each output.

Each of the low-side motor drivers shown in Figure 3 are, of course, integrated power NPN transistors scaled for a maximum output current of three amps with a very low saturation voltage

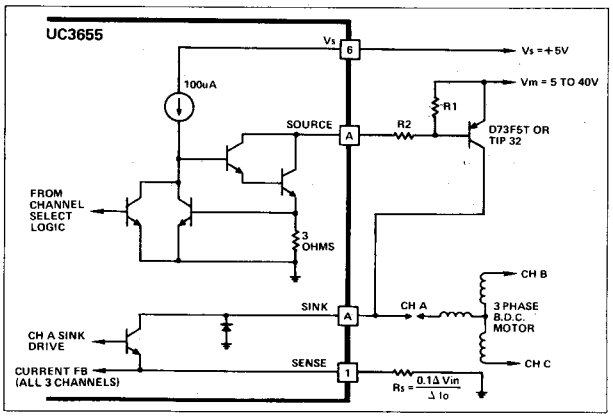

Figure 3: Interfacing the UC3655 to a BDC motor.

drop. At full load, these transistors may need a base drive of up to 50 mA which must come from the five volt supply; however, since they are also used as the means to control the motor current, the action of the control amplifier reduces the base drive as it commands less motor current. The overall schematic of both the amplifier and one of the three low-side drivers is shown in Figure 4.

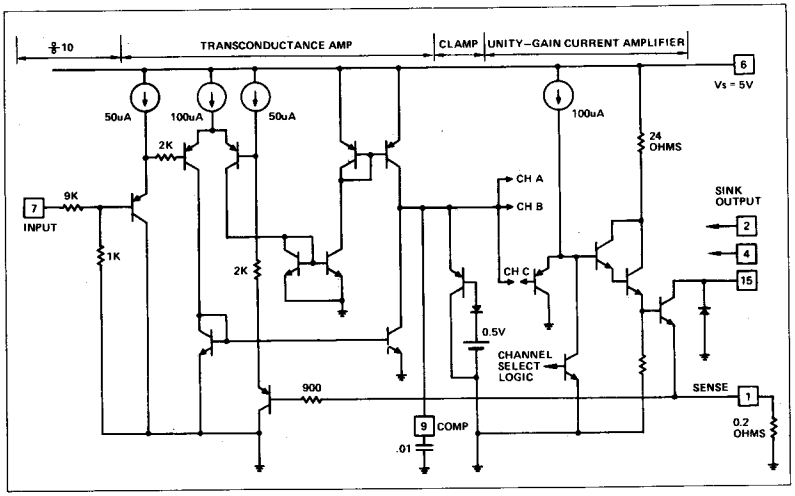

Figure 4: Control of the motor's current requires the four functions shown above, plus the decode logic to define which of the three outputs is active.

This circuitry includes an internal feedback loop to configure the transfer function as a transconductance amplifier controlling motor current from a voltage command. For full control, four functions are included:

1. An input divide-by-ten attenuator to scale a four volt input command range on Pin 7 to a 400 millivolt range across the current sense resistor connected to Pin 1.

2. An amplifier to provide voltage gain. This is also a transconductance type so that the feedback loop may be easily stabilized by a single capacitor from its output on Pin 9 to ground. There is a 100 mV offset built in so that, in conjunction with the input divider, zero output current is commanded with a one volt input.

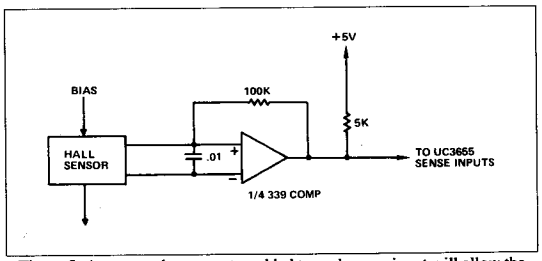

Figure 5: An external comparator added to each sense input will allow the use of low-level, analog Hall sensors.

3. A unity-gain output stage (to the sense resistor) provides the high current output drive with a high input impedance so that the transconductance amplifier is not unduly loaded. Note that the analog command input is gated by the Channel Select Logic so that only one output is on at a time with the other two drivers draining only 100 uA apiece from the supply.

4. A clamp on the output of the transconductance amplifier limits the voltage drop across the sense resistor to approximately 500 mV and thereby provides some measure of over-current protection.

The remaining portion of the UC3655 consists of the decode logic to generate the proper output switch timing from the Hall sensor position indicators. This logic is easily mask programable for other than the standard 60 degree output phasing. The input circuitry to these Channel Select stages has a high impedance, stabilized threshold of 1.5 V and is designed for single-ended, digital-output Hall sensors. For maximum flexibility, pull-up resistors are not included but in niosy environments, should probably be added externally. Where analog, two-terminal Hall sensors are used, the comparator circuit of Figure 5 can be used at each input to give fast, clean transitions.

A fourth input to the decode logic is the direction function addressed through Pin 10. This input circuitry, shown schematicly in Figure 6, has three states:

1. A low input pulls REV low and FWD high, setting up the decoding for a forward rotation.

2. A high input reverses the states of REV and FWD, which the logic decodes as a command for the opposite direction of rotation.

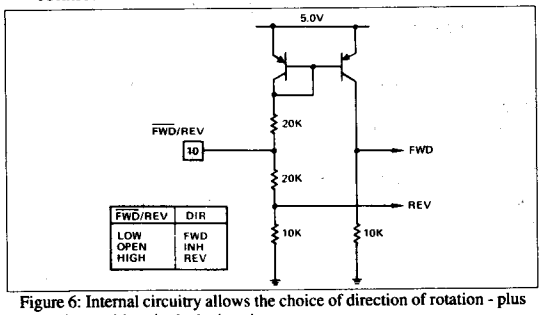

Figure 6: Internal circuitry allows the choice of direction of rotation - plus inhibiting - with a single device pin.

3. If the input is open - or connected to a voltage between 1.8 and 3.2 volts - both FWD and REV are high which the logic defines as a coast condition with all six outputs off.

All outputs are also inhibited if the three Hall inputs are all in the same state, either high or low.

While no braking function is built into the UC3655, it is entirely feasible to provide a rapid deceleration by switching the direction command from FWD to REV with the only precaution being to allow the output transistors to turn off while the command is passing through the INH region. Typically, this might require a 10 usec delay which is easily accommodated with either digital or analog techniques.

It can be seen from the block diagram of Figure 2 that the only supply voltage connection to the UC3655 is a single 5 volt source. From this supply, the quiescent current is less than 10 mA with the outputs inhibited and increases with motor current to approximately 25 mA with a two amp load. The motor voltage is defined by the supply used for the emitters of the PNP transistors and can range from 5 V to 40 V. Note that with this design, a 5 V supply could deliver more than 4 V to the motor - a difficult task for any other integrated circuit topology.

Finally, this device includes the protection of undervoltage lockout, with a threshold of 4.2 V, and thermal shutdown when the junction temperature rises above 150°C. Since the UC3655 is a linear driver, the potential for high dissipation is possible but a Multiwatt power package with adequate heat sinking will accommodate up to 25 watts. For smaller motors, a power 28-pin surface-mount, PLCC configuration with 4 watt capability will be offered.

INTERFACING TO THE MOTOR

The schematic of Figure 3 illustrates the added components necessary to interface the UC3655 to a typical BDC motor with the other two outputs identical to that shown. While resistor R1 serves merely to speed the turn off of the PNP transistors, R2, while optional, serves two functions: It can reduce the PNP base current to less than the internally limited 100 mA, and it absorbs the PNP base drive power losses which would otherwise add to the IC package dissipation.

In driving a BDC motor, there is no concern for cross-conduction current flow where both an NPN and a PNP experience overlapping conduction during switching transitions. This is because the commutation logic never switches any output from low to high or vice versa - there is always an off state in between. The inductance of the motor does force current transients when any transistor turns off, however. When a PNP turns off, residual current transfers to the internal diode at that output, pulling the output slightly below ground potential. When an NPN turns off, the transient current then flows through the PNP in the reverse direction, pulling the output voltage momentarily above the motor supply. Most PNP transistors will readily accept this as long as the voltages are low, but it should be evaluated for each application. Of course, the body diode of a P-channel FET provides this current path inherently.

Typical waveforms for voltage and current at one output are shown in Figure 7. While the voltage always switches to Vm on the high side due to the saturated PNP's, the value on the low side will be determined by the motor resistance and the commanded current. The large negative glitch occurs when the active PNP turns off; the tall spike above Vm occurs with turnoff of the NPN. The two short negative transients which occur while the current sinking NPN is on are caused by state-changes on the other two outputs momentarily interrupting current flow.

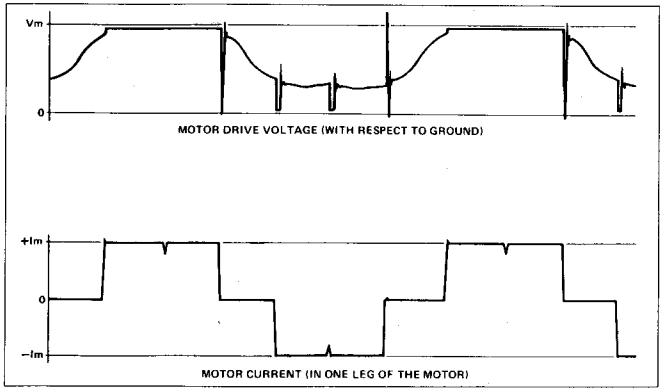

Figure 7: Voltage and current waveforms experienced at each output of the UC3655.

For disk drive or other applications where EMI noise generation at phase changes could be a problem, some slope control should be used on the outputs. While there are several ways to accomplish this, one effective technique is with R-C snubbers as shown in Figure 8. The circulating currents which will flow in these snubbers control the output rise and fall times and significantly reduce the higher frequency harmonics without contributing additional stress to the drive transistors.

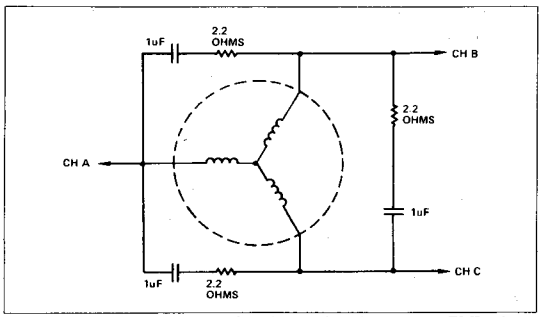

Figure 8: These three sets of R-C snubbers will help to reduce EMI noise.

ALTERNATE CONFIGURATIONS

Although the primary goal in developing the UC3655 was the implementation of a linear, current controlled BDC drive, that is not the only way this device may be used. The benefit of very low saturation voltage drop across the conducting switches has obvious advantages for efficient motor drive without linear control. The internal transconductance amplifier can be disabled by merely connecting the input terminal to the 5 V supply which will pull the compensation terminal up to the internal clamp level and allow the NPN low-side transistors to be switched fully on through the action of the decode logic. Current limiting may still be included by appropriate selection of the sense resistor, or for maximum voltage to the motor, the sense terminal may be connected directly to ground.

In this configuration, the circuit is only utilizing the position decode and output drive circuitry, and the motor will run open loop with its speed (or torque) determined solely by the motor voltage. This suggests another method of control. Since the UC3655 operates with only a 5 volt supply and is unaffected by the motor voltage, Vm, on the PNP emitters, controlling Vm will control motor speed. This can be done with either a linear or switch-mode regulator with the regulator control loop used to control the motor rather than hold the output voltage constant. An example of switching regulator control is shown in Figure 9 where an L296 PWM power supply IC is used as a 100kHz buck regulator. This circuit offers several advantages over other control techniques:

1. Since all power devices are used as switches, overall efficiency can be higher than with a linear approach.

2. The PWM frequency is converted back to DC before it gets to the motor minimizing the potential for harmful EMI.

3. High switching frequencies can be used in the regulator to keep the filter components small but with only ripple current through the motor, internal AC losses there are minimized.

4. A boost configuration could also be used to raise the motor voltage above the supply for faster response, lower currents, and a potentially significant increase in efficiency.

There are also some disadvantages:

1. The added complexity and components of the PWM regulator,

2. The additional switch in series with the motor.

PULSE WIDTH MODULATION OF MOTOR CURRENT

If the application will accept direct switch-mode control of motor current, this approach is also possible with the UC3655. Figure 10 shows the use of a UC3843 Power Supply PWM IC as the control element. Since this device has a very low impedance output drive, it will override the output of the UC3655's control amplifier and apply the PWM signal to whichever output has been activated by the decode logic. To keep switching and motor losses low, the frequency should be limited to the 20-40 kHz range.

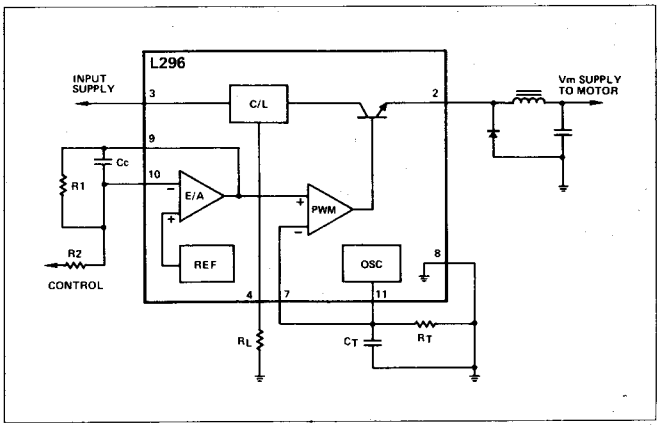

Figure 9: The L296 Buck Switching Regulator will efficiently control motor speed with the internal control loop disabled, by controlling the motor voltage instead.

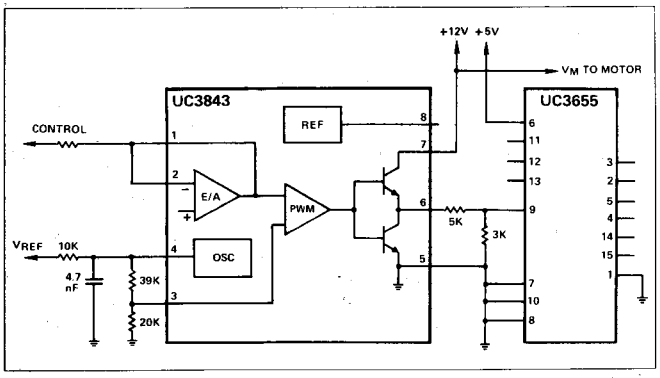

Figure 10: The UC3843 PWM Power Supply Chip can be used as a switch-mode controller for motor current by overriding the UC3655's internal amplifier with a PWM command.

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PHASE LOCK LOOP SPEED CONTROL

In many applications where very accurate speed control is required - disk drives, for example - a phase lock loop, locked to a crystal frequency reference, is often utilized. The UC3633 PLL chip has been designed to supply this capability and its use with the UC3655 is shown in Figure 11. In this circuit, a 4.9125 MHz crystal is divided down and compared with a signal from one of the motor's Hall sensors to force rotation at exactly 3600 rpm, +/- 60 ppm. This figure shows the UC3655 used in its conventional linear control mode, but the UC3633 is equally applicable to the other modes of operation discussed above. For further information on the UC3633, refer to Unitrode's Application Note U-113.

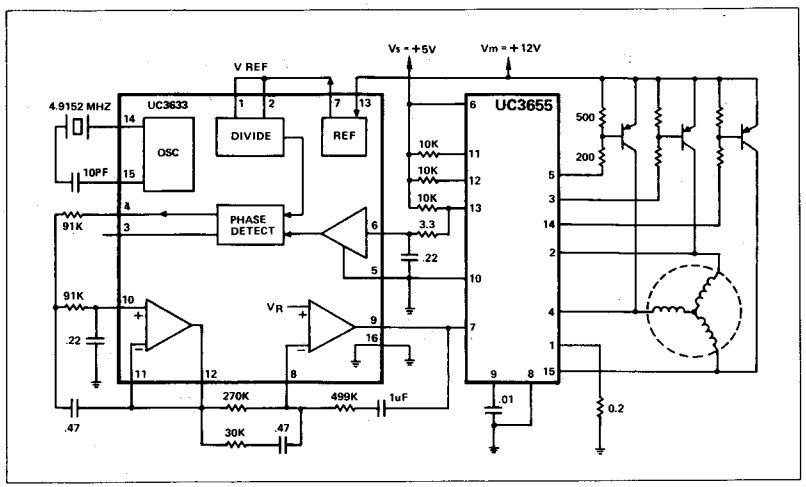

Figure 11: A UC3633 Phase Lock Loop IC can be used with the UC3655 to provide crystal-controlled speed accuracy.

SENSORLESS DRIVE

Finally, with the utilization of a microcontroller it should be possible to implement a drive system without the need for Hall position sensors and thus gain significant cost savings in the motor. Utilizing techniques developed for synchronous and stepper motors, commutation could be done "open loop" without angular position feedback but since the actual commutation point is not likely to occur at the optimum point, motor efficiency will be poor and will vary with load. One approach to solving this problem is the use of a single sensor to generate a reference point, and a digital PLL locked to this reference to generate the correct commutation timing. While this can yield commutation accuracy even higher than that obtainable with a typical sensor-type motor, the obvious disadvantage is increased cost over a completely sensorless design.

By using the back EMF generated by the motor, a signal proportional to the torque angle (commutation error angle) may be derived which can be used to correct the timing. However, simply forcing the commutation generator to deliver the correct timing will not control the speed of the motor. If instead, this signal is used to control the motor current by the approach shown in Figure 12, the commutation points are still generated open loop but, instead of forcing the commutation generator to follow the motor, the motor now follows the commutation generator. If the motor leads or lags, drive current is modified to force the torque angle to be optimum, yielding a PLL motor control system requiring no position sensors.

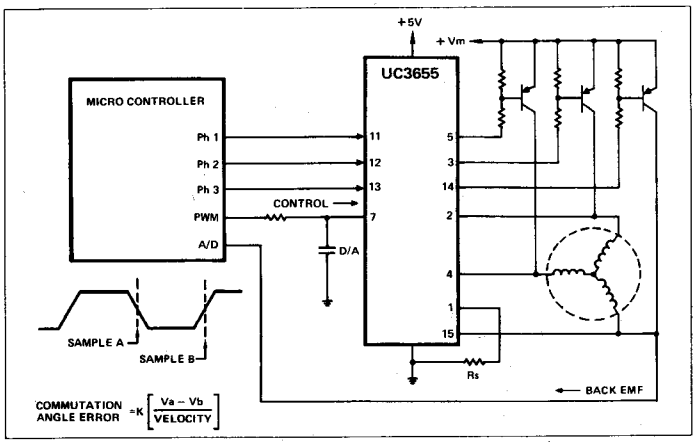

Figure 12: This approach to sensor-less control digitizes the back EMF on one motor phase and computes the commutation angle error from measurements made during the middle of the "off-time".

A NEW LINEAR REGULATOR FEATURES SWITCH MODE OVERCURRENT PROTECTION

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George Harlan, Power General

ABSTRACT

This paper presents a new linear regulator control circuit which, in addition to offering benefits such as low input-output differential and a precise reference voltage, features a unique and innovative approach to overload protection. By using duty-ratio, switch-mode protection, this circuit eliminates both the high internal dissipation of constant current limiting and the latch-up tendencies of limiting with current foldback.

THE CURRENT LIMIT PROBLEM

As an opening statement, let us offer as a "given" that all linear power supplies need some form of over-current protection. Traditionally, this protection consists of configuring the supply to control current - rather than output voltage - once an established threshold of maximum current has been exceeded. The method of current control can usually be classified as either "constant-current" or "current-foldback" current limiting and, while simple to classify, choosing between these two methods is often less than satisfying.

The protective method most acceptable to the user is constant current limiting with a characteristic as shown in Figure 1. With the knowledge that a power supply will only deliver a maximum current regardless of what he might do to it, the user's job of scaling his cables, switches, connectors, and other components associated with the power inputs to his system is greatly eased. He knows that no matter how non-linear his load may be, he can count on a regulated voltage whenever his current drain is within the supply's rating. Further, he knows that the maximum rated current is always available to meet any demand asked of the supply.

The "benefits" of constant current limiting are another matter to the power supply designer, however. For example, a regulator designed to deliver 12 Volts at a maximum load current of 5 Amps would probably start with a bulk input voltage of approximately 15 Volts and a constant current limit of 5.5 Amps. Under maximum rated load, the internal dissipation of the regulator is 3V x 5A or 15 watts but with a short to ground, this dissipation jumps to 15V x 5.5A or more than 80 Watts! This means that the thermal management and heat sinking must be sized for the short circuit condition resulting in a massive overkill in terms of volume, complexity, and cost with respect to normal operating conditions.

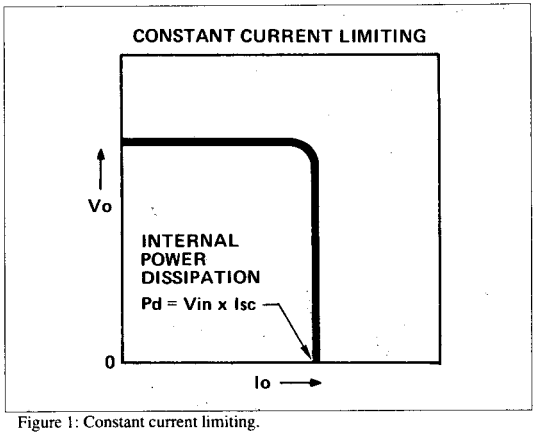

Figure 1: Constant current limiting.

A common solution to this problem is to design a current limiting scheme as illustrated in Figure 2. Here the protection is actuated at 5.5 Amps when the output voltage is at 12 Volts but the allowable current then "folds back" as the output voltage falls due to increasing overload, until it reaches some much lower value - say one Amp in this example - with a shorted output. Now the dissipation with a short circuit is close to the same as it was with rated current and our designer's thermal problems are solved.

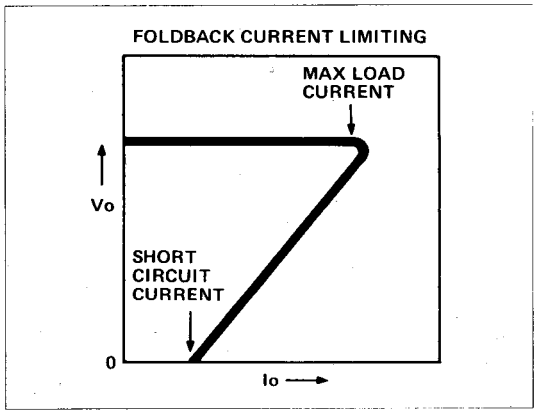

Figure 2: Foldback current limiting.

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But what about his customer? His load may be complex, non-linear, and often not even well understood. Figure 3 shows typical load characteristics for digital and analog circuitry but an actual system may include all of these plus motors which need to be started and capacitors which need to be charged. Any protection scheme which allows the static load line to intersect the foldback current curve as shown in Figure 4 is potentially subject to latch up because the load draws more current than the regulator can supply at the voltage where the curves cross.

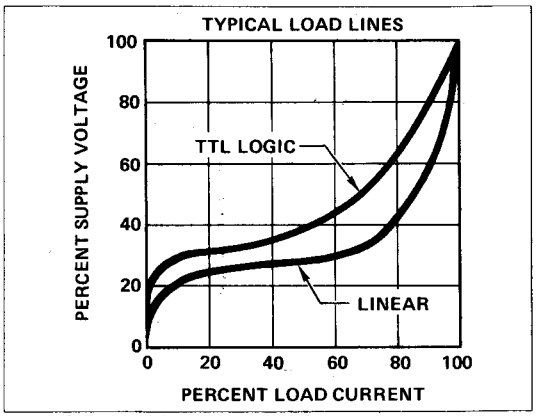

Figure 3: Typical digital and analog load lines.

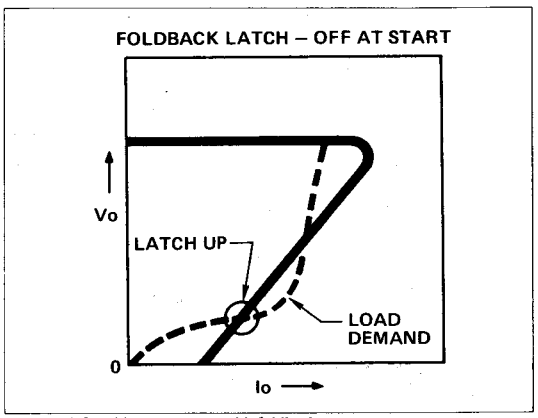

Figure 4: Latching at start-up with foldback.

An application particularly susceptible to latch up due to foldback current limiting occurs when two supplies are used to provide positive and negative voltages to a load where there is a path for "rail-to-rail" loading. As the regulators turn on, their output capacitors are charged at rates determined by the values of the capacitors and the amount of current each regulator can provide as its output rises up the foldback curve. Since these curves are unlikely to be perfectly matched, one output will dominate the other. As the faster one's output voltage increases, it provides more current through the common load. This forces the slower one back down the foldback curve where it provides less current, compounding the problem and ultimately latching when its output is driven past zero to a reversed polarity. Thus a foldback-limited regulator, which might be stable when used by itself, may latch when used as one-half of a dual-polarity system due to this "turn-on slew rate" phenomenon.

So what we have concluded is that while the power supply designer needs to incorporate foldback current limiting to reduce power dissipation, his customer needs constant-current limiting to insure reliable starting. It is the contention of this paper that what they both really need is duty-ratio protection.

DUTY-RATIO OVERCURRENT PROTECTION

Duty-ratio protection can be simply described as a constant current limiting regulator with a timer. The timer's function is to turn the regulator's power stage OFF and ON with an established duty cycle ratio such that the high internal power dissipation of constant current limiting is reduced by the duty ratio to a much more manageable average value.

Referring back to our earlier example of a 12V, 5A regulator, consider setting the constant current limit at 5.5 amps but additionally establish a duty ratio for the timer at 1 to 20 for "ON" to "OFF". If we set the "ON" time sufficiently long to charge whatever capacitance might be on the output, the regulator will power up with the constant current characteristic, insuring start-up regardless of the loading. In the event of an overload or short circuit (defined in this device as remaining in current limiting for a period of approximately 2 x Ton), the regulator will periodically shut down for a time equal to 20 x Ton and then continue to cycle in a 1 to 20 duty cycle until the fault is removed. Although the peak power during Ton might be 80 Watts, the average fault dissipation at this duty ratio is only 4 Watts - less than the normal 15 watt operating power loss, and we have thereby satisfied both the designer and his customer.

INTRODUCING THE UC1833 / UC3833

The block diagram of this new linear regulator control IC is shown in Figure 5. This circuit can be used in many different ways but its primary intent is as a high-efficiency regulator implemented with an external PNP pass transistor as shown in the figure. The circuitry in the right half of the UC1833 block generates the voltage error signal used to activate an NPN Darlington driver which, in turn, drives the base of the PNP pass device. This common-emitter pass transistor configuration allows this type of regulator to operate with a minimum input-output differential of well less than one Volt, even at high loads.

Duty-cycle current limiting is accomplished with the circuitry on the left half of the block diagram, where an Amplifier and a Comparator are seen, both monitoring the voltage drop across a single current sense resistor. The Comparator has an input threshold of 100 mV and, when activated, initiates a timer to alternately clamp and release the base of the driver to ground thereby switching the output of the regulator from Vout to Zero with a low duty ratio.

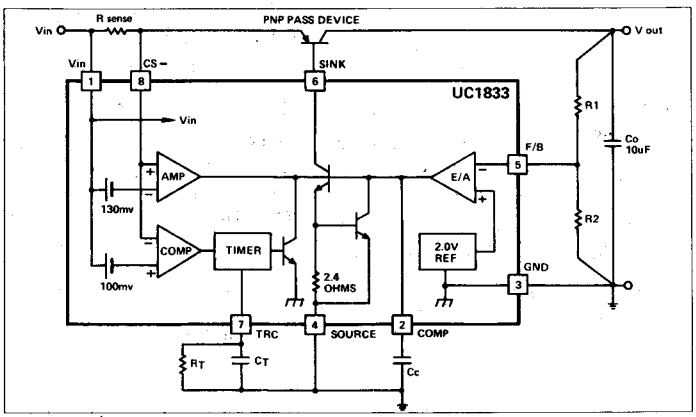

Figure 5: The new UC1833 / UC3833 linear regulator.

The Amplifier part of the current sense circuitry has an input threshold of 130 mV and overrides the output of the Error Amplifier to control the driver - when enabled by the ON-time of the timer - to regulate the supply's output current to a maximum amount determined by 130 mV divided by the value of the sense resistor. The 30 mV differential between the thresholds of the Amplifier and Comparator insures that current limiting can never occur without prior initiation of the timer.

OVERLOAD PROTECTION CIRCUITRY

The operation of the overload protection circuitry can be better understood by referring to the simplified schematic of Figure 6.

The current sensing portion of this circuit is to the left of this figure where the current-sense Comparator and Amplifier are shown sharing the same input sense pins. Note that their offset voltages are derived by a constant current through R1 and R2 in series rather than independently as shown in the more simplified earlier block diagram. By adding 30 mV to the 100 mV offset of the Comparator, the Amplifier's offset will more accurately track that of the Comparator should any variations occur, and the criteria to have the Comparator always activate first is assured.

A characteristic important to current protection is the accuracy of its threshold as any tolerance represents a window of undefined operation which works to the disadvantage of both designer and user of the power supply. Recognizing this, the UC1833's thresholds are derived from its precision reference resulting in a Timer activation threshold guaranteed to 5 percent over all operating conditions.

The output of the Current Amplifier connects into the output stage of the Error Amplifier where it can easily take command when activated. The compensation capacitor must compensate both the voltage and current feedback loops, and since the current loop must override the voltage control, its gain will be higher making the current loop the more difficult to stabilize. To evaluate the current loop, grounding the Timing pin will disable the Timer and allow continuous constant current operation. This can be useful either as a temporary measure while designing the current compensation network, or permanently to implement a constant-current limited power supply.

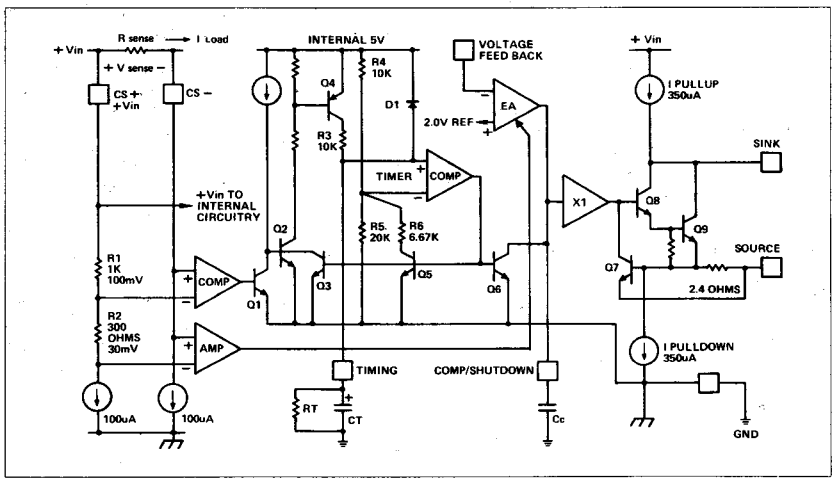

Figure 6: A simplified schematic of the UC1833 control circuitry.

The Current Sense Comparator is phased such that its activation turns off Q1 which turns on Q2 and Q4 to start the timing cycle. The timer is a gated astable relaxation oscillator with ON and OFF times independently programmed using an external resistor and capacitor, RT and CT. The external components work in conjunction with an internally switched 10k timing resistor shown in the schematic as R3. With RT much greater than 10k, the ON time is defined by R3 and CT, while RT and CT determine the OFF time. The thresholds for the Timing Comparator are set at 1/3 and 2/3 of the internally regulated 5 V source by the values of R4, R5, and R6.

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Timing waveforms during an overload cycle are shown in Figure 7 where the upper graph shows the output current from the regulator, the center one plots the voltage on the timing components, and the regulator's output voltage is shown in the lower graph. Following the sequence of events as drawn in the figure, when the load current ramps up and crosses the 100 mV Comparator threshold, the initial ON time begins. This initial period is about twice the duration of successive ON-times as the timing capacitor starts its charge from zero initially, while subsequent ramps begin from the lower Comparator threshold. While the timing capacitor is charging, the regulator current is limited by the action of the Current-sense Amplifier to maintain a level of 130 mV across the sense resistor. While in current limiting, the regulator's output voltage falls to whatever value that current will allow across the faulted load impedance.

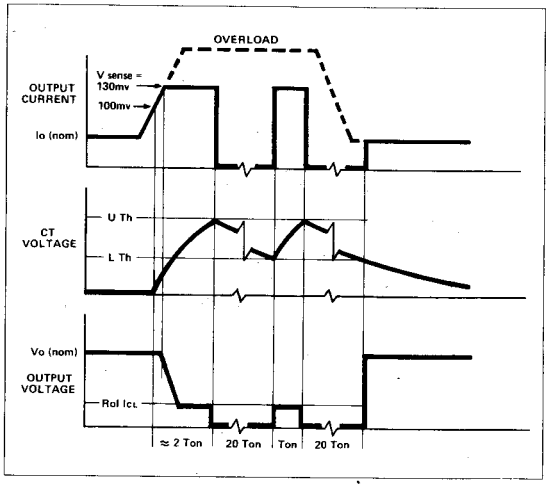

Figure 7: Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.

The ON-time continues until the internal 10k resistor charges the timing capacitor to the upper Timer threshold. At this point, both the ON-time of the regulator and the charging of the timing capacitor are terminated, and the capacitor now discharges through RT, while the regulator is held OFF until the voltage on CT reaches the lower threshold, at which point the cycle repeats. If the load fault is removed during an ON-time, the Timer is immeadiatly disabled allowing the regulator to recover and the timing capacitor to discharge back to zero. If the fault is removed during an OFF-time, the Timer must complete that cycle of capacitor discharge before allowing the regulator to turn back on. In special applications requiring an extended ON-time, the correspondingly long recovery may be accelerated by interrupting the input voltage, as the falling internal 5 V source will discharge CT through D1 and an equivalent 1k impedance.

Duty-ratio protection has greatly eased the problem of heat sinking created with a constant-current solution since the area of the heat sink, or its thermal resistance, need only remove the average power as reduced by the duty ratio. Heat sinks for the internal power devices must now only have adequate thermal mass to absorb the high peak power of the initial ON period.

REMAINING CONTROL CIRCUITRY

Other blocks within the UC1833 include a 2.0 Volt band-gap reference internally trimmed to 1% and a low input-offset Operational Transconductance Amplifier (OTA) to serve as the error sensing and amplifying circuitry. The OTA Error Amplifier has a gm of about 4 millimho and an output current capability of +/- 300 uA. This form of amplifier can usually be compensated with a simple network - often a single capacitor - from its output to ground; but more commonly, an R-C pole-zero pair is also added to compensate for an external PNP pass transistor's gain characteristics.

The Error Amplifier is followed by a unity-gain Buffer Amplifier which controls the Driver Stage consisting of a Darlington transistor pair with local current limiting. This Driver can either source or sink current, allowing its use as a driver for either NPN or PNP pass transistors. The Pullup and Pulldown current-sources shown at the Sink and Source terminals of Figure 6 are to provide turn-off bias to the pass transistor during duty-ratio switching so that it is not turned off into a BV_{CEO} condition.

Not shown on the schematic are two additional forms of protection built into the UC1833: Thermal Shutdown (TSD), and Under Voltage Lockout (UVLO). While it could be argued that thermal protection on the control chip does nothing to protect the pass transistor, the fact that the Driver can conduct up to at least 100 mA with a large portion of the input supply voltage across it, can result in more than acceptable internal heating of the UC1833. A good practice, when voltage levels permit, is the addition of an external resistor in series with either the Source or Sink outputs of the Driver to remove some of the voltage - and therefore some of the dissipation - from the controller.

Under Voltage Lockout keeps the Error Amplifier output low until the supply voltage reaches approximately 4 Volts insuring that all internal circuits - particularly current limiting functions - are intelligent before allowing the pass transistor to turn on. The UVLO function also disables the Pullup current feeding into the Sink terminal, for low input voltages, so that the pass transistor cannot be driven in the reverse direction should the input supply fall with a charged capacitor or other energy source on the output. The Source Pulldown current source is also disabled with UVLO but this terminal also has a two-diode path from the Source to the Compensation terminals. This is to allow any shutdown function which pulls the Comp pin low to discharge capacitance at the regulator's output without reverse-biasing the Driver's emitter-base junction.

THE UC1832 14-PIN CONTROLLER

An important objective in the design of the UC1833 was that in addition to providing significant operating benefits over the omnipresent uA723, the resulting product should be cost-competitive with that device. Committing the UC1833 to an 8-pin

Minidip package allows the potential for meeting the cost objective (plus the benefit of less PC board area), but in several important ways, also restricts the device's versatility. Recognizing this fact led to the introduction of the same chip in a 14-pin package with a UC1832 designation. The block diagram of this device, in a uA723-type application, is shown in Figure 8.

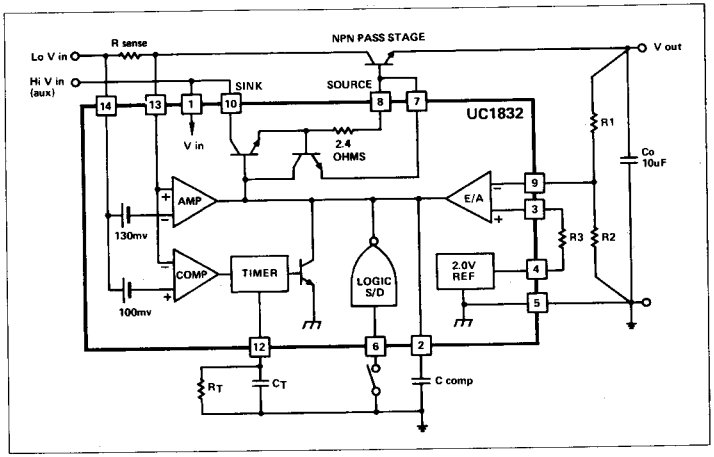

Figure 8: A 14-pin version, designated UC1832 / UC3832, offers enhanced versatility.

The characteristics of the UC1832 include all the performance features of the UC1833 plus the following:

1. Separating the +Vin line from the CS+ terminal so that the controller could be supplied from a higher potential, low-current, auxiliary voltage while sensing current from the main supply.

2. Separating the Reference from the Error Amplifier (+) input and making both accessible to the user. Among other things, this allows phase reversal, an external or divided-down reference, and a convenient access point for soft-start.

3. Providing a separate input to the Driver's local current limiter allows considerable flexibility in setting that limit either higher or lower than the 300 mA (typical) defined by the internal 2.4 ohm resistor.

4. A separate logic-level digital shutdown function has been added to give more programming options such as accepting a shutdown command from an over-voltage sensor or implementing a turn-on delay. This input is fail-safe as it must be pulled low to allow the regulator to turn on.

TYPICAL CIRCUIT APPLICATIONS

Unitrode's Power General Division has already utilized the UC3833 (the commercial version of the UC1833) in several successful power supply designs. A brief description of some of these products will illustrate both the range of applications and the simplicity which this new device brings to power supply design.

The circuit of Figure 9 shows one of the simplest applications of the UC3833 repeated twice to implement a dual-polarity 12 volt, 200 mA supply. The timing components for duty-ratio protection are determined from the following equations:

$$Ton = .69 \times 10k \times CT$$

$$Toff = .69 \times RT \times CT$$

$$\text{Duty-ratio} = Ton/(Ton+Toff)$$
$$= 10k/(10k + RT)$$

The values shown provide approximately 7 mS ON time and 140 mS OFF. These fairly rapid time constants minimize the need for any significant thermal mass in the heat sinks and also allow fast recovery after an overload is removed. With the knowledge that the initial conducting time can be twice the ON time, the maximum output capacitance can be calculated from:

$$C = Imax\ (dt/dV)$$

$$C = 130mV/.5ohm\ (\ 14mS/12V\ ) = 300\ uF.$$

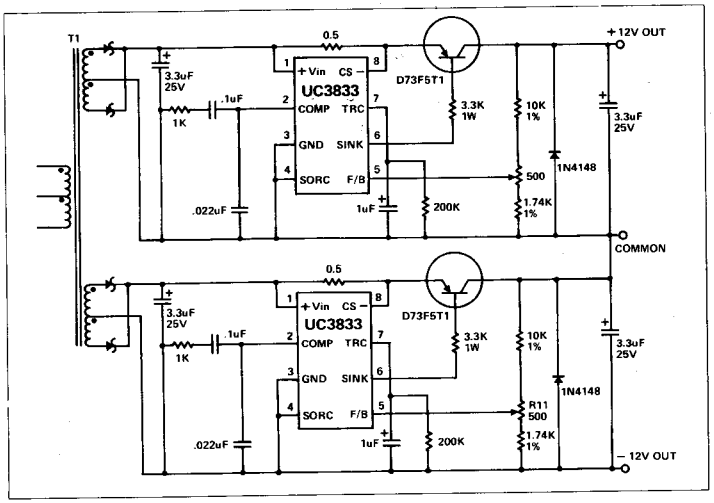

Figure 9: A +/-12V, 200mA regulator is easily implemented with two UC3833 devices.

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A higher power application is shown in the schematic of Figure 10 which was designed to supply 5 Volts at 5 Amps. The UC3833, configured as shown, will meet this requirement with an input voltage as low as 6 Volts due to the low saturation voltage of the paralleled 2N6489 transistors and the fact that the maximum non-fault voltage on the sense resistor is less than 100 mV. Actually, a little more sense voltage was sacrificed in the interests of selecting a standard resistor value, with the excess divided down by the 56/100 ohm divider. The additional BD438 drive transistor was added to boost the UC3833 drive current and keep the internal power dissipation low.

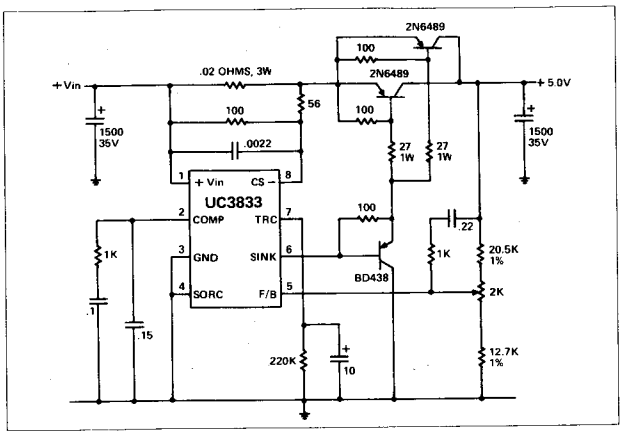

Figure 10: A high-efficiency configuration with added current boost will deliver 5V at 5A from a 6V source.

A third application of the UC3833 is one which took particular benefit from duty-cycle current limiting. This was for a disk drive power supply which required considerable current at turn-on to accelerate the disk. The circuit schematic is the same as that shown in Figure 10 with the voltage sense resistors selected for a 12 Volt output. The power requirements dictated a peak start current of 5 Amps decaying to 3 Amps in 30 seconds as the motor reached operating velocity. The current sense resistor was chosen to give a Timer initiation at 4.75 A and a constant current limit of 6.1 Amps. The timing capacitor value was set at 3300 uF yielding an ON-time of approximately 20 seconds, with 40 seconds for the initial turn on period - during which time the motor current will decrease to less than the lower threshold. With a duty-ratio of 20:1, when a fault does occur, the OFF-time will now be greater than 6 minutes, but, if this is excessive, recycling the input voltage to the regulator will reset the timing capacitor.

CONCLUSION

While no one can deny the long-term success of the uA723 as a general-purpose linear regulator controller, there has also long been a call for a device to improve its many limitations. While other products have been marketed offering some parametric improvements, the UC1833 - and its companion UC1832 - are the first to offer an innovative solution to a very basic problem. By combining switch-mode protection with linear regulation, these devices answer the question of which form of protection is best for whom, with a solution that is best for everyone.

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