BY CLAUDE ABRAHAM • BENDIX COMMERCIAL VEHICLE SYSTEMS

Quiet-node current sensing tames noise problems

WHERE YOU LOCATE THE CURRENT-SENSE RESISTOR IN YOUR DC/DC CONVERTER CAN HAVE A PROFOUND EFFECT ON THE DEVICE'S PERFORMANCE.

In designing dc/dc converters, one of your options is the CMC (current-mode-control) method. PCMC (peak CMC) offers some well-known benefits as well as drawbacks. When compared with VMC (voltage-mode control), CMC more quickly satisfies demands to supply load-current transients. With CCM (continuous-conduction-mode) operation, the VMC error amplifier generally requires a Type 3 compensation network, which comprises three poles and two zeros. A ceramic output-filter capacitor requires only two poles and two zeros. You can implement this transfer function with a resistor and two capacitors around the error amp, and a parallel RC (resistor/capacitor) between the LC (inductance-capacitance) output and the error-amp input. With a PCMC converter operating in CCM with a ceramic output capacitor, the capacitor across the resistor from the LC output to the error-amp input is unnecessary. PCMC requires two poles and only one zero for compensation. Thus, the PCMC error-amp-compensation network is generally simpler than its VMC counterpart. PCMC is more complex because you must compensate the slope of the inner loop.

Because the PCMC error amp recovers more quickly than does that of the VMC, PCMC reduces compensating-capacitor overcharging when the error amp saturates during large load-current transients. Also, compared with VMC—except for input-fed-forward VMC—PCMC corrects sooner for input-voltage changes and disturbances. With symmetrical transformer-coupled converters, such as full-bridge, half-bridge, push-pull center-tapped, and associated variations, PCMC corrects volt-second asymmetry in the PWM (pulse-width-modulated) drive, preventing magnetic-core saturation known as stair casing or flux walking.

With PCMC, clamping the error amplifier's output easily provides inherent pulse-by-pulse current limiting. Also, in CCM, PCMC eliminates the complex-conjugate, high-Q, low-frequency double pole that the VMC's LC power stage forms, leaving a single low-frequency RC pole and a complex-conjugate double pole at or near the Nyquist frequency (half the switching frequency). The result in general is improved dynamics. Also, using PCMC or ACMC (average CMC) allows paralleling several power stages to obtain increased output current.

As desirable as these benefits are, PCMC exhibits some limitations that you shouldn't ignore: The state variable that you should control is the average—not the peak—inductor current. However, with proper design techniques, as long as you maintain CCM, controlling the peak value can be as effective as controlling the average. Should the load current decrease to the point of DCM (discontinuous-conduction mode), the voltage-control (outer) loop, which is generally slower than the current-control (inner) loop, must correct an associated peak-to-average error, partially negating PCMC's speed benefit. Also, you must employ slope compensation to optimize load-current and input-voltage dynamics, as well as to ensure the current-control loop's unconditional stability. To optimize load-current and input-voltage dynamic response, the compensating ramp's slope should be 50% of the inductor current's equivalent downward slope. However, to maintain stability and sufficient damping in the current-control loop, a ramp-slope value of 50% works effectively only for duty factors less than approximately 36%. Above 36%, the required ramp slope must exceed 50%, which compromises the load current's and input voltage's dynamic response.

You encounter another PCMC shortcoming when the input voltage varies over a wide range. To ensure CCM operation at high-line input, deep-CCM operation occurs at low-line input. The ramp of the sensed-current signal becomes shallow, and SNR (signal-to-noise ratio) suffers. Using a current-sensing resistor with a larger value improves SNR at the expense of increased dissipation and lower efficiency. Also, with half-bridge converters that use a floating or soft (capacitive) center point, PCMC can cause the capacitive midpoint voltage to "walk" into either rail.

PROPER DESIGN OVERCOMES LIMITATIONS

PCMC's limitations are substantial, but proper design tech-

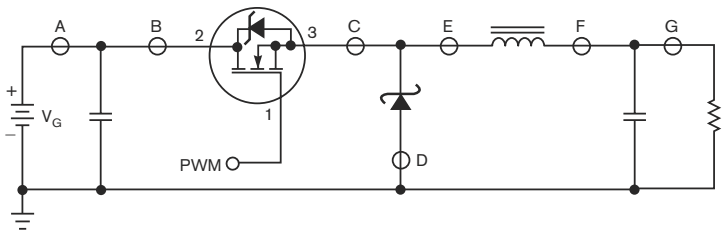


Figure 1 In a buck converter, you can obtain the inductor-current waveform by sensing the power-switch current, which equals the inductor current during the power switch's on-time.

niques can overcome all of them. However, one remaining problem has plagued PCMC since its invention and has caused some designers to abandon the approach altogether and instead employ VMC or ACMC. This problem is the leading-edge spike on the sensed-current waveform as the power switch turns on. This spike is large enough to prematurely terminate the PWM pulse before regulation. Because of output droop, the error signal on the next pulse is larger, and the pulse is longer. Over many cycles, the result is PWM-pulse jitter, which is quite visible on a scope.

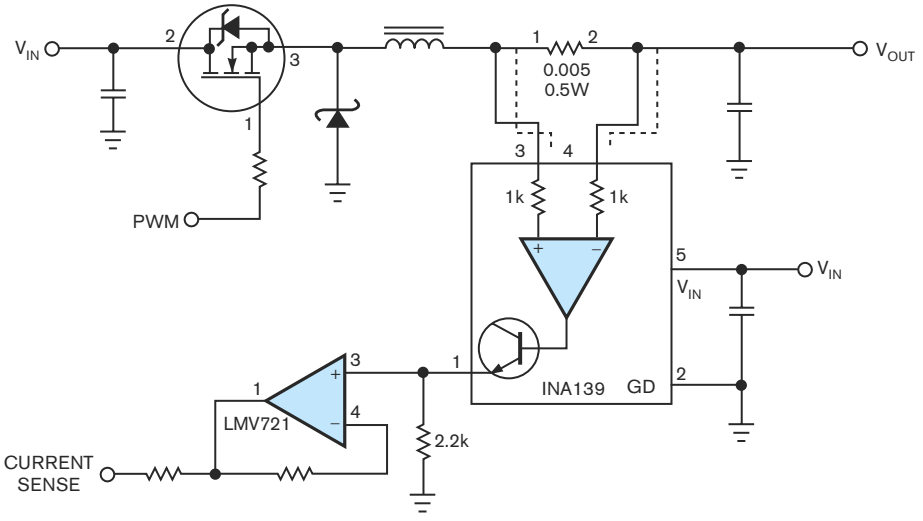


Figure 2 By using a low-valued sense resistor and locating an instrumentation amplifier very near the resistor, you can sense the dc/dc converter's output current with low noise and low power dissipation.

One way of dealing with this spike is to use leading-edge blanking, which momentarily disables current sensing at the leading edge of power-switch turn-on, preventing premature turn-off. One problem with this approach is that it imposes a minimum duty-cycle limit. Because the current-sense function is effectively blind at the moment of power-switch turn-on, a minimum pulse-width value exists. This problem, which exists at very light loads or no load, causes the output capacitor to overcharge, because the duty cycle cannot be low enough. Also, the occurrence of a fault, such as a direct short circuit on the output, delays current limiting, resulting in possibly destructive power dissipation. In many cases, this trade-off is sometimes undesirable. If a converter must operate without a minimum-duty-cycle limit, needs fast-acting fault protection, or both, then leading-edge blanking is undesirable.

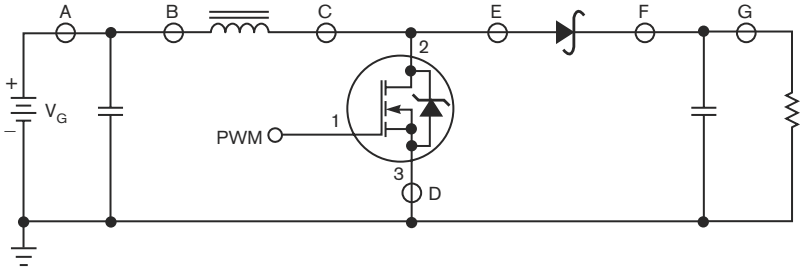


Figure 3 In a boost converter, locating the sense resistor in the conventional place yields suboptimal performance. The best location is Point B.

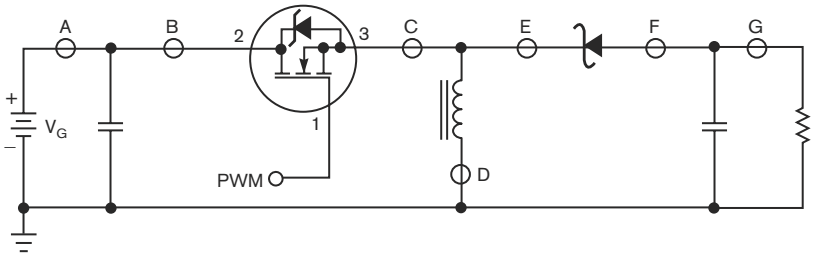


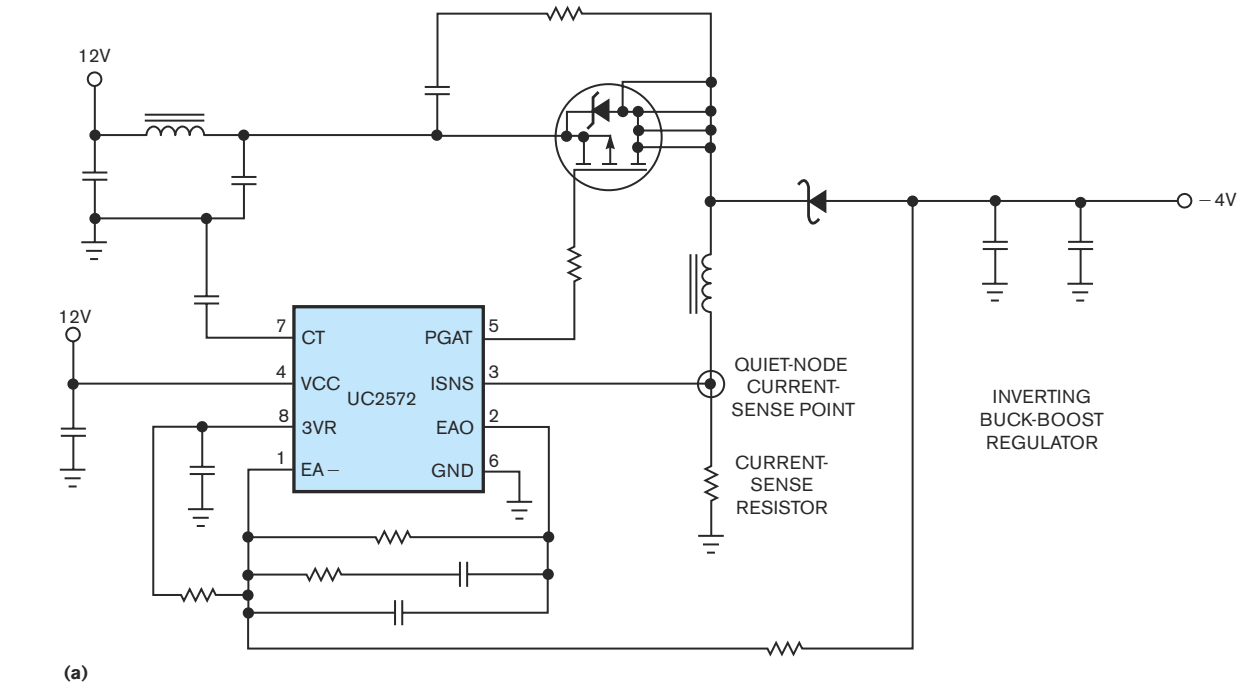
Figure 4 With the inverting buck-boost topology, the sensing locations have traditionally been B for PCMC and D for ACMC. Using D for PCMC produces quiet-node benefits, albeit with increased dissipation.

Another commonly employed method is RC filtering of the spike. The problems with this approach are similar to those of leading-edge blanking. If the RC time constant is long enough to adequately suppress the spike, it is generally long enough to delay turn-off in response to an output short circuit. Also, as with leading-edge blanking, a long time constant can impose a minimum duty-cycle limit, which is undesirable at light loads. One additional problem is that the RC time constant adds a pole to the current-loop transfer function. This pole with its associated phase lag can produce instability or underdamped response. To ensure stability, the time constant should be short, so that the associated pole resides at a high frequency, well above the unity-gain bandwidth. In that case, the problem is that the short time constant provides only a limited amount of filtering of the

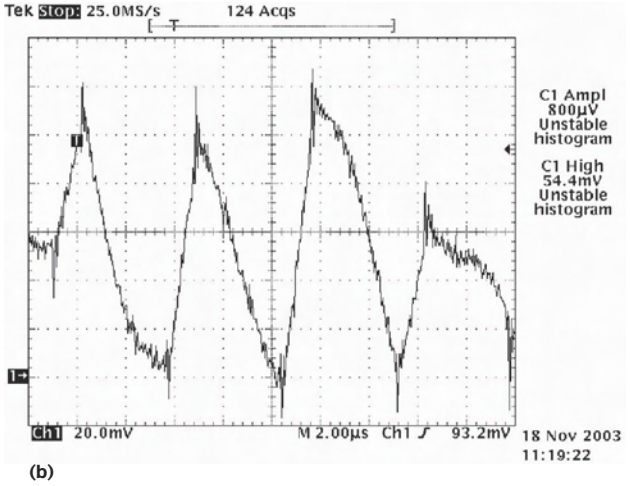
spike. You must usually seek another approach to the leading-edge current-spike problem. Some engineers correctly call this issue the bane of PCMC. Without a doubt, it is the most severe limitation they will encounter with PCMC. It is a result of the current-sense element's location; relocating that element provides the solution.

FINDING THE BEST SENSE-RESISTOR LOCATION

Begin with the buck topology, which allows locating the current-sense resistor in several places. For PCMC, the most popular location is Point B (**Figure 1**). You obtain the inductor-current waveform by sensing the power-switch current, which equals the inductor current during the power-switch on-time. This location results in low power dissipation, because current flows in the sense resistor only during the on-time, and no current flows during the off-time. With low-duty-cycle converters, this location is advantageous. Also, because of the pulsating current, you can use a current transformer, allowing a sense-resistor value that further reduces dissipation. Finally, the common-mode voltage at B is stable, equal



(a)



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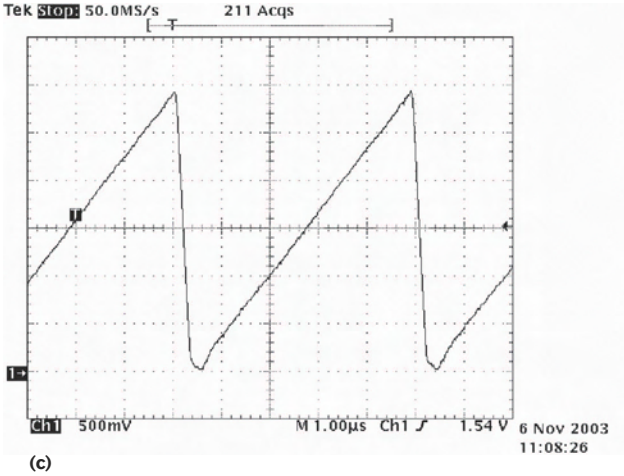

(c)

Figure 5 In this inverting buck-boost voltage-mode converter, a common sense-resistor location is in series with the output inductor (a). The sensed-current wavefore (b) is not beautiful but has no nasty current spike. The jagged edges are measuring artifacts. A second oscillogram (c) depicts the sawtooth-oscillator voltage waveform.

to the value of the input-voltage source during both the on- and the off-times. For PCMC, engineers have extensively used B and consider it optimum.

Now, examine Point F (**Figure 1**) for current sensing: Engineers traditionally use this location for ACMC. The advantages are that F has a stable common-mode voltage, roughly equal to the output voltage during both the on- and the off-times. Also, F represents the average inductor current, which equals the average output-load current. Additionally, the entire inductor-current waveform is sensed, which is necessary for ACMC but not for PCMC. For ACMC, F, a quiet node, is the optimum location.

Now, examine the disadvantages of B and F. With B, the sensed current is pulsed. The current in the sense resistor increases abruptly when you turn on the power and decreases abruptly when you turn it off. Power-switch inductance and neighboring stray inductance combine with this switching action to produce a large turn-on spike on the leading edge. Attempts to filter this noise spike produce only limited success. With current sensing at F, the power dissipation is larger than at B, because conduction and dissipation occur for the entire cycle, versus only during the on-time. Also, at F, a nonzero dc average value exists, and no switching takes place, precluding the use of a current transformer. For these reasons, B is popular for PCMC, and F is popular for ACMC.

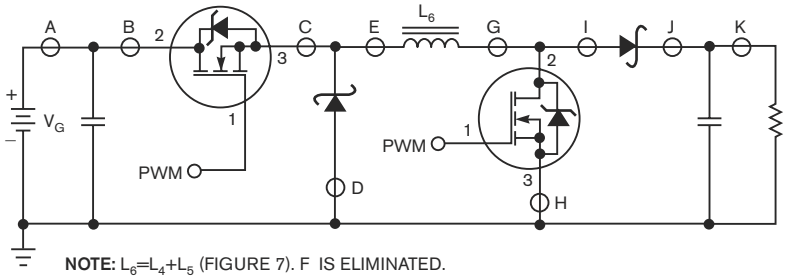

Figure 6 In the noninverting buck-boost topology, it at first appears that there is no acceptable sense-resistor location.

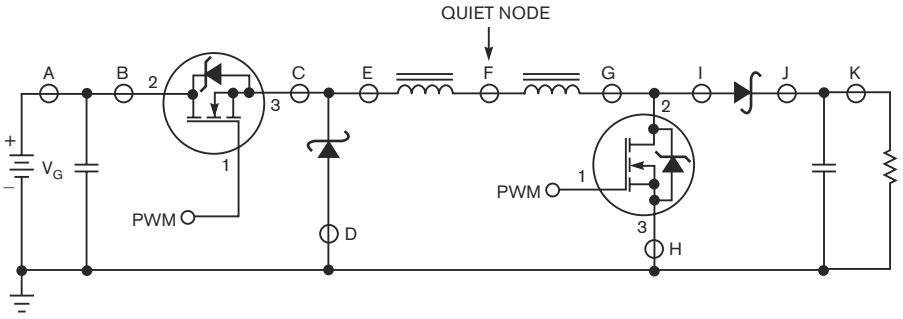

Figure 7 If you can replace the output inductor with two inductors, each having half the value, placing the sense resistor between them yields optimal results.

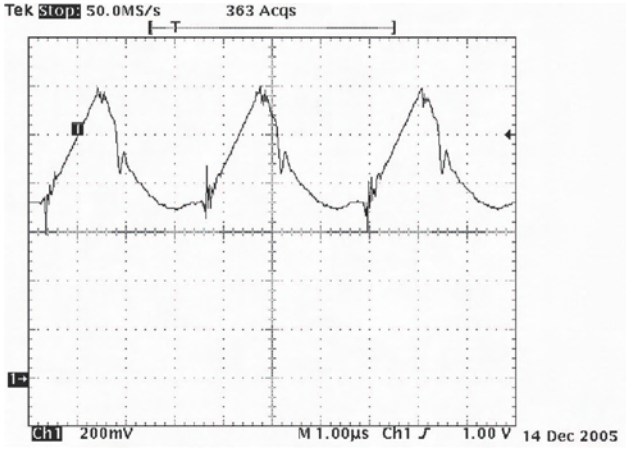

Figure 8 This current waveform shows that the instrumentation amplifier nicely rejects the small common-mode variation that appears at both ends of the sense resistor.

One salient advantage with F is that there is no turn-on spike. Because the sense resistor in F is directly in series with the inductor, neither a turn-on spike nor a turn-off spike occurs. One way of eliminating the spike with PCMC is to use F for current sensing, as ACMC does. The price is higher dissipation, but recently introduced instrumentation amplifiers have alleviated this problem. By using a low-valued sense resistor and locating the instrumentation amp near the resistor, you can obtain low noise and low dissipation (**Figure 2**). One suitable such amplifier is Texas Instruments' (www.ti.com) INA139. The differential, transconductance amp has an input-common-mode range that exceeds the supply. The transconductance value, g_M, is 1 reciprocal kΩ, or 1 mS (millisiemen). The specified gain-bandwidth product is 4.4 MHz. Should this value be insufficient for your application, you can use an additional single-ended op amp in addition to the instrumentation amp. This quiet-node sensing technique produces a waveform relatively free of switching noise.

The price you pay, in addition to the expense of the amplifier, is sense-resistor current, which flows throughout the cycle, increasing the dissipation and, in some cases, the cost of the additional op amp you need to provide additional gain.

BEST FOR AVERAGE AND PEAK CONTROL

Now, focus on the boost-converter topology (**Figure 3**). The quiet nodes for this topology are A and B. For sensing

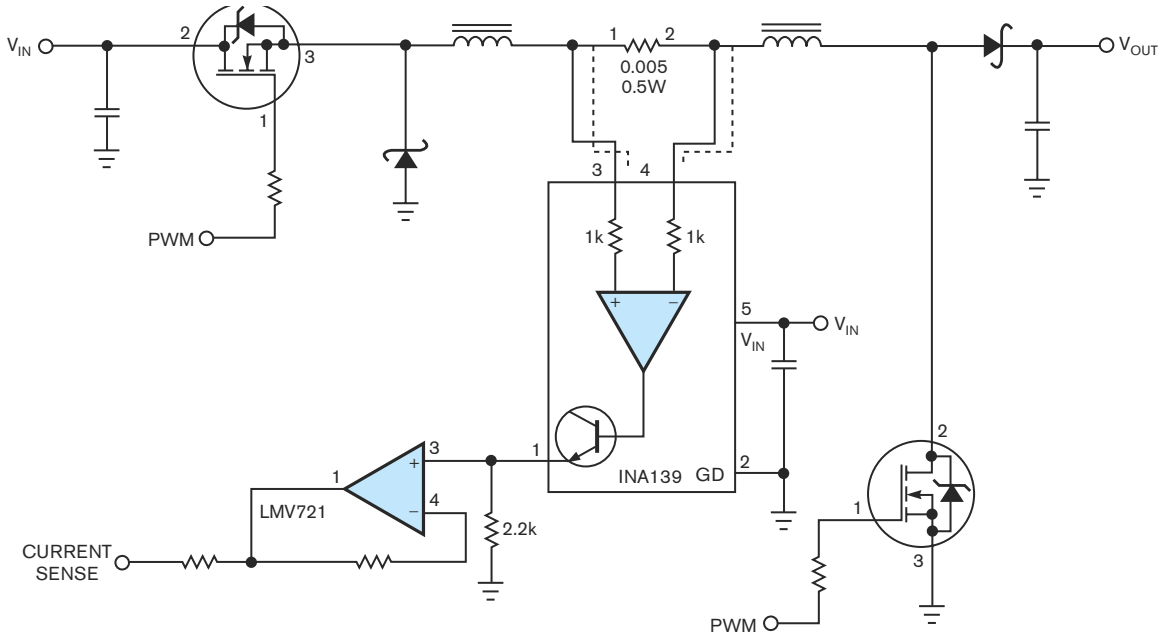

Figure 9 In this noninverting buck-boost converter, the optimal location for the sense resistor and booster-amplifier input is between the two series output inductors.

inductor current, B is optimum and is the choice location for ACMC. PCMC traditionally employs D, but you should use B for PCMC, as well. Note that B is in series with the inductor and has a fixed common-mode voltage, so that the current waveform does not contain the leading-edge spike. Again, power dissipation at B is greater than at D because of conduction over the entire cycle.

With the inverting buck-boost topology (**Figure 4**), the sensing locations have traditionally been B for PCMC and D for ACMC. Using D for PCMC gives the quiet-node benefits, albeit with increased dissipation. One commercially available PWM-control IC dedicated to inverting buck-boost operation—Texas Instruments' UC2572 series—uses this location for current sensing (**Figure 5a**). It is a VMC type with direct duty-cycle control rather than input feedforward control. The current-sense waveform appears in **Figure 5b**. Once again, the normal location for ACMC is actually optimum for PCMC, as well (**Figure 5c**).

Now, turn your attention to the noninverting buck-boost topology (**Figure 6**). As far as sensing inductor current goes, the location possibilities include B, C, D, E, G, H, I, and J. Unfortunately, all of these locations carry a disturbance, either current- or voltage-related. Locations B, D, H, and J have a quiet voltage but pulsating current, which is prone to the turn-on spike. Nodes C and I have the same noisy current, plus a pulsating voltage, switching from V_G to ground. Nodes E and G have quiet currents but pulsating voltages. Unfortunately, none of the locations offers both quiet current and quiet voltage. There appears to be no good location for current sensing.

However, if you recall how you derive a noninverting buck-boost inverter, you observe the following: The converter is merely a cascade of a buck stage followed by a boost stage (**Figure 7**). With the buck stage, an inductor is in the output, whereas, in the boost stage, an inductor is in the input. If you observe the midpoint of the two series inductors, you see that Node F, the midpoint of the two series inductors, has a quiet current because it is between two inductors. Also, the voltage is quiet and stable. During the switch's on-time, Node E is near V_G, and Node G is near ground, so the voltage at Node F is about half of V_G. During the switch's off-time, Node E is near ground, and Node G is near the output voltage, V_O, so that F is about half of V_O. If the input voltage, V_G, spans 9 to 16V, then during the on-time, Node F is at about 4.5 to 8V. If the output, V_O, is 12V, then, during the off-time, Node F is at about 6V. The voltage at F is not absolutely constant but certainly is steadier than the voltage anywhere else. As the current waveform of **Figure 8** shows, the instrumentation amplifier rejects the small common-mode variation. Hence, for the noninverting buck-boost converter, the optimum location, or quiet node for current sensing, is the midpoint of the two series-connected inductors. Unfortunately, combining the two inductors into one inductor with twice the value often eliminates this quiet node, an undesirable consequence. Instead, if you realize the inductive energy-storage element as a pair of series-connected inductors, their midpoint offers a quiet node for optimum current sensing. Place the sense resistor and instrumentation amplifier as **Figure 9** shows.

Figure 8 depicts a prototype for the noninverting-buck-boost-converter topology with quiet-node current sensing, and **Figure 9** shows the corresponding current-sense waveform. On a scope, the waveform is quiet, stable, and free of jitter. It looks much like a VMC sawtooth waveform (**Figure 5c**), which is quiet and jitter-free. The switching-node pulse waveforms are also stable, with low jitter. The converter in this example accepts inputs of 9 to 16V and produces 12.1V at 4A. At low-line input, the duty factor is 0.6, or 60%, and the power loss in the current-sense resistor is 0.303W. If you place the resistor at B, the traditional PCMC practice, power loss would be 0.182W, a difference of 0.121W. With the output power of 48.4W, 0.121W constitutes an efficiency penalty of just 0.25%. At high-line input, the power loss is 0.166W with a 0.452 duty factor. Sensing at B gives a loss of 0.075W, a 0.091W differential. The efficiency penalty is a mere 0.19%.

The leading-edge noise spike, the most severe problem you encounter with PCMC, is a direct result of the location of the current-sense resistor.

For nonisolated dc/dc converters using PCMC, the leading-edge noise spike, the most severe problem you encounter with PCMC, is a direct result of the location of the current-sense resistor. Relocating this resistor to a point you traditionally use for ACMC eliminates the leading-edge spike and greatly improves SNR performance at the cost of increased dissipation. Using an instrumentation amplifier close to a low-valued resistor minimizes this penalty. A noninverting buck-boost topology traditionally implements the power-stage inductor as a single component. Using a series-connected pair of inductors, each half the value of the single part, eliminates the leading-edge turn-on-current spike and realizes a quiet node at the inductors' midpoint, making it possible to obtain PCMC with low noise. Until now, this goal had been unattainable. **EDN**

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REFERENCES

1. "UC3842/3/4/5 provides low-cost current-mode control," Unitrode application note U-100A, Texas Instruments, 1999.
2. Spaziani, Larry, "Conditioning a power-supply current signal using TI op-amps," Texas Instruments application report SLOA 044, 2000.
3. Mammano, Bob, "Current-sensing solutions for power-supply designers," Texas Instruments, 2001.
4. Dixon, Lloyd, "Average current-mode control of switching power supplies," Texas Instruments, 2001.
5. Rogers, Everett, "Understanding buck-boost power stages in switch-mode power supplies," Texas Instruments Application Report SLVA059, 1999.
6. "A new integrated circuit for current-mode control," Unitrode application note U-92, Texas Instruments, 2003.
7. UCC28C40-45 Data Sheet, Texas Instruments, 2003.
8. Andreycek, Bill, "The UCC38C42 family of high-speed, BiCMOS current-mode PWM controllers," Texas Instruments application report SLUA257, 2002.
9. UC3842B Data Sheet, On Semiconductor, 2001.
10. Current-mode control, Venable Industries, Venable Technical Paper No. 5.