

# ASUS CONFIDENTIAL

MODEL NAME : *Elsa*

PCB NO : ???

ASUS P/N : ???

## Lanai UMA Schematics Document

uFCPGA Mobile Merom  
Intel Crestline-GM + ICH8M

2007-03-19

REV :1.2(DELL: X02)

MB PCB

Part Number	Description
DA800004H0L	PCB 00B LA-3071P REV0 M/B

*BOM NO. ???*

*PCB P/N: ???*

PROJECT:

REVISION

1.2

DATE: Monday, March 19, 2007

SHEET 1 OF 68

DESCRIPTION:

Cover Page

SCHEMATIC FILE NAME :

RELEASE DATE :

DESIGN ENGINEER :

# LANAI: UMA

**CLOCK**  
CK410M+LP  
PG 21

**POWER**

POWER SEQUENCE LOGIC	PG 51
POWER CHARGER	PG 57
POWER CONTROL SWITCH	PG 49
DISCHARGE PATH	PG 49
+3.3V_SUS/+5V_SUS/+3.3V_RUN +5V/+3.3V/+1.8V/+1.25V_RUN	

POWER CON. PG 59

**Merom**  
(478 Micro-FCPGA)  
PG 7,8  
(Symbol Rev.09)

**POWER**

POWER I/O	PG 55
+1.5V_RUN/+1.05V_VCCP	
REGULATOR	PG 58
+VCC_GFX_CORE/+1.25V_RUN	
POWER VCORE	PG 53
POWER SYSTEM	PG 54
5V_ALW & 3.3V_ALW	
REGULATOR	PG 56
+1.8V_SUS/+0.9V_DDR_VTT	

Panel Connector  
PG 28

**Crestline**  
1299 uFCBGA  
PG 9,10,11,12,13,14  
(Symbol Rev.09)

DDR2-SODIMM1  
PG 19

DDR2-SODIMM2  
PG 19

**IO Board**

CRT CONN.	VGA	D.B CON PG 50
TV CONN.	TVOUT	
USB CONN.x2	USB2.0 (P2,3)	
MINI-CARD WLAN	PCIEx1 (Lane2)	
MINI-CARD WWAN	USB2.0 (P9)	

**ICH8-M**  
676 BGA  
PG 15,16,17,18  
(Symbol Rev.09)

USB CONN.  
PG 39  
USB Board

SIM CARD Board

AUDIO/AMP  
PG 44,45,46

MDC  
PG 36

S/PDIF TO TV CONN.  
PG 30

DIGITAL MIC.  
PG 28

Speaker CON  
PG 46

WtoB CON  
PG 46

Audio Jacks \*3  
JACK Board

RJ11 Board

SIO MEC5025  
128KB Flash  
TMKBC  
128 Pins VTQFP  
PG 37

SIO ECE5011  
Expander  
USB 2.0 Hub (4)  
128 Pins VTQFP  
PG 38

CAMERA  
PG 28

SATA-HDD  
PG 31

CD-ROM  
PG 31

CARD READER  
1394/R5C833  
PG 32,33,34

EXPRESS-CARD  
R5538  
PG 35

BCM5906KMLG  
QFN-68  
PG 47

RJ45/Magnetic  
PG 48

Bluetooth  
PG 41

CIR  
PG 41

FLASH  
PG 40

Touchpad CON.  
PG 41

FAN & THERMAL  
EMC4001  
PG 43

USER INTERFACE  
PG 42

SNIFFER  
PG 42

CAPBTN CON.  
PG 40

PROJECT:	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME:	DESIGN ENGINEER:
	1.2	SHEET 2 OF 68	BLOCK DIAGRAM	RELEASE DATE:	



Footprint Definition	
Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

**Layout Note**

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE			
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

PCI Express TABLE	
Lane 1	WWAN / Mini Card
Lane 2	WLAN / Mini Card
Lane 3	
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5906KMLG

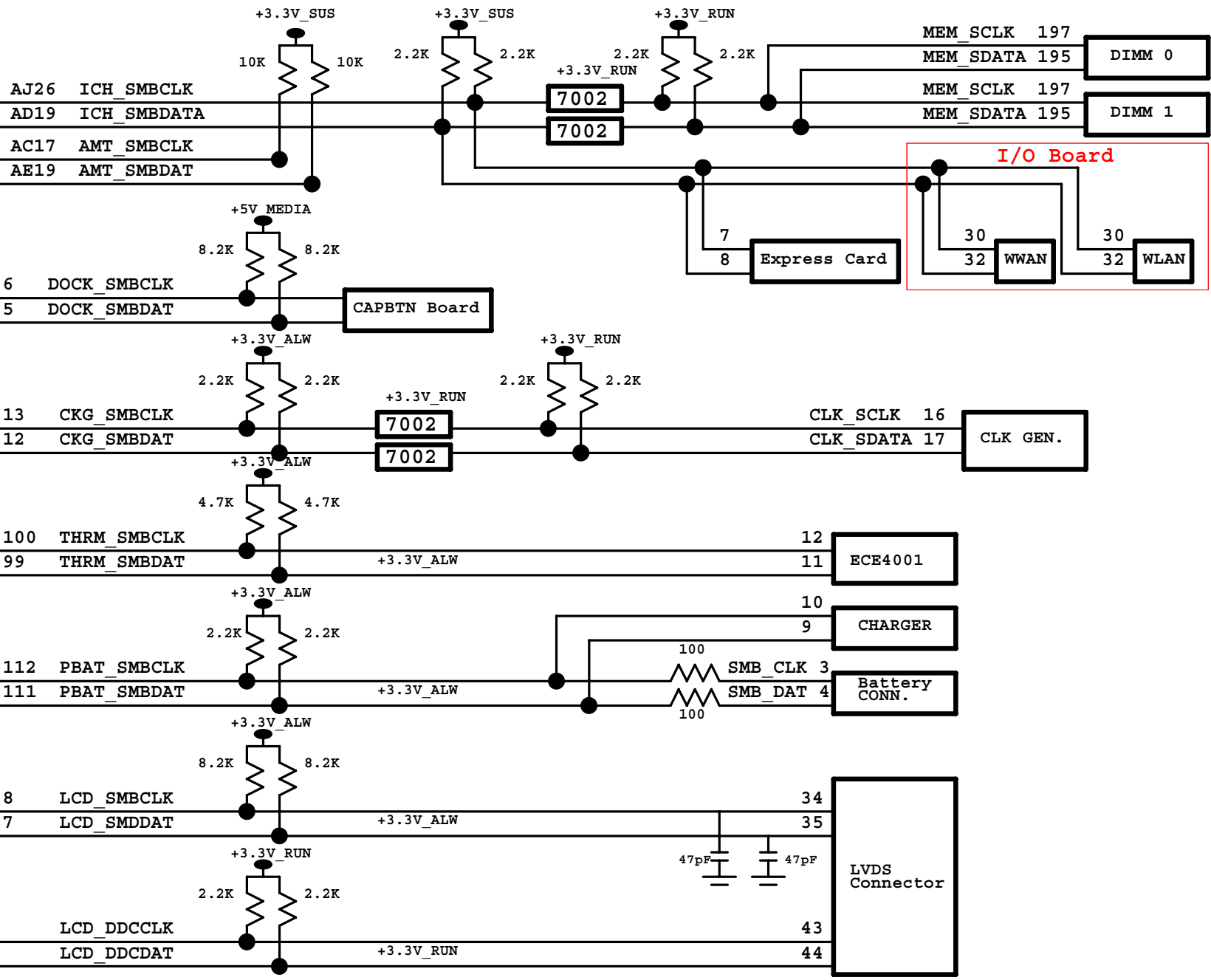
USB TABLE	
ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	User2 (Single port , in USB BD)
ICH8-2 (EHCI#1)	User3 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User4 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	
ICH8-5 (EHCI#1)	Camera
ICH8-6 (EHCI#2)	ExpressCard
ICH8-7 (EHCI#2)	BT Module
ICH8-8 (EHCI#2)	
ICH8-9 (EHCI#2)	WWAN / Mini Card

Note : No USB for WLAN

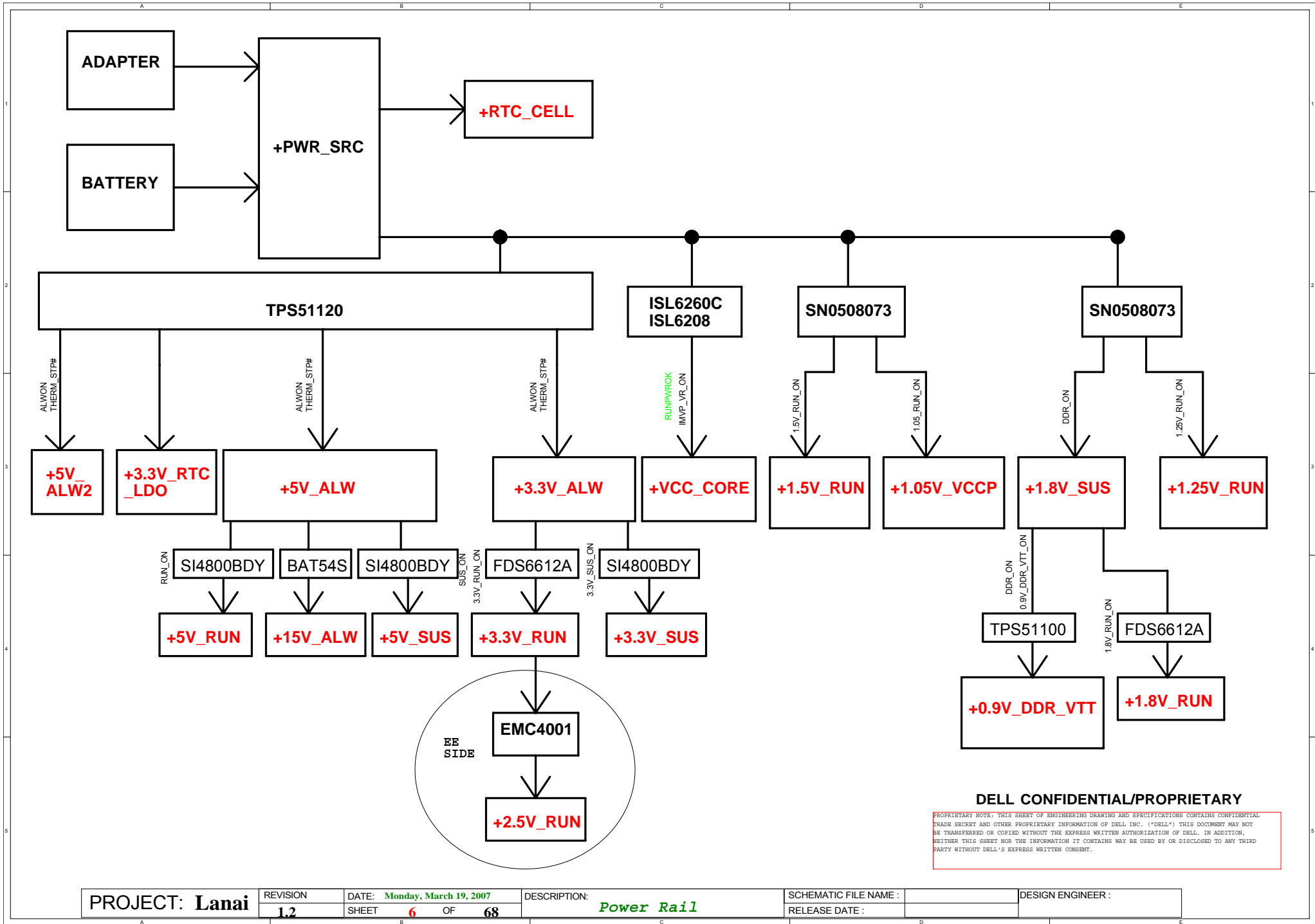
**ICH8-M**

**SIO  
MEC5025**

**VGA**



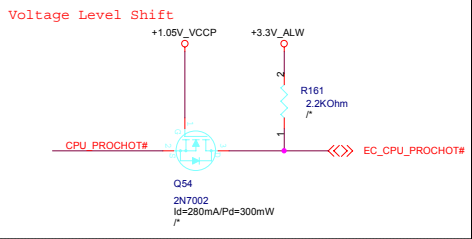
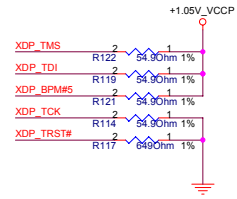
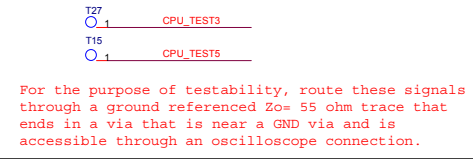
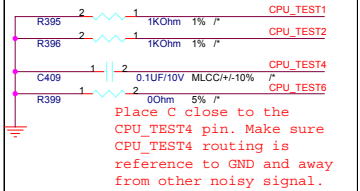
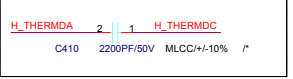
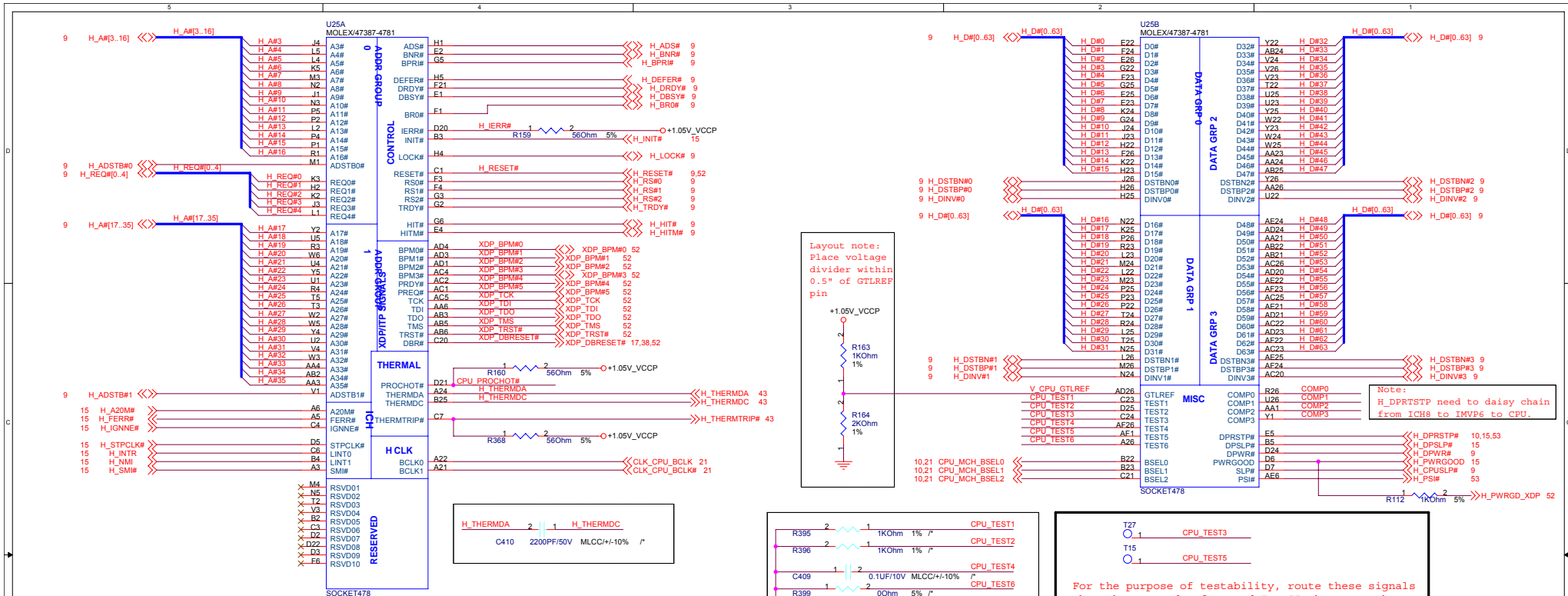
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME:	DESIGN ENGINEER:
	1.2	SHEET 5 OF 68	SMBUS BLOCK	<OrgName>	
				RELEASE DATE:	



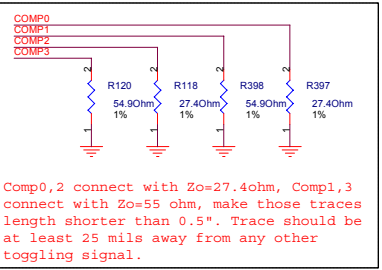
**DELL CONFIDENTIAL/PROPRIETARY**

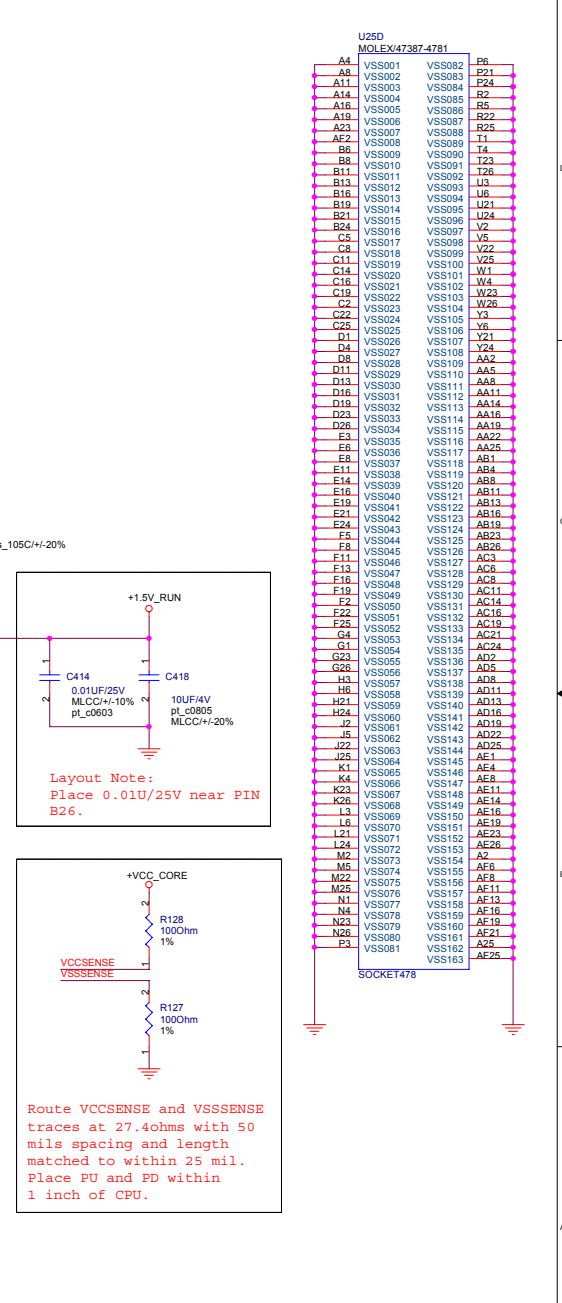
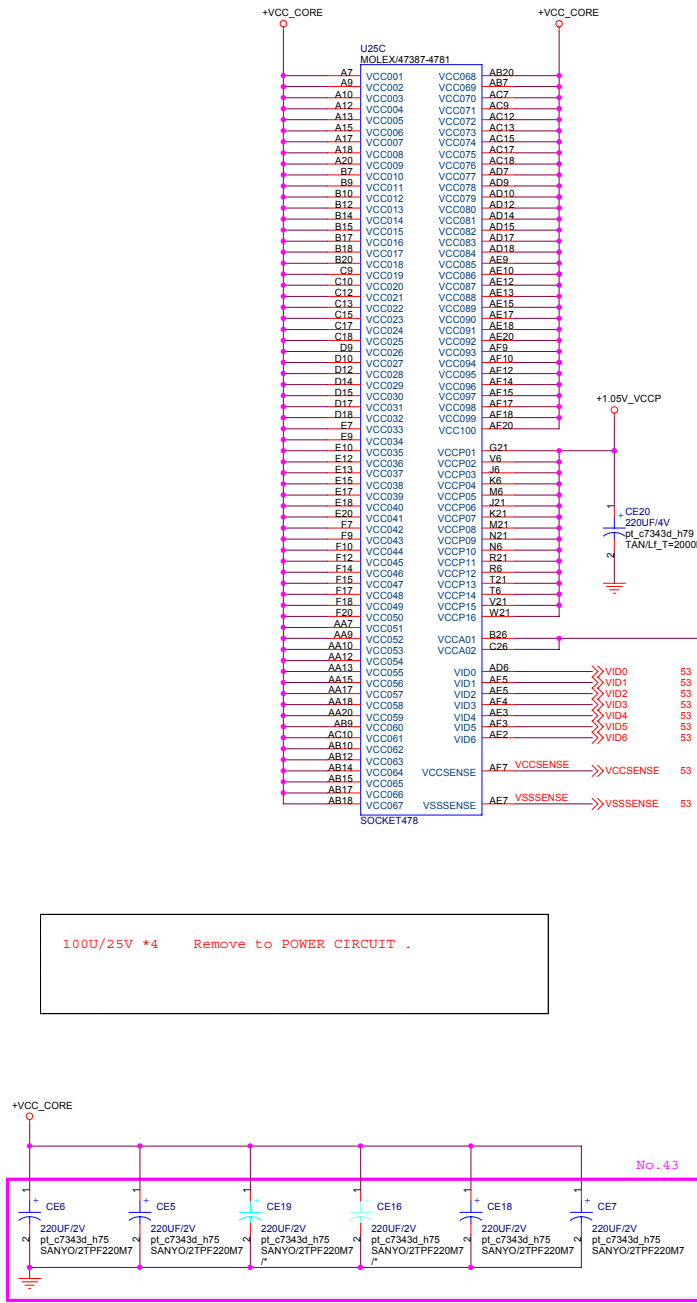
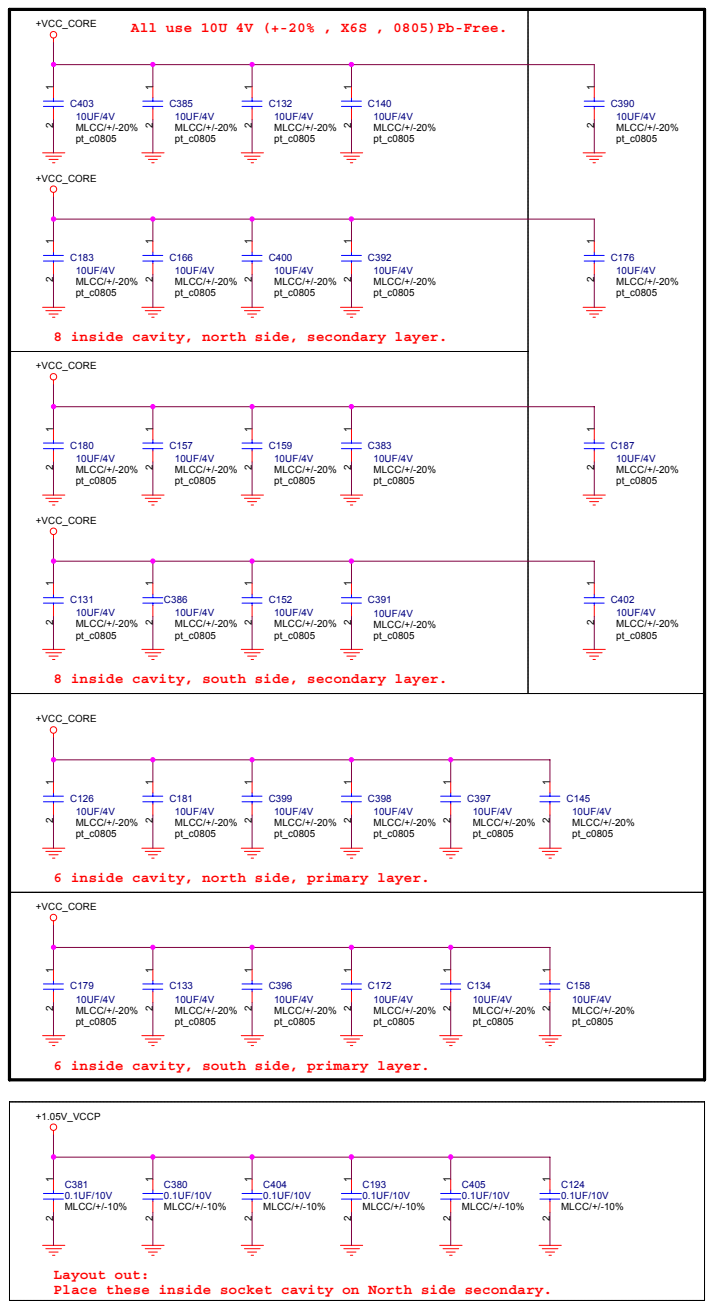
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

PROJECT: <b>Lanai</b>	REVISION <b>1.2</b>	DATE: <b>Monday, March 19, 2007</b>	DESCRIPTION: <b>Power Rail</b>	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET <b>6</b> OF <b>68</b>		RELEASE DATE :	

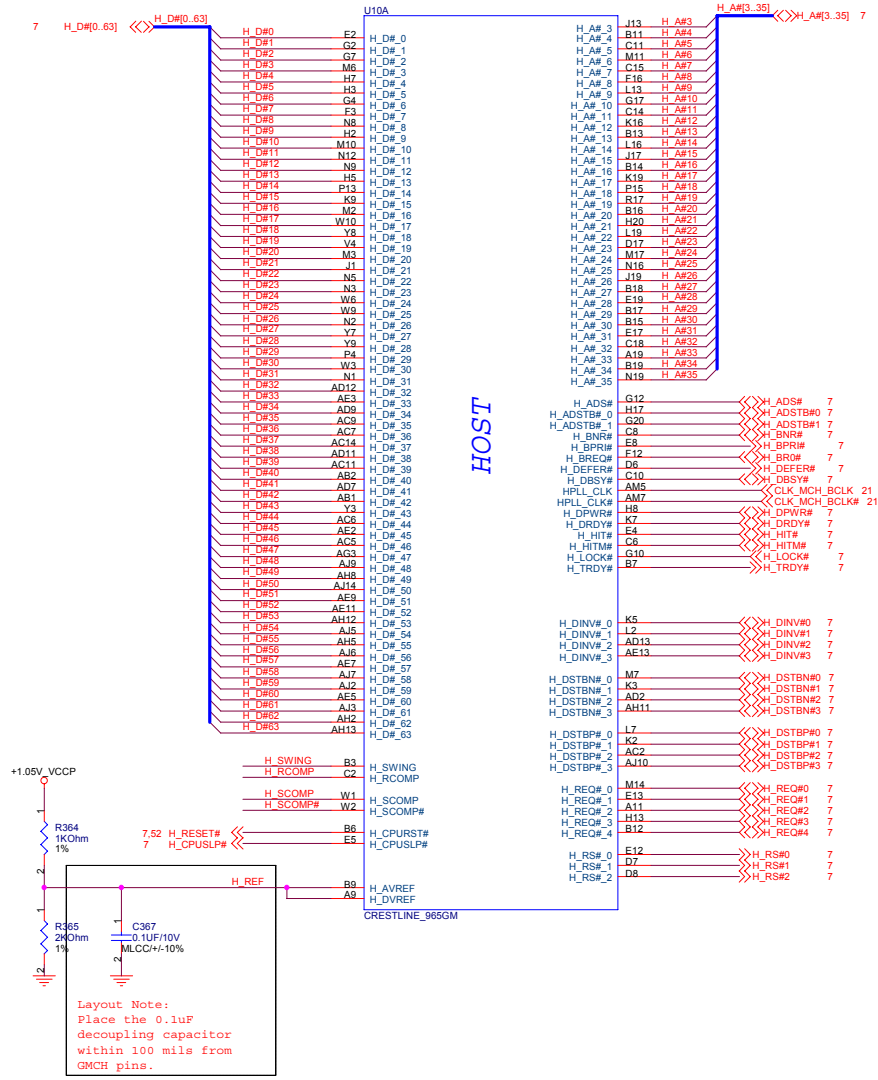
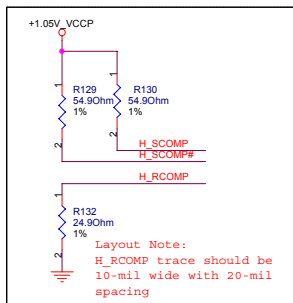
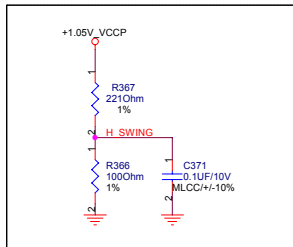


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

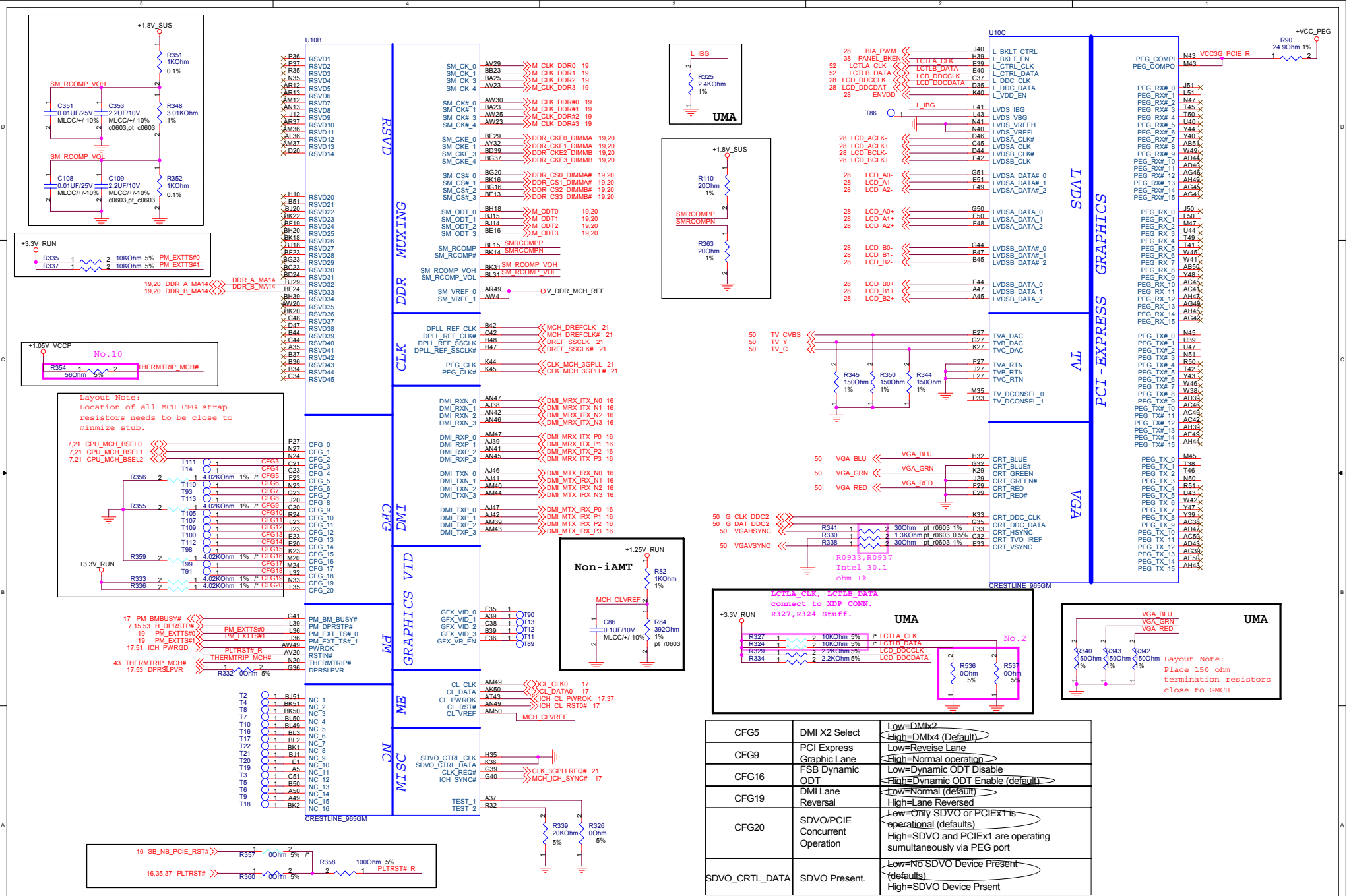




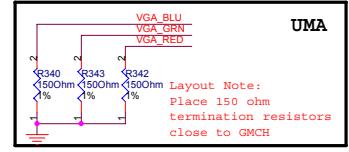
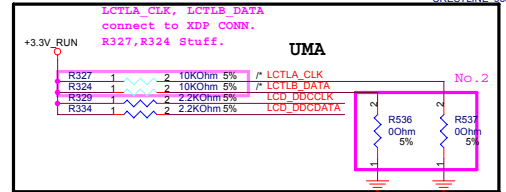
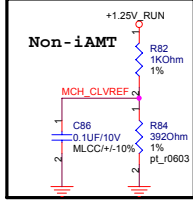
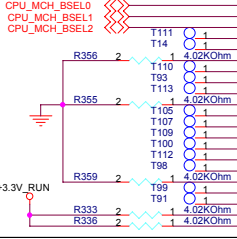




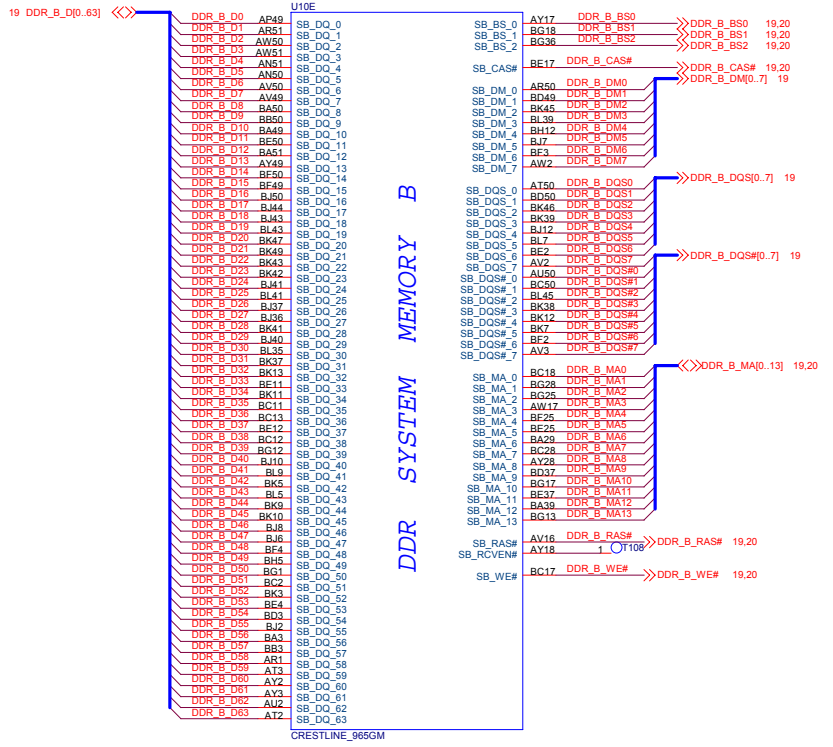
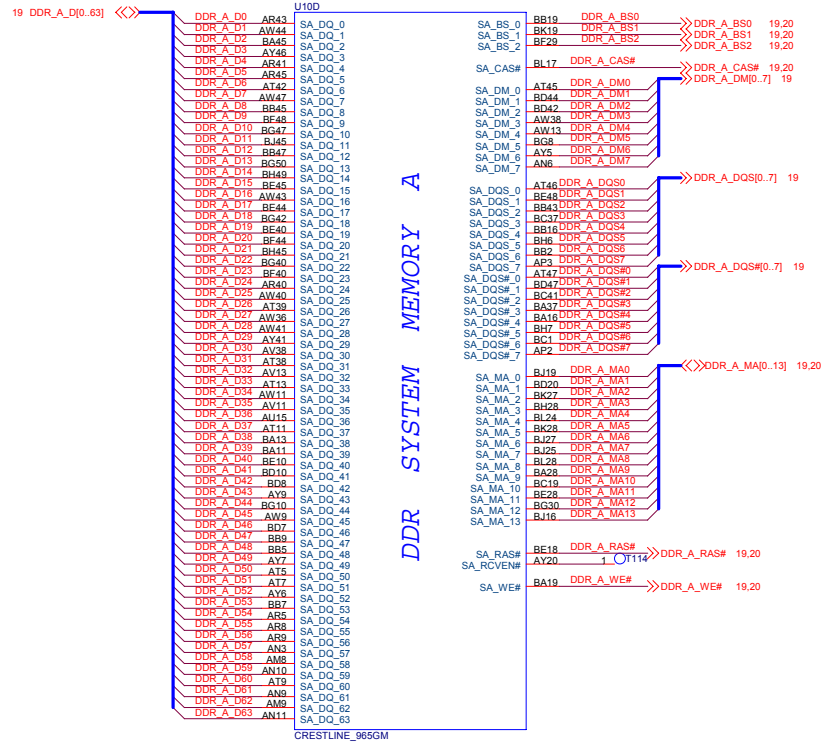
Layout Note:  
Place the 0.1uF  
decoupling capacitor  
within 100 mils from  
GMCH pins.



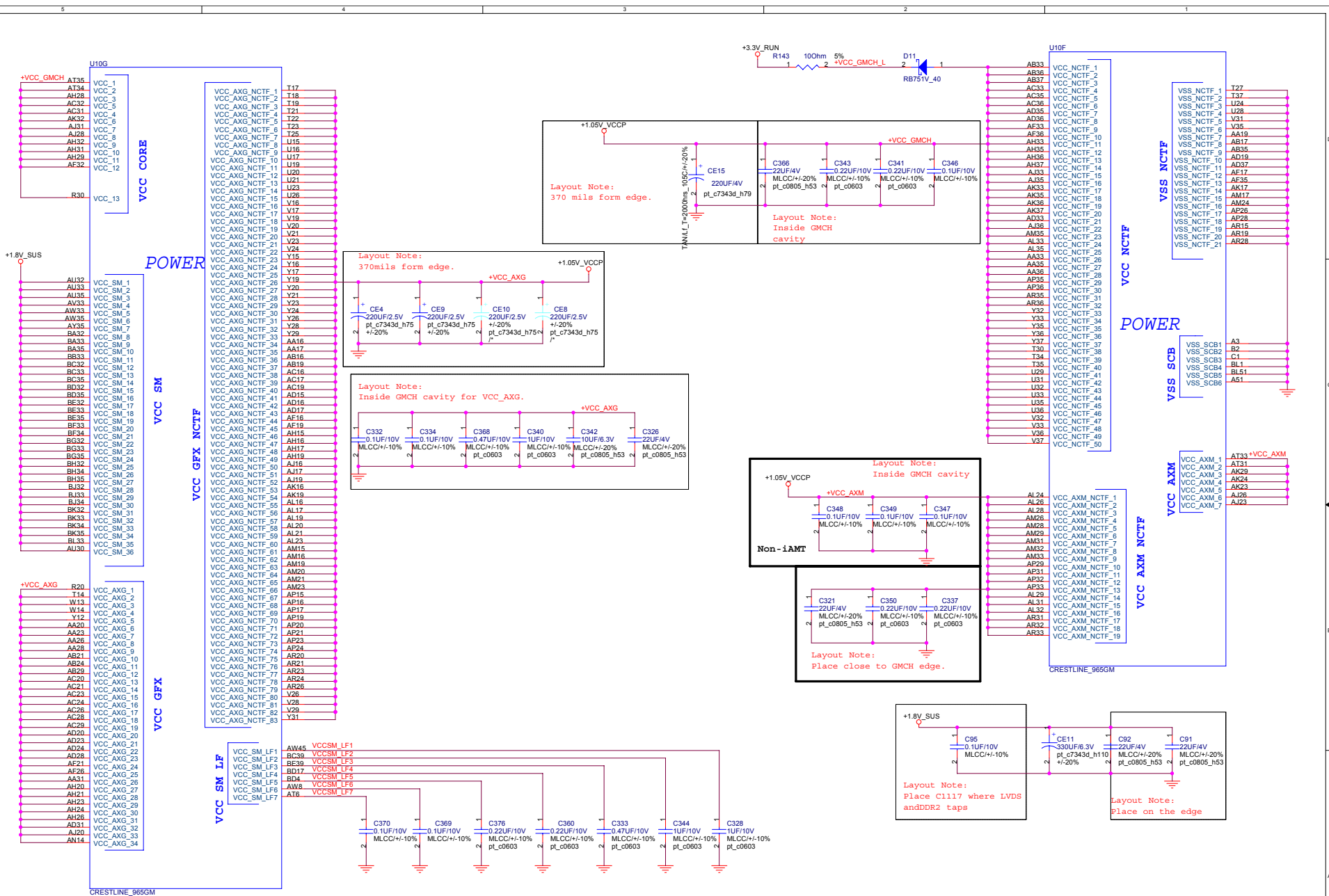
**Layout Note:**  
Location of all MCH\_CFG strap resistors needs to be close to minimize stub.



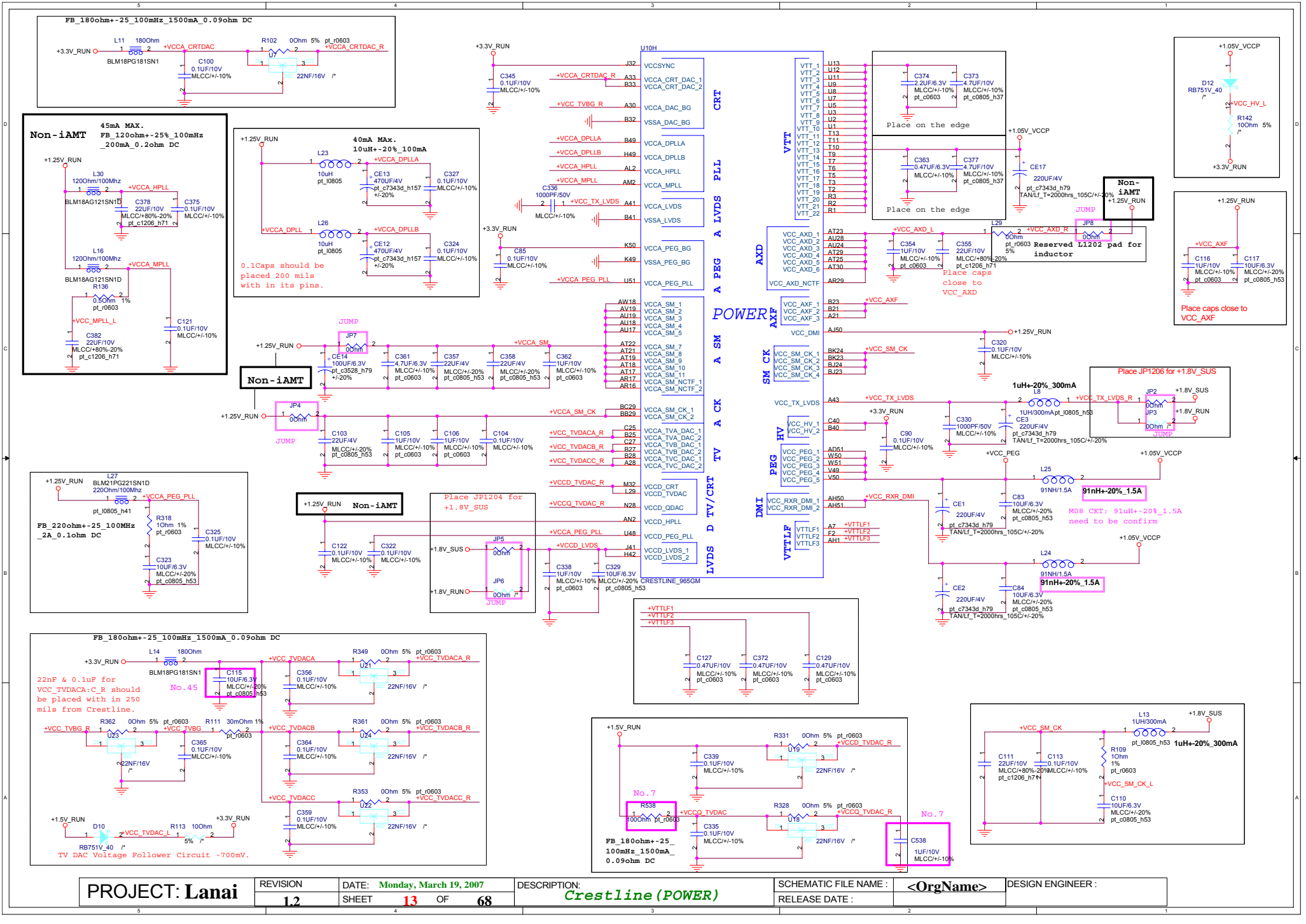
CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reverse Lane High=Normal operation
CFG16	FBSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIe Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (defaults) High=SDVO Device Present



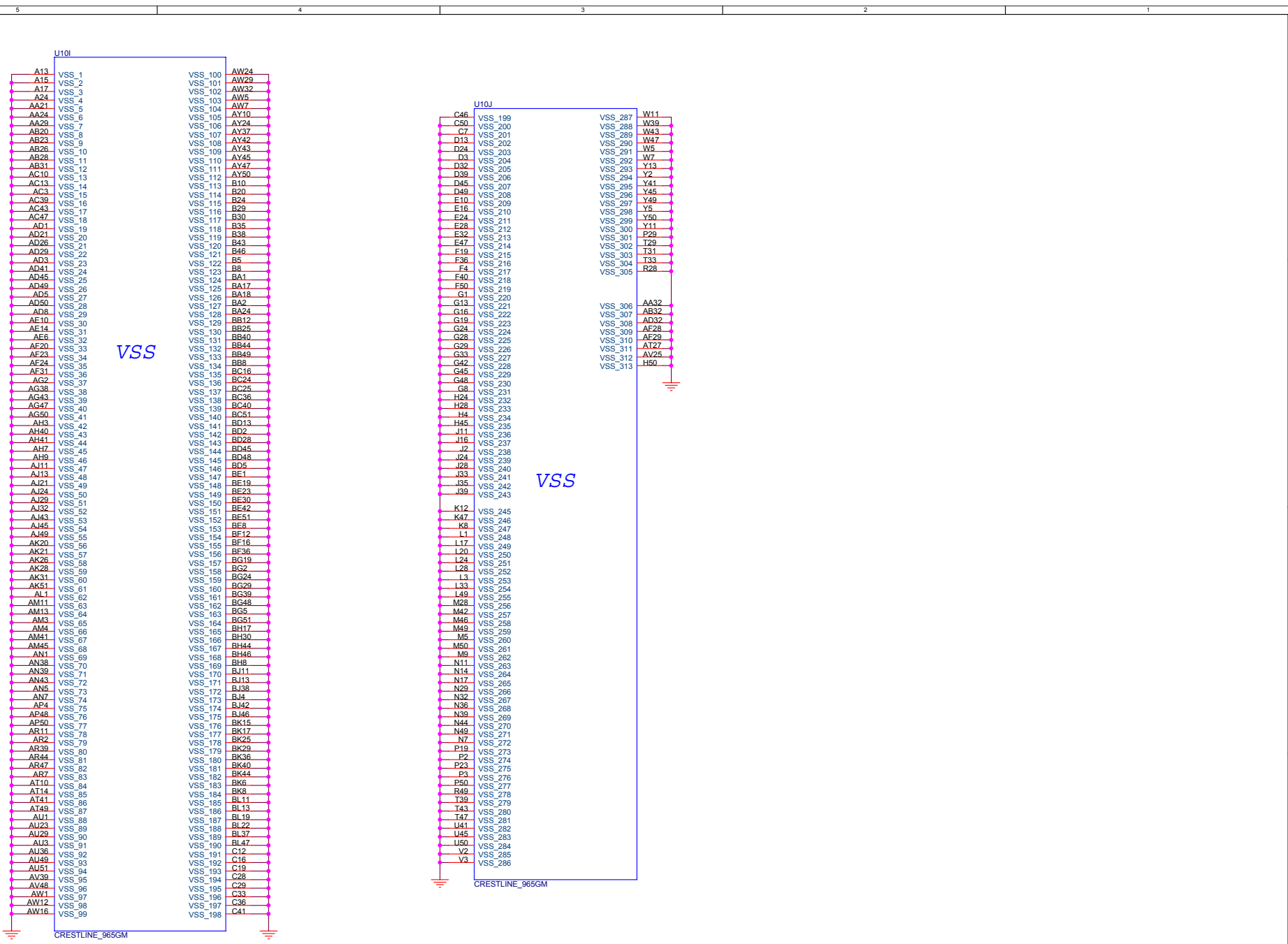
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME:	<OrgName>	DESIGN ENGINEER:
	1.2	SHEET 11 OF 68	Crestline (DDR2)	RELEASE DATE:		



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME:	DESIGN ENGINEER:
	12	SHEET 12 OF 68	Crestline (VCC, NCTF)	<OrgName>	
				RELEASE DATE:	

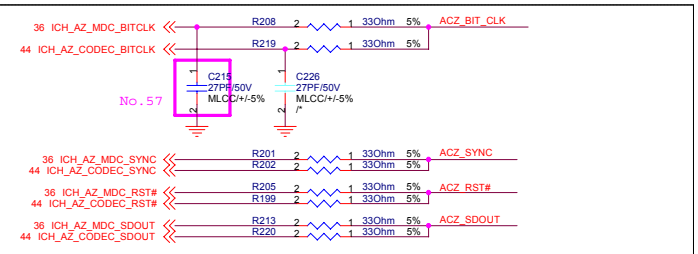
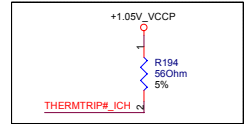
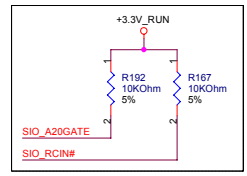
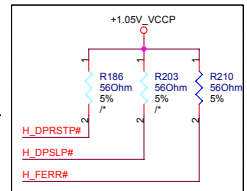
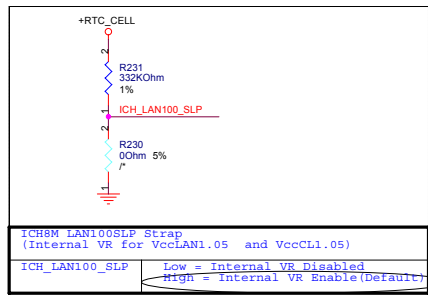
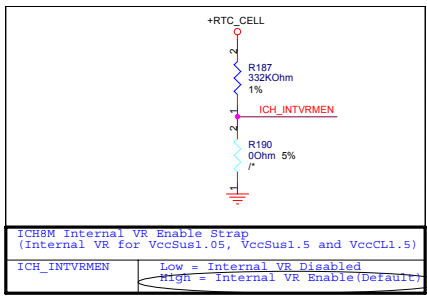
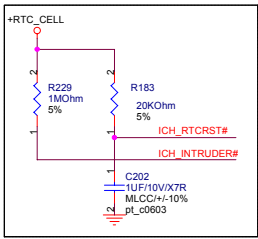
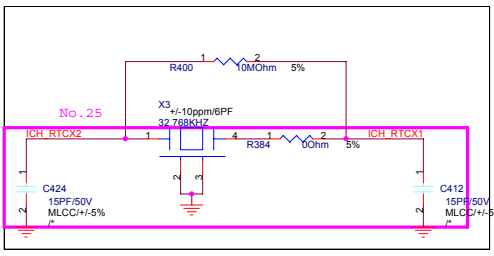


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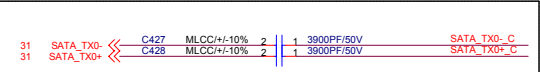


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 14 OF 68	Crestline (VSS)	RELEASE DATE :		

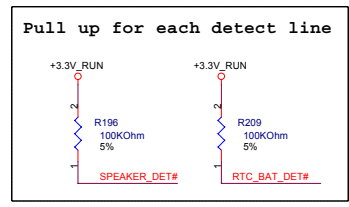
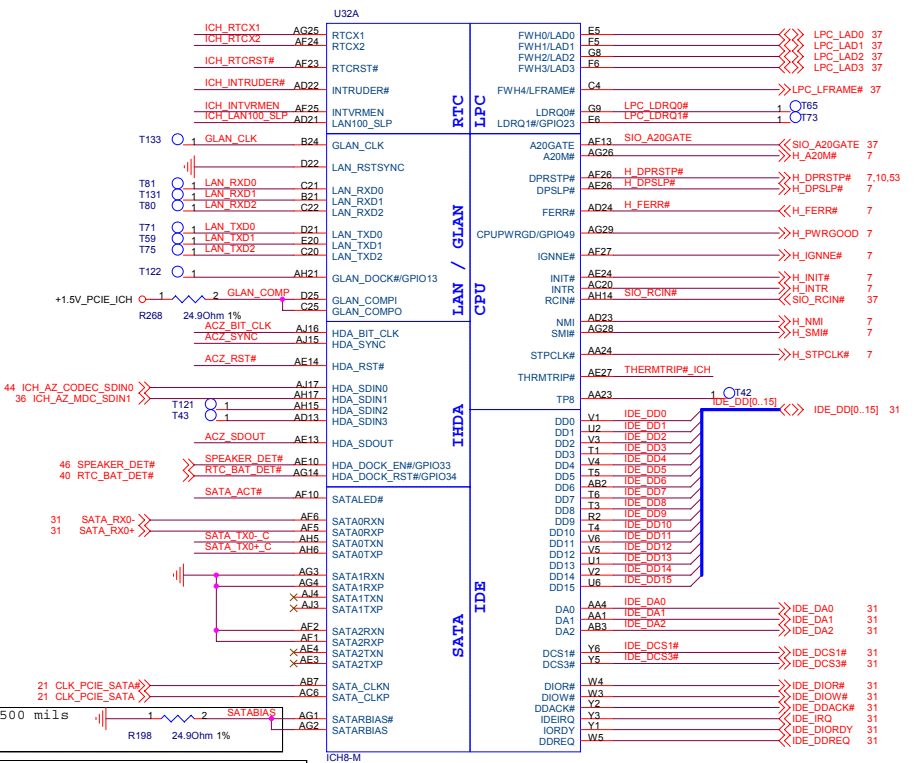
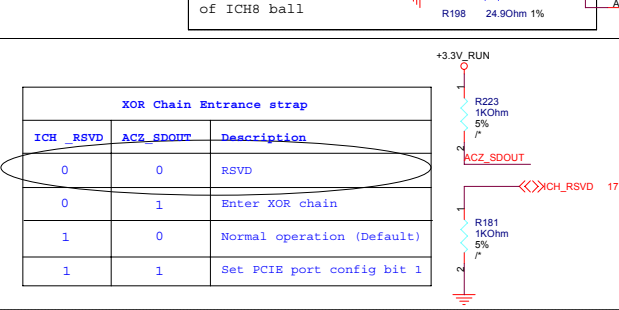
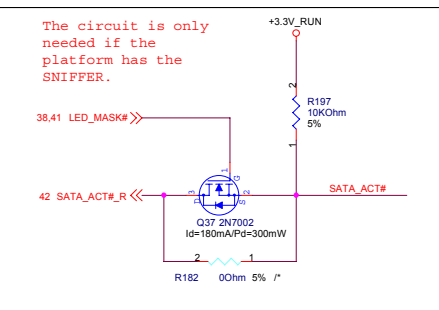


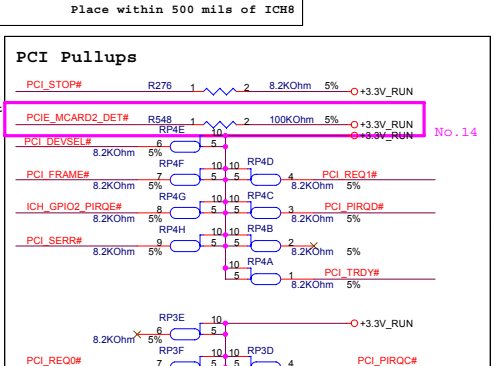
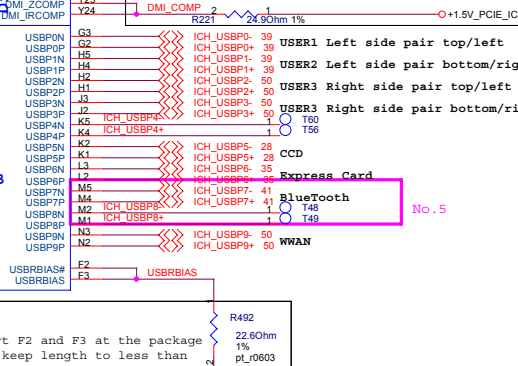
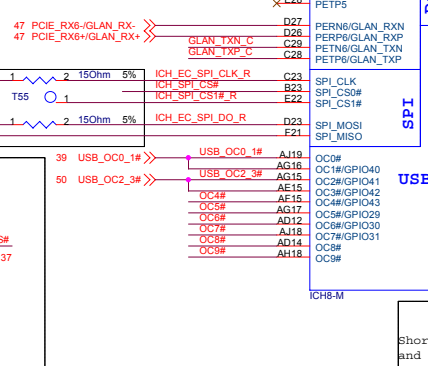
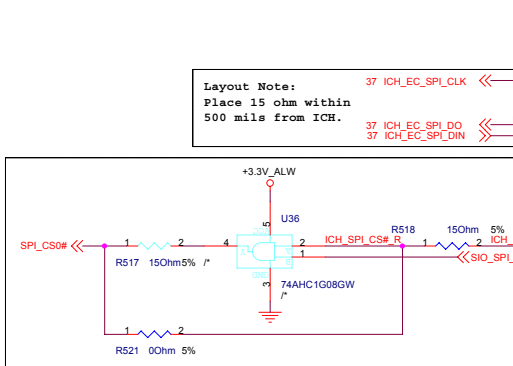
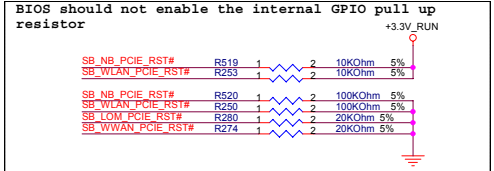
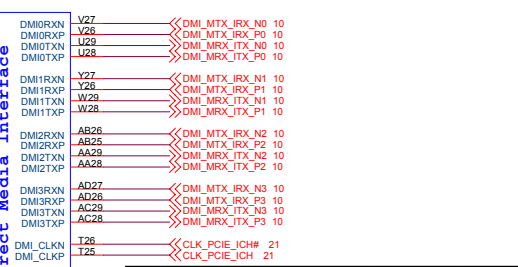
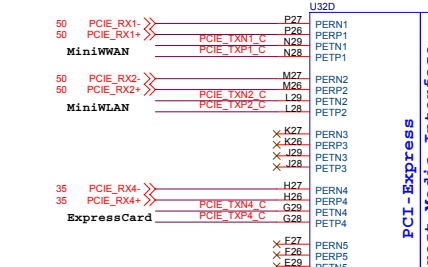
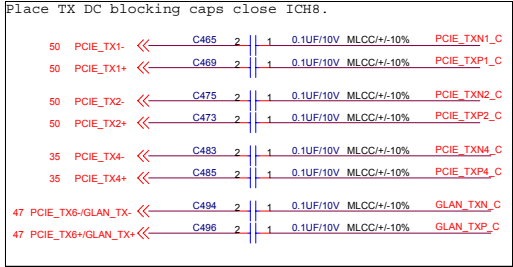


Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R208, R201, R205, R213 should equal distance to the T split trace point as R219, R202, R199, R220 respective. Basically, keep the same distance from T for all series termination resistors.

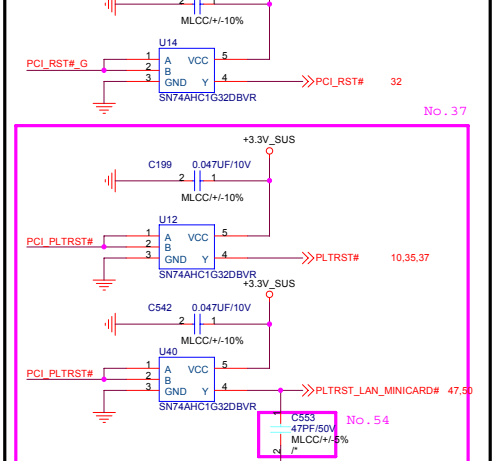
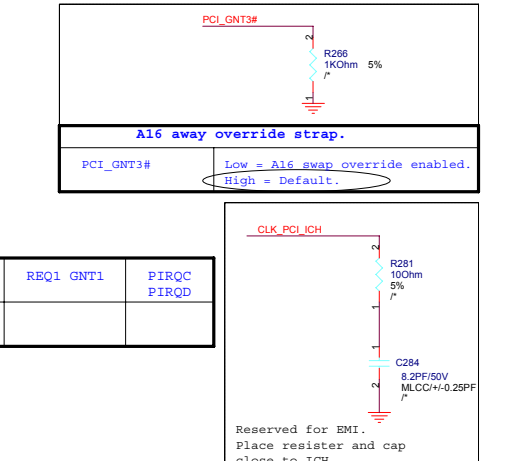
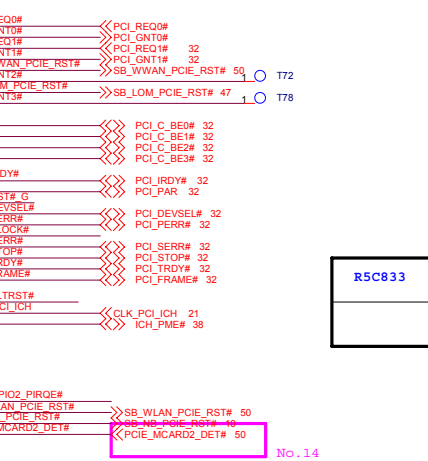
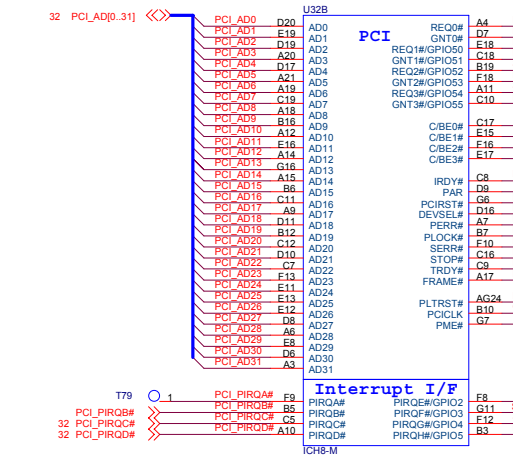
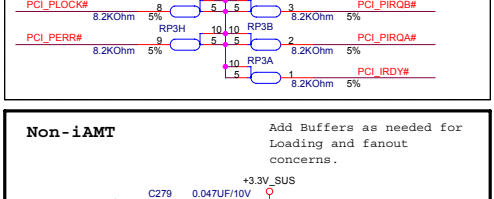
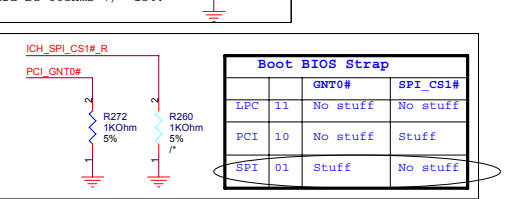
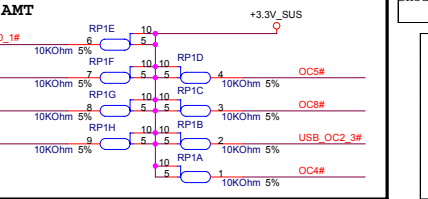


Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.

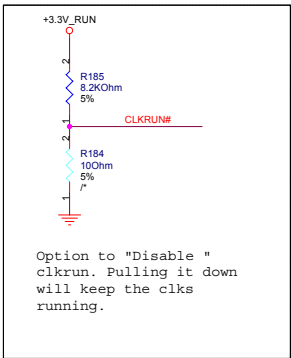
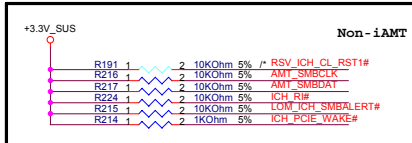
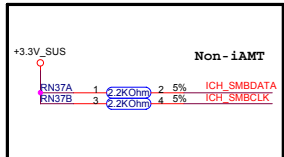




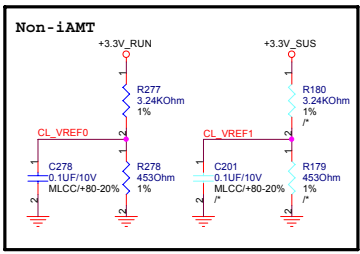
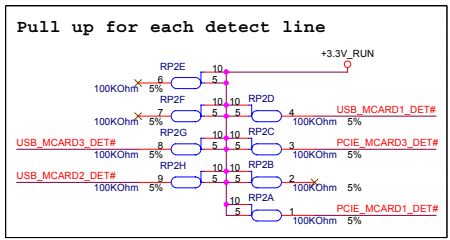
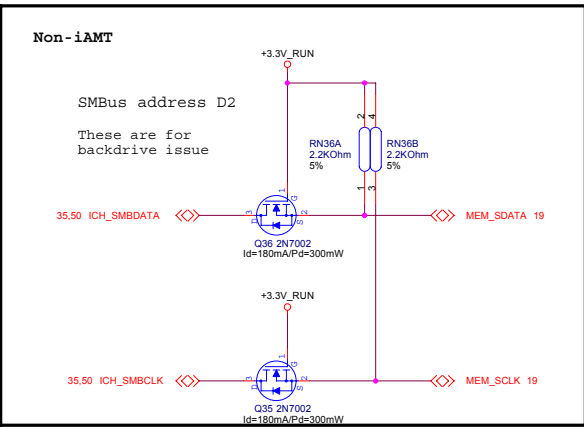
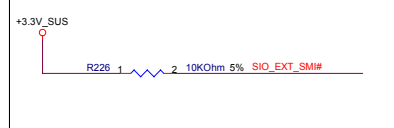
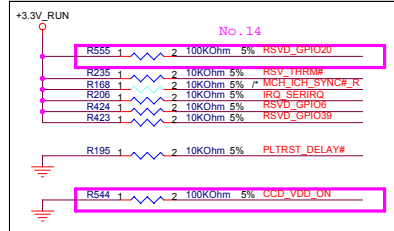
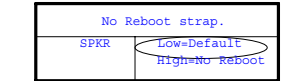
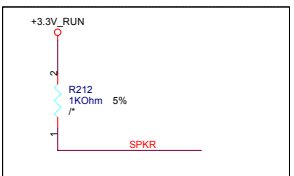
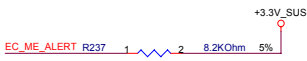
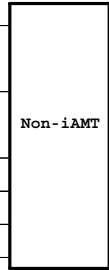
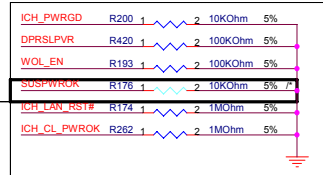
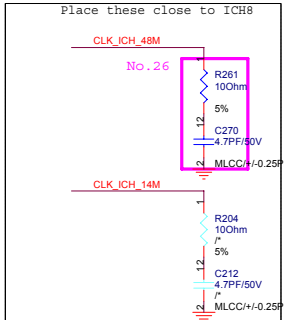
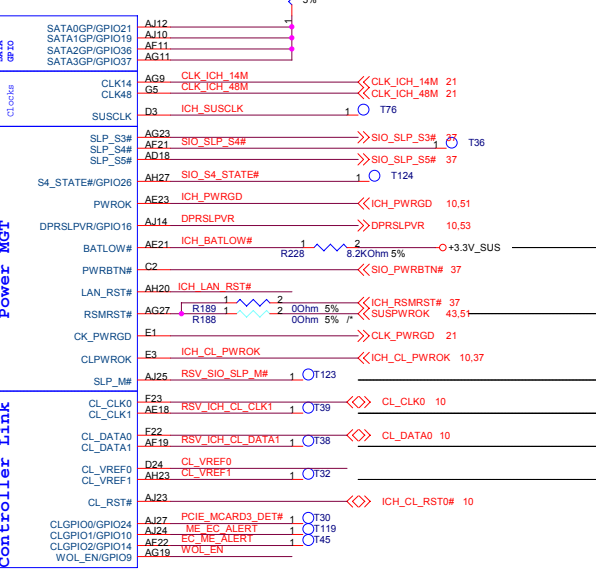
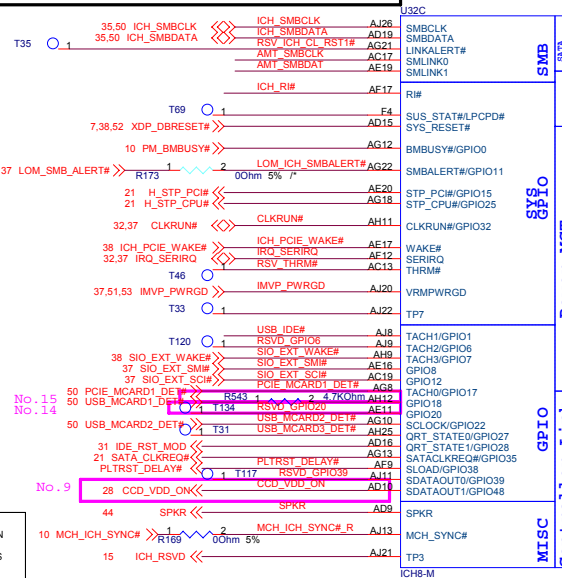
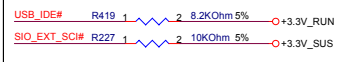
**Layout Note:**  
Place 15 ohm within 500 mils from ICH.





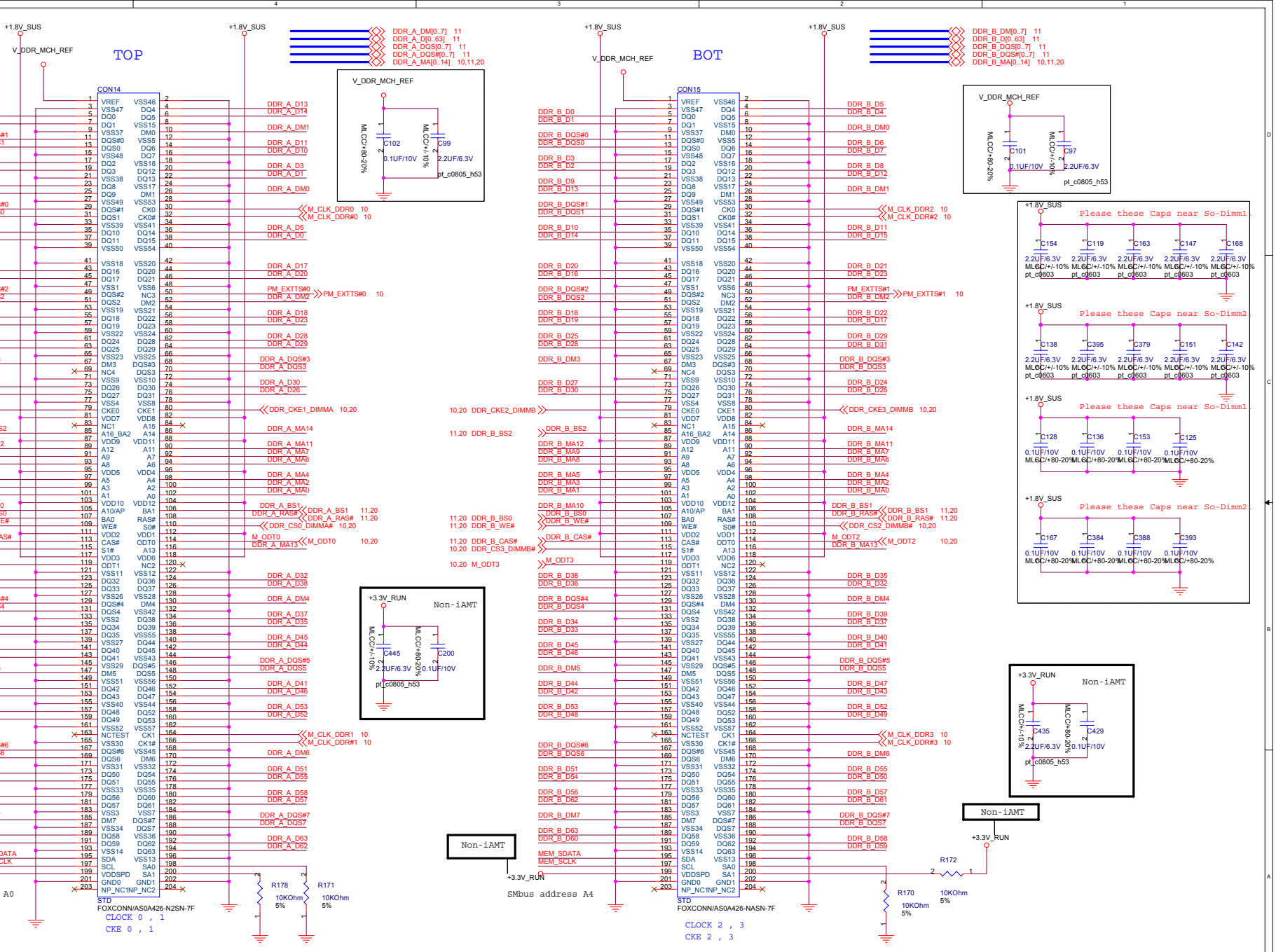


Option to "Disable" clkrun. Pulling it down will keep the clks running.

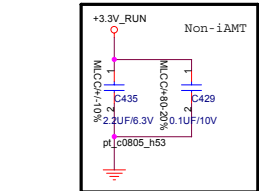
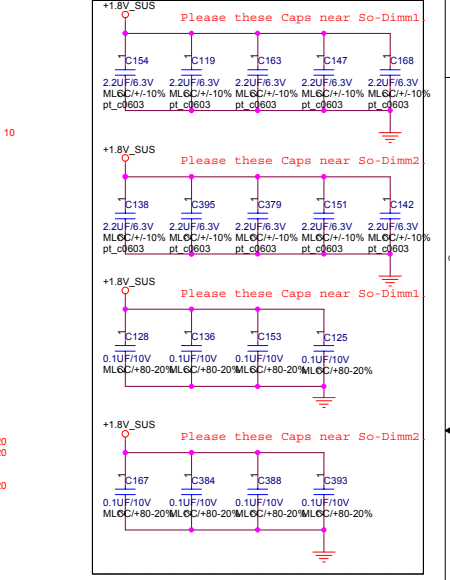
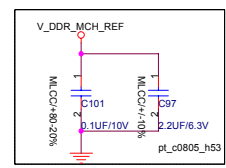




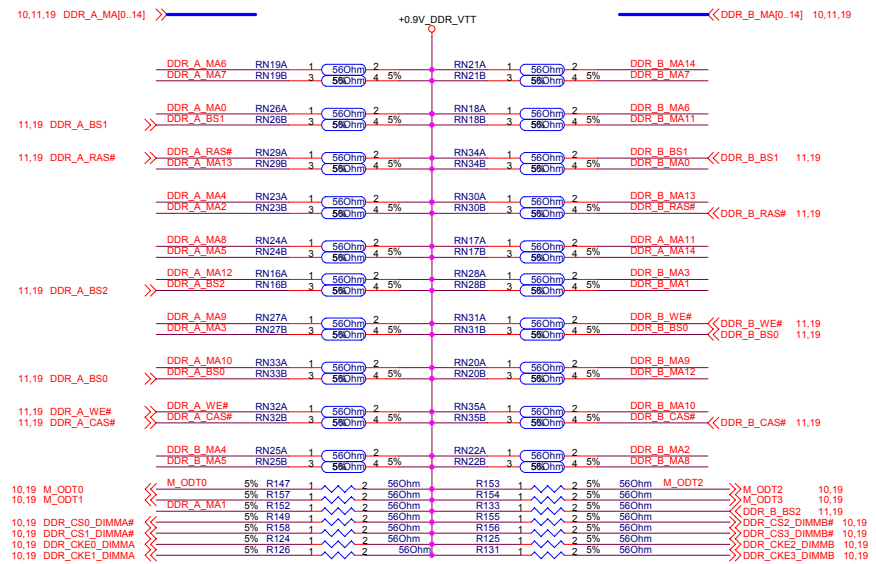
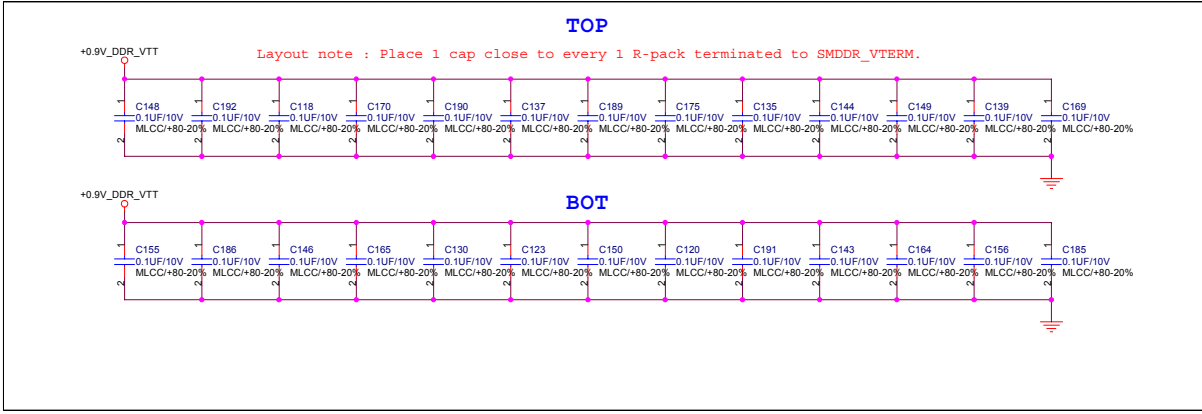
A is required to route to Top  
SODIMM for AMT to function  
Ch.A SODIMM needs to be  
populated for Intel AMT support.



DDR\_A\_DM[0..7] 11  
DDR\_A\_DQ[63] 11  
DDR\_A\_DQS[0..7] 11  
DDR\_A\_DQS#0..7 11  
DDR\_A\_MA[0..14] 10,11,20



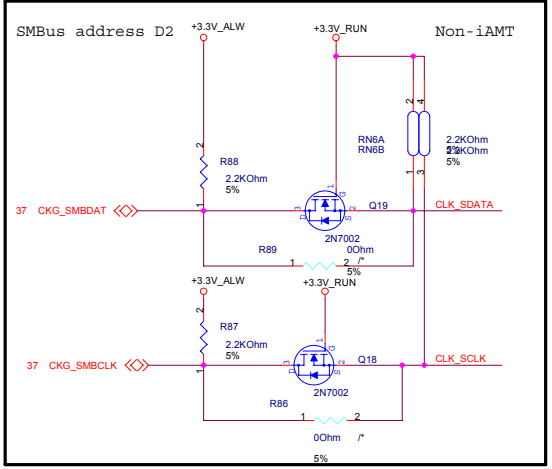
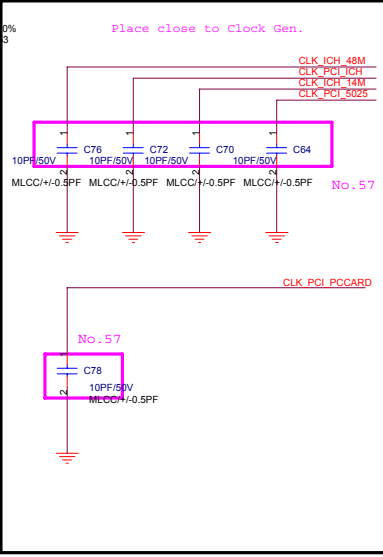
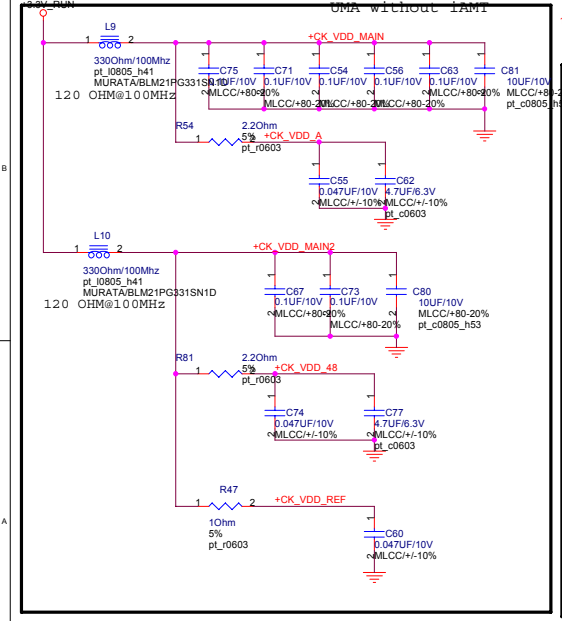
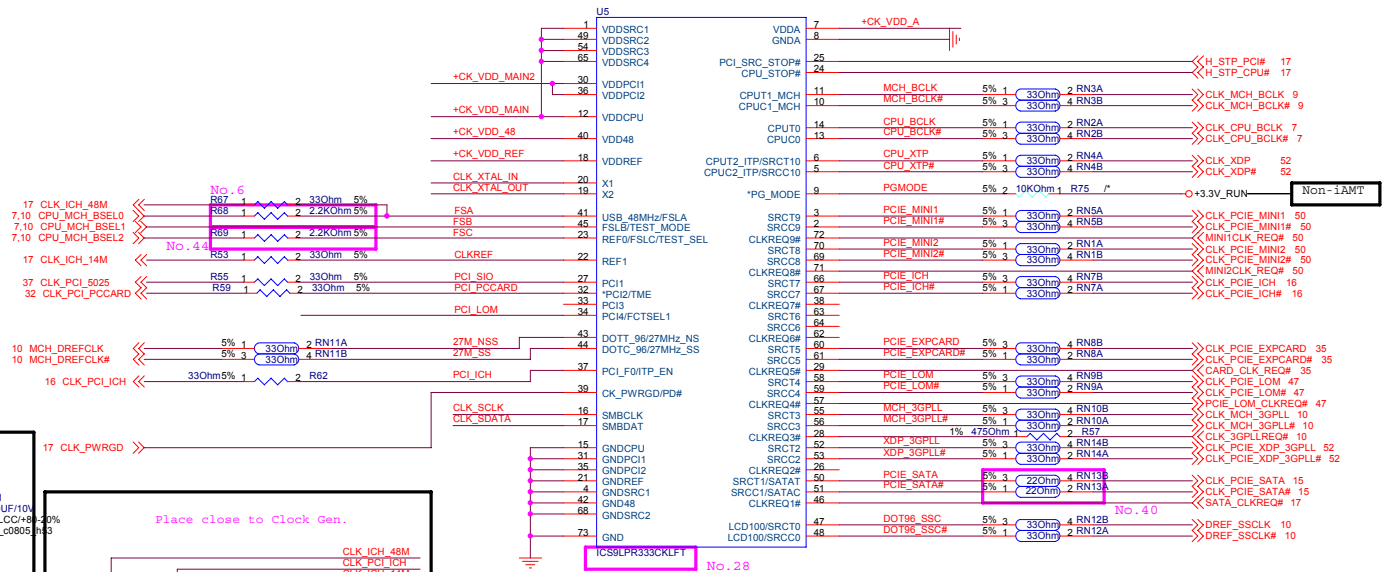
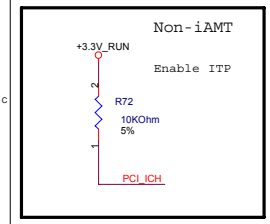
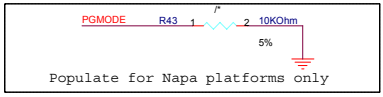
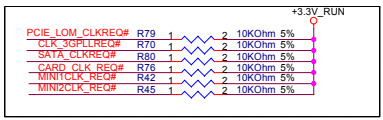
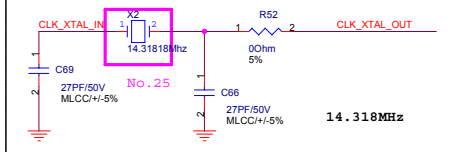
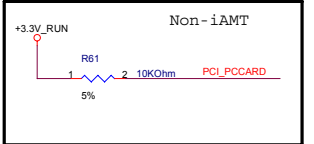
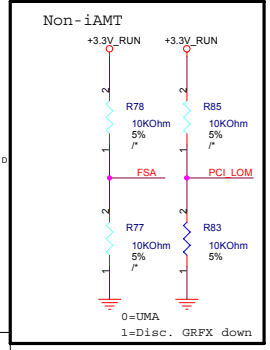
www.laptop-schematics.com



Please these resistor closely DIMMA, all trace length<750 mil.

Please these resistor closely DIMMB, all trace length<750 mil.

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME:	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 20 OF 68	DDR2 SO-DIMM (1)	RELEASE DATE :		



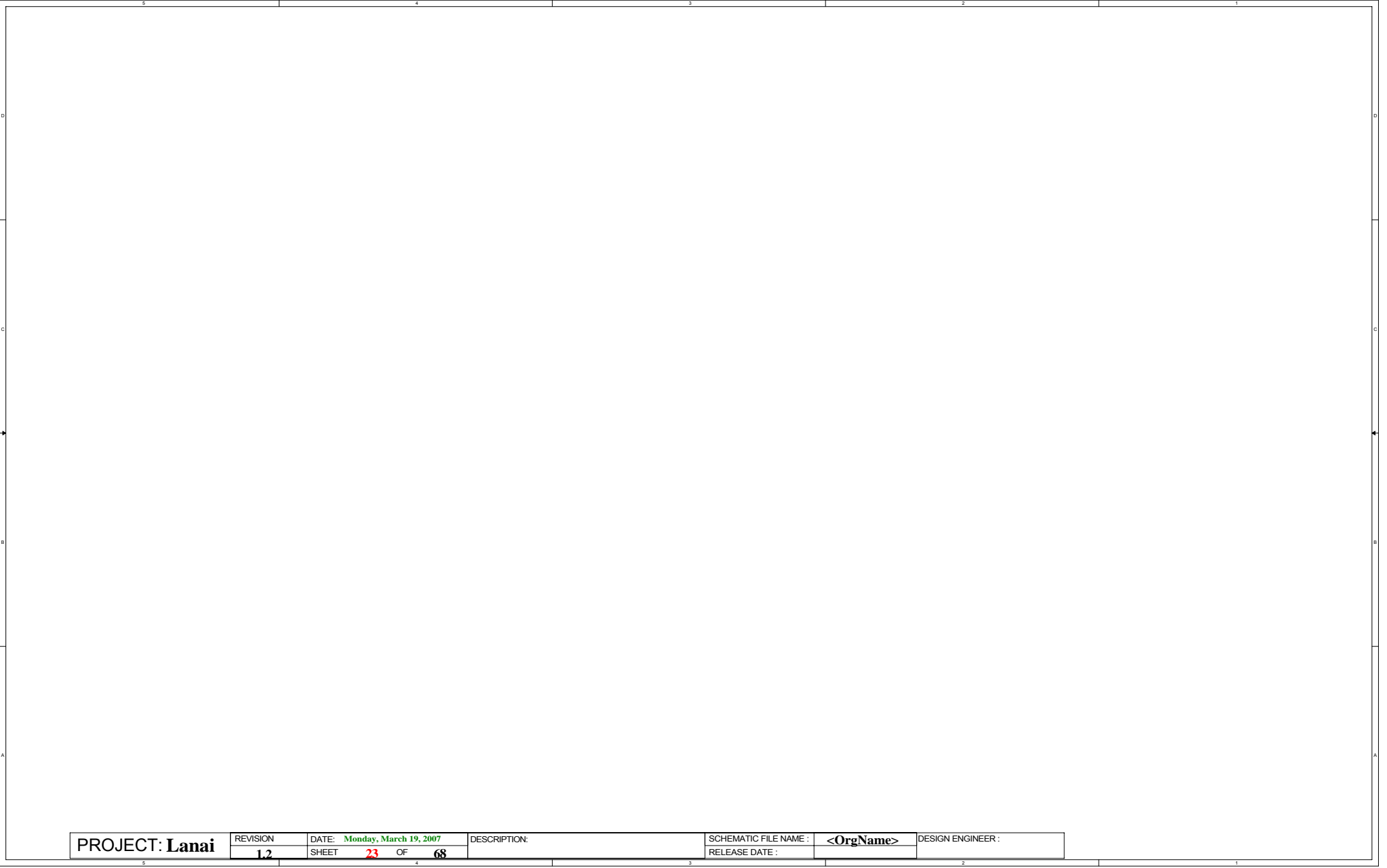
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI\_LOM=FCTSEL1

FCTSEL1 (PIN 34)	Pin43	Pin44	Pin47	Pin48
0 = UMA	DOT96T	DOT96C	96/100M T	96/100M C
1 = Disc.	27Mout	27M Sout	SRCT0	SRCC0

GRFX down





PROJECT: **Lanai**

REVISION  
**1.2**

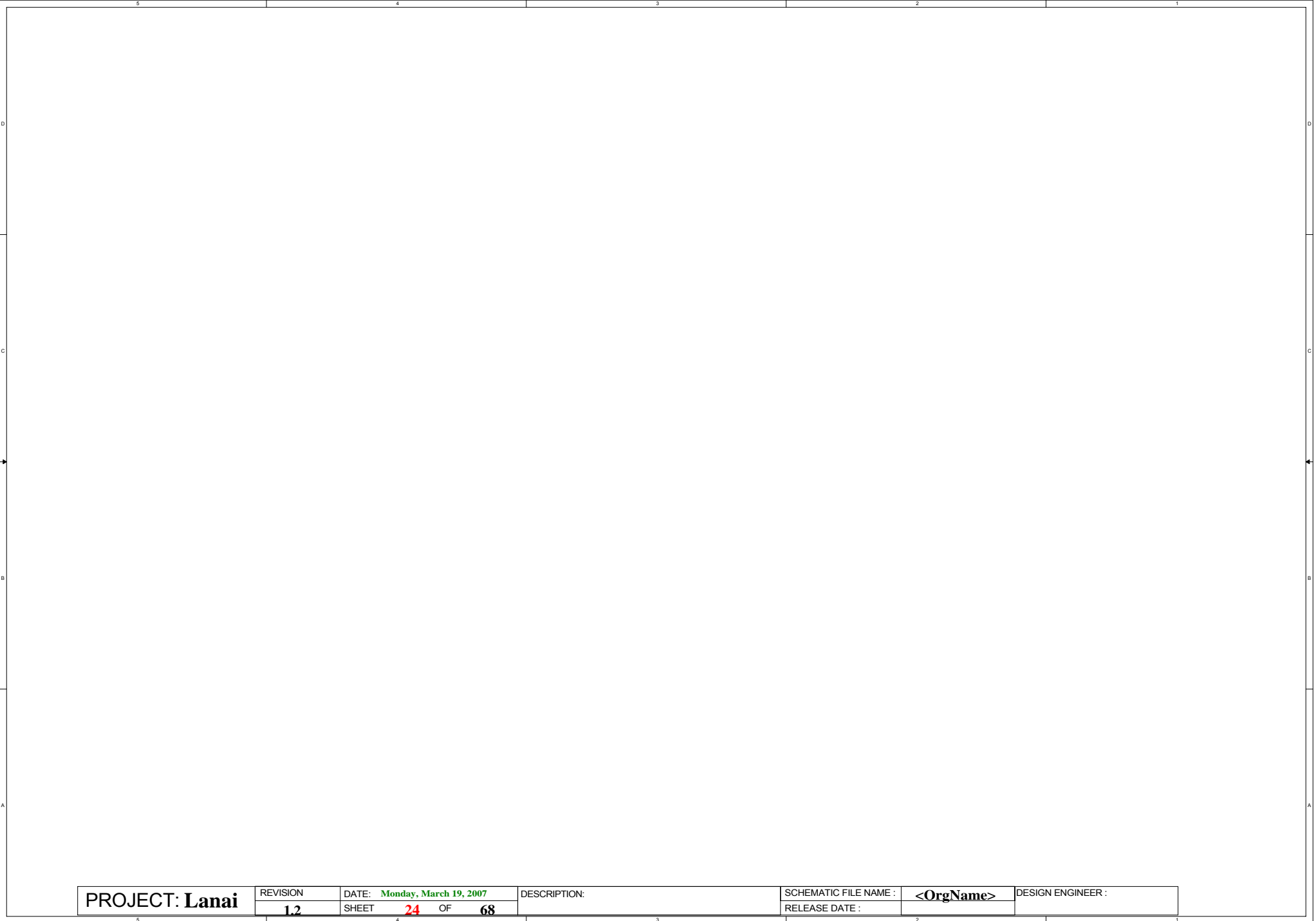
DATE: **Monday, March 19, 2007**  
SHEET **23** OF **68**

DESCRIPTION:

SCHEMATIC FILE NAME :  
RELEASE DATE :

**<OrgName>**

DESIGN ENGINEER :



<b>PROJECT: Lanai</b>	REVISION	DATE: <i>Monday, March 19, 2007</i>	DESCRIPTION:	SCHMATIC FILE NAME :	<b>&lt;OrgName&gt;</b>	DESIGN ENGINEER :
	<b>12</b>	SHEET <b>24</b> OF <b>68</b>		RELEASE DATE :		



1	A	B	C	D	E
2					
3					
4					
5					

**PROJECT: Lanai**

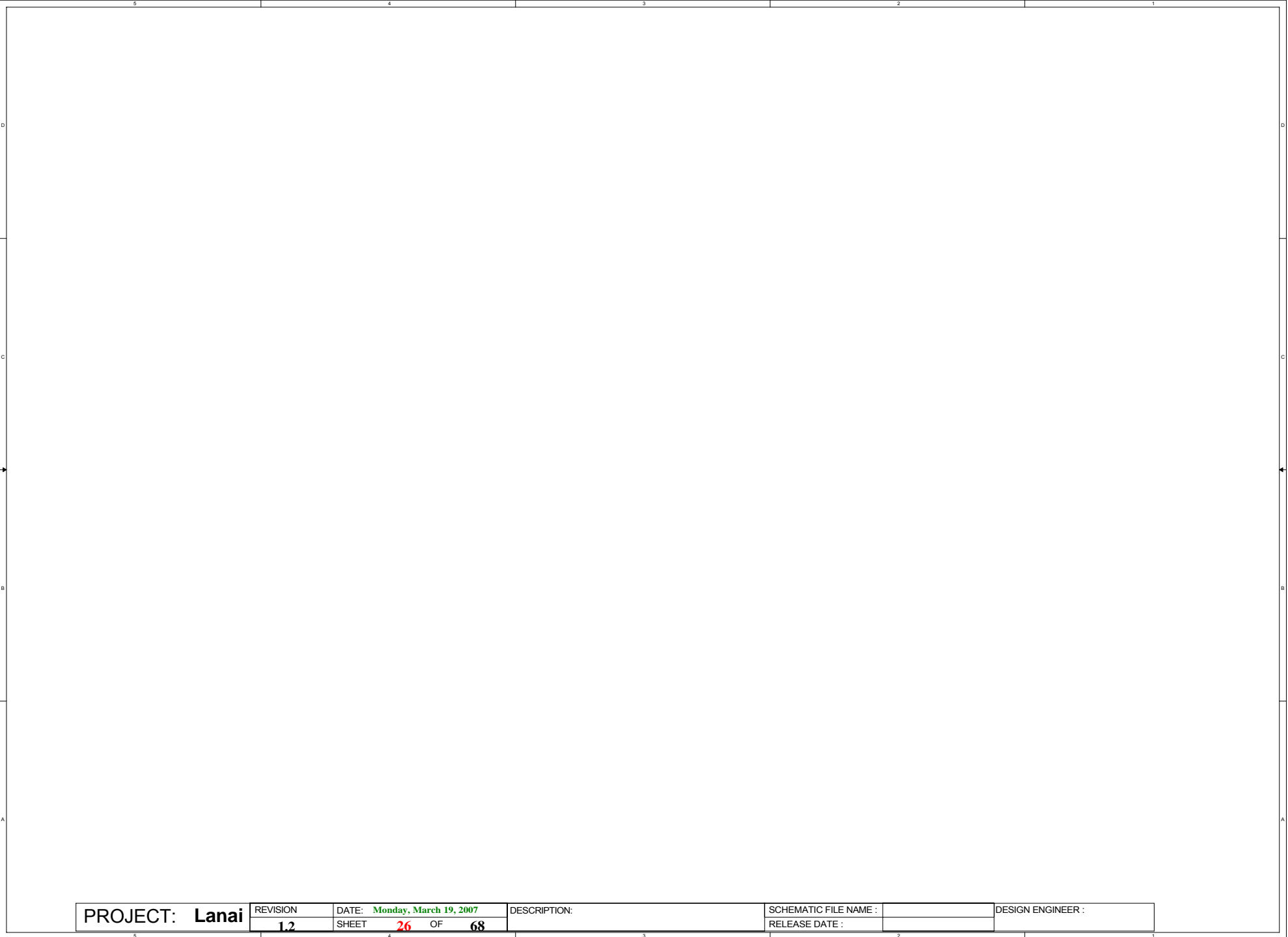
REVISION  
**1.2**

DATE: Monday, March 19, 2007  
SHEET **25** OF **68**

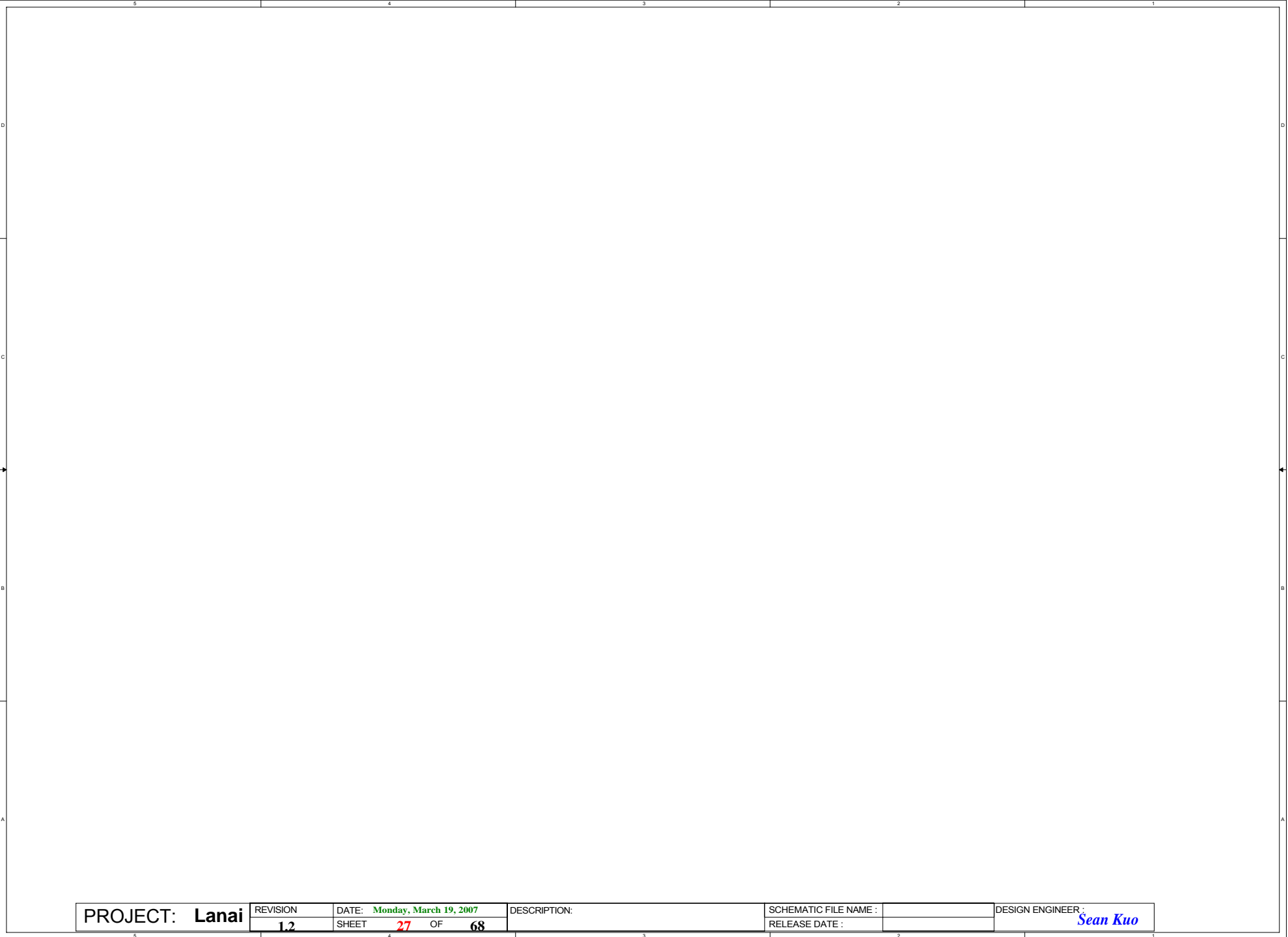
DESCRIPTION:

SCHEMATIC FILE NAME : **<OrgName>**  
RELEASE DATE :

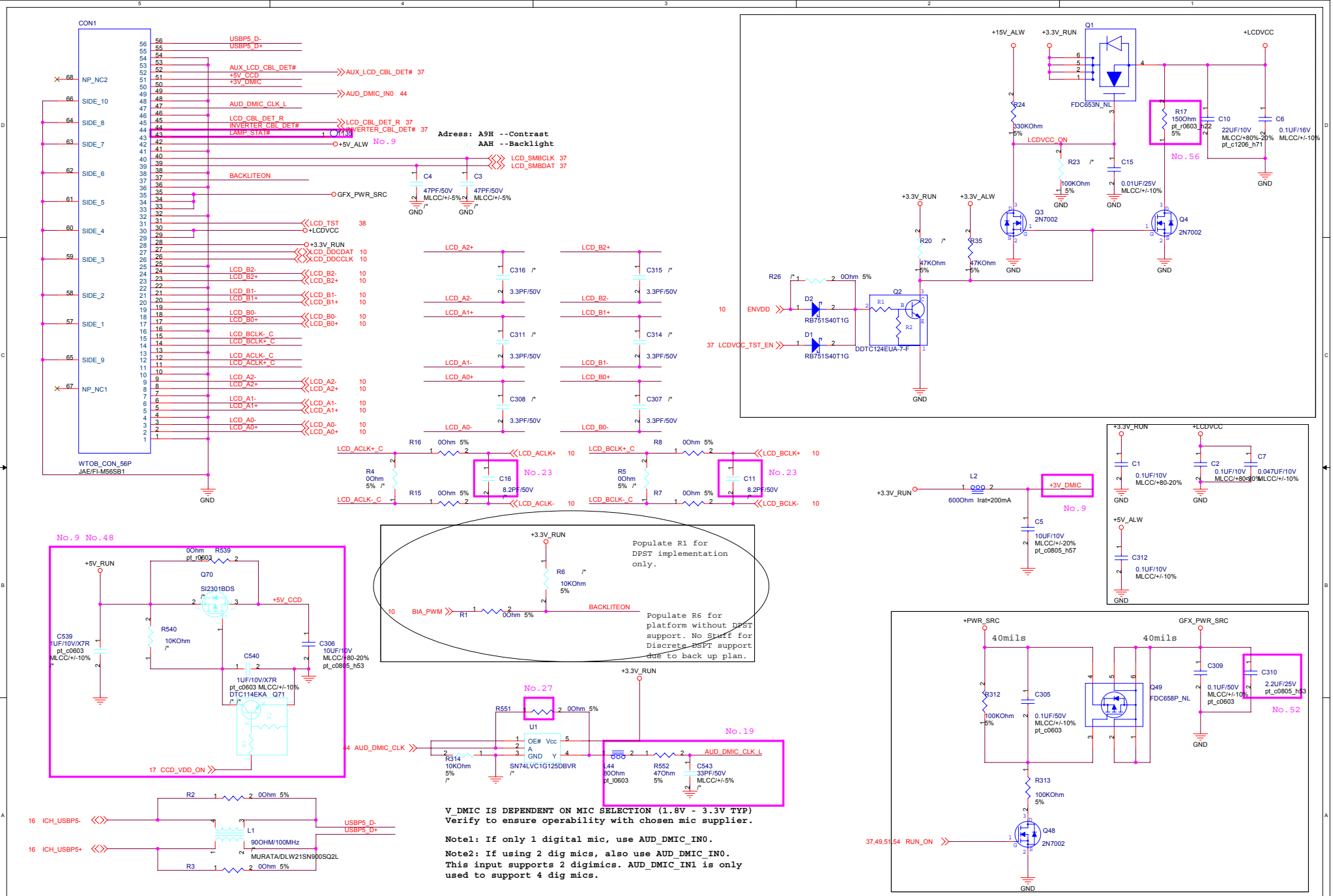
DESIGN ENGINEER :

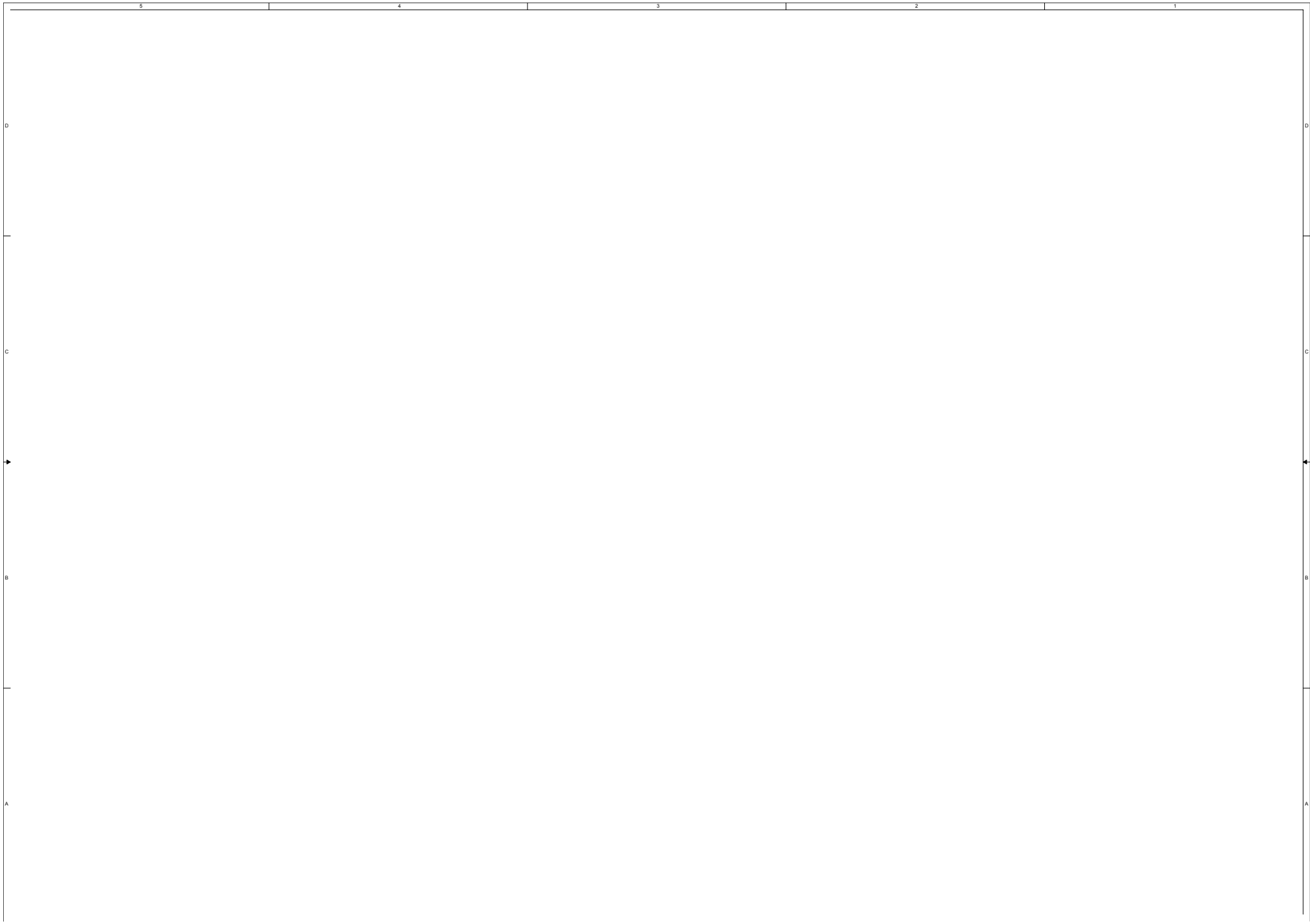


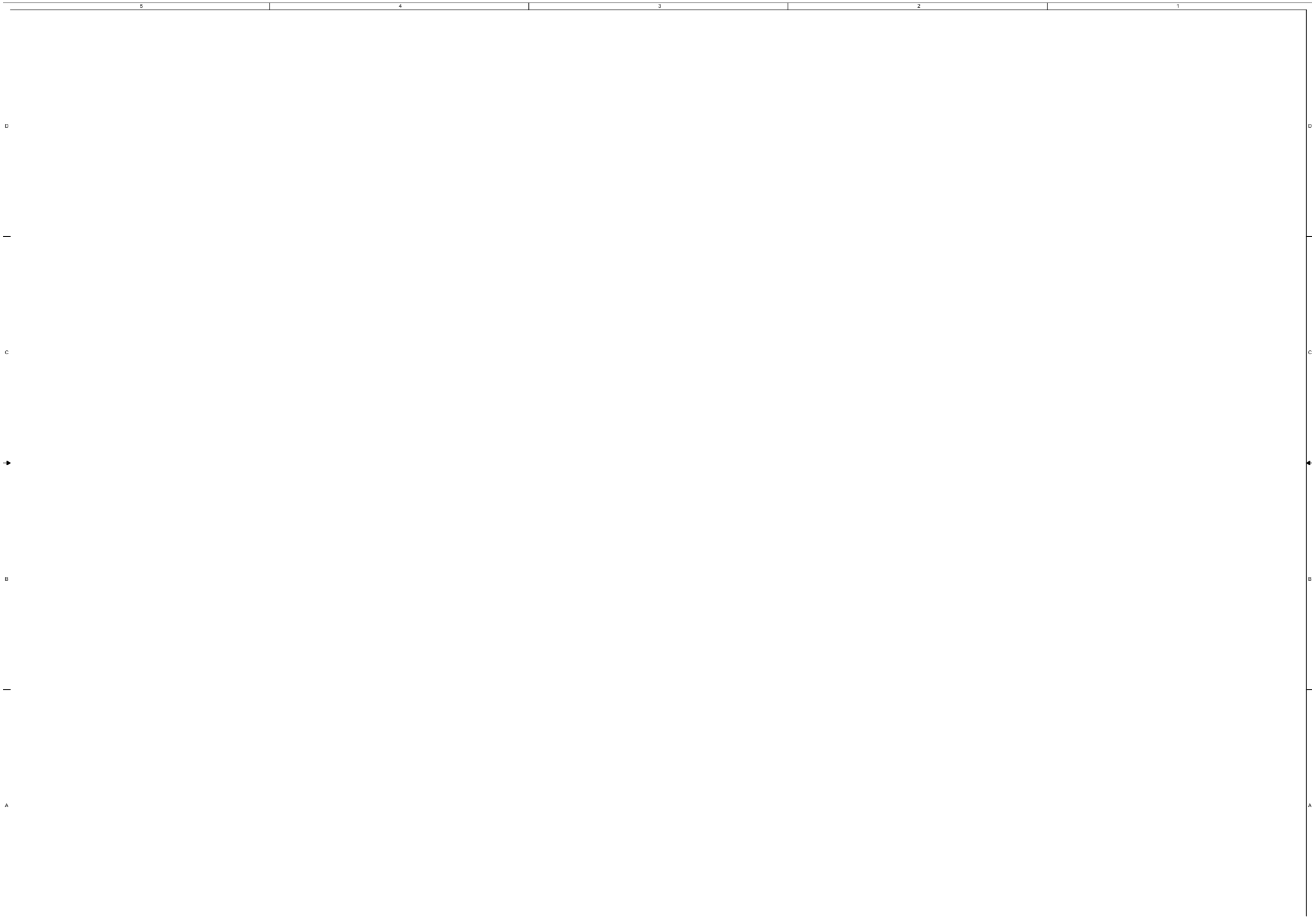
<b>PROJECT: Lanai</b>	REVISION	DATE: <b>Monday, March 19, 2007</b>	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	<b>1.2</b>	SHEET <b>26</b> OF <b>68</b>		RELEASE DATE :	



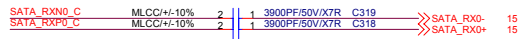
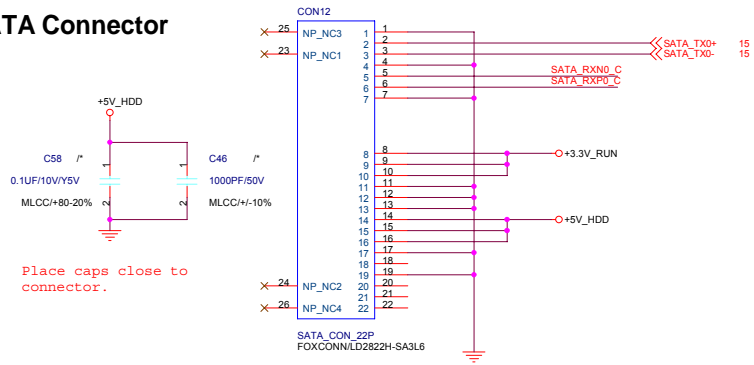
<b>PROJECT: Lanai</b>	REVISION	DATE: <b>Monday, March 19, 2007</b>	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	<b>1.2</b>	SHEET <b>27</b> OF <b>68</b>		RELEASE DATE :	<i>Sean Kuo</i>



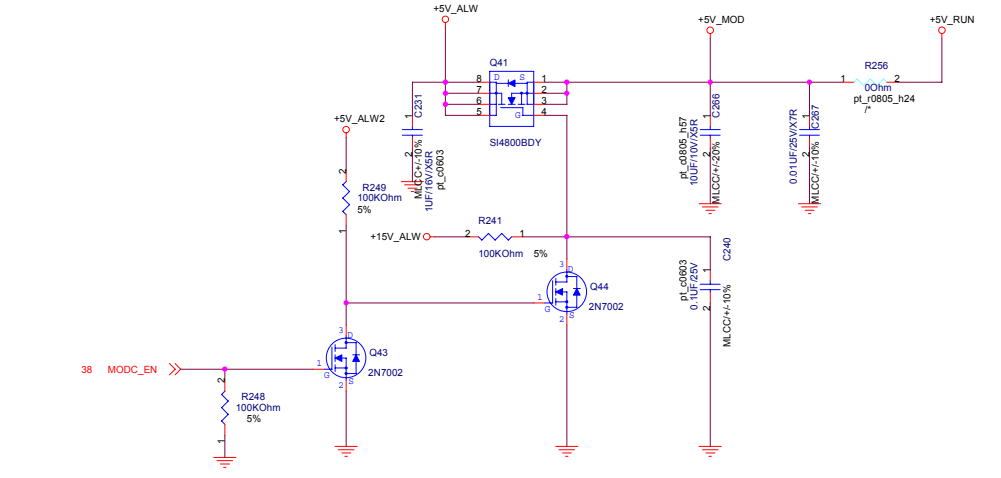
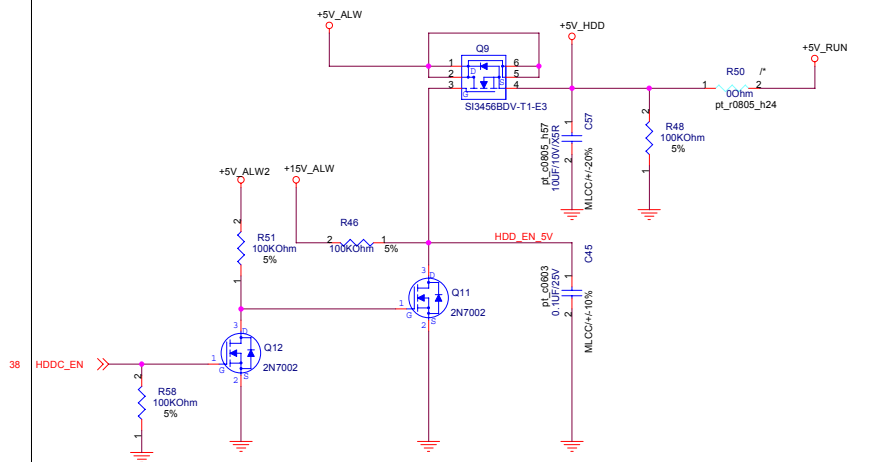
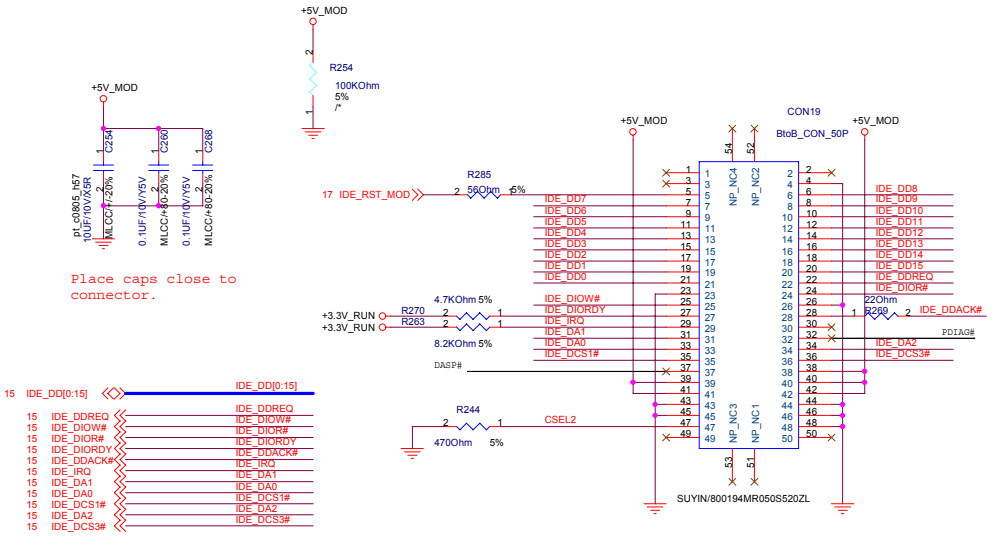




### SATA Connector



### ODD Connector

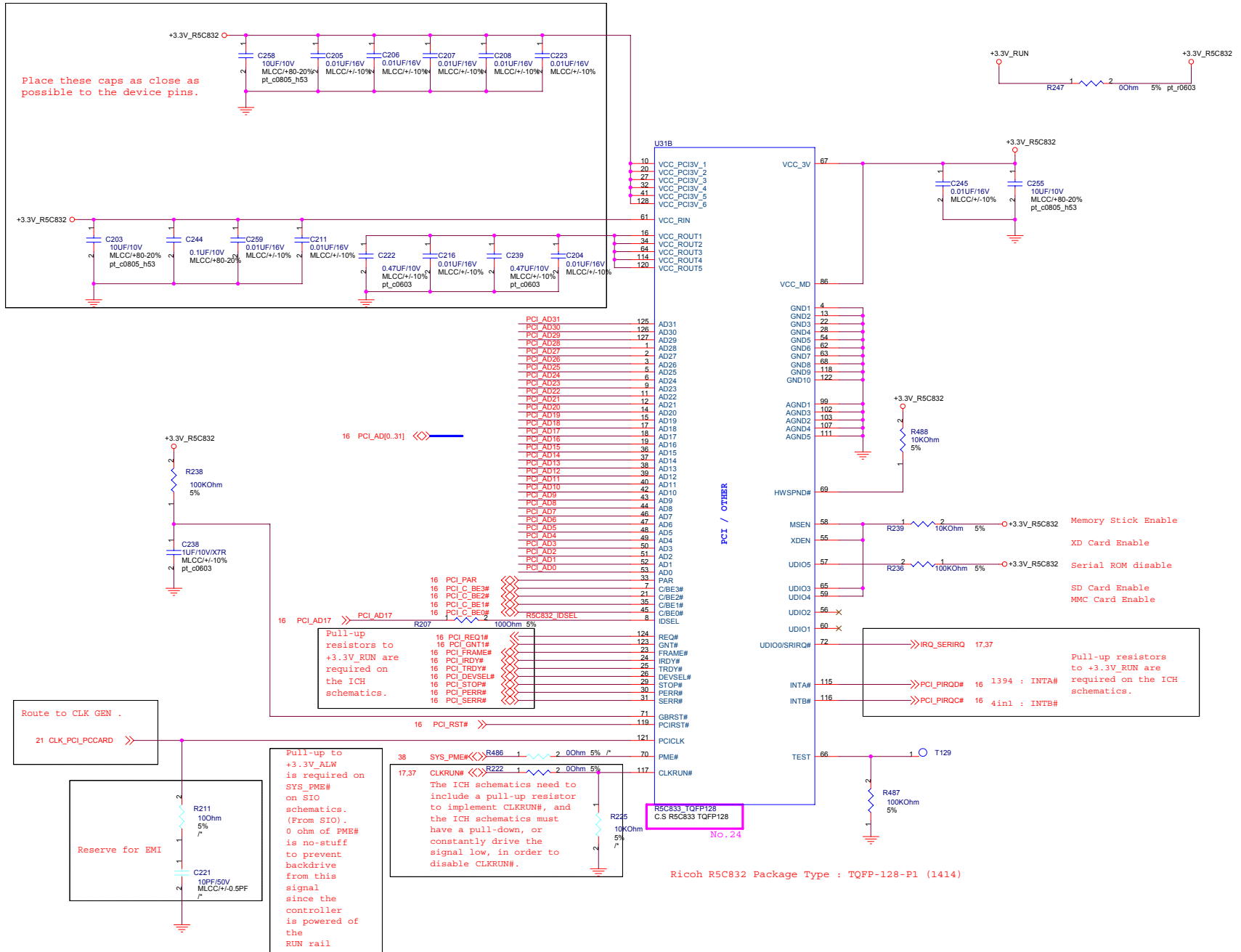


PROJECT: Lanai

REVISION: 1.2  
 DATE: Monday, March 19, 2007  
 SHEET: 31 OF 68

DESCRIPTION: SATA (HDD & CD\_ROM)

SCHEMATIC FILE NAME: <OrgName>  
 DESIGN ENGINEER:  
 RELEASE DATE:

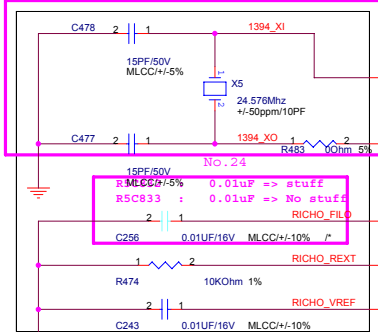


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME:	DESIGN ENGINEER :
	1.2	SHEET 32 OF 68	R5C833 - PCI INTERFACE	<OrgName>	
RELEASE DATE :					

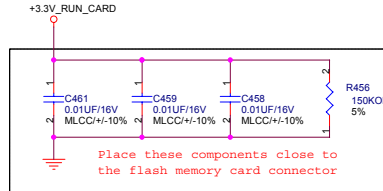


Recommended Crystal Specs from Data Sheet:

Normal Frequency : 24.576 Mhz  
 Frequency Tolerance : +/- 50ppm @ 25C  
 Driver Level : .1 mW  
 Load capacitance : 10pF  
 Equ. Resistance : 50 Ohm Max  
 Shunt Capacitance : 7.0pF Max

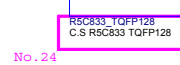
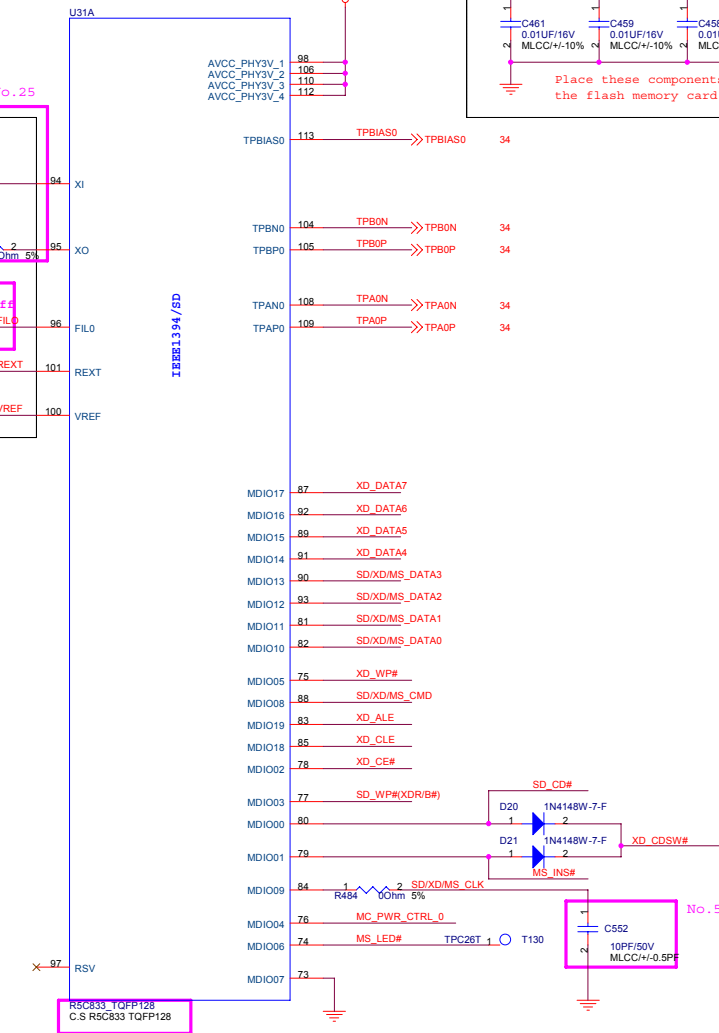
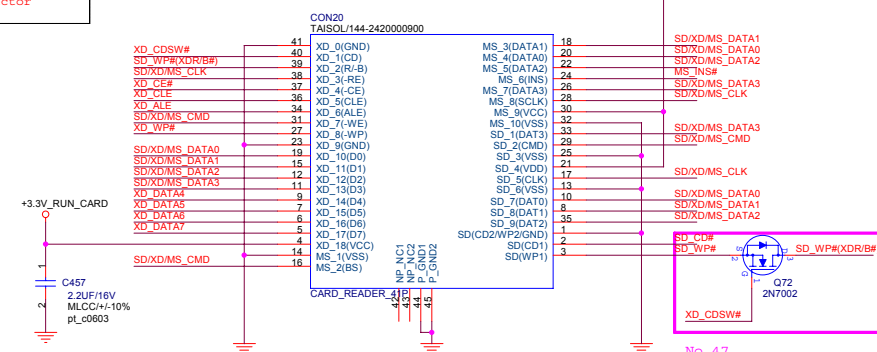
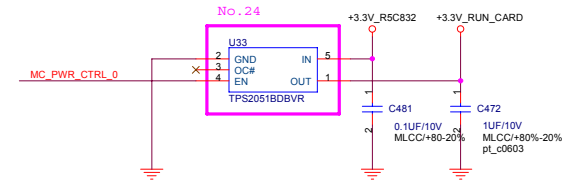


Place as close to R5C832 as possible.

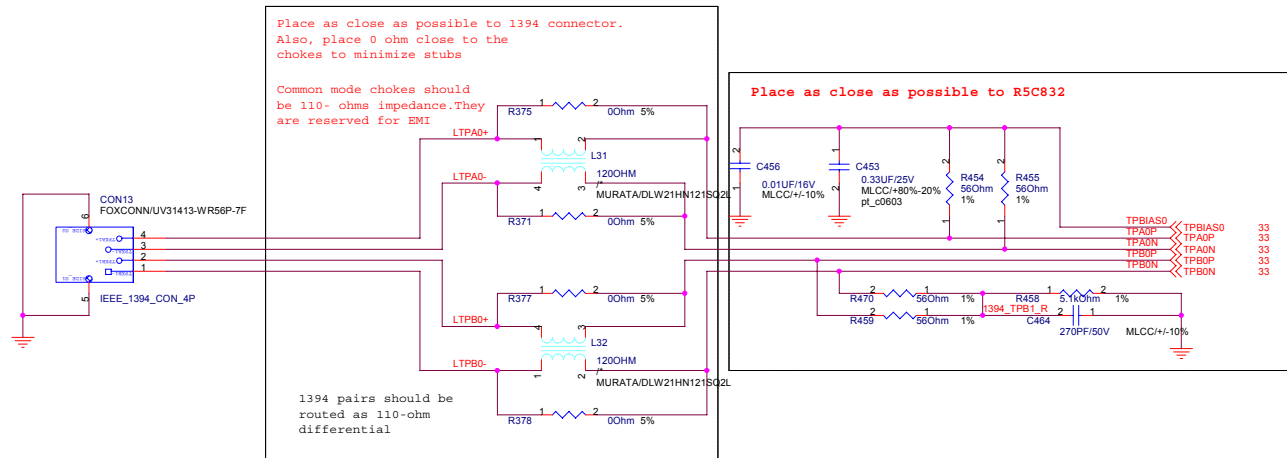
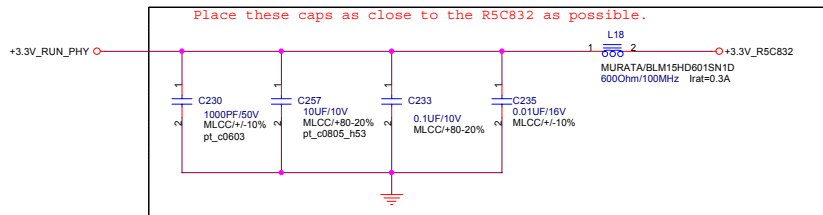


Place these components close to the flash memory card connector

For SD/MS Card Power

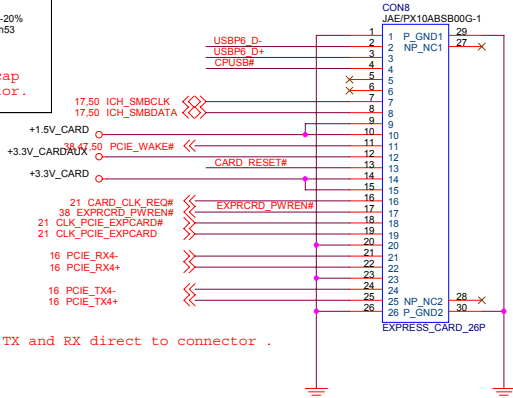
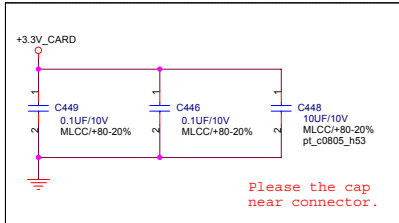
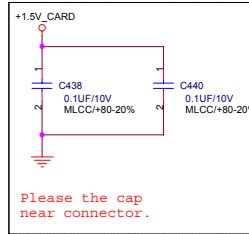
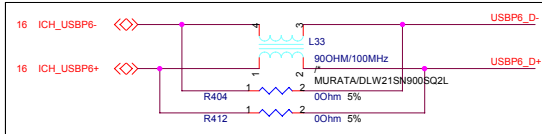


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 33 OF 68	R5C833 - FLASH MEMORY PART	RELEASE DATE :		



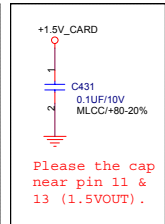
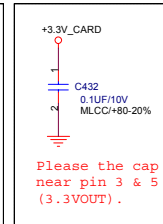
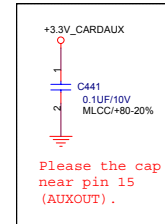
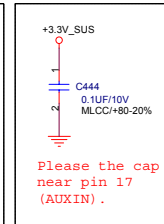
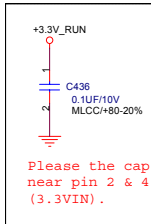
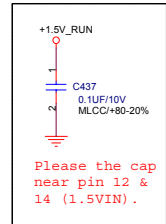
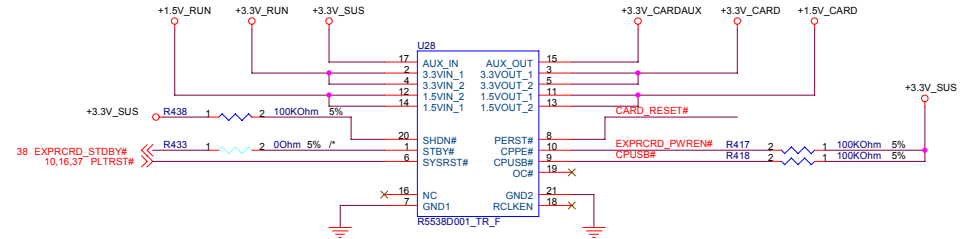
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 34 OF 68	R5C833 - IEEE1394 PART	RELEASE DATE :		

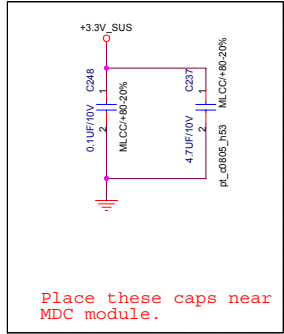
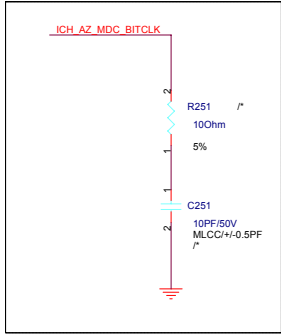
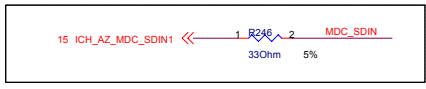
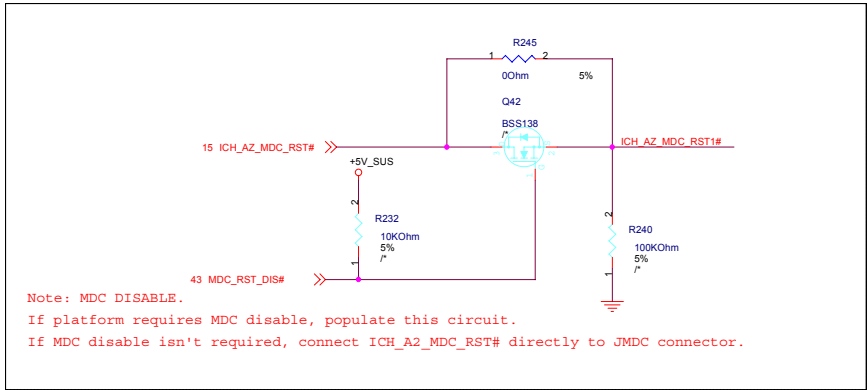
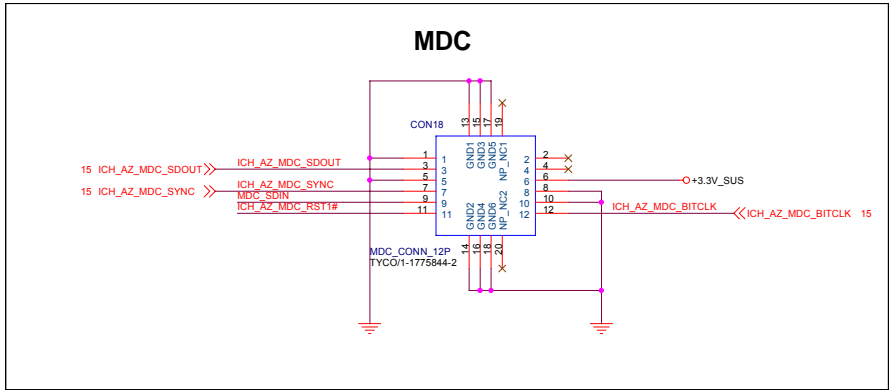
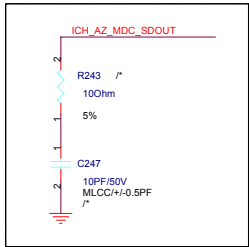
# Express Card



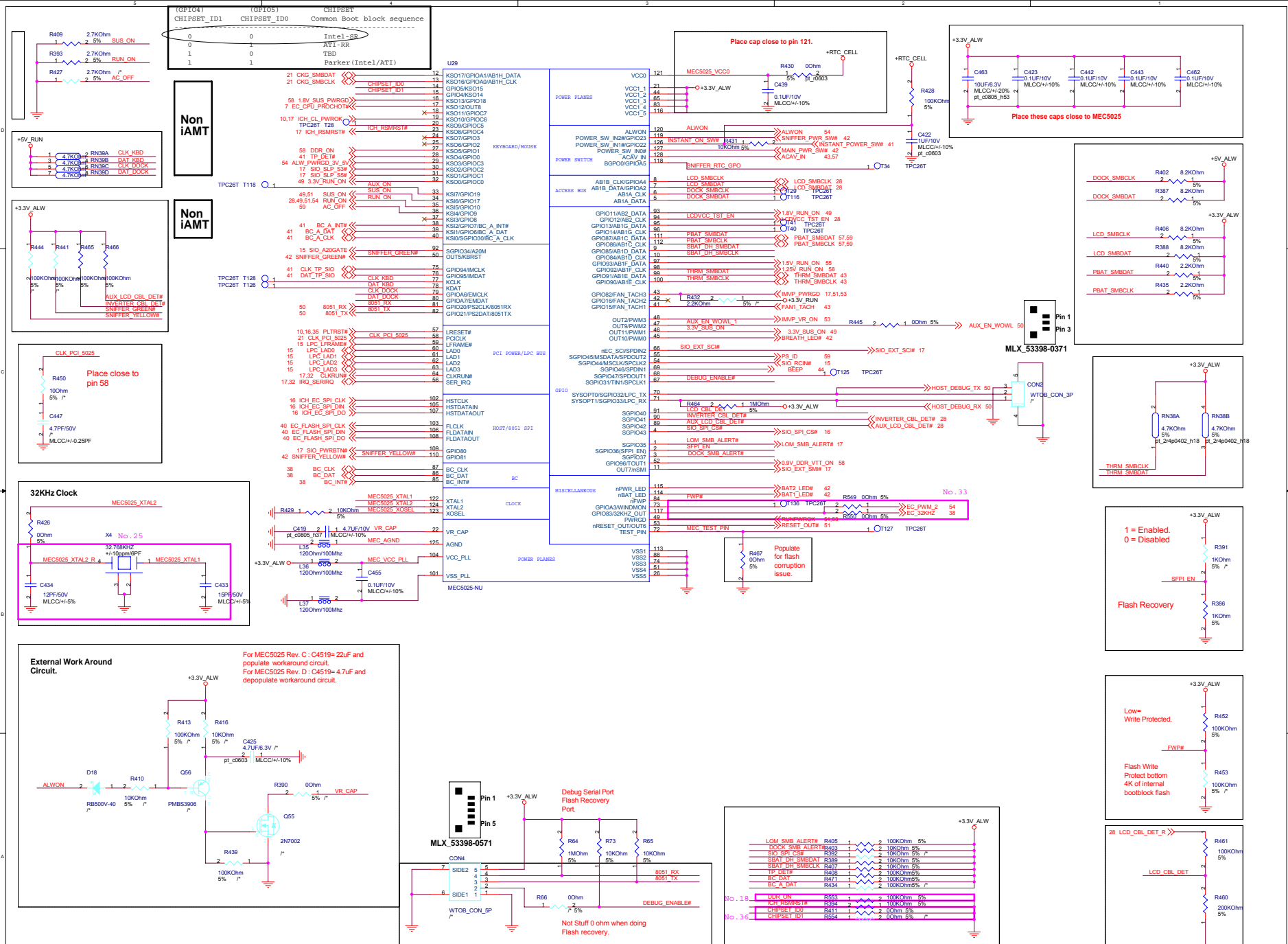
PCI-Express TX and RX direct to connector .

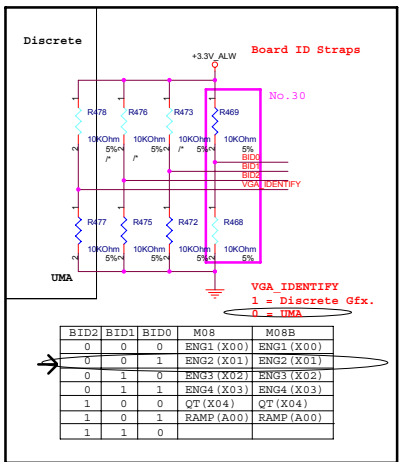
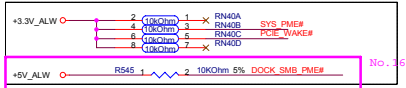
+1.5V\_CARD Max. 650mA, Average 500mA.  
+3V\_CARD Max. 1300mA, Average 1000mA.



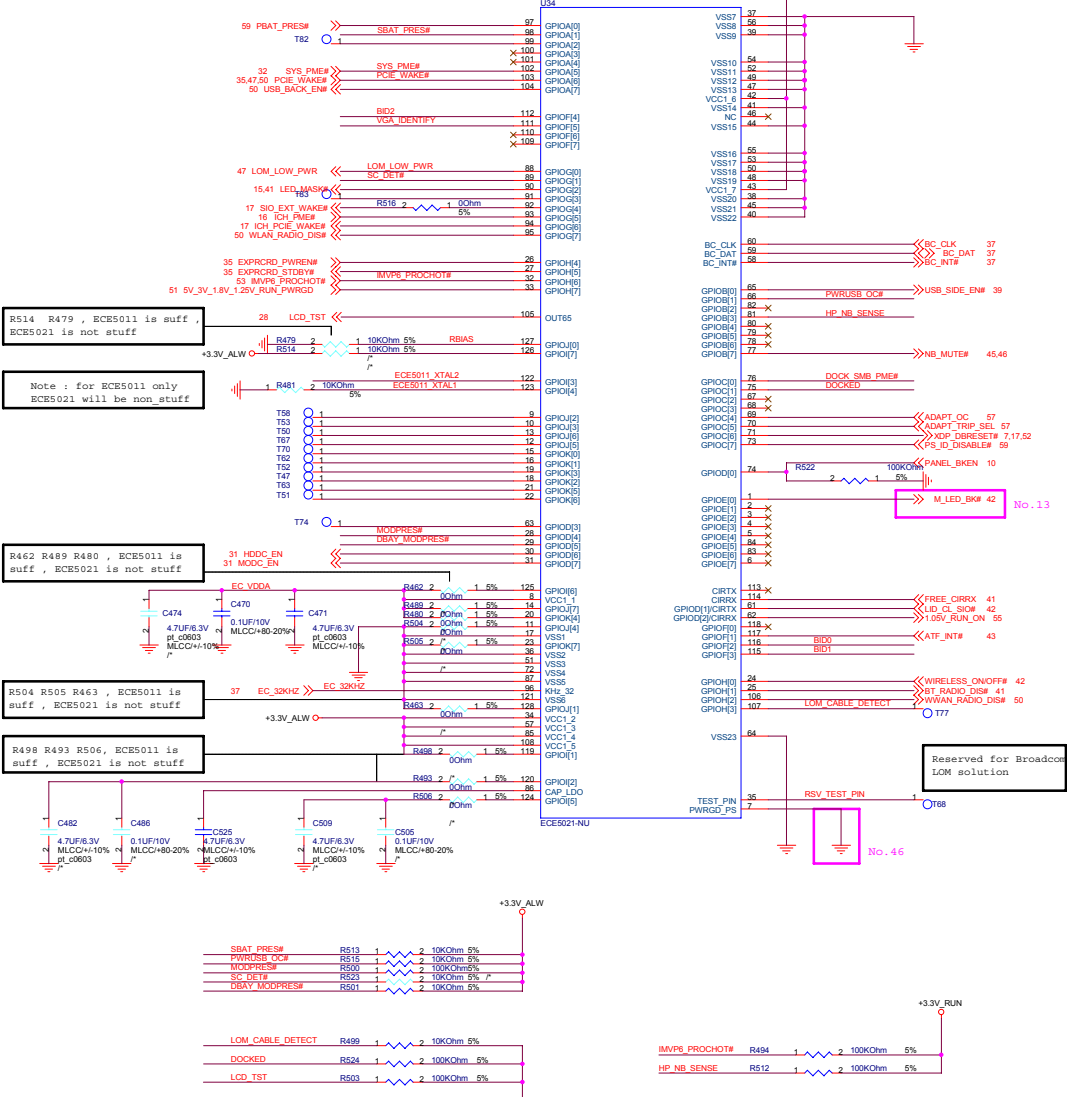
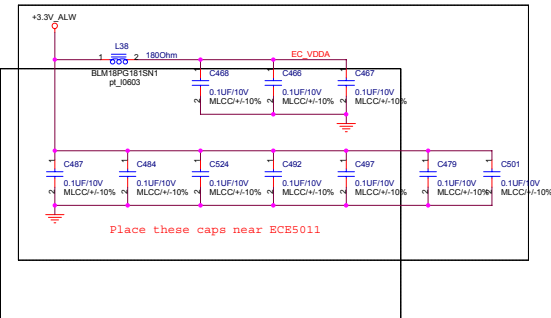
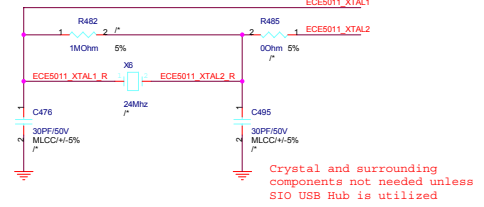


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 36 OF 68	MDC CONN	RELEASE DATE :		





24MHz Clock



R514 R479, ECES011 is suff,  
ECE5021 is not stuff

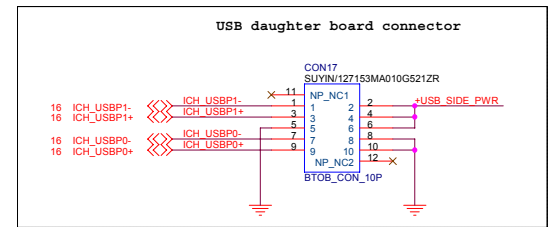
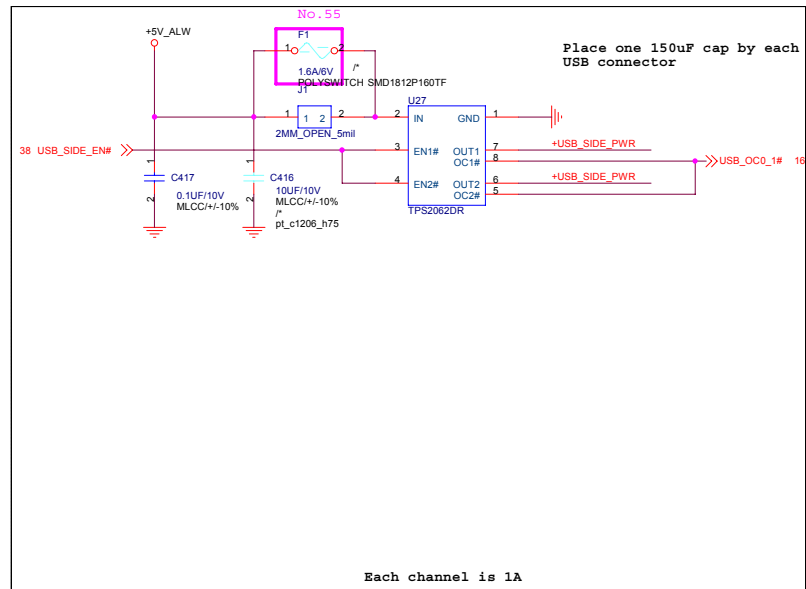
Note: for ECES011 only  
ECE5021 will be non\_stuff

R462 R489 R480, ECES011 is  
suff, ECES021 is not stuff

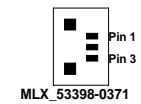
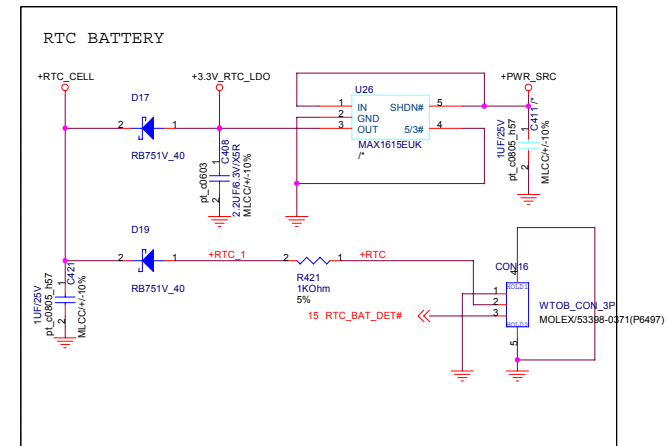
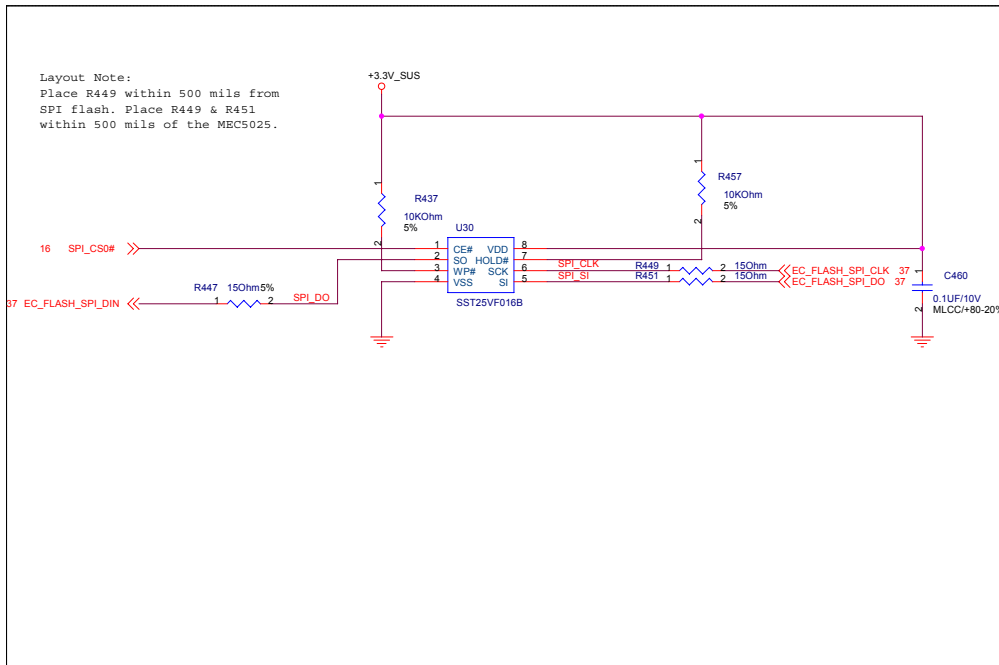
R504 R505 R463, ECES011 is  
suff, ECES021 is not stuff

R498 R493 R506, ECES011 is  
suff, ECES021 is not stuff

Reserved for Broadcom  
LOM solution



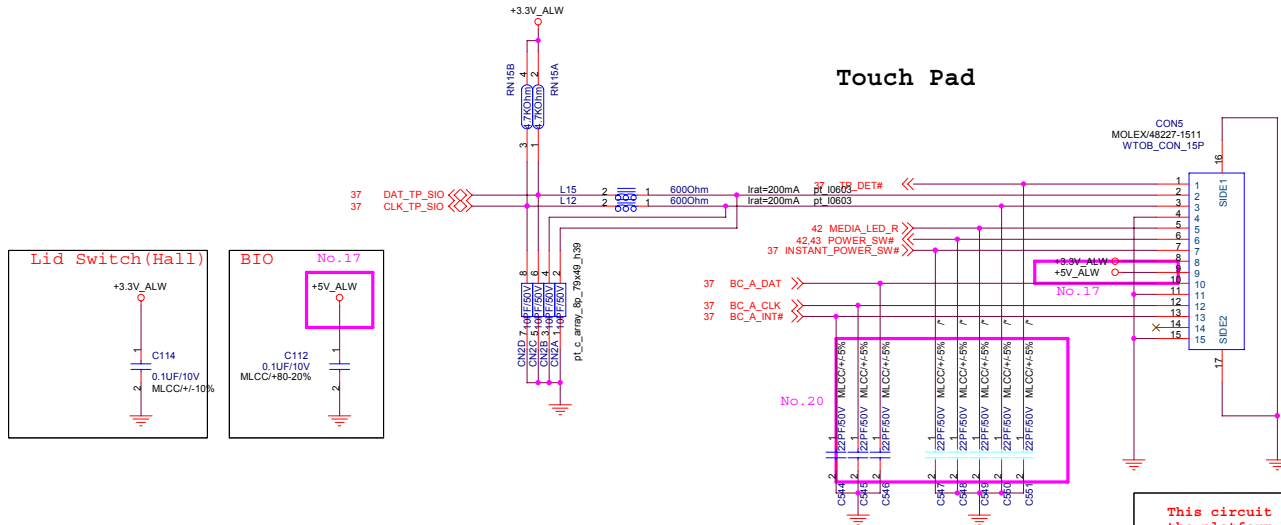
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 39 OF 68	USB PORT x 2	RELEASE DATE :		Terry Lin



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 40 OF 68	FLASH & RTC	RELEASE DATE :		C.L. Ho

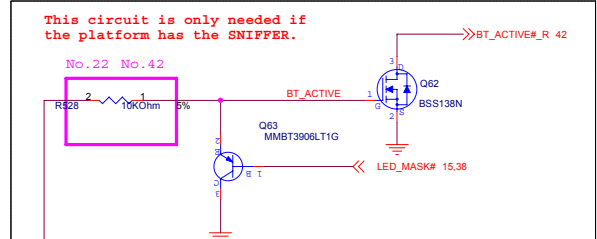
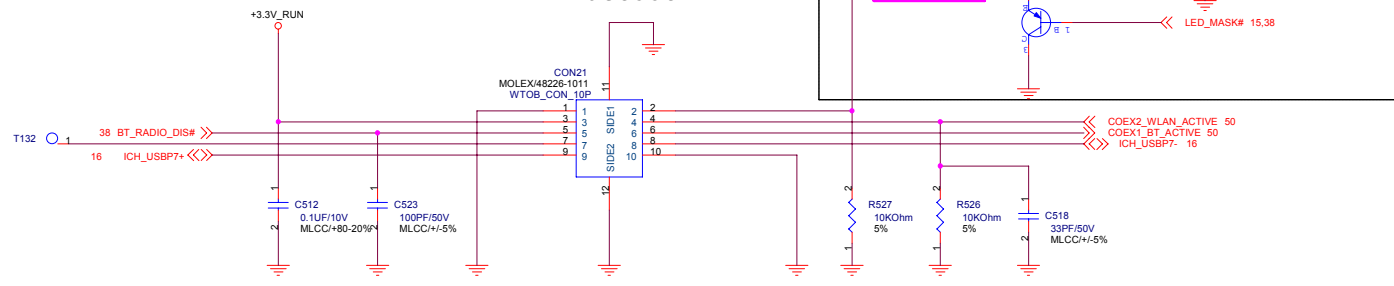


### Touch Pad

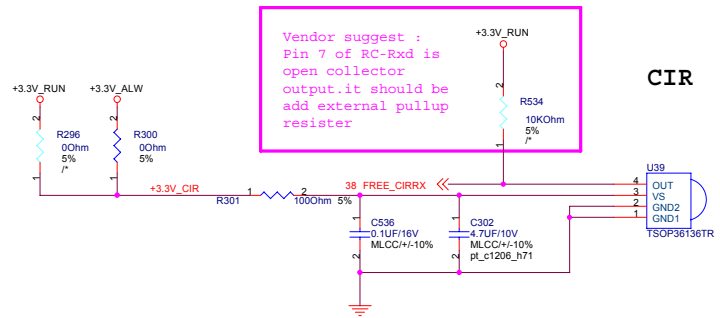


Please refer to item 191 of issue\_list\_0517\_TDC ,  
 "Lanai plan to use 3V TP controller. No need  
 TP\_VCC ". So we delete this circuit which  
 supply TP\_VCC power.

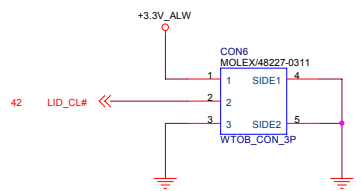
### Bluetooth



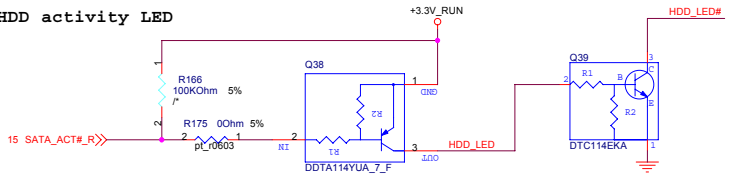
### CIR



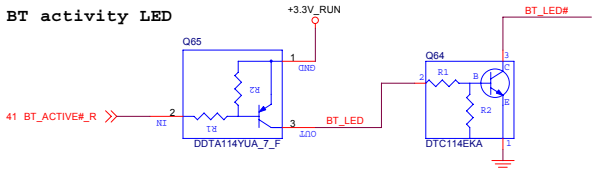
### HALL SENSOR



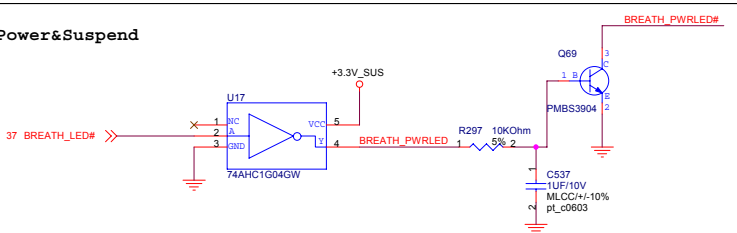
### HDD activity LED



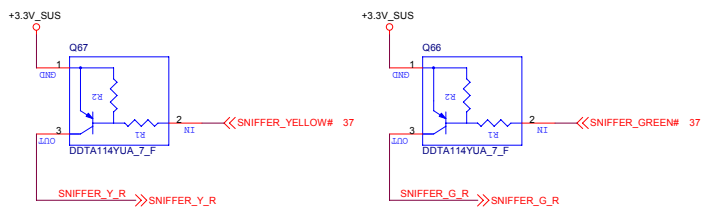
### BT activity LED



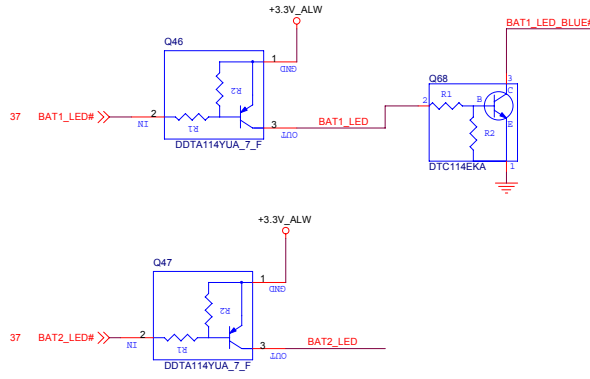
### Power&Suspend



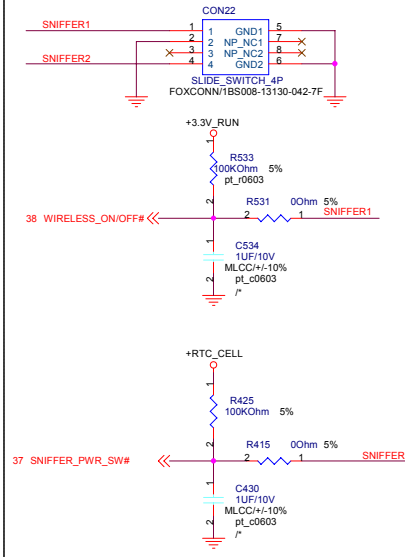
### Sniffer LED driver circuit



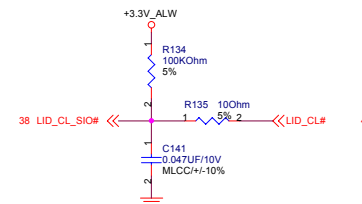
### Battery status



### Sniffer Switch

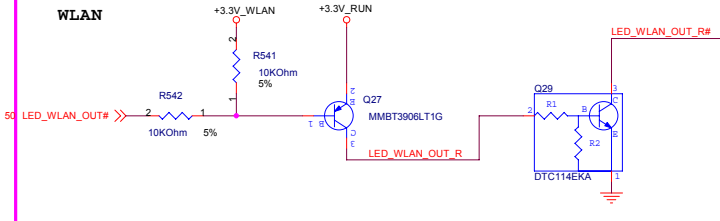


### Hall Switch

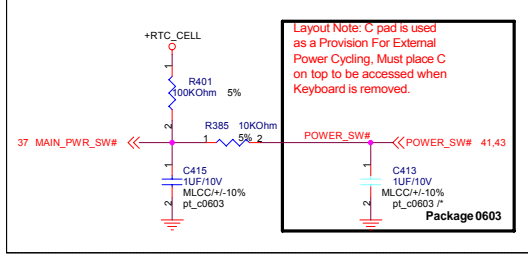
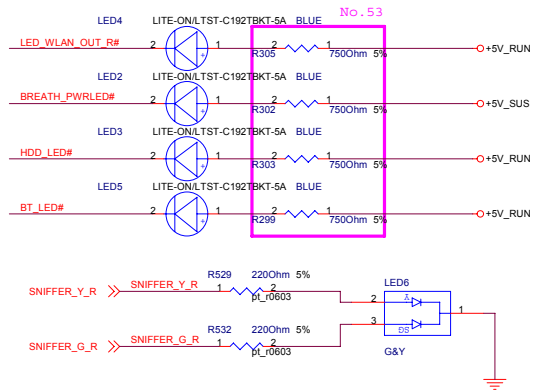
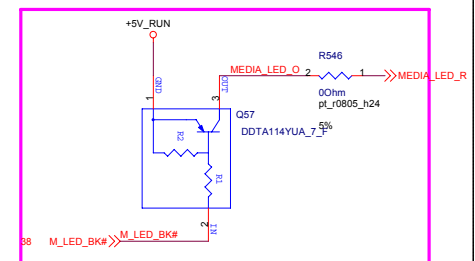


No. 8

### WLAN



### Media Bottom Board LED drive circuit



Layout Note: C pad is used as a Provision For External Power Cycling. Must place C on top to be accessed when Keyboard is removed.

No. 39

No.13 No.35

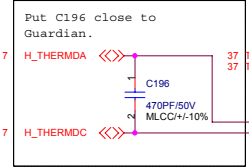
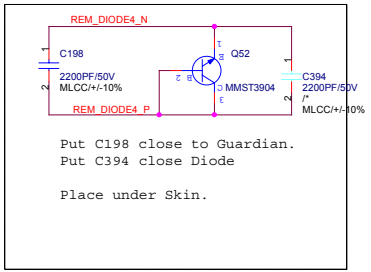
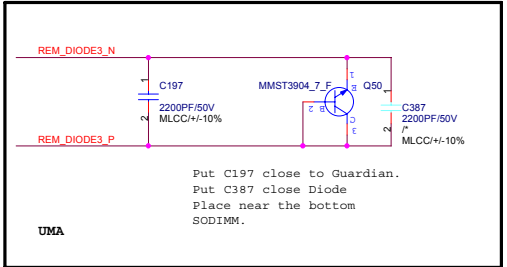
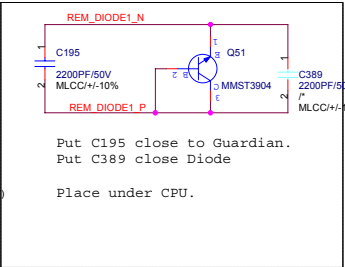
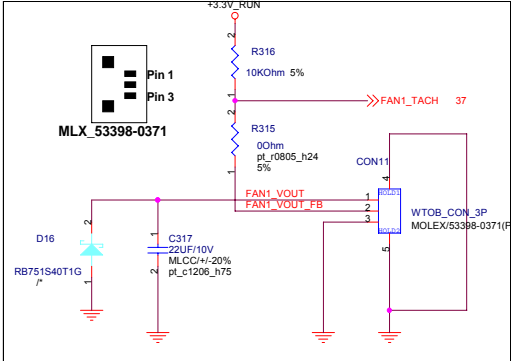
PROJECT: Lanai

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DESCRIPTION: SWITCH & LED

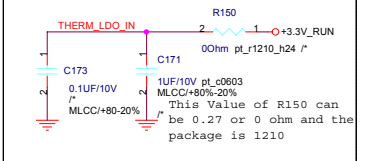
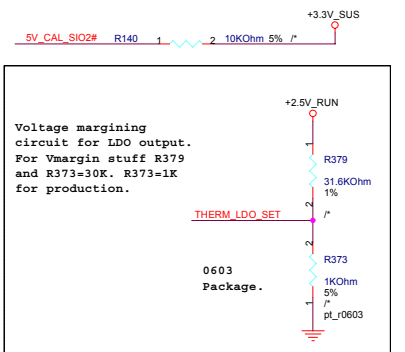
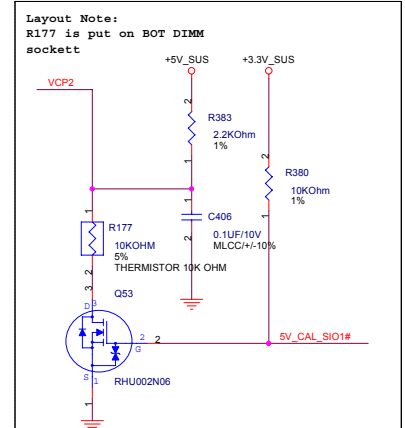
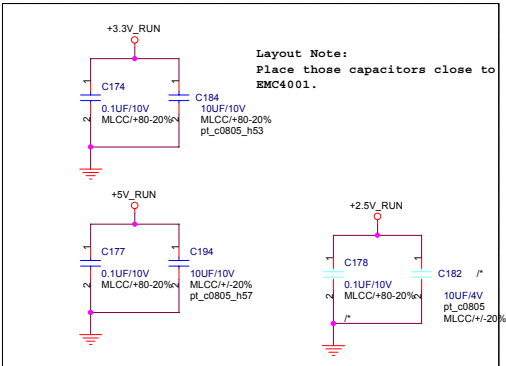
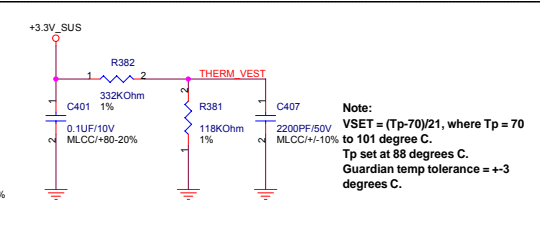
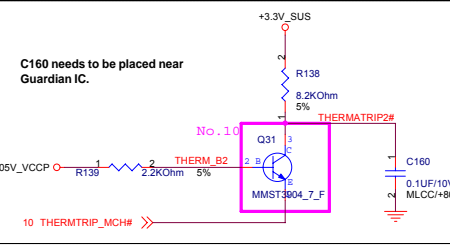
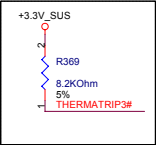
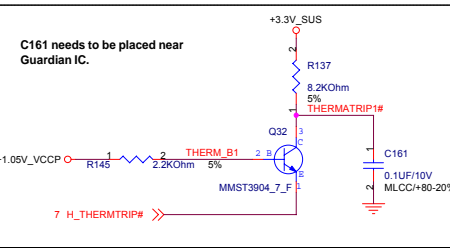
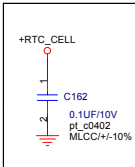
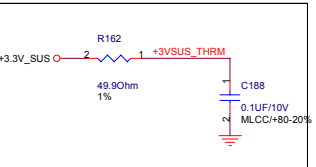
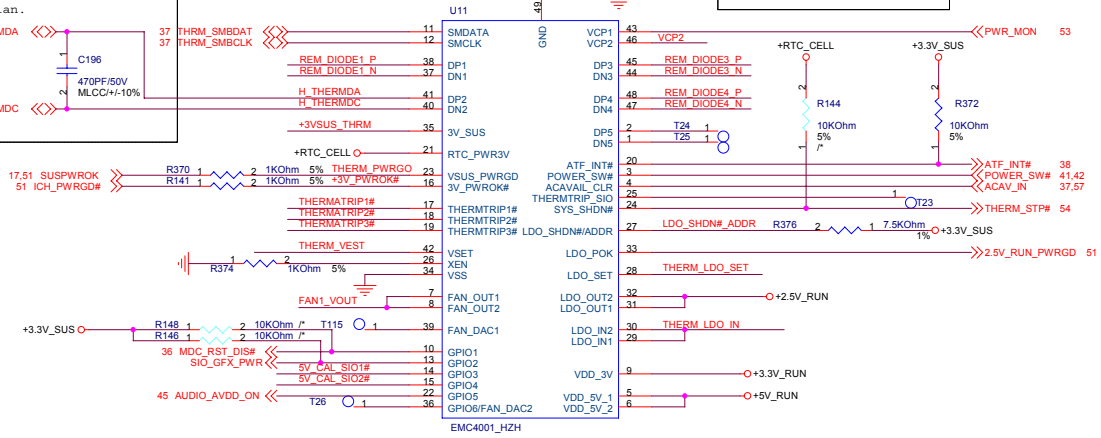
SCHEMATIC FILE NAME: <OrgName>  
RELEASE DATE:

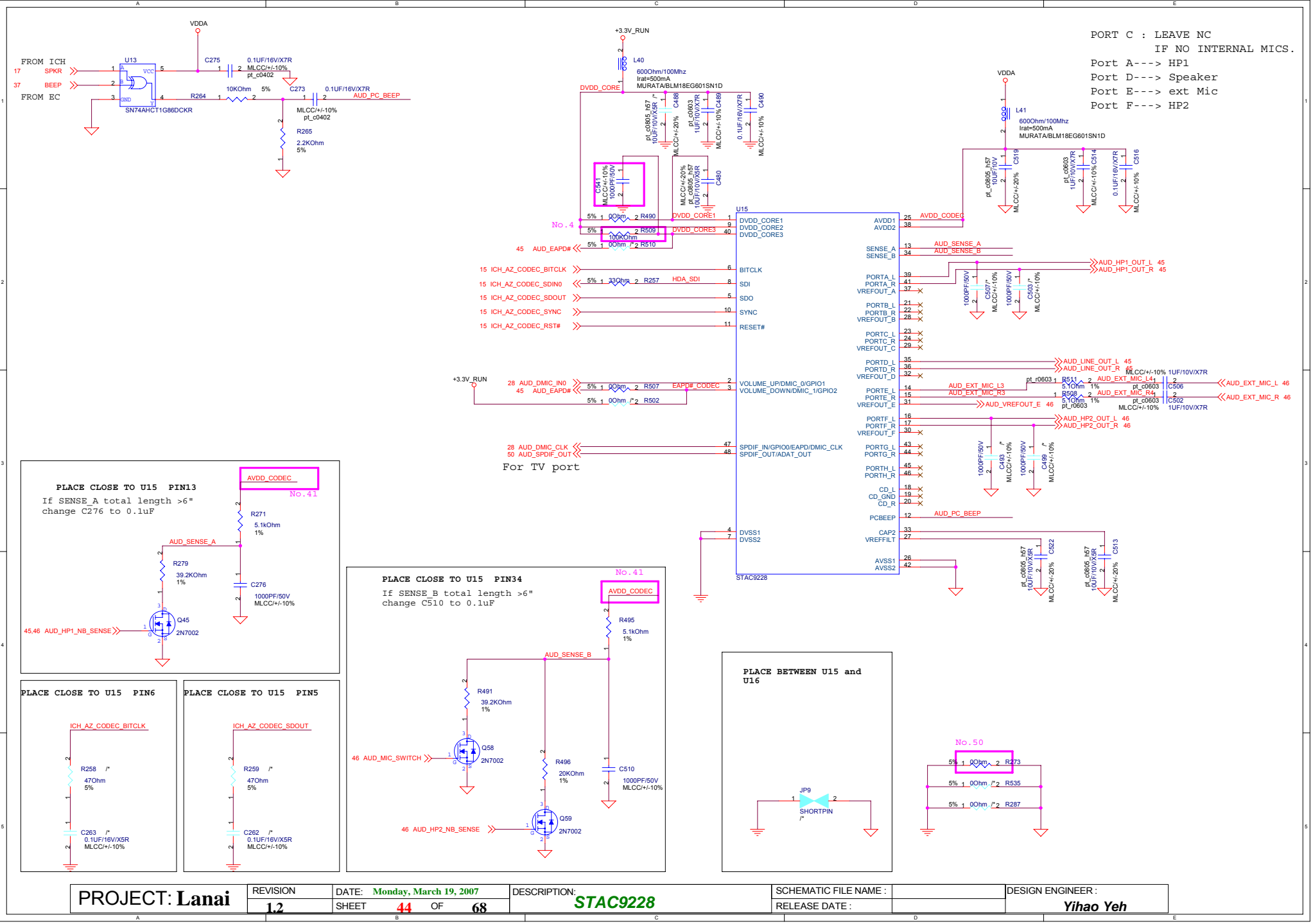
DESIGN ENGINEER: C



### Guardian

Note:  
150K input impedance on VCP1 (Pin 43)





PROJECT: Lanai

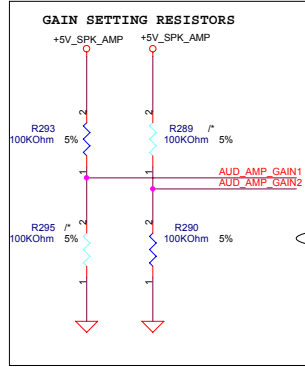
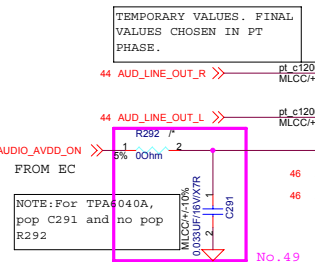
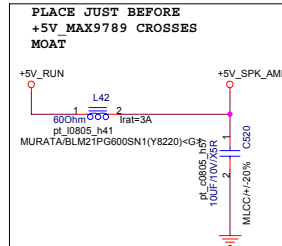
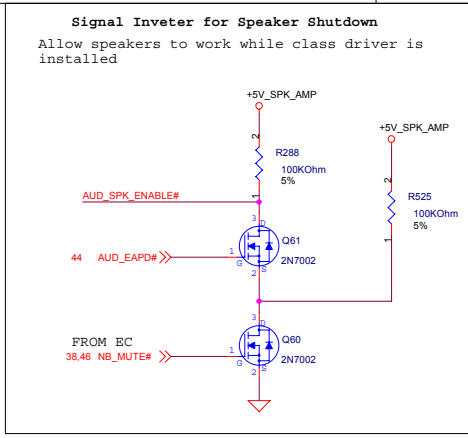
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DATE: Monday, March 19, 2007  
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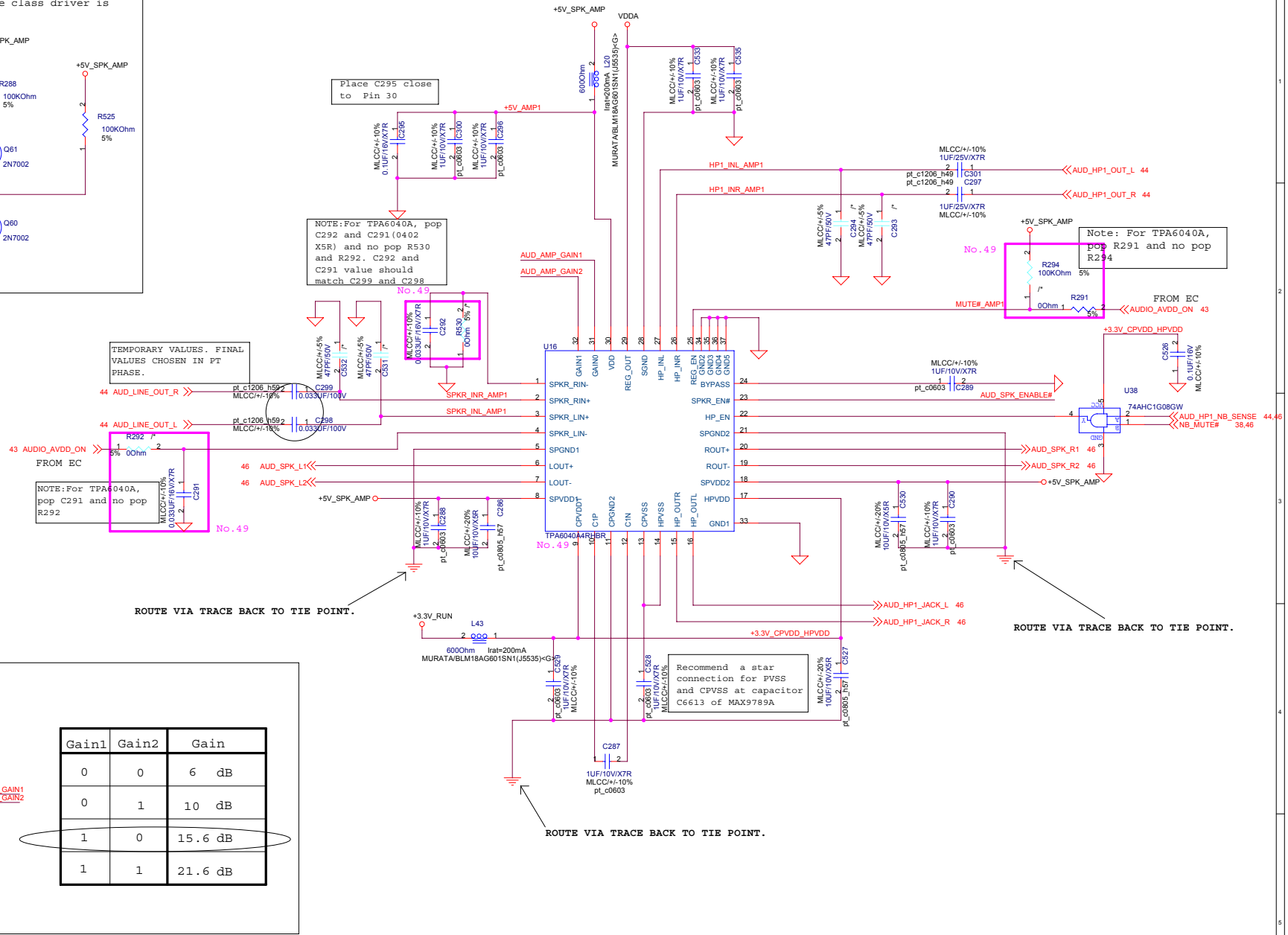
DESCRIPTION:  
STAC9228

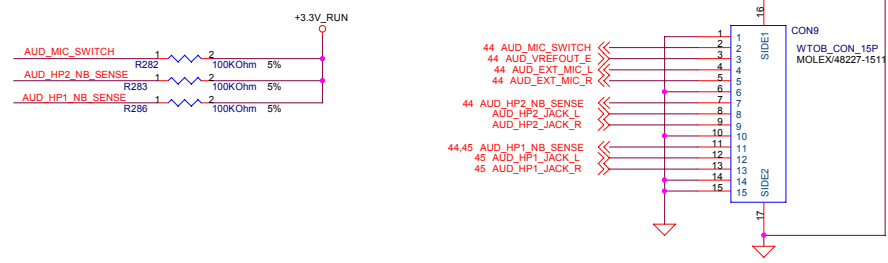
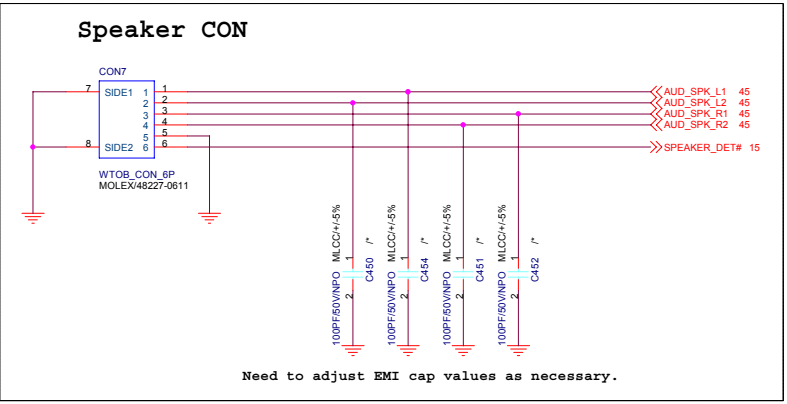
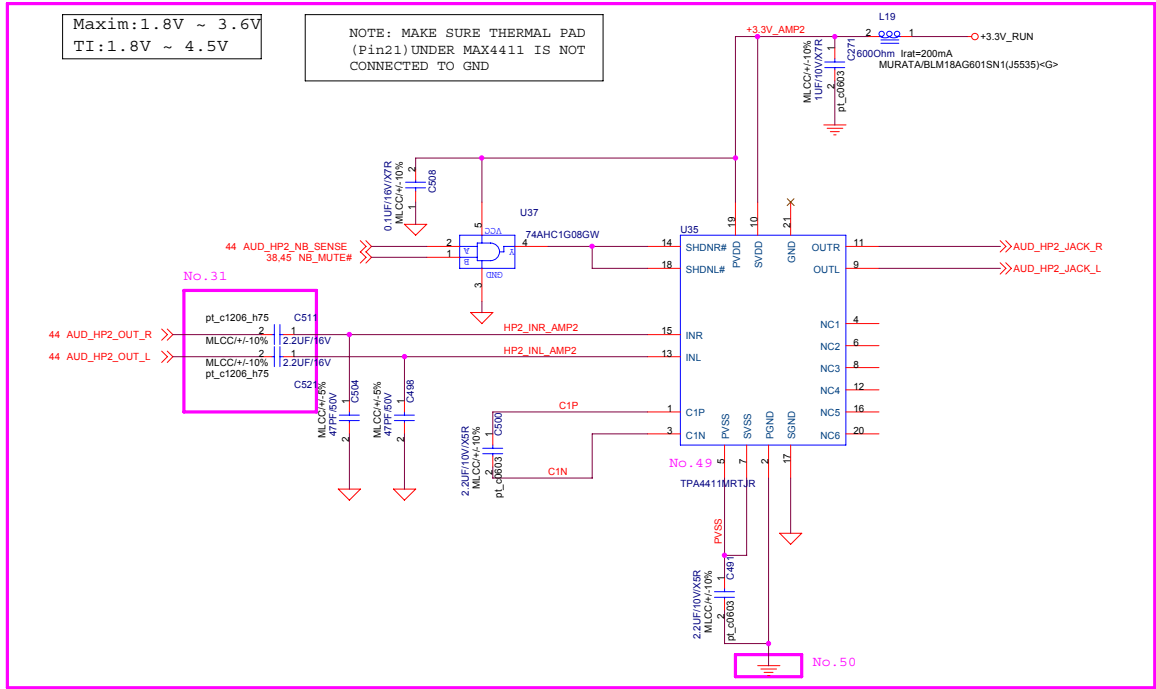
SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER :  
Yihao Yeh

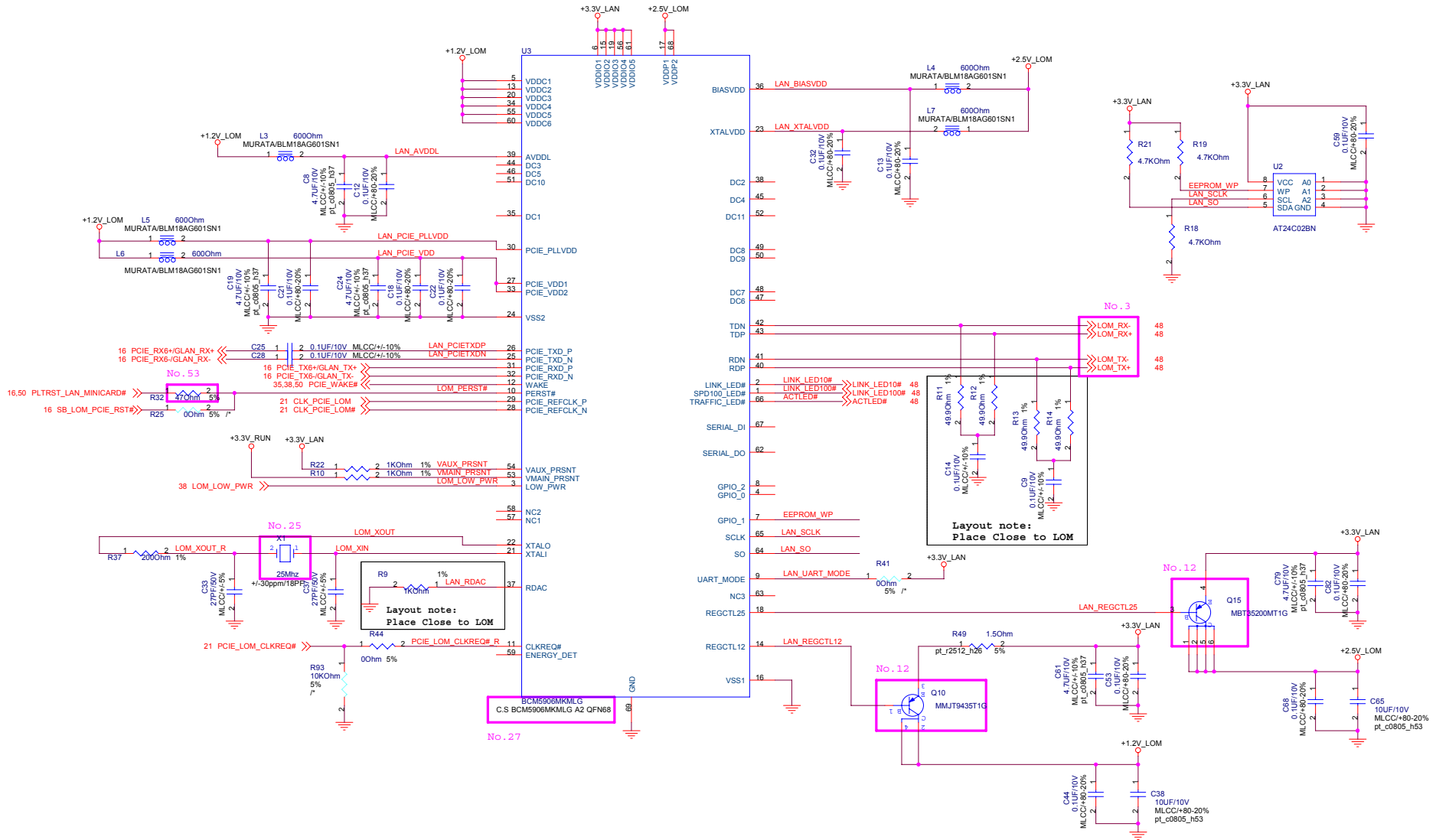
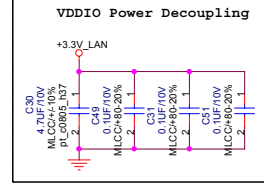
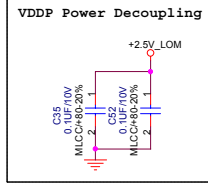
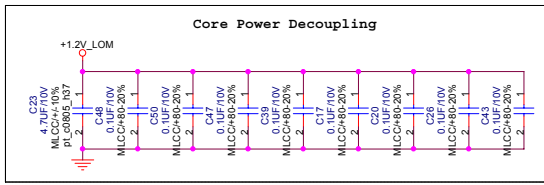


Gain1	Gain2	Gain
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB





PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 46 OF 68	AMP MAX4411 & AUDIO JACK	<OrgName>	Yihao Yeh



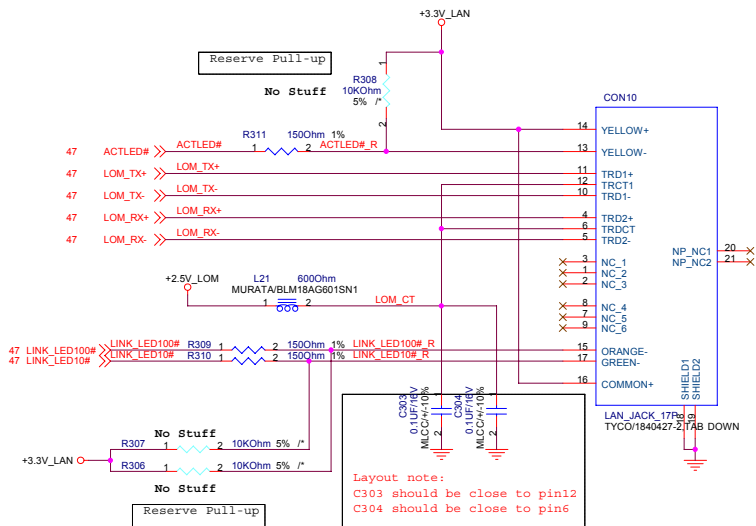
**PROJECT: Lanai**

REVISION: **1.2**  
 DATE: **Monday, March 19, 2007**  
 SHEET: **47** OF **68**

DESCRIPTION: **LAN BCM5906MKMLG(QFN-68)**

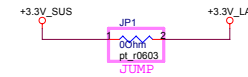
SCHEMATIC FILE NAME: **<OrgName>**  
 RELEASE DATE:

DESIGN ENGINEER: **Ivan Chou**



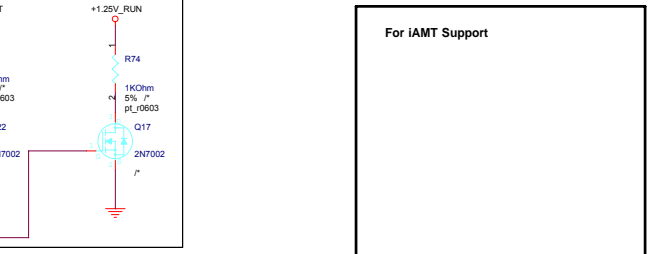
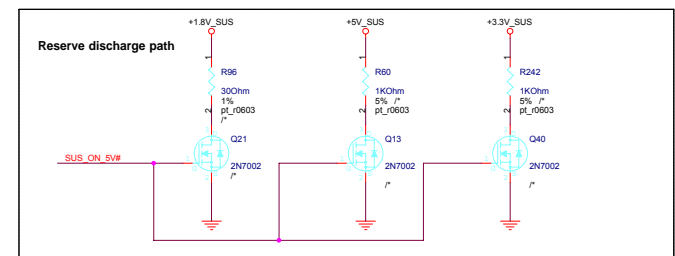
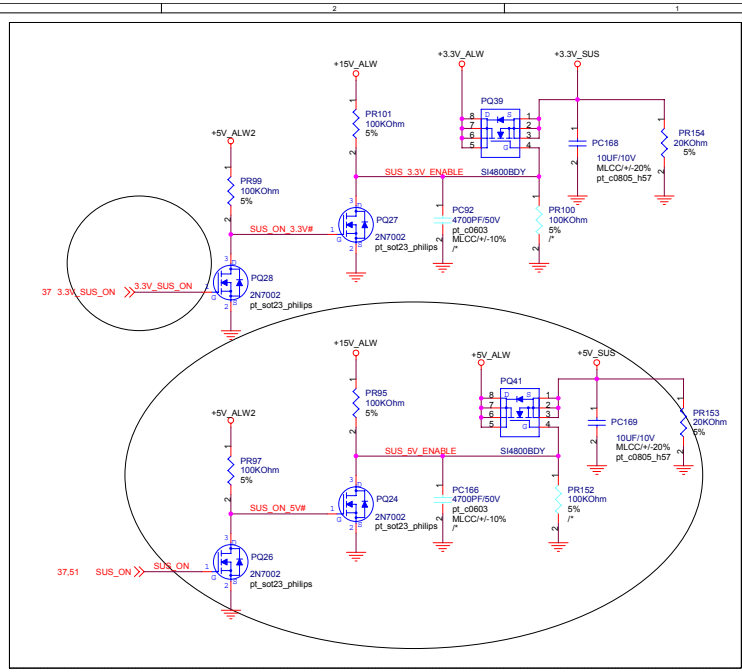
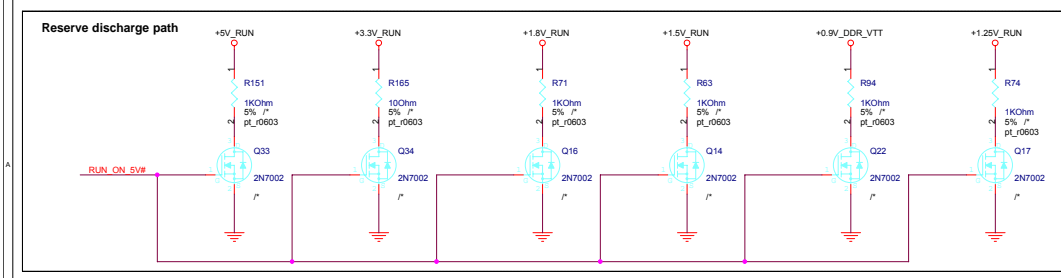
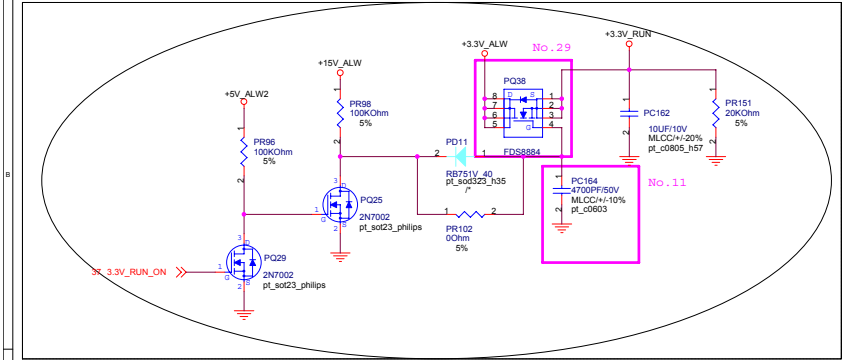
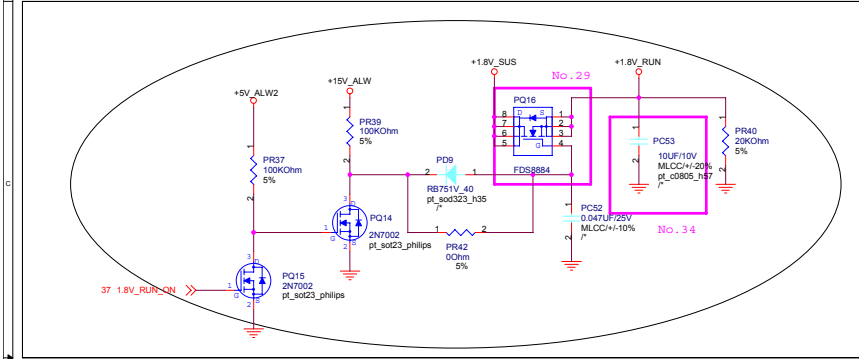
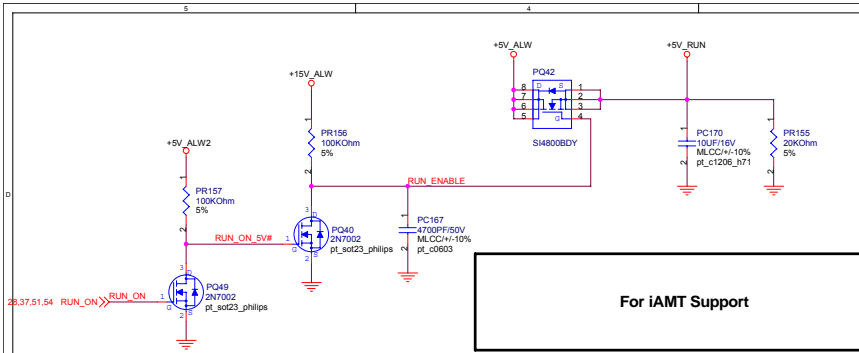
**+3.3V LAN Source Guideline:**

1. Use +3.3V\_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V\_SRC if Wake-on-LAN is required out of S4, S5

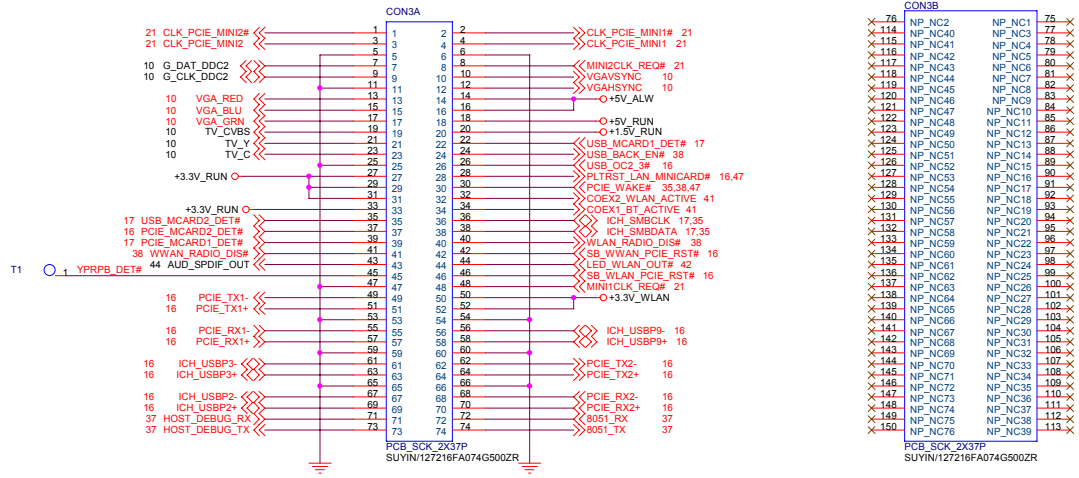
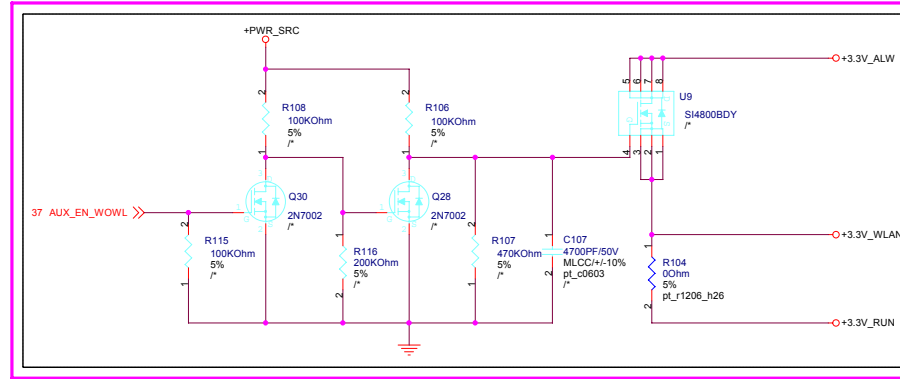


<b>PROJECT: Lanai</b>	REVISION	DATE: <b>Monday, March 19, 2007</b>	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	<b>1.2</b>	SHEET <b>48</b> OF <b>68</b>	<b>Magnetics and RJ-45</b>	RELEASE DATE :		<b>Ivan Chou</b>

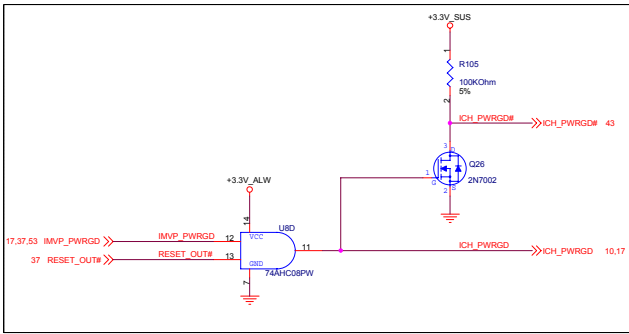
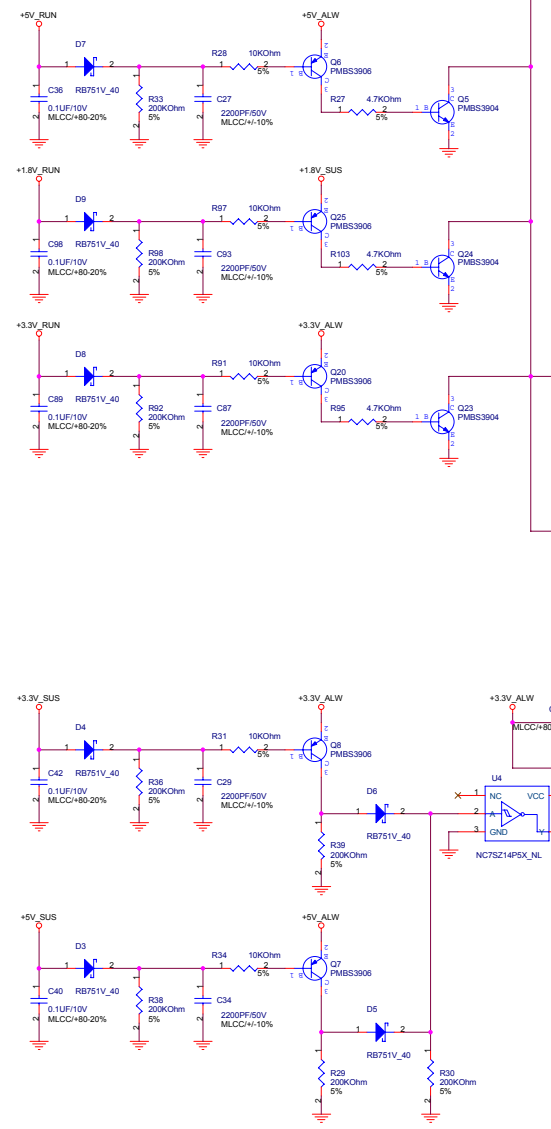
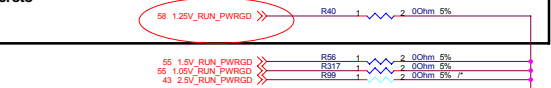




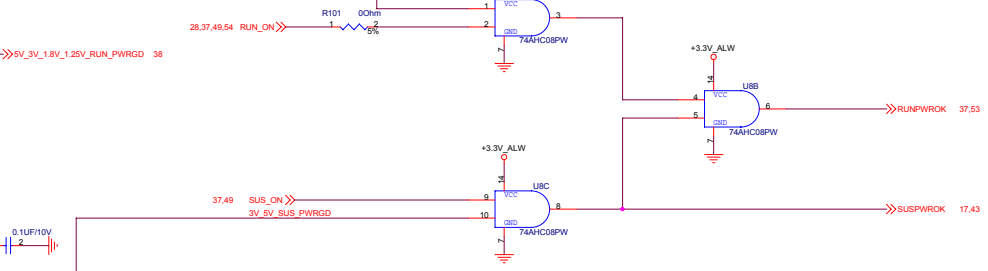
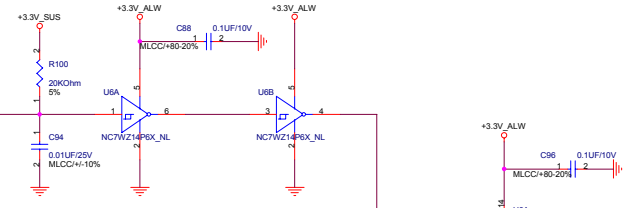
No. 21



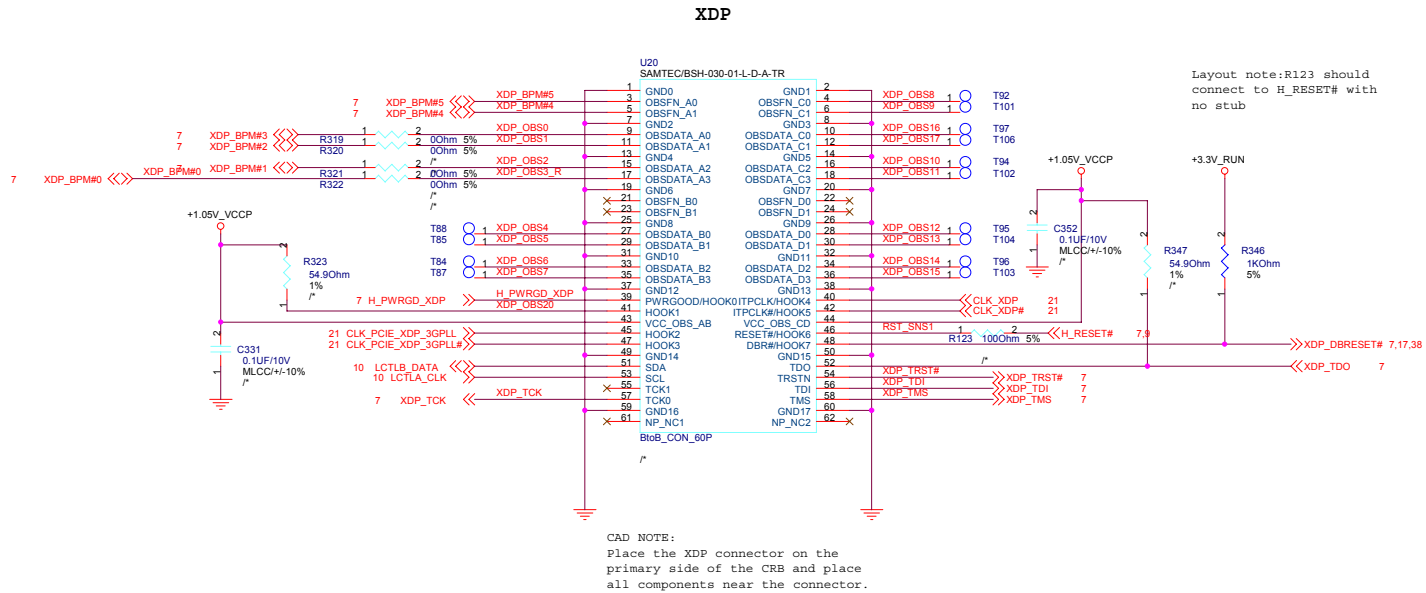
Discrete



Keep Away from high speed buses

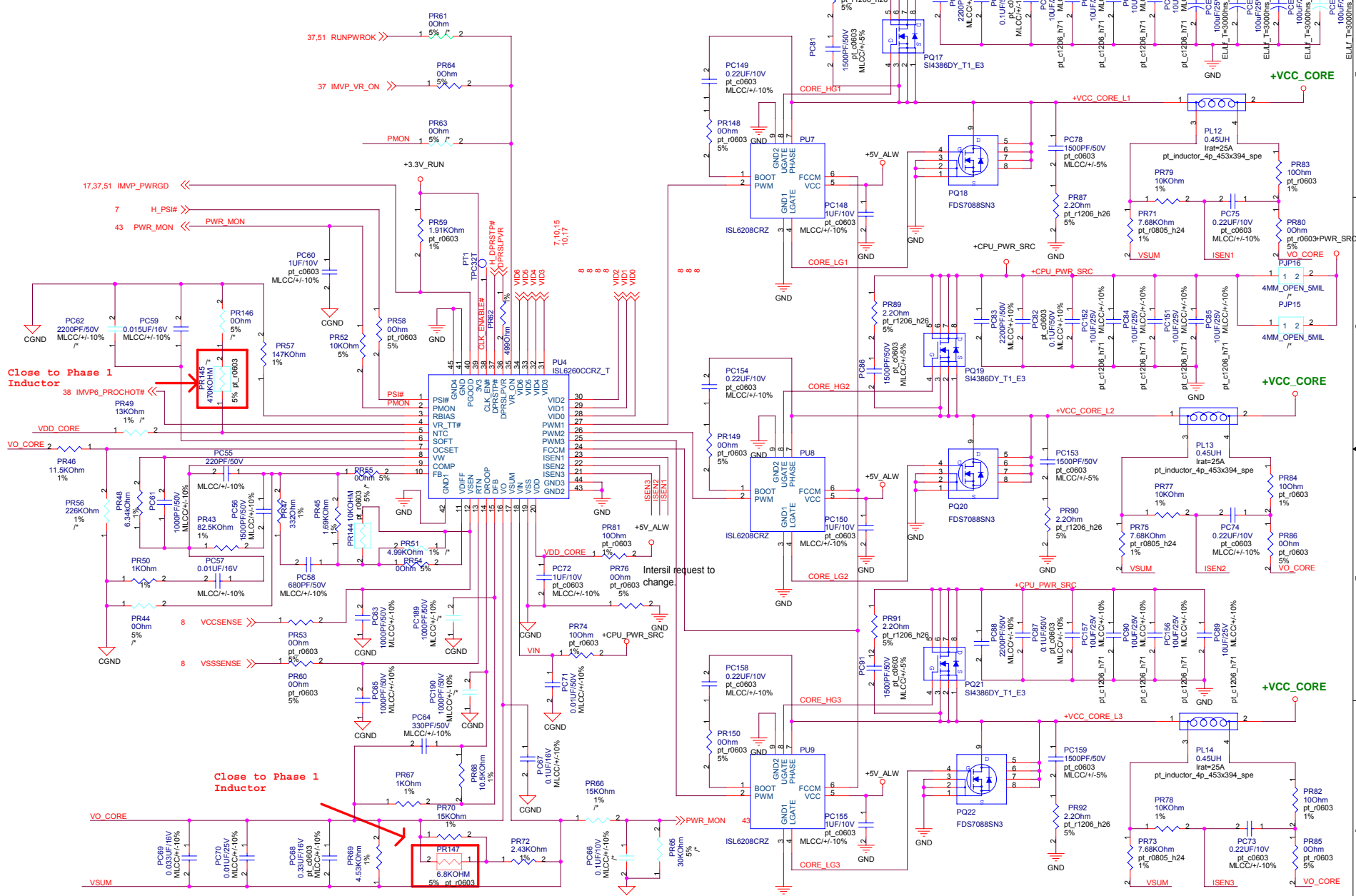


PROJECT: Lanai	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Power Sequence Logic	SCHEMATIC FILE NAME:	DESIGN ENGINEER: C.L. Ho
	SHEET: 51	OF: 68		RELEASE DATE:	



<b>PROJECT: Lanai</b>	REVISION	DATE: <b>Monday, March 19, 2007</b>	DESCRIPTION:	SCHMATIC FILE NAME:	DESIGN ENGINEER:
	<b>1.2</b>	SHEET <b>52</b> OF <b>68</b>	<b>XDP</b>	<b>&lt;OrgName&gt;</b>	<b>Terry Lin</b>
				RELEASE DATE:	

Design Current:35.2A  
 Maximum current:44A  
 OCP point min.50A



PROJECT: Lanai

REVISION: 1.2  
 DATE: Monday, March 19, 2007  
 SHEET: 53 OF 68

DESCRIPTION: POWER\_VCORE

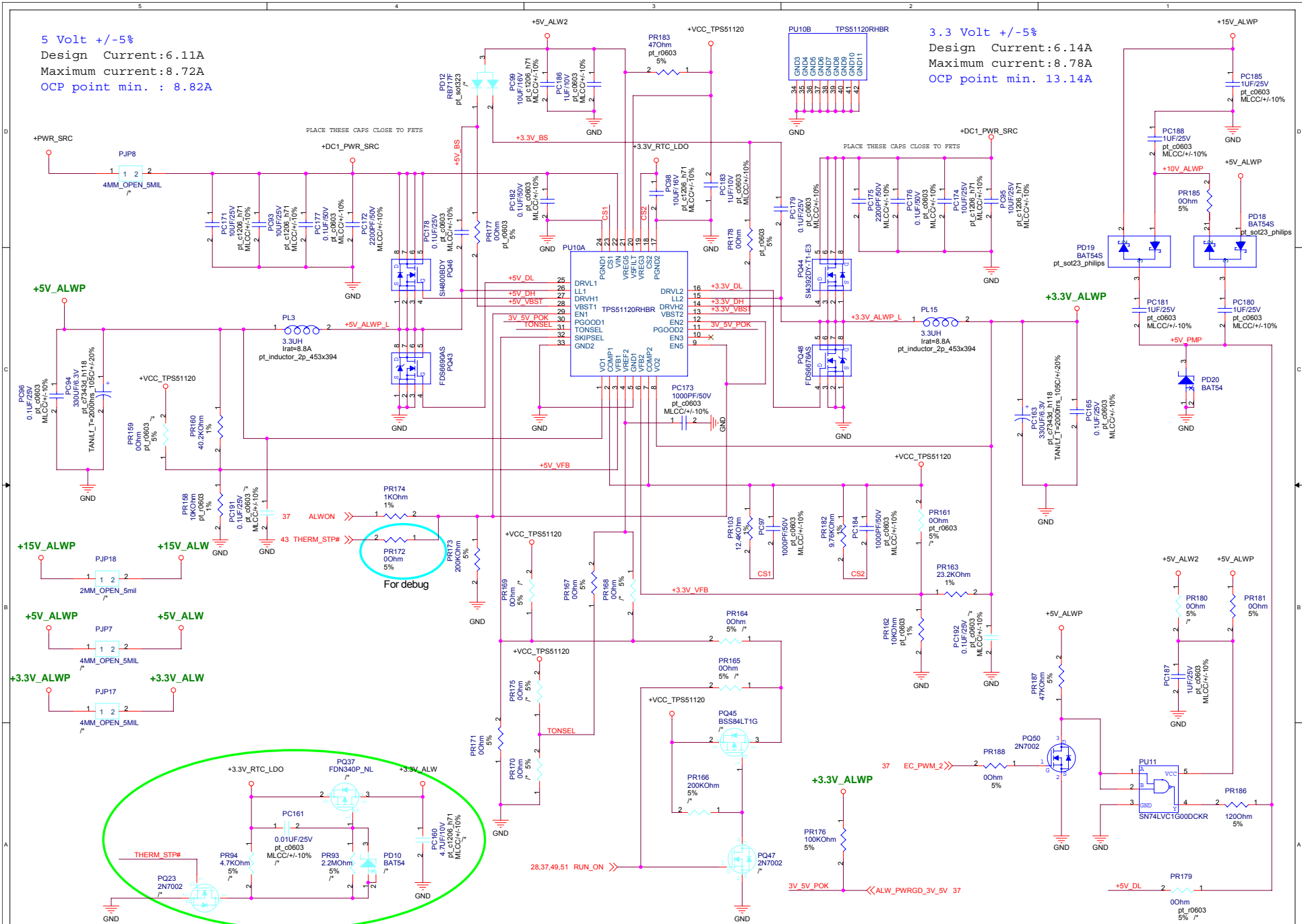
SCHEMATIC FILE NAME: <OrgName>  
 RELEASE DATE:

DESIGN ENGINEER: JEFF

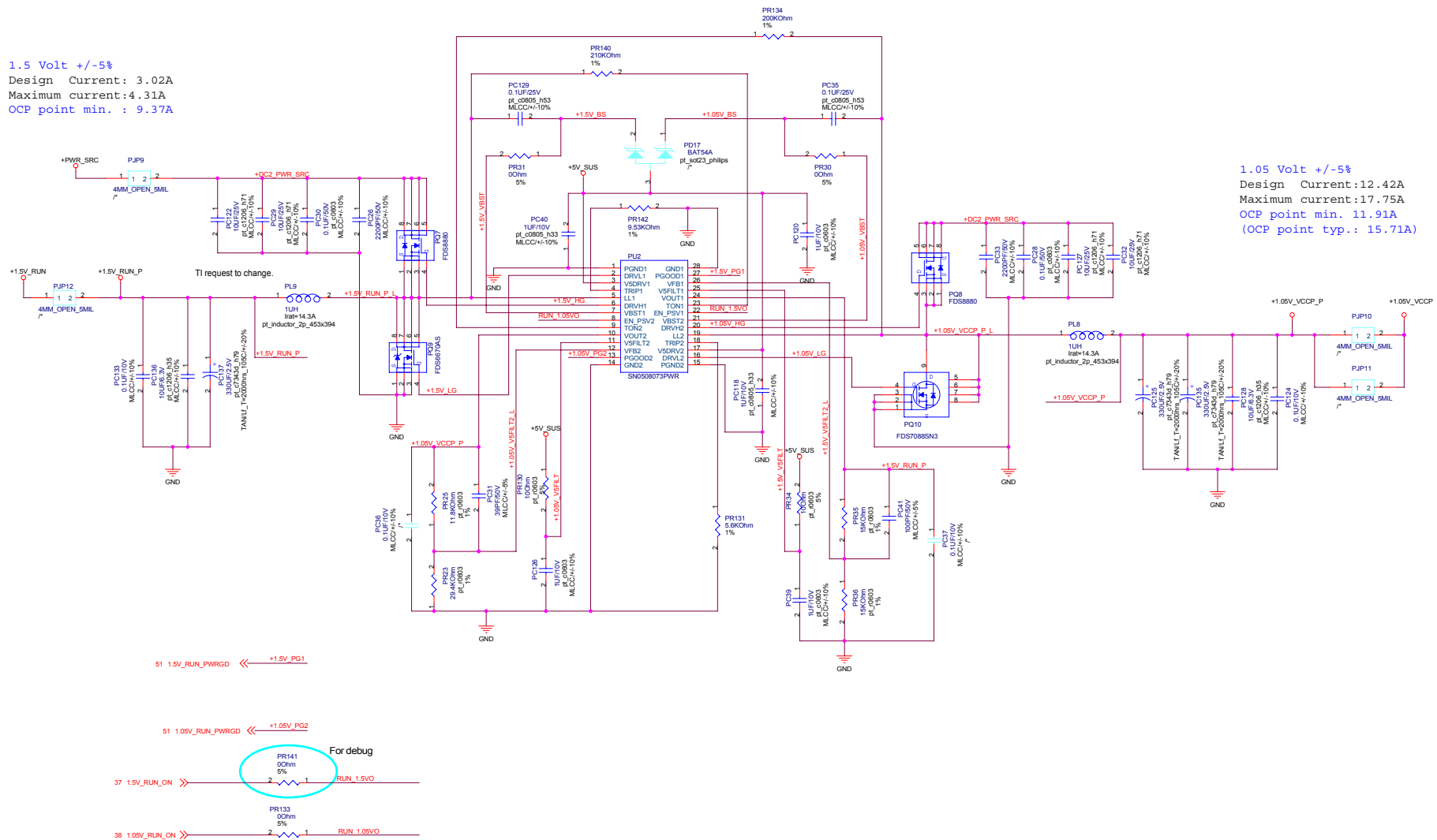
www.laptop-schematics.com

5 Volt +/-5%  
 Design Current:6.11A  
 Maximum current:8.72A  
 OCP point min. : 8.82A

3.3 Volt +/-5%  
 Design Current:6.14A  
 Maximum current:8.78A  
 OCP point min. 13.14A



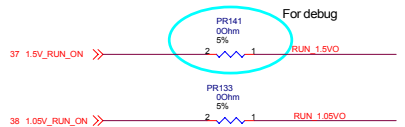
1.5 Volt +/-5%  
 Design Current: 3.02A  
 Maximum current: 4.31A  
 OCP point min. : 9.37A



1.05 Volt +/-5%  
 Design Current: 12.42A  
 Maximum current: 17.75A  
 OCP point min. 11.91A  
 (OCP point typ.: 15.71A)

51 1.5V\_RUN\_PWRGD ← +1.5V\_PG1

51 1.05V\_RUN\_PWRGD ← +1.05V\_PG2



PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: POWER I/O 1.5VS & 1.05VS	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: JEFF
		SHEET 55 OF 68		RELEASE DATE:	





TOTAL POWER=6.5W  
-->3.34A

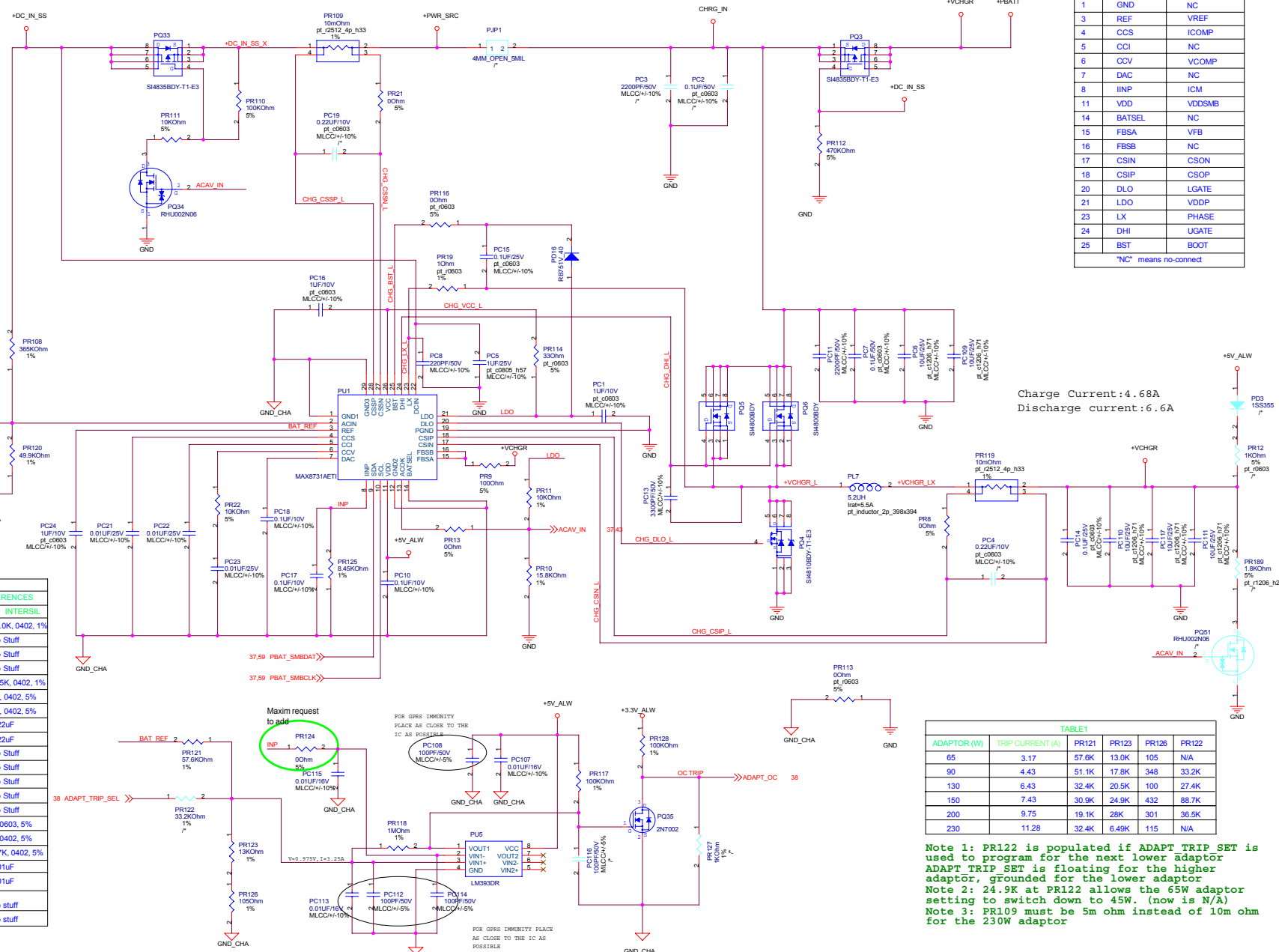
TABLE3  
PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDD5MB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect

TABLE2  
MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL
PR125	8.45K, 0402, 1%	16.0K, 0402, 1%
PC115	0.01uF	No Stuff
PC17	0.1uF, 0402, 10V	No Stuff
PC24	1.0uF, 0603, 10V	No Stuff
PR106	365K, 0402, 1%	215K, 0402, 1%
PR8	0, 0402, 5%	10, 0402, 5%
PR21	0, 0402, 5%	10, 0402, 5%
PC4	No Stuff	0.22uF
PC19	No Stuff	0.22uF
PC22	0.01uF	No Stuff
PC18	0.1uF, 0402, 10V	No Stuff
PC8	220pF, 0402, 50V	No Stuff
PD16	RB751V-40	No Stuff
PC13	3.3nF	No Stuff
PR19	1, 0603, 1%	0, 0603, 5%
PR9	100, 0402, 5%	0, 0402, 5%
PR22	4.7K, 0402, 5%	4.7K, 0402, 5%
PC23	0.01uF	0.01uF
PC21	0.01uF	0.01uF
PD3	1SS355	No stuff
PR12	1K, 0603, 5%	No stuff



Charge Current: 4.68A  
Discharge current: 6.6A

TABLE1

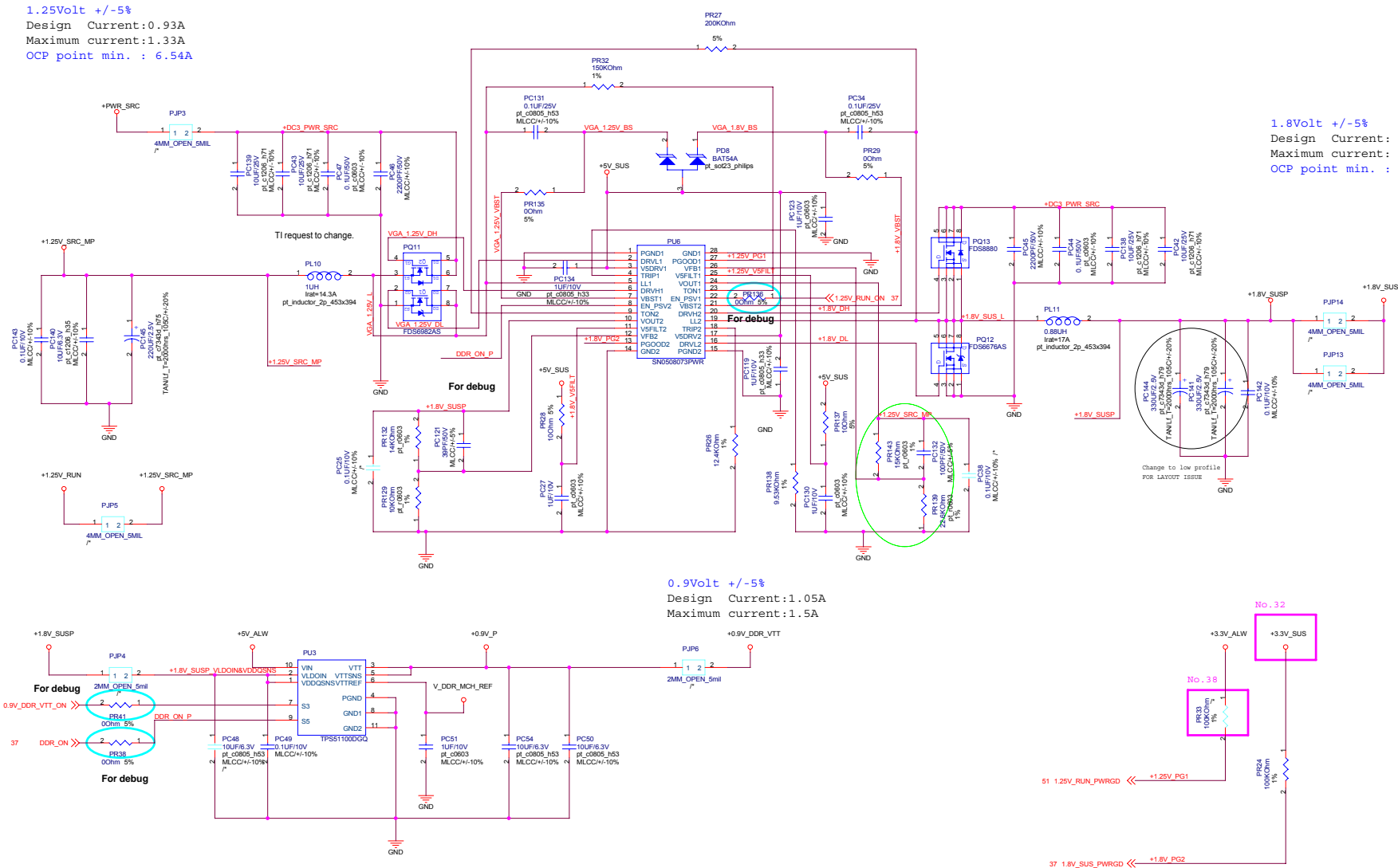
ADAPTOR (W)	TRIP CURRENT (A)	PR121	PR123	PR126	PR122
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR122 is populated if ADAPT\_TRIP\_SET is used to program for the next lower adaptor. ADAPT\_TRIP\_SET is floating for the higher adaptor, grounded for the lower adaptor.  
Note 2: 24.9K at PR122 allows the 65W adaptor setting to switch down to 45W. (now is N/A)  
Note 3: PR109 must be 5m ohm instead of 10m ohm for the 230W adaptor

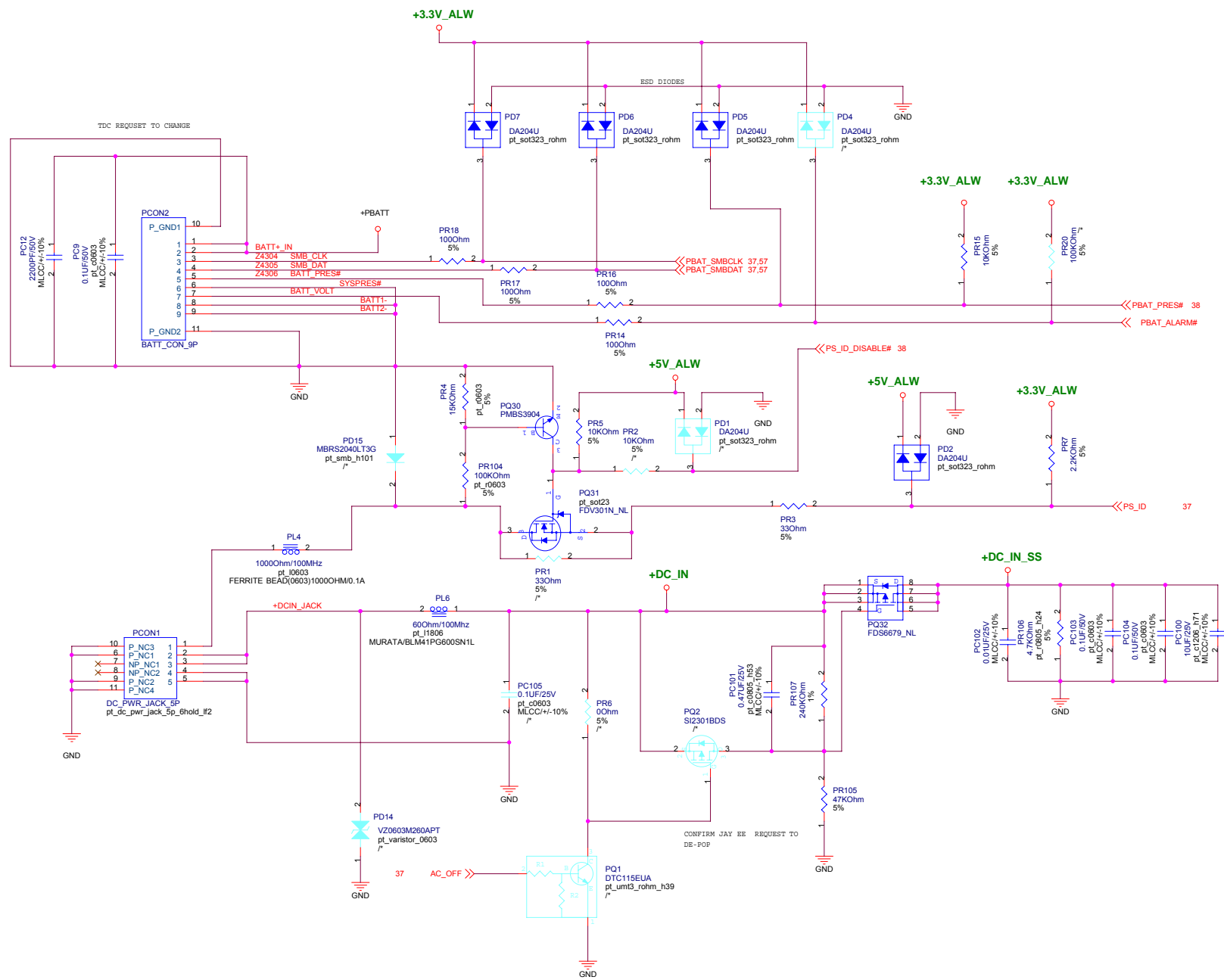
1.25Volt +/-5%  
 Design Current:0.93A  
 Maximum current:1.33A  
 OCP point min. : 6.54A

1.8Volt +/-5%  
 Design Current: 6.59A  
 Maximum current: 9.42A  
 OCP point min. : 16.93A

0.9Volt +/-5%  
 Design Current:1.05A  
 Maximum current:1.5A

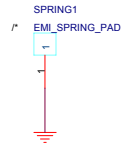
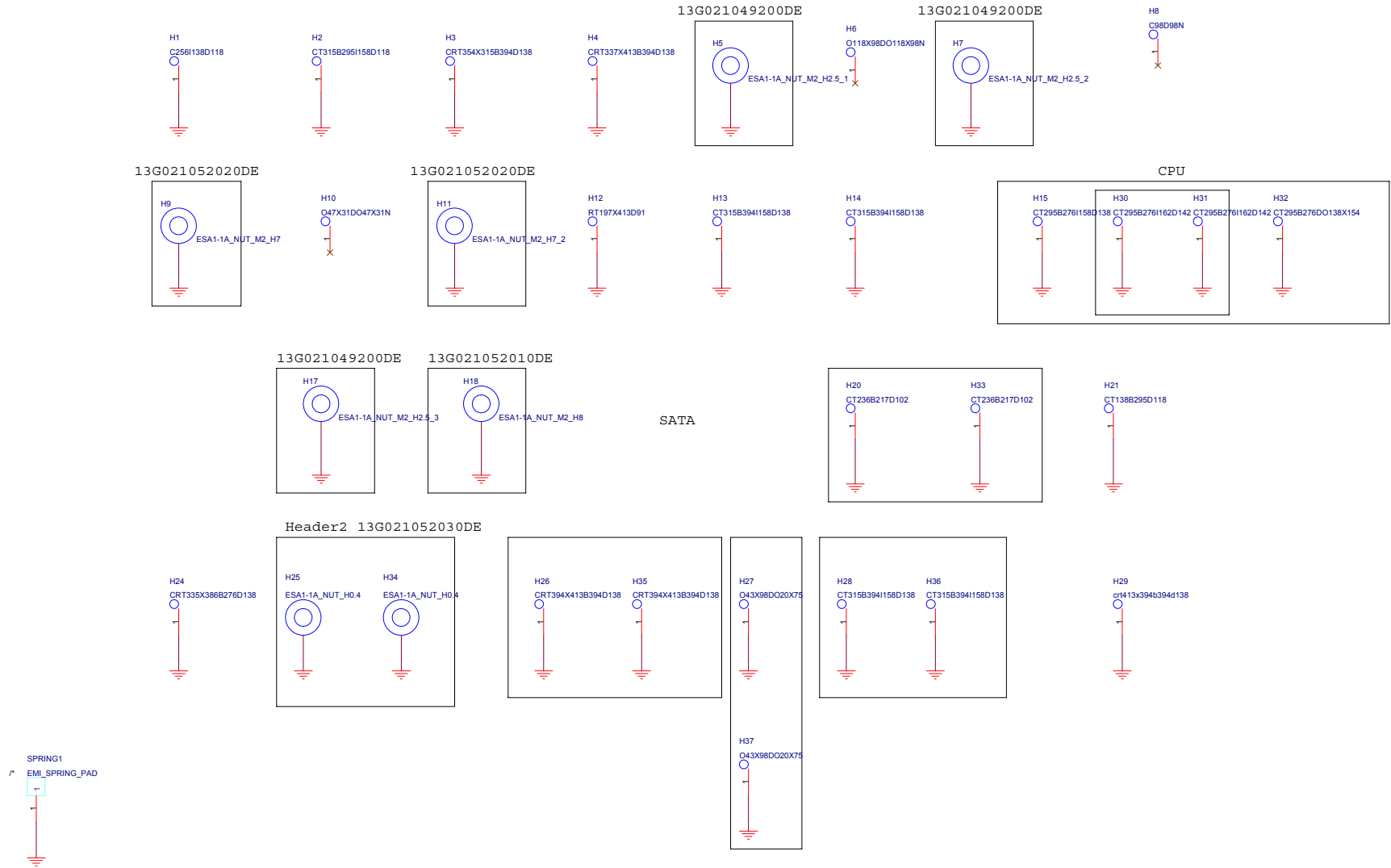


PROJECT: Lanai	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: POWER VGA 1.25V & DDR & VTT	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: Jeff
		SHEET 58 OF 68		RELEASE DATE:	



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 59 OF 68	POWER_CONNECTOR	<OrgName>	JEFF

GM screw pad

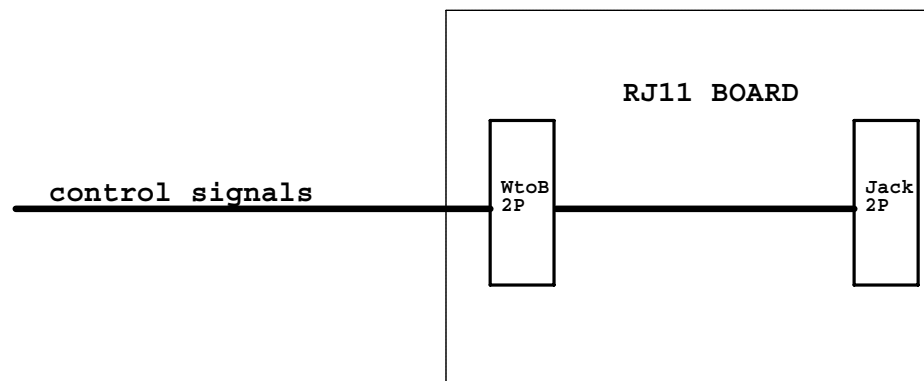


PROJECT: Lanai	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: SCREW PAD	SHEET: 60 OF 68	SCHEMATIC FILE NAME :	DESIGN ENGINEER: Sean Kuo
					RELEASE DATE :	

**ASUS CONFIDENTIAL**

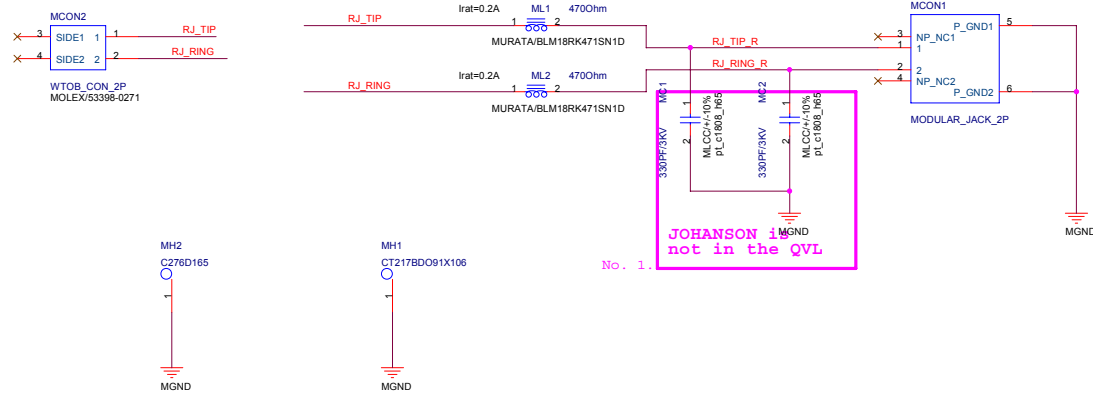
MODEL NAME : *Elsa*

## *Lanai:Modem Board*



**REV : 1.1(DELL: X01)**

<b>PROJECT: Lanai</b>	REVISION	DATE: <i>Monday, March 19, 2007</i>	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	<b>1.2</b>	SHEET <b>64</b> OF <b>68</b>	<b>BLOCK DIAGRAM</b>	RELEASE DATE :	<b>Stanly Hsu</b>



No. 1.  
JOHANSON is not in the QVL

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 65 OF 68	RJ-11 CONN	RELEASE DATE :		Stanly Hsu

# ASUS CONFIDENTIAL

MODEL NAME : *Elsa*

PCB NO : ???

ASUS P/N : ???

## Lanai PP2 USB Board

REV : 1.1(DELL: X01)

MB PCB

Part Number	Description
DA80004H0L	PCB 00B LA-3071P REV0 M/B

*BOM NO. ???*

*PCB P/N: ???*

PROJECT: **Lanai**

REVISION  
**1.2**

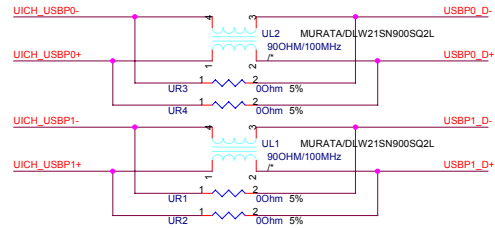
DATE: **Monday, March 19, 2007**  
SHEET **67** OF **68**

DESCRIPTION: **Cover Page**

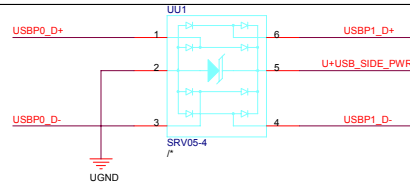
SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER :  
**Terry Lin**

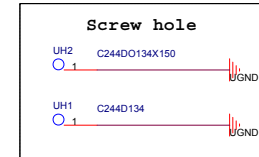
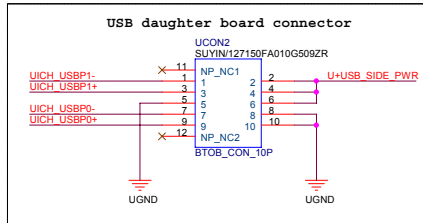
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .



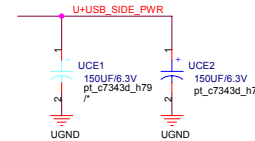
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C ( 1pf vs 3pf ) .

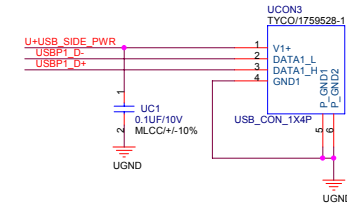
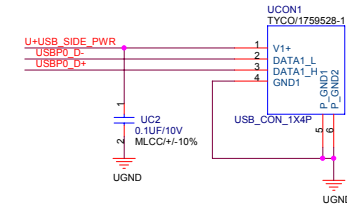


Place one 150uF cap by each USB connector



Each channel is 1A

Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines. Add PADS ONLY until proven diodes are really needed.



PROJECT: Lanai

REVISION 1.2

DATE: Monday, March 19, 2007  
SHEET 68 OF 68

DESCRIPTION: USB PORT ( SINGLE \* 2 )

SCHEMATIC FILE NAME: <OrgName>  
RELEASE DATE:

DESIGN ENGINEER: Terry Lin