

Compal Confidential

KAW60 Schematics Document

AMD AM2 / RS690MC / SB600

2008 / 07 / 25

Rev:0.2

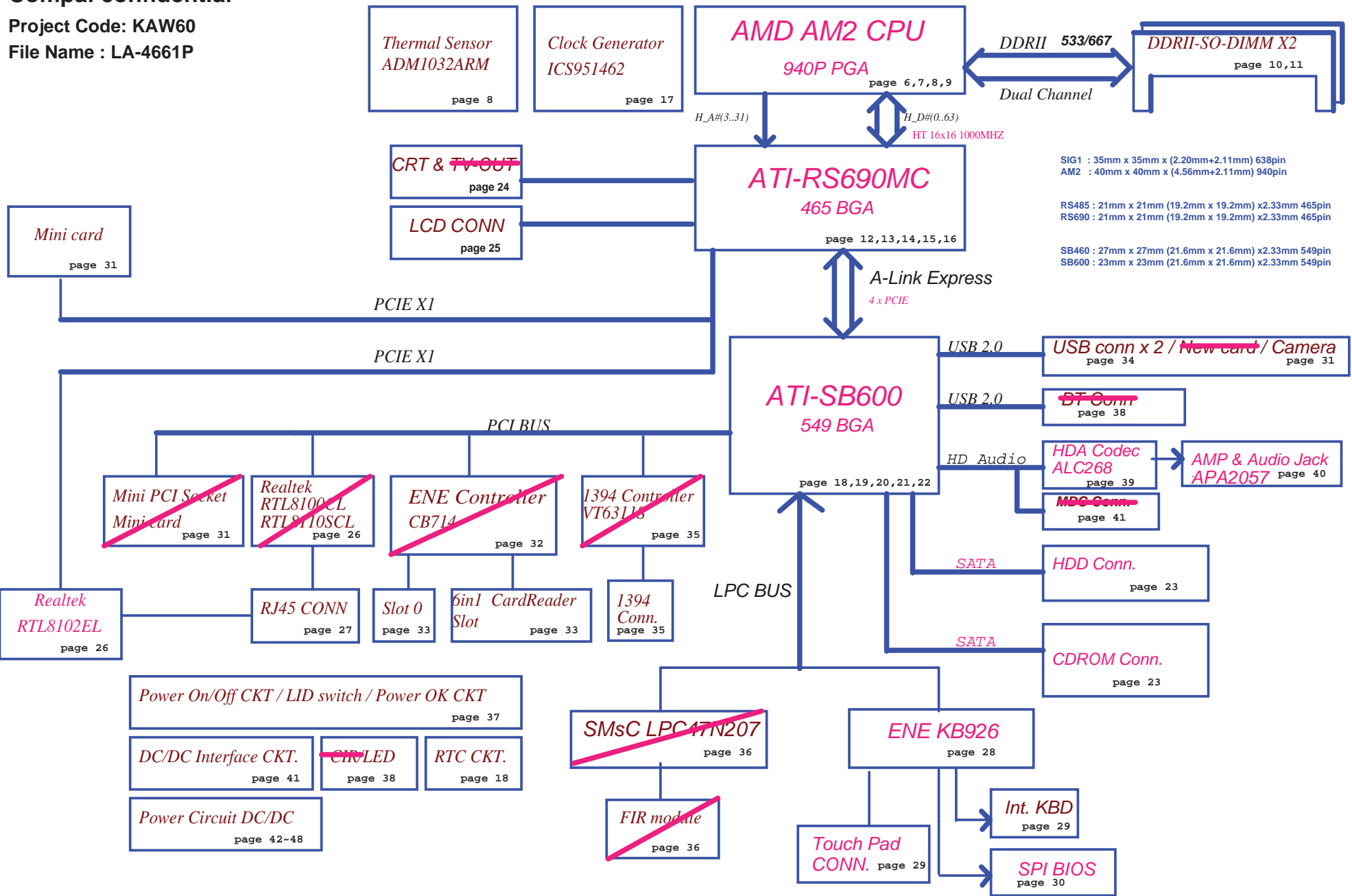
FOR PVT

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Project Code: KAW60

File Name : LA-4661P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		
(24C04)	1011 000X b		

EC SM Bus2 address

SB600 SM Bus address

Device	Address
Clock Generator (ICS951462)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

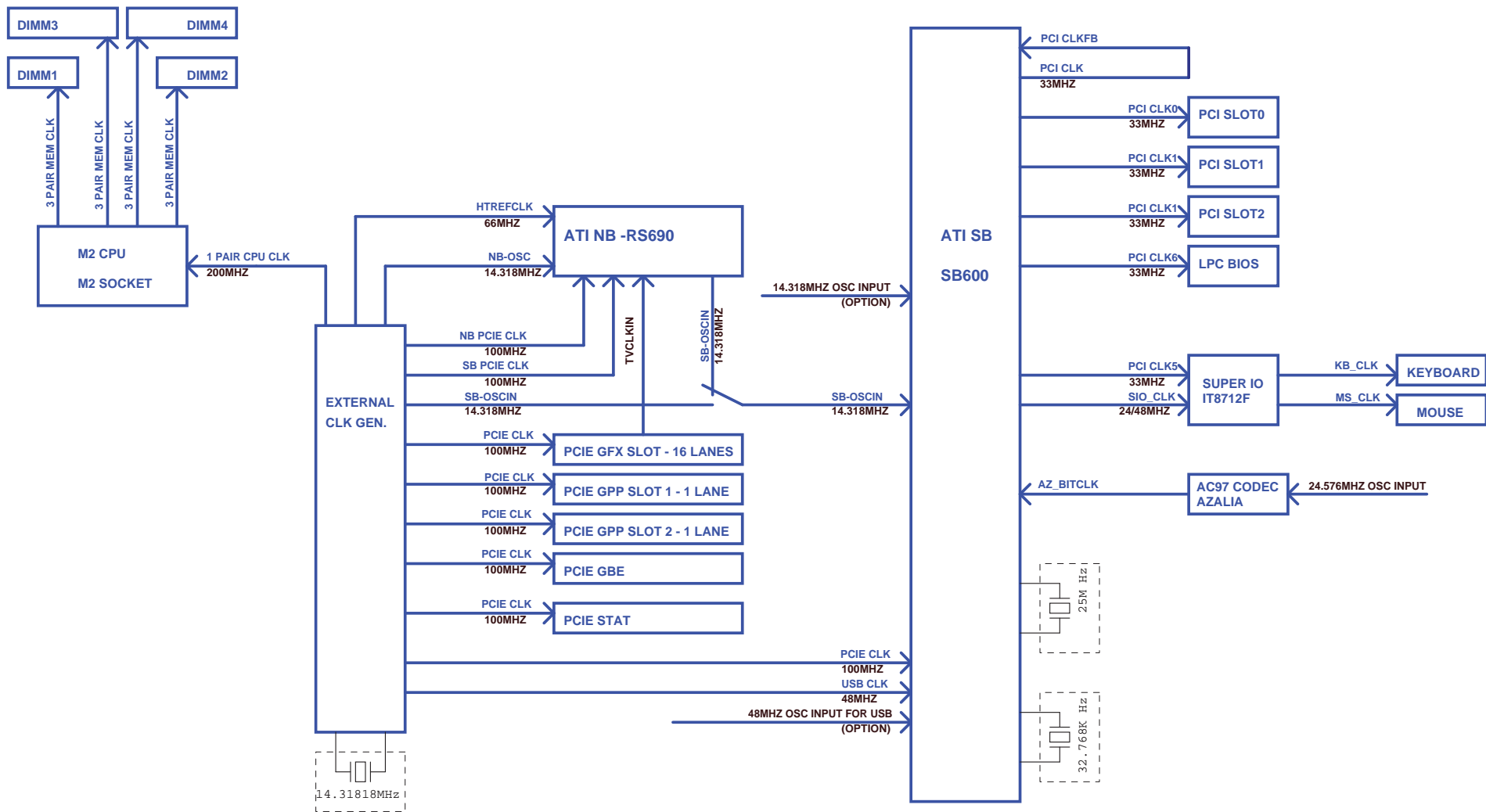
SKU ID Table

SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

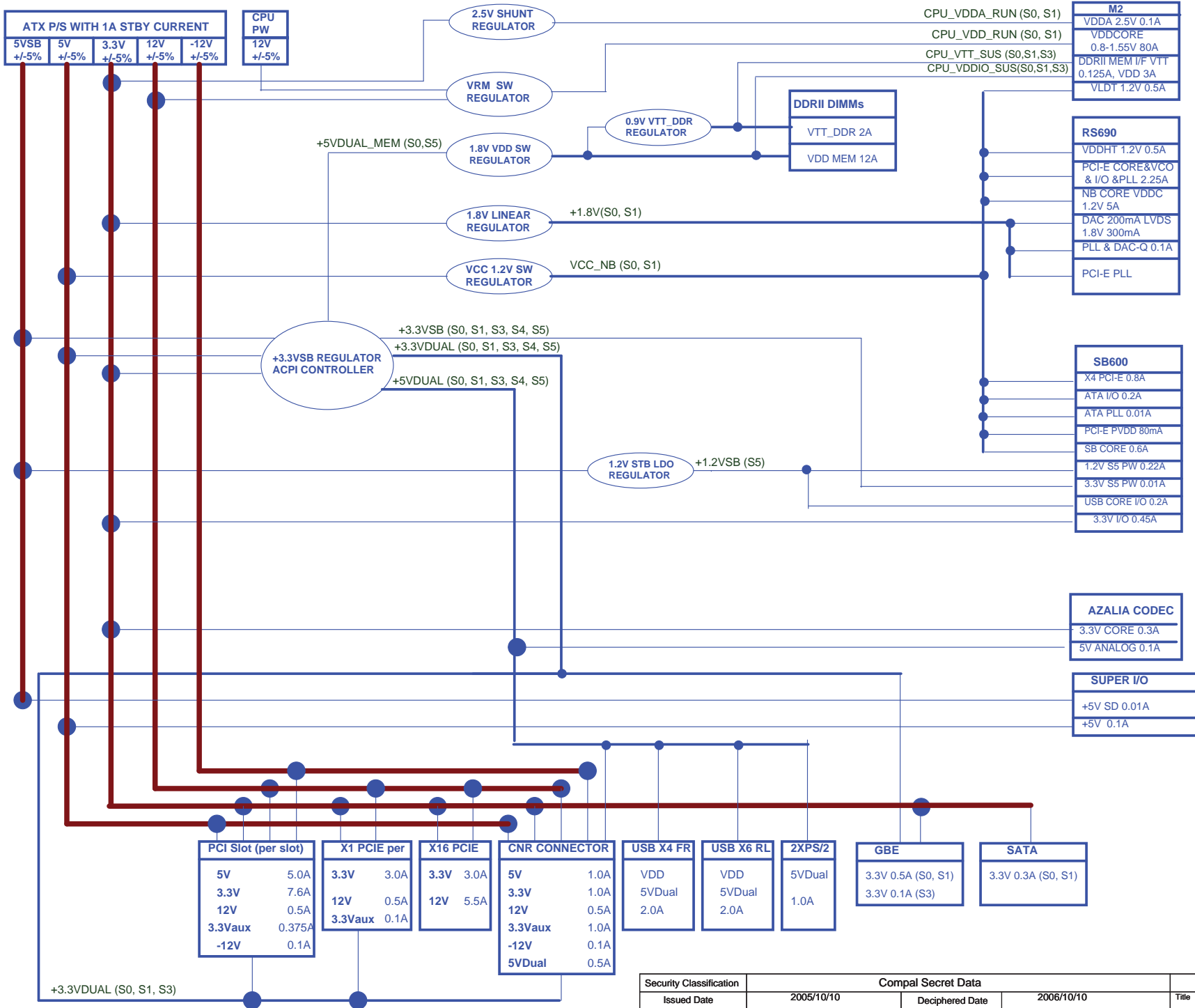
BTO Option Table

BTO Item	BOM Structure
WITH AMD HDT Debug port	HDT@
WITH USBx2	USB2@
USBX1 WITH CHOKE	EMI@
USBX1 WITHOUT CHOKE	WOEMI@
USBx2 WITH CHOKE	USB2EMI@
USBx2 WITHOUT CHOKE	USB2WOEMI@
WITH MODEM	MDC@
SPI ROM under SB600	SB600SPI@

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M2	
VDDA 2.5V	0.1A
VDDCORE	0.8-1.55V 80A
DDRII MEM I/F VTT	0.125A, VDD 3A
VLDI	1.2V 0.5A

RS690	
VDDHT	1.2V 0.5A
PCI-E CORE&VCO & I/O & PLL	2.25A
NB CORE VDDC	1.2V 5A
DAC	200mA LVDS 1.8V 300mA
PLL & DAC-Q	0.1A
PCI-E PLL	

SB600	
X4 PCI-E	0.8A
ATA I/O	0.2A
ATA PLL	0.01A
PCI-E PVDD	80mA
SB CORE	0.6A
1.2V S5 PW	0.22A
3.3V S5 PW	0.01A
USB CORE I/O	0.2A
3.3V I/O	0.45A

AZALIA CODEC	
3.3V CORE	0.3A
5V ANALOG	0.1A

SUPER I/O	
+5V SD	0.01A
+5V	0.1A

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X1 PCIE per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.1A

X16 PCIE	
3.3V	3.0A
12V	5.5A

CNR CONNECTOR	
5V	1.0A
3.3V	1.0A
12V	0.5A
3.3Vaux	1.0A
-12V	0.1A
5VDual	0.5A

USB X4 FR	
VDD	2.0A
5VDual	2.0A

USB X6 RL	
VDD	2.0A
5VDual	2.0A

2XPS/2	
5VDual	1.0A

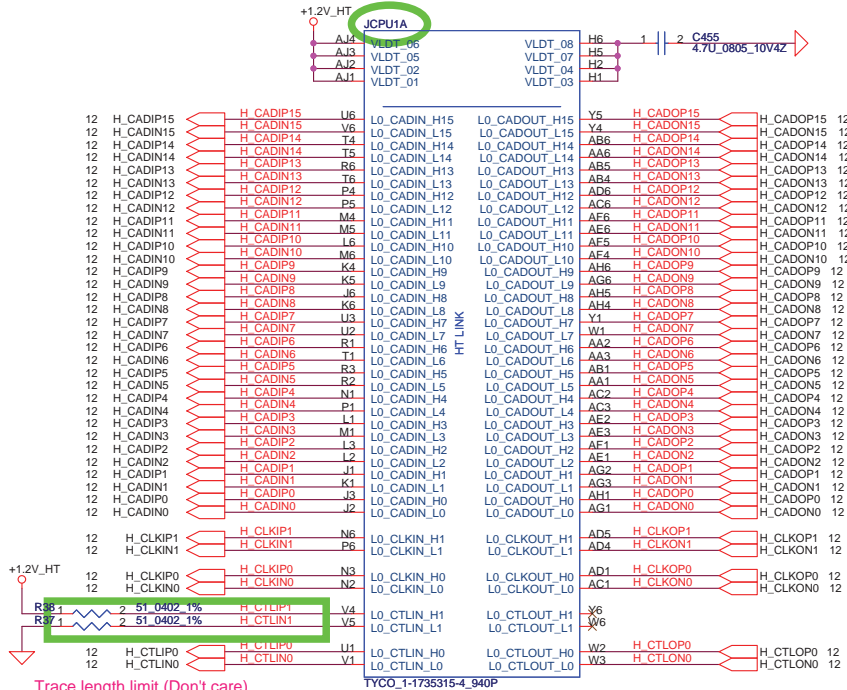
GBE	
3.3V	0.5A (S0, S1)
3.3V	0.1A (S3)

SATA	
3.3V	0.3A (S0, S1)

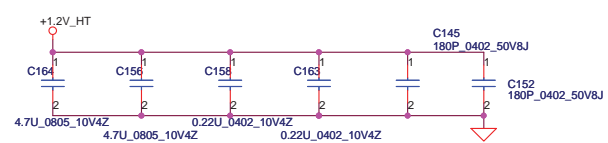
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Issued Date	2005/10/10	Deciphered Date	2006/10/10	POWER DELIVERY CHART	
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PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

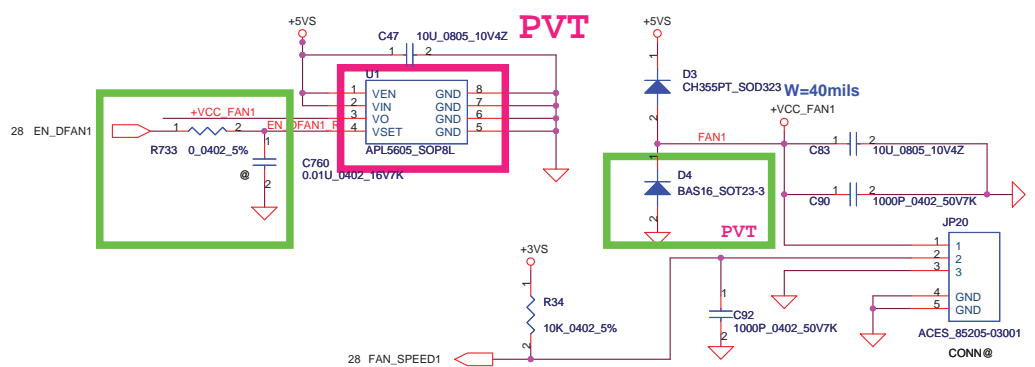


CONN@
 SOC127MM48X51-948! 6090022000; JCPU1
 TEMP SYMBOL



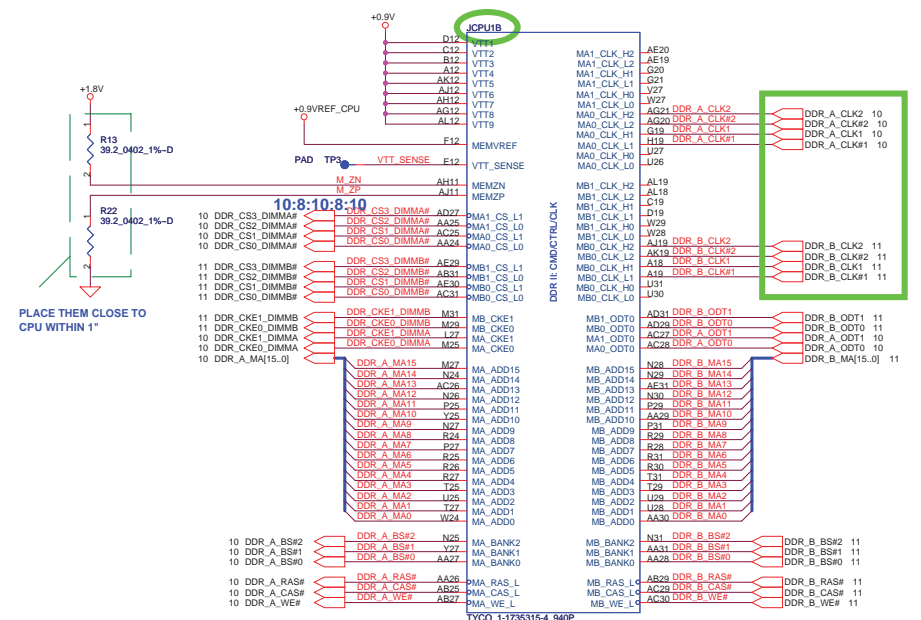
LAYOUT: Place bypass cap on topside of board
 NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
 PLACE CLOSE TO VLDTO POWER PINS

FAN Conn

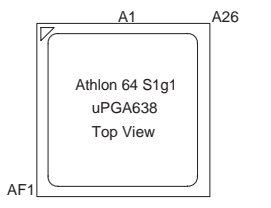
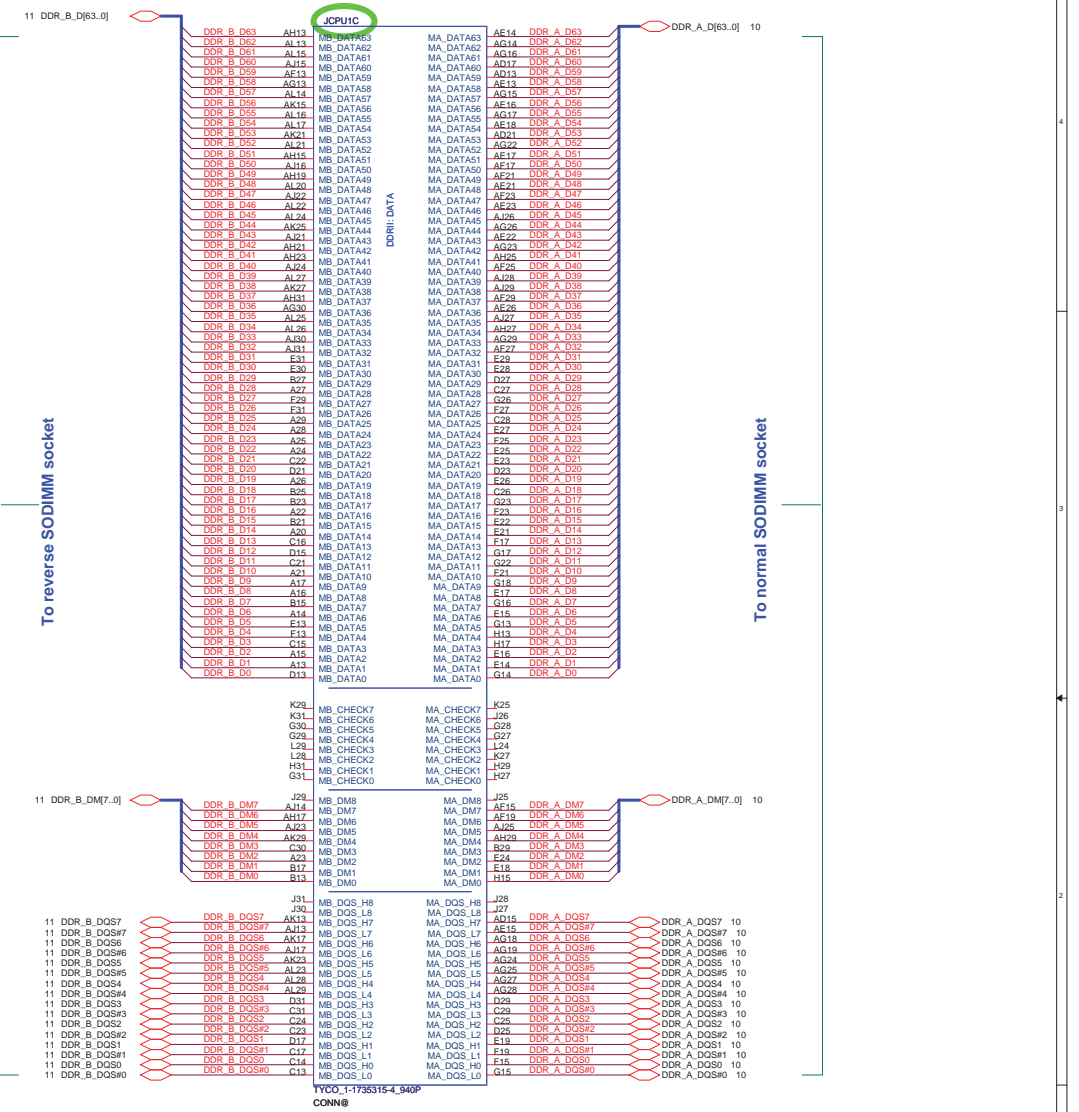


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VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

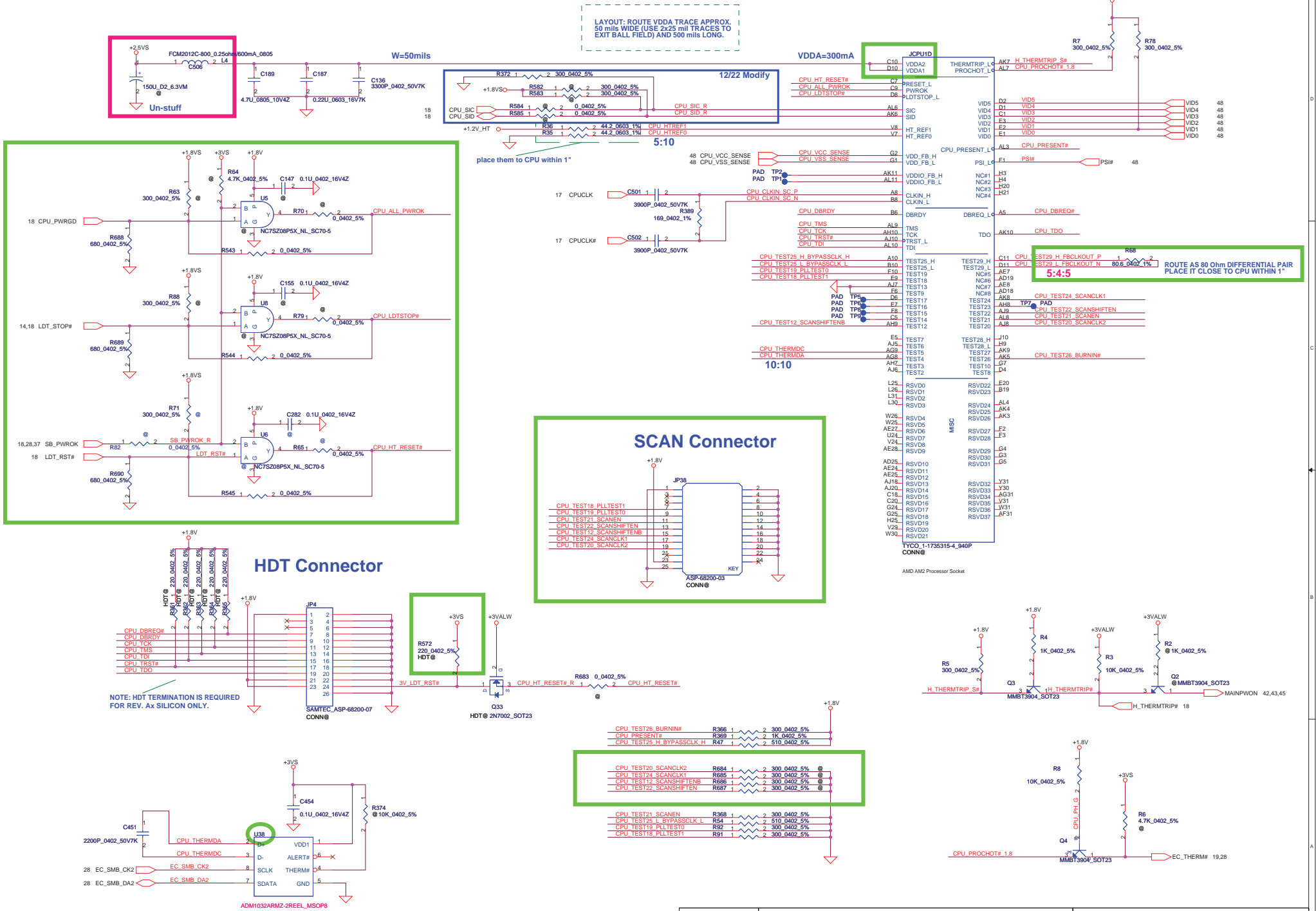


Processor DDR2 Memory Interface



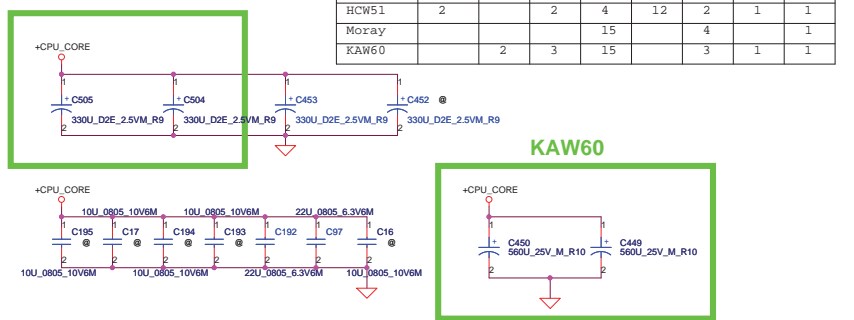
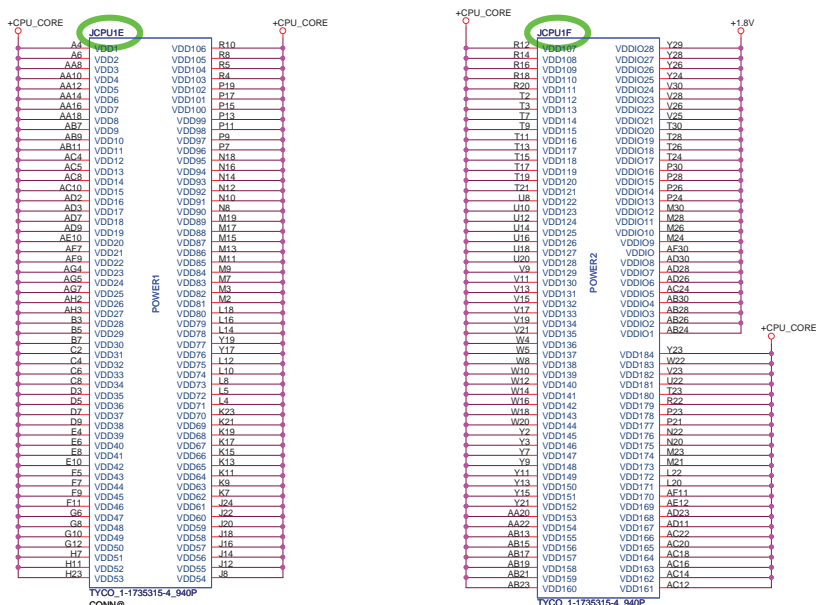
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ATHLON Control and Debug



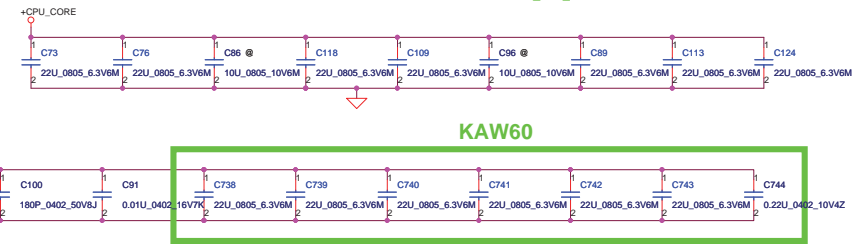
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	820u	560u	330u	22u	10u	.22u	.01u	180p
HCW51	2			4	12	2	1	1
Moray				15		4		1
KAW60		2	3	15		3	1	1



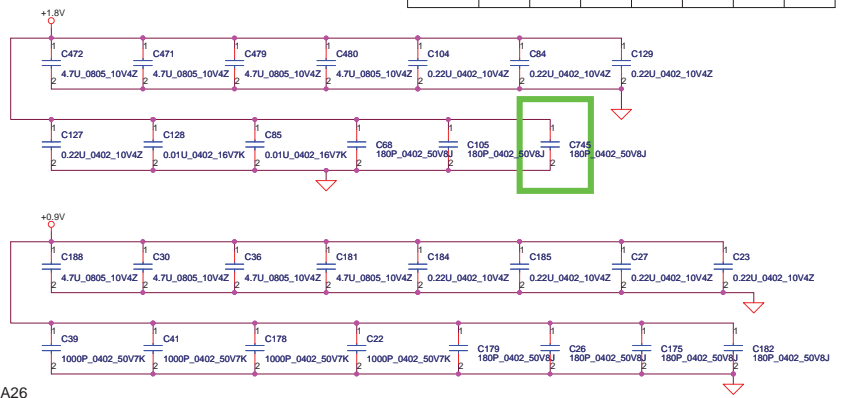
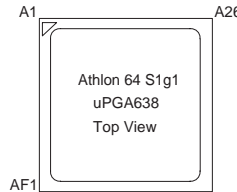
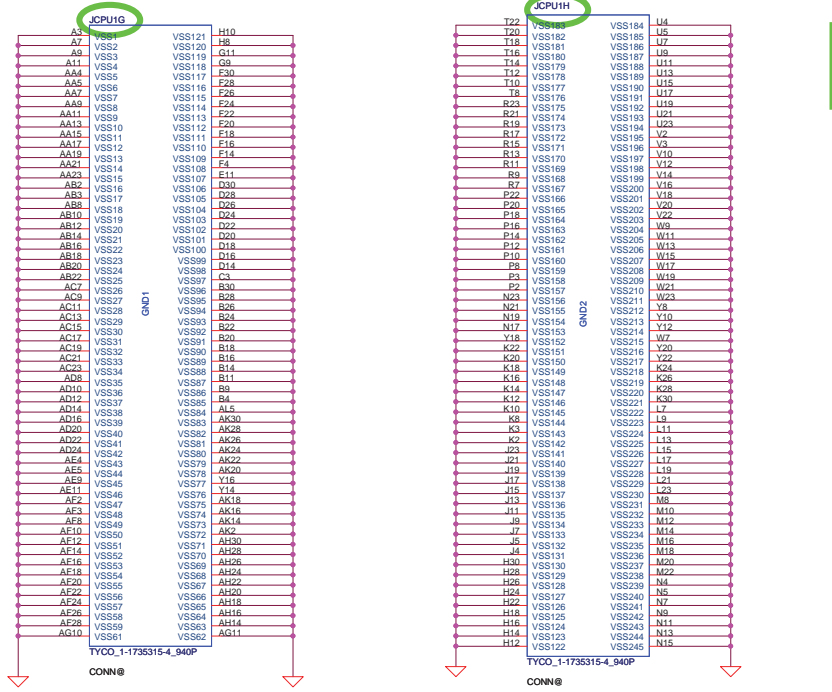
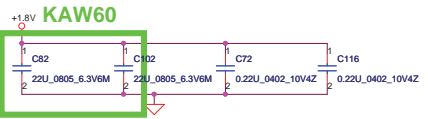
CPU SOCKET AM2 DECOUPLING

SMD POLY CAP
SF000001K00 S_A-P_CAP 560U 2.5V M 6.3X5.7 LESR10M H5.7
SF000003J00 S_A-P_CAP 560U 2.5V M 6.3X5.7 LESR13M H5.7



**DECOUPLING BETWEEN PROCESSOR AND DIMMS
PLACE CLOSE TO PROCESSOR AS POSSIBLE**

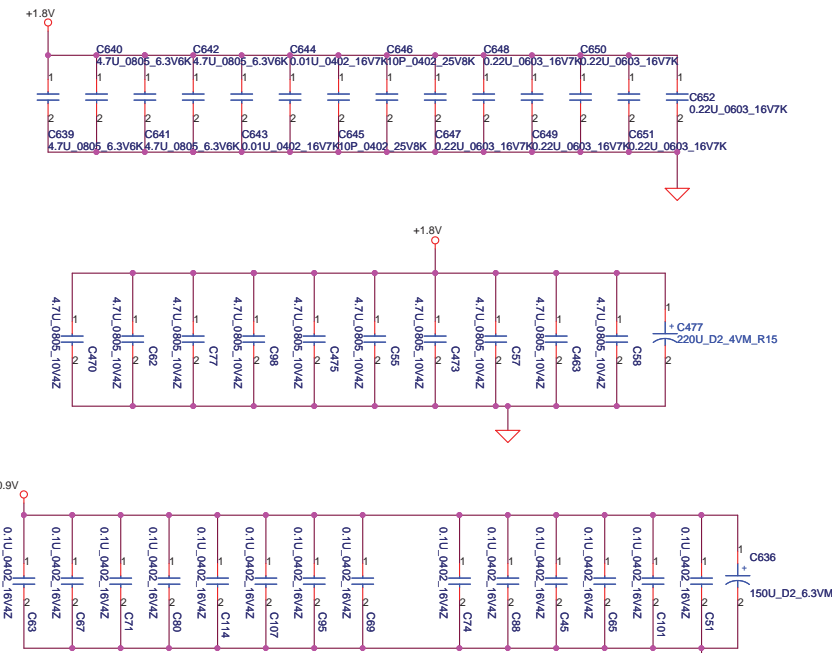
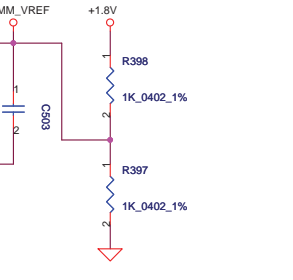
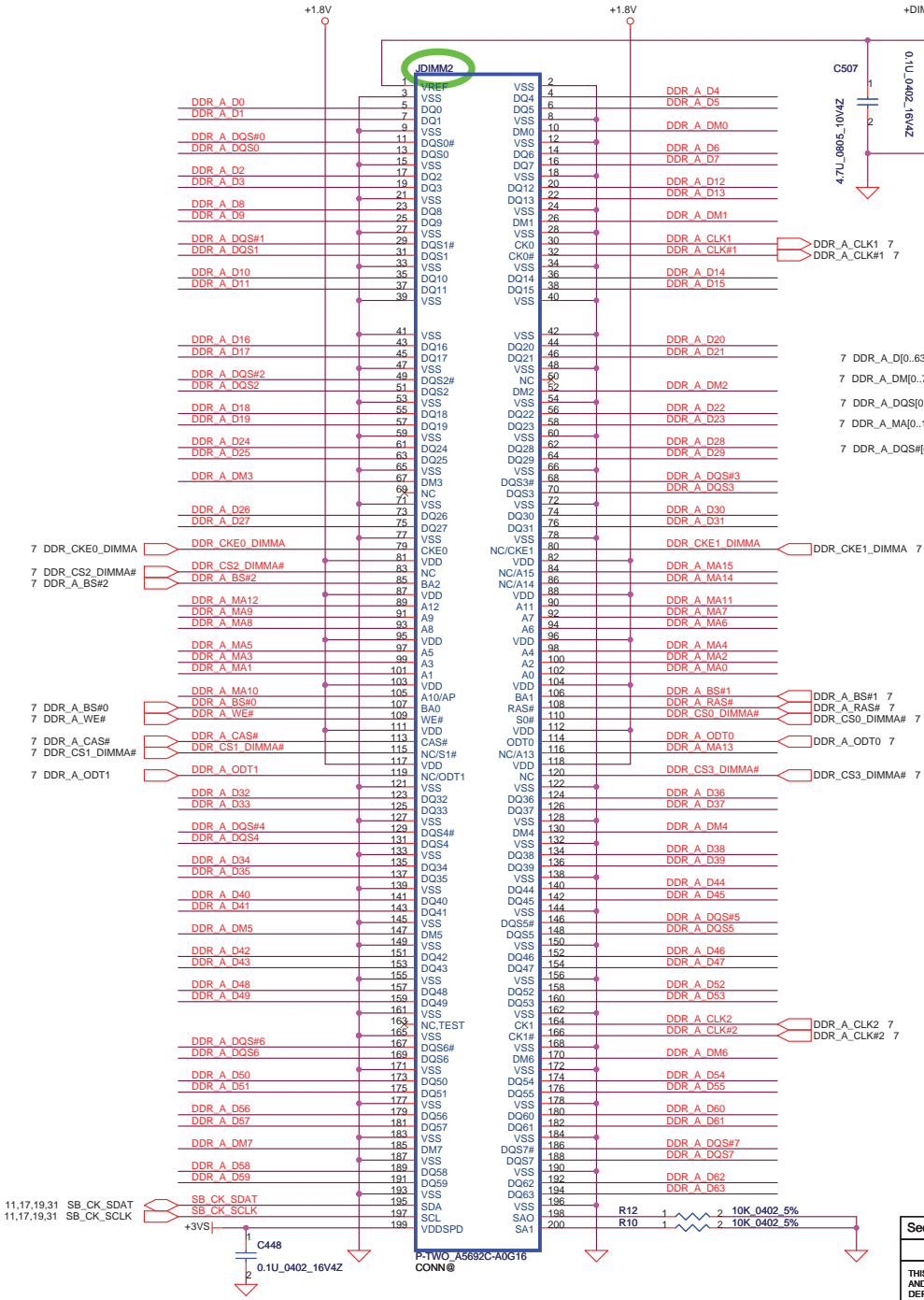
+1.8V	22u	10u	4.7u	.22u	.01u	180p	.0047u
HCW51		2	4	6	2	2	
Moray	2		2	5	1	3	2
KAW60			4	6	2	3	



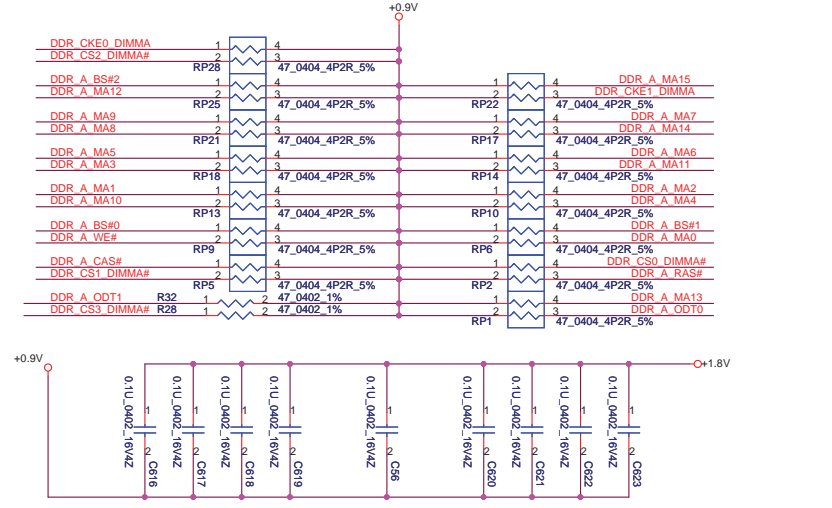
+0.9V	4.7u	.22u	.0047u	1000p	180p
HCW51	4	4		4	4
Moray	2	4	4	4	4
KAW60	4	4		4	4

PROCESSOR POWER AND GROUND

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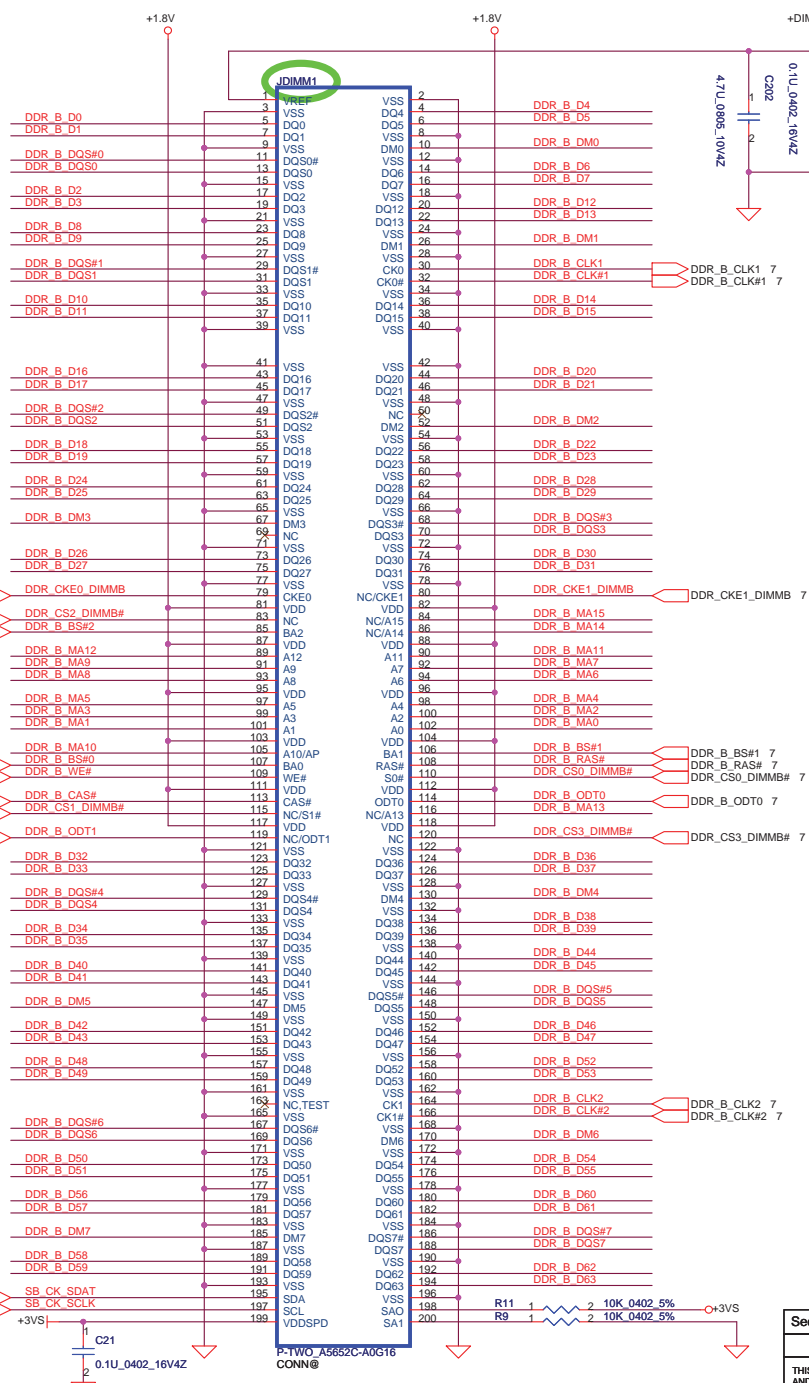


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

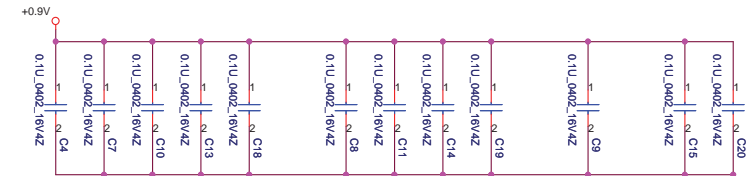
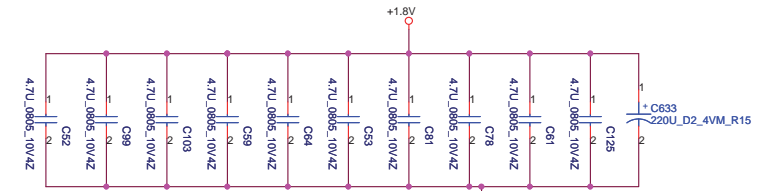


Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

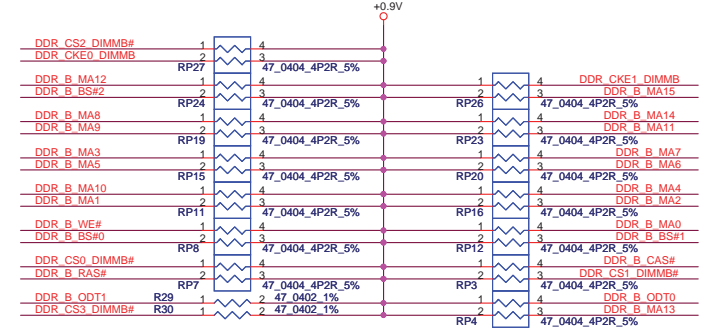
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- 7 DDR_B_D[0..63]
- 7 DDR_B_DM[0..7]
- 7 DDR_B_DQS[0..7]
- 7 DDR_B_MA[0..15]
- 7 DDR_B_DQS#[0..7]

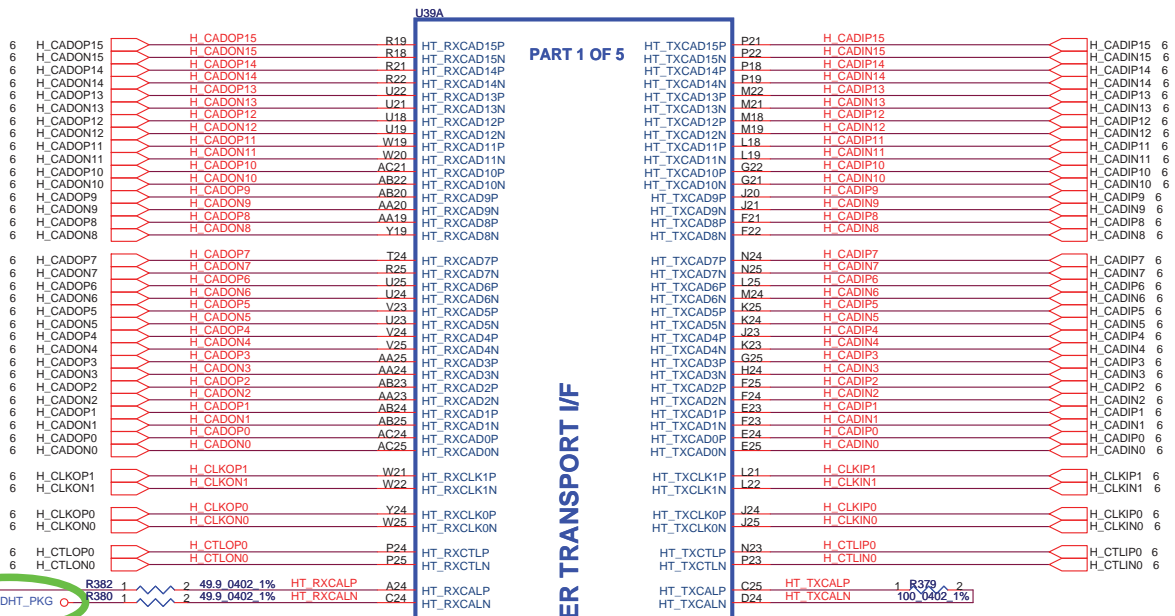


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

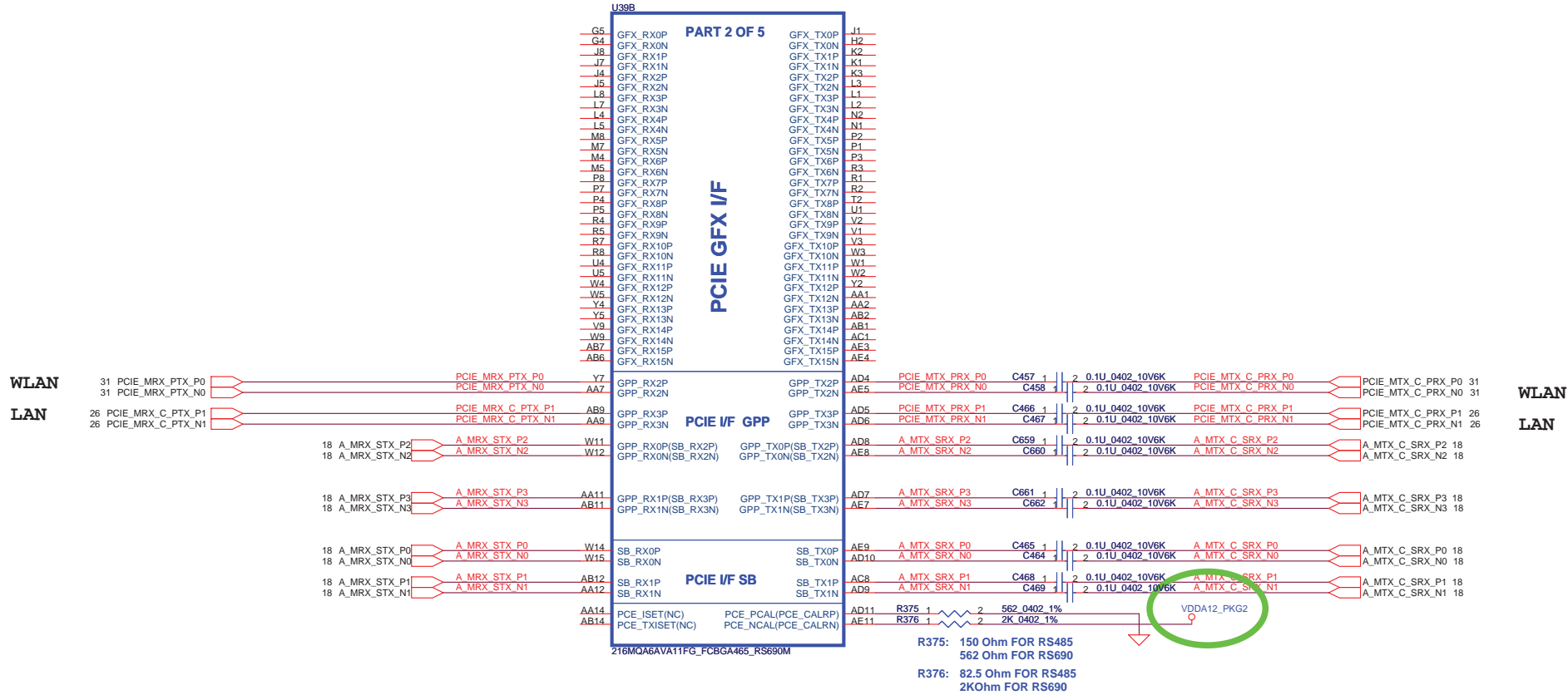
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216MQA6AVA11FG_FCBGA465_RS690M

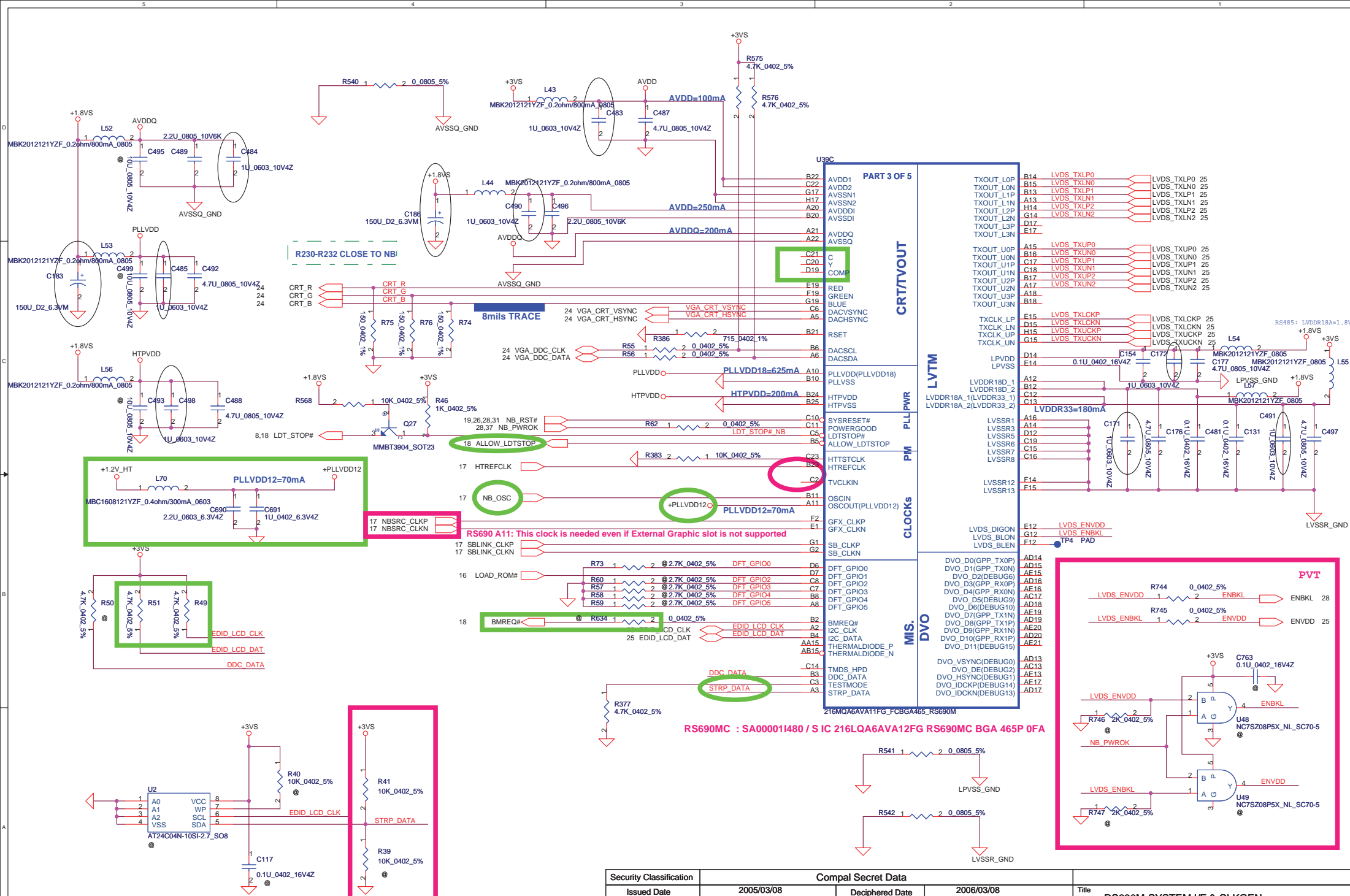
RS690MC : SA000011480 / S IC 216LQA6AVA12FG RS690MC BGA 465P 0FA

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RS690MC : SA00001I480 / S IC 216LQA6A12FG RS690MC BGA 465P 0FA

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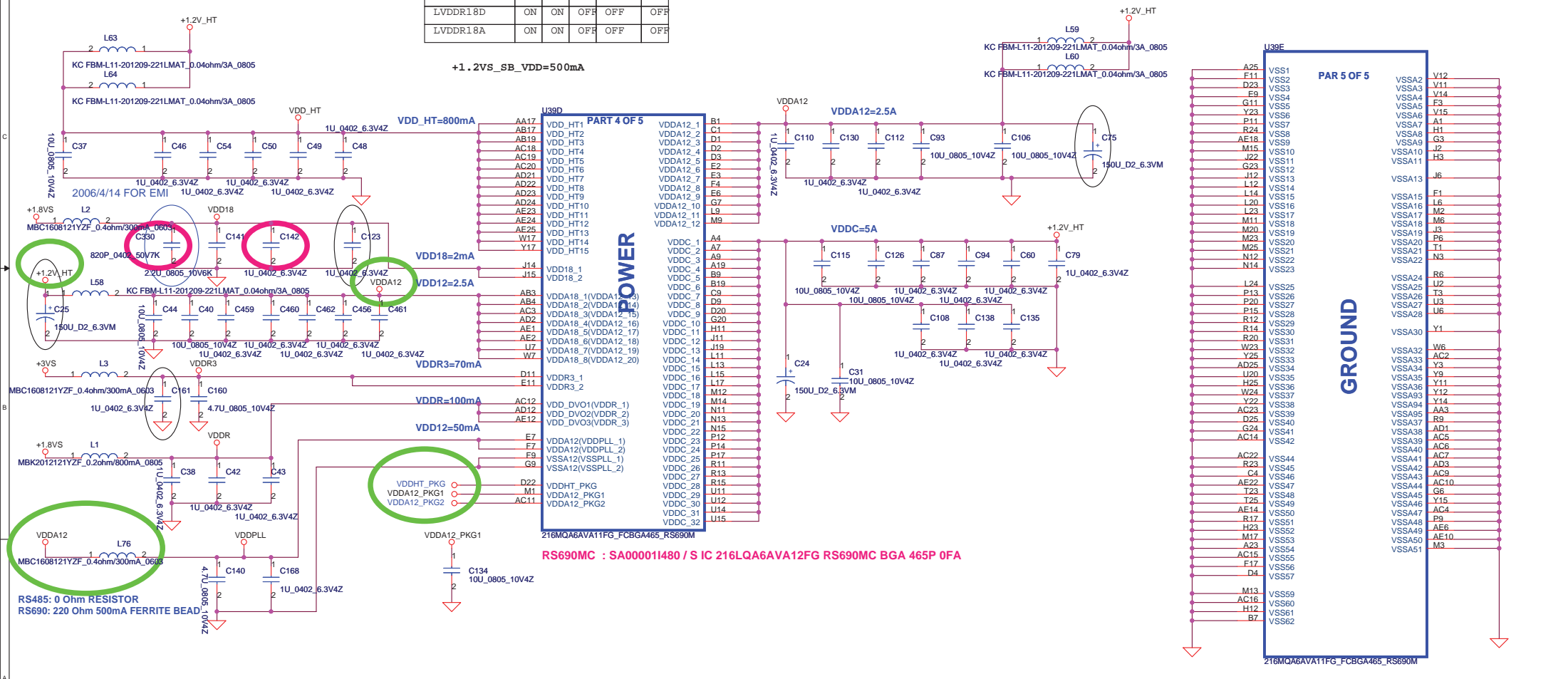
RS690MC : SA000011480 / I / SC I216LQA6AVA12FG RS690MC BGA 465P 0FA

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NOTE: ACCESS TO STRAP_DATA and I2C_CLK PINS IS MANDATORY.

NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

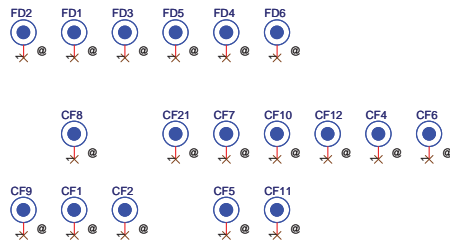
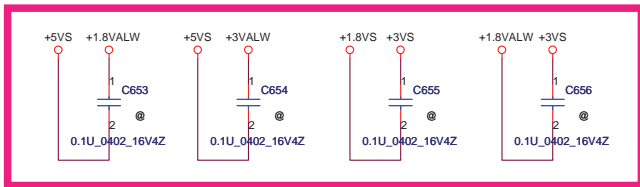


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Date:	Thursday, July 10, 2008	Sheet	15	of	50	

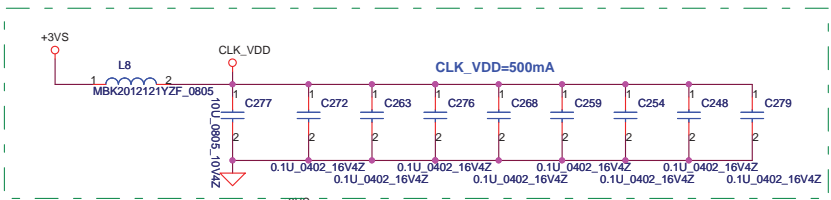


LOAD_ROM#: LOAD ROM STRAP ENABLE

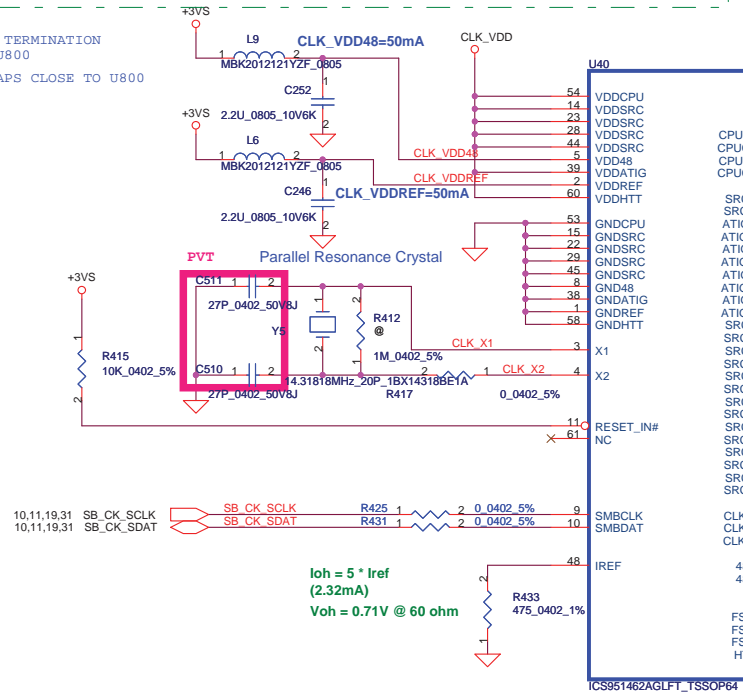
High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE



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				Date:	Friday, July 25, 2008
				Sheet	16 of 50
				Rev	2.0

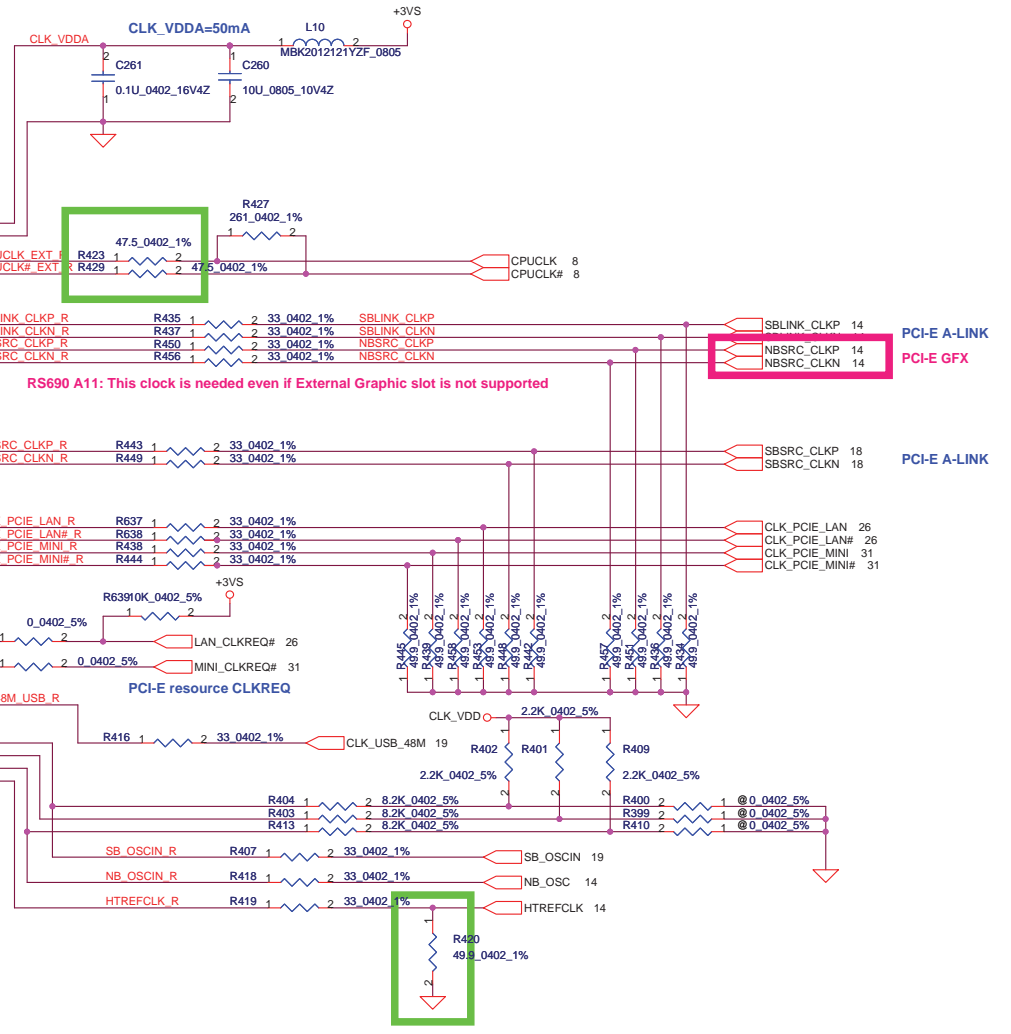


- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



$$I_{oh} = 5 * I_{ref} \text{ (2.32mA)}$$

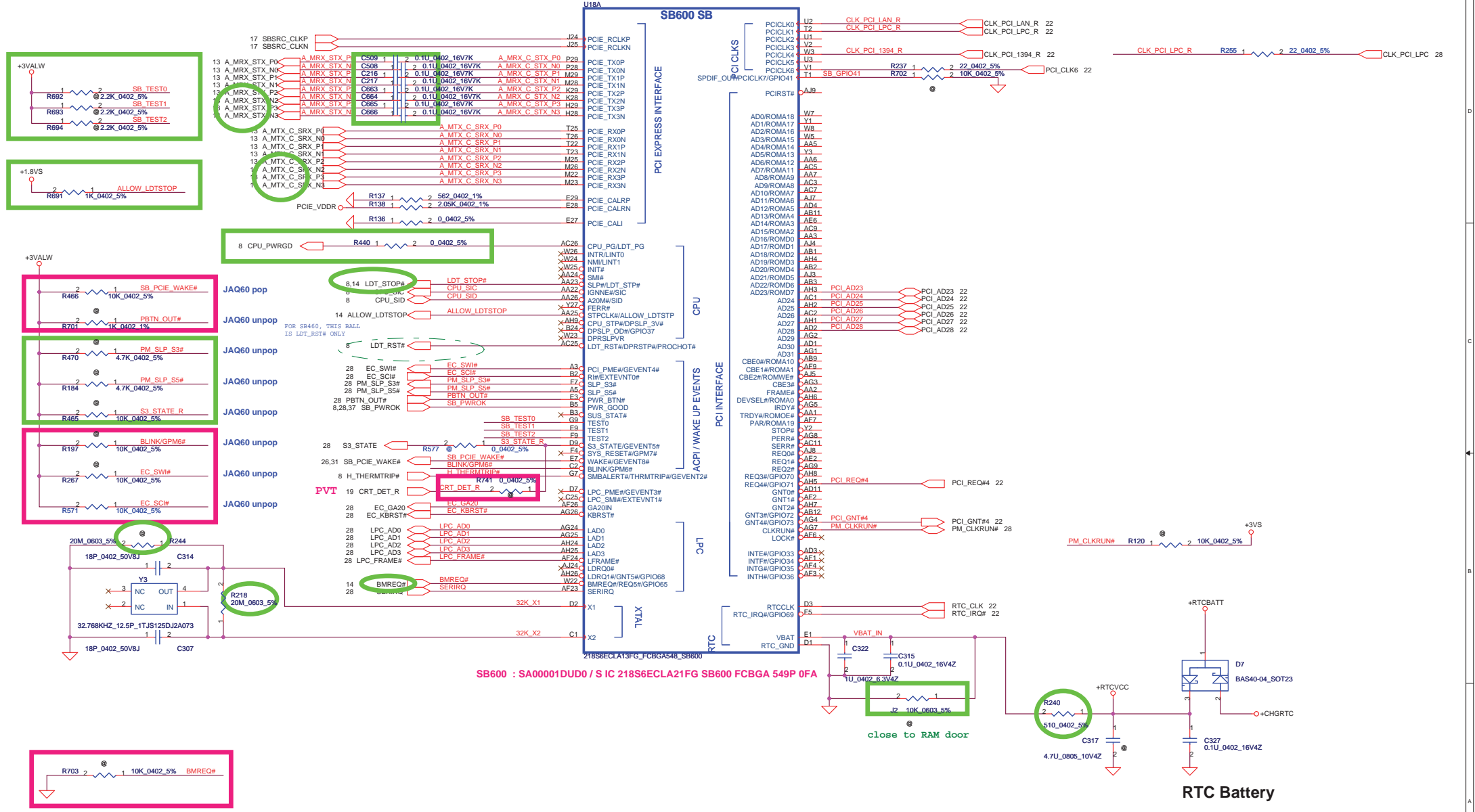
$$V_{oh} = 0.71V @ 60 \text{ ohm}$$



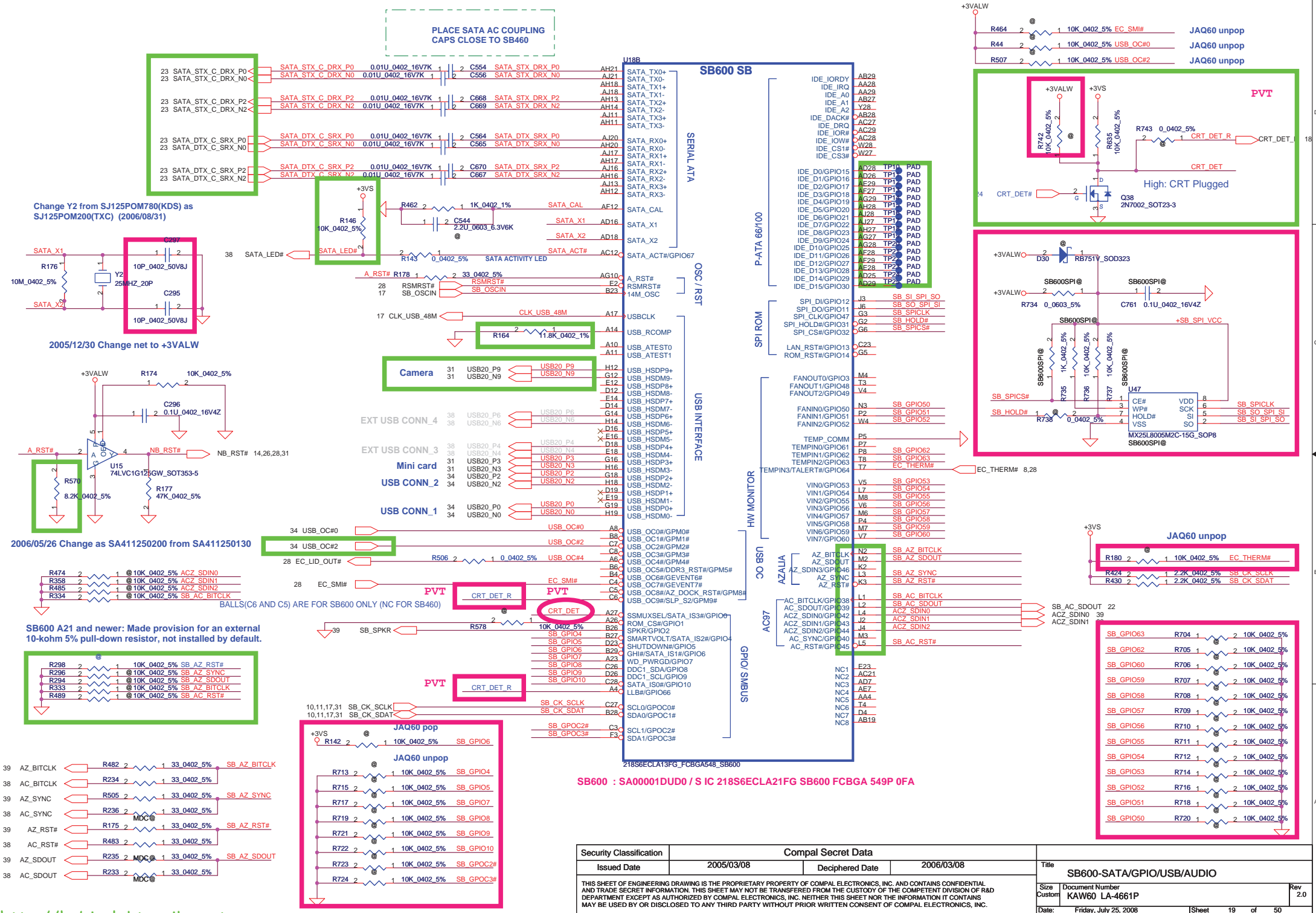
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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Date:	Friday, July 25, 2008	Sheet	17	of	50	

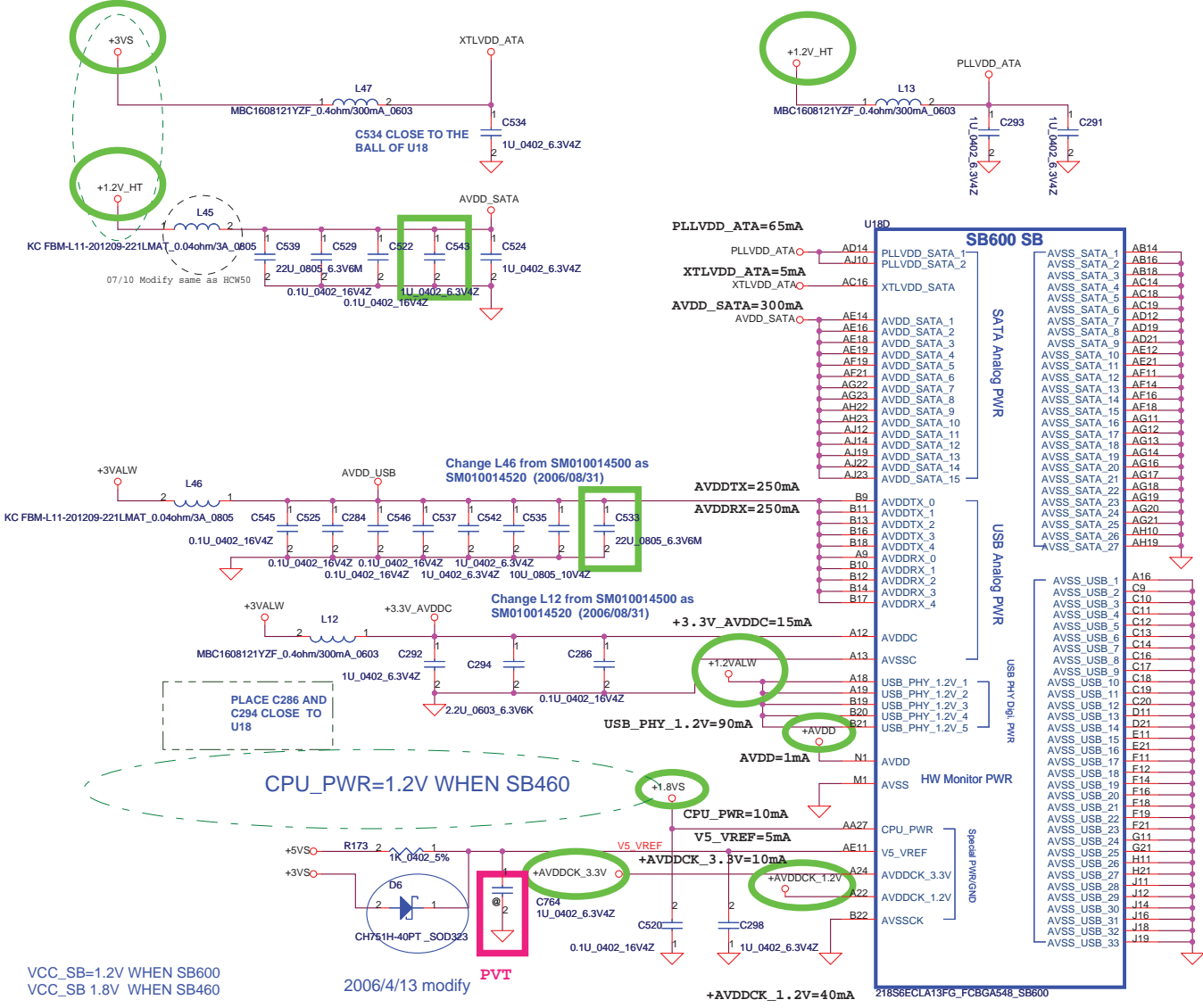


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SB600 : SA00001DUD0 / S IC 21856ECLA21FG SB600 FCBGA 549P 0FA

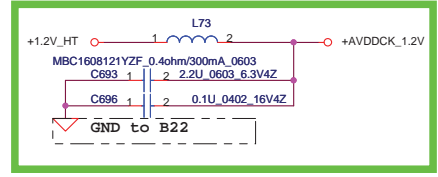
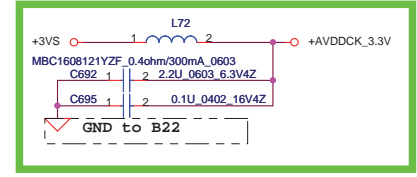
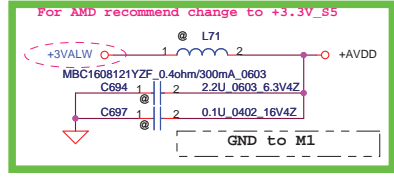
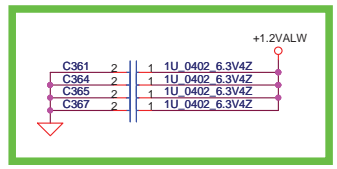
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Issued Date	2005/03/08	Deciphered Date	2006/03/08	SB600-SATA/GPIO/USB/AUDIO	
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VCC_SB=1.2V WHEN SB600
VCC_SB 1.8V WHEN SB460

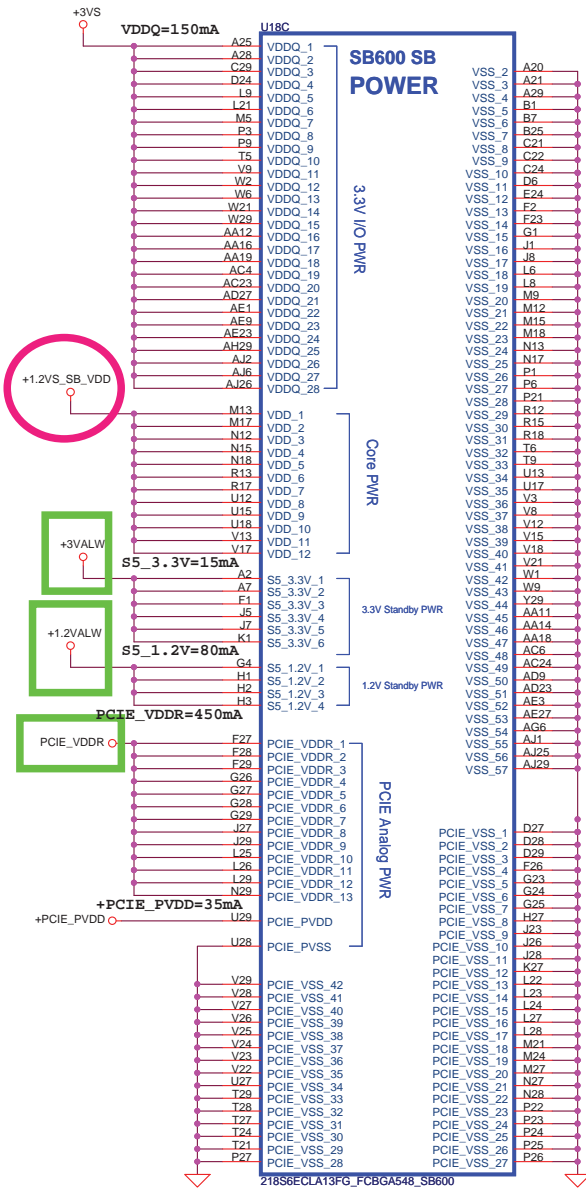
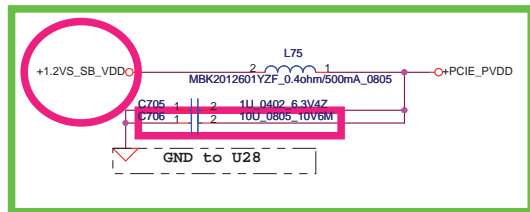
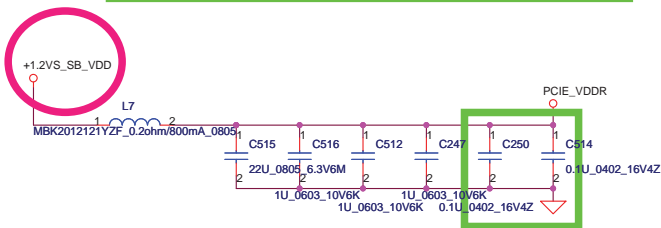
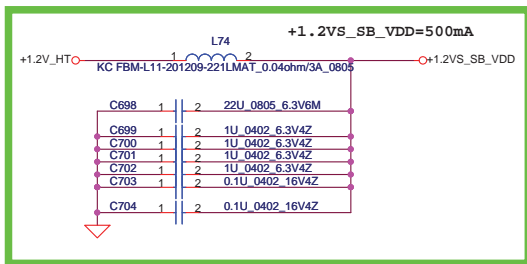
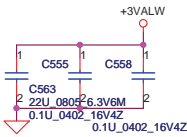
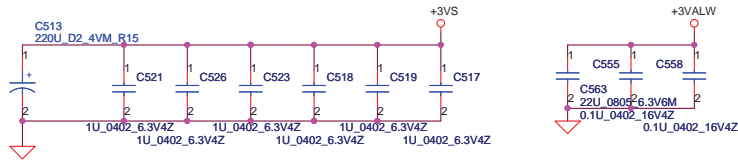
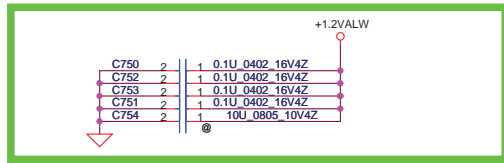
PLACE SATA_CAL RES & CAP VERY CLOSE TO BALL OF U18

NOTE:
R462 IS 1K 1% FOR 25MHZ
XTAL, 4.99K 1% FOR 100MHZ
INTERNAL CLOCK



SB600 : SA00001DUD0 / S IC 218S6ECLA21FG SB600 FCBGA 549P 0FA

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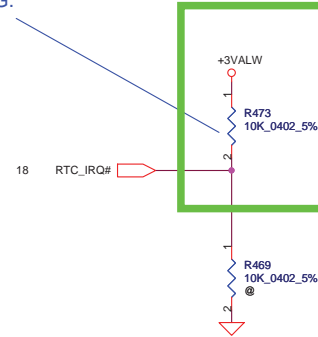
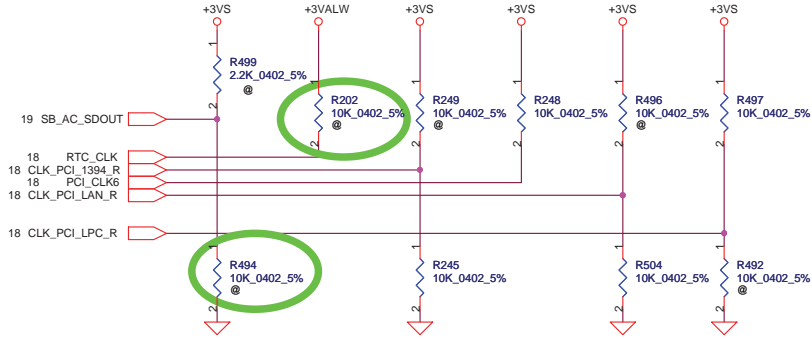
SB600 : SA00001DUD0 / S IC 218S6ECLA21FG SB600 FCBGA 549P 0FA

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REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT, 15K PU FOR RTC_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED

NOTE: R473 PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB600 TO KEEP THE INPUT FROM FLOATING.



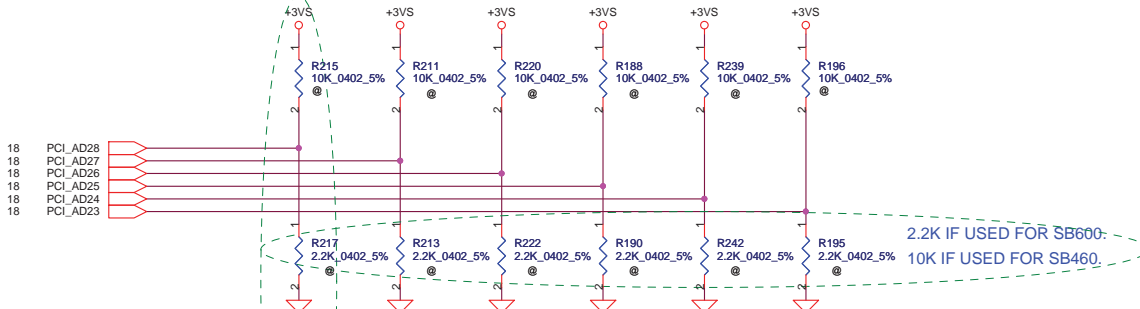
SB460 ONLY

PULL HIGH	AC_SDOUT	RTC_CLK	PCI_1394_R	PCI_CLK6	SB600		SB460	
					PCI_LAN_R	PCI_LPC_R	PCI_LAN_R	PCI_LPC_R
USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM			
IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4					

	ACPWON	SPDIF_OUT	PCI_MINI_R	PCI_PCM_R	PCI_SIO_R	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

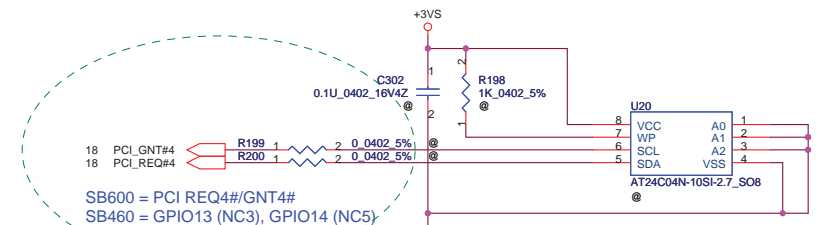


	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

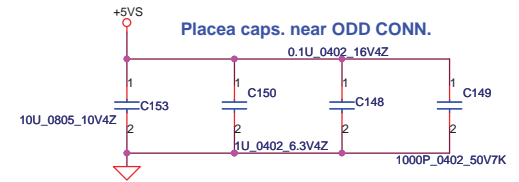
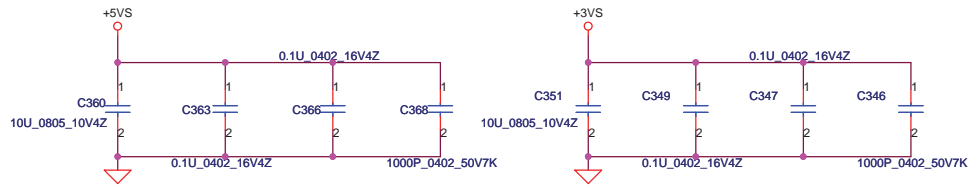


SB PCIE EEPROM STRAPS

SB460 ONLY

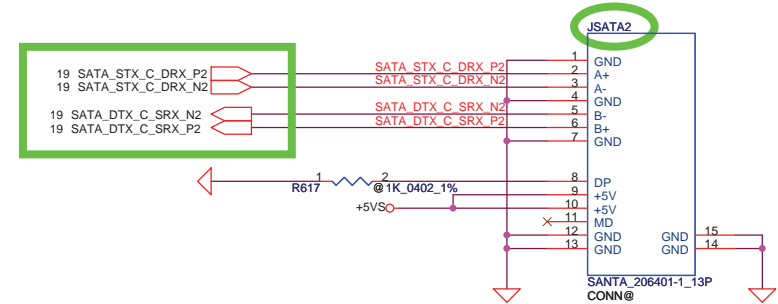
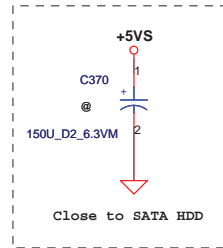
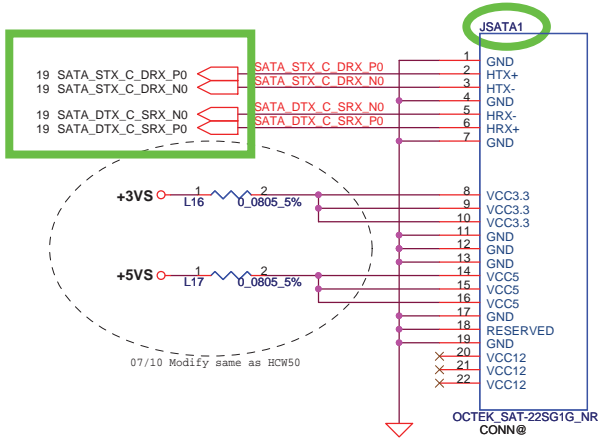
SB600 ONLY

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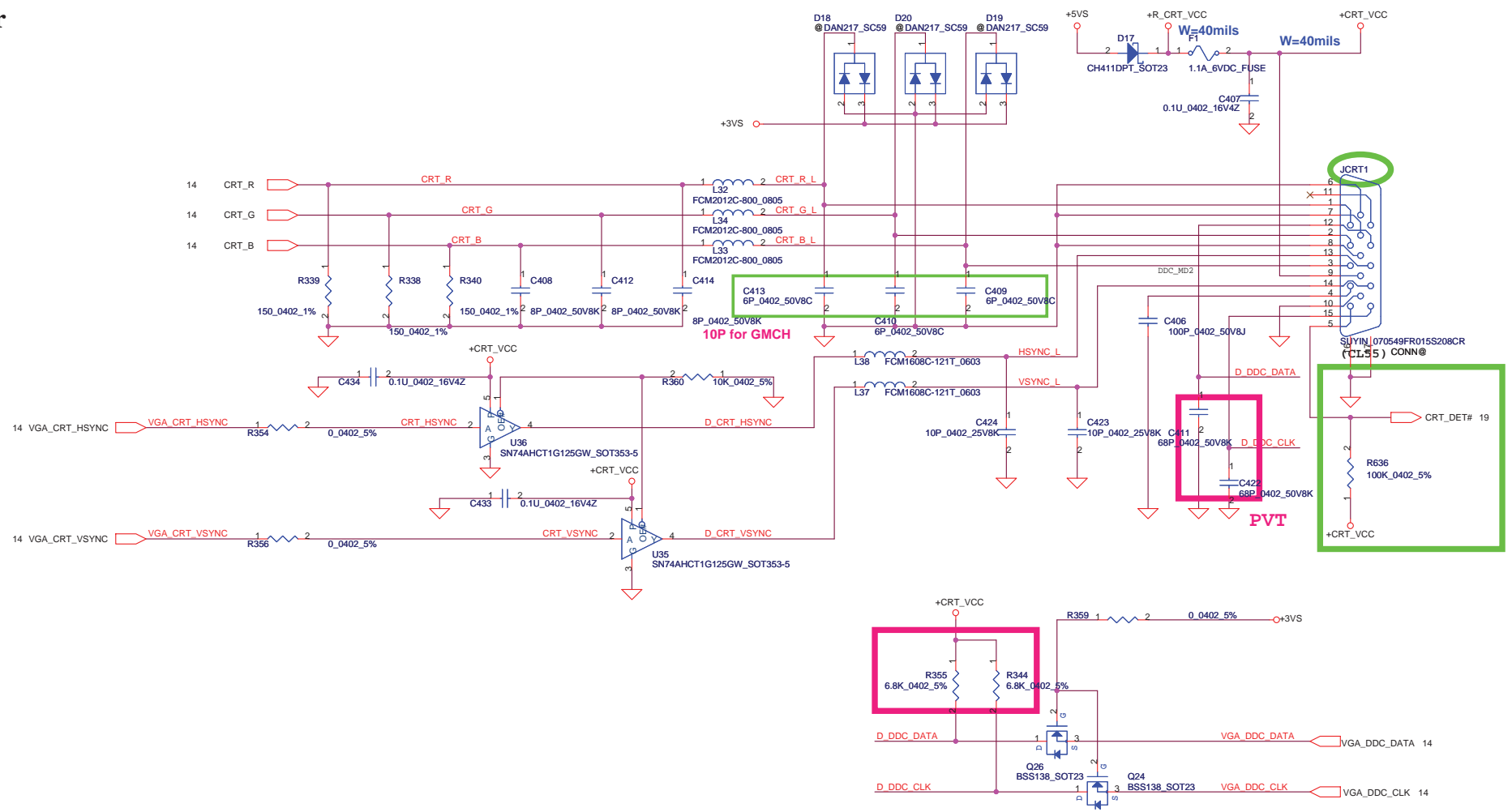
SATA HDD CONN

SATA ODD CONN



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				B	2.0
				Date:	Sheet
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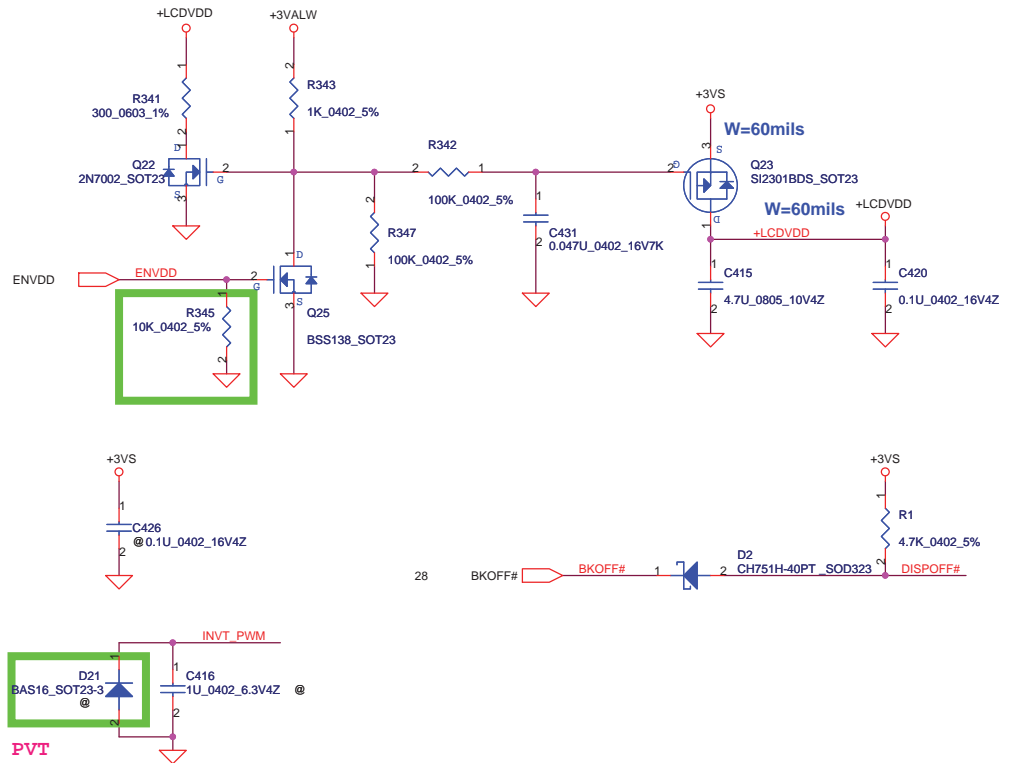
CRT Connector



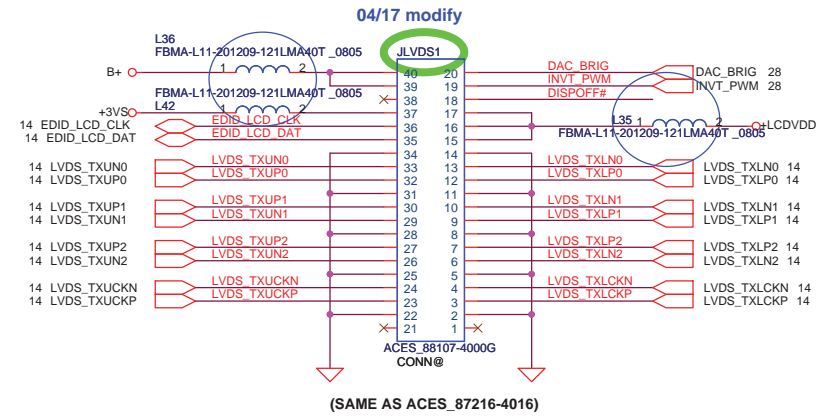
<http://hobi-elektronika.net>

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Date:	Tuesday, July 29, 2008	Sheet	24	of 50
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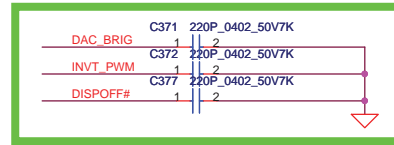
LCD POWER CIRCUIT



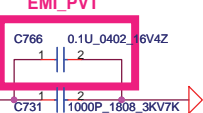
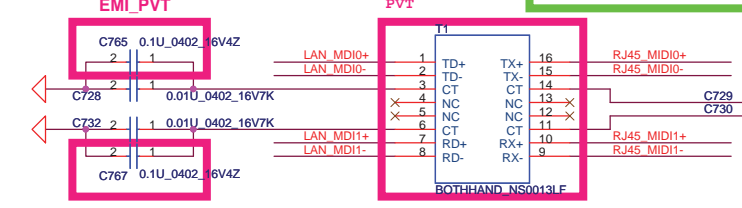
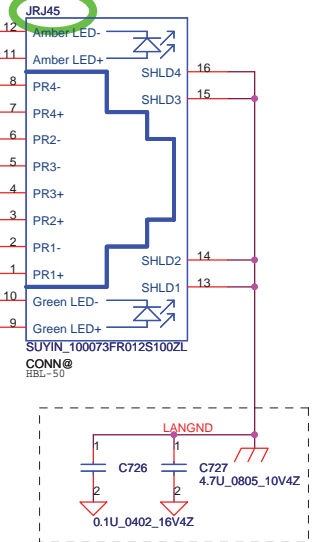
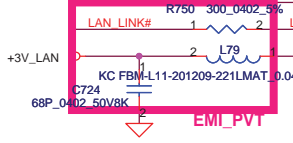
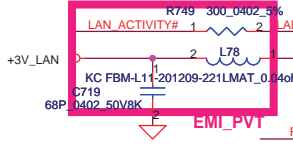
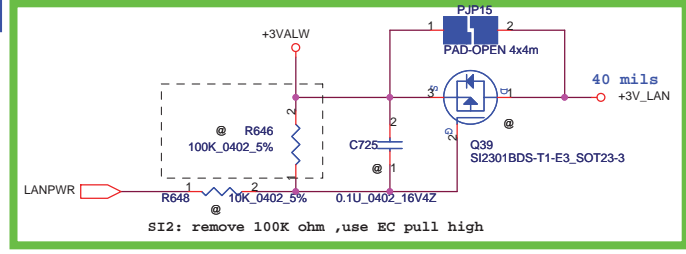
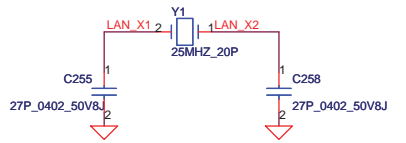
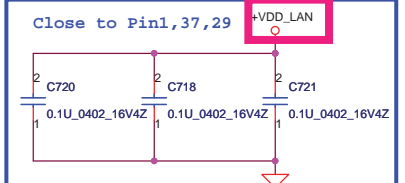
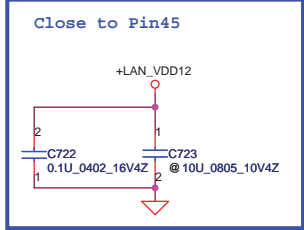
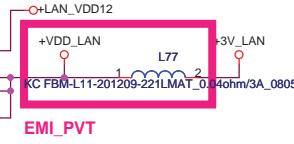
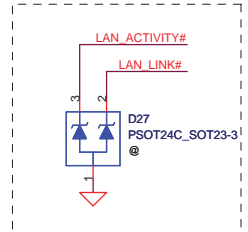
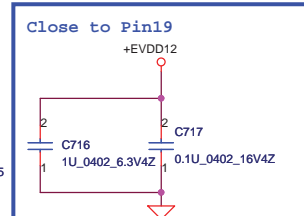
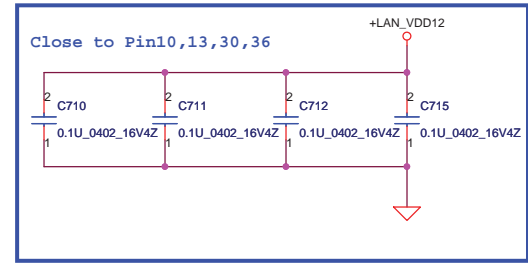
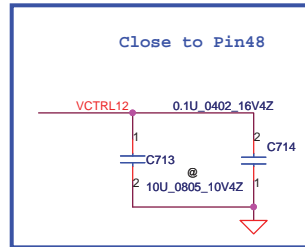
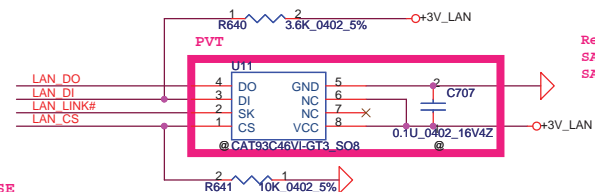
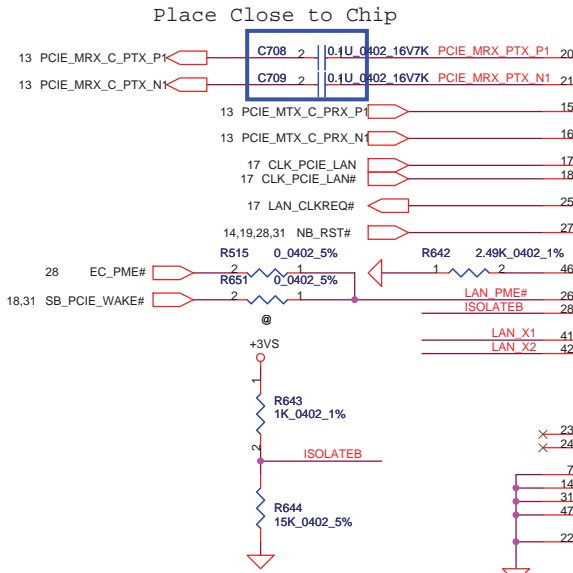
LCD/PANEL CONN.



EMI



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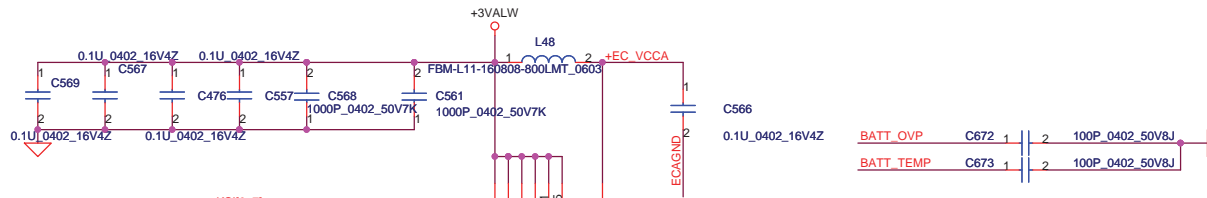


SP050003N00 S X'FORM_NS681680 LAN (MHPC , Not for ABO)
 SP050001210 S X'FORM_NS0013LF LAN (BOTHHAND)
 SP050001310 S X'FORM_LF-H80P-1 COUPLING (lankom)
 SP050004L00 S X'FORM_LD-024A 10/100 PC CARD LAN (TAIMAG)

<http://hobi-elektronika.net>

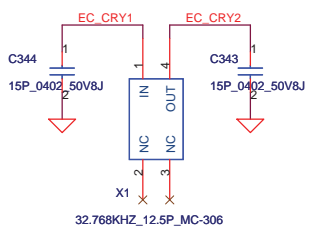
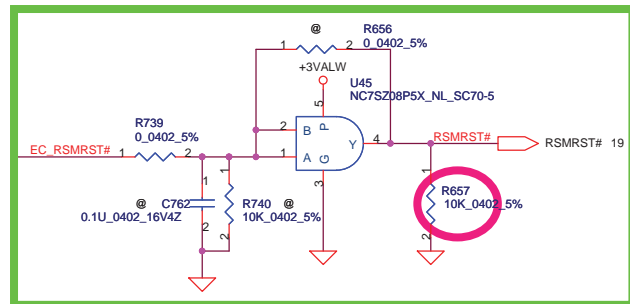
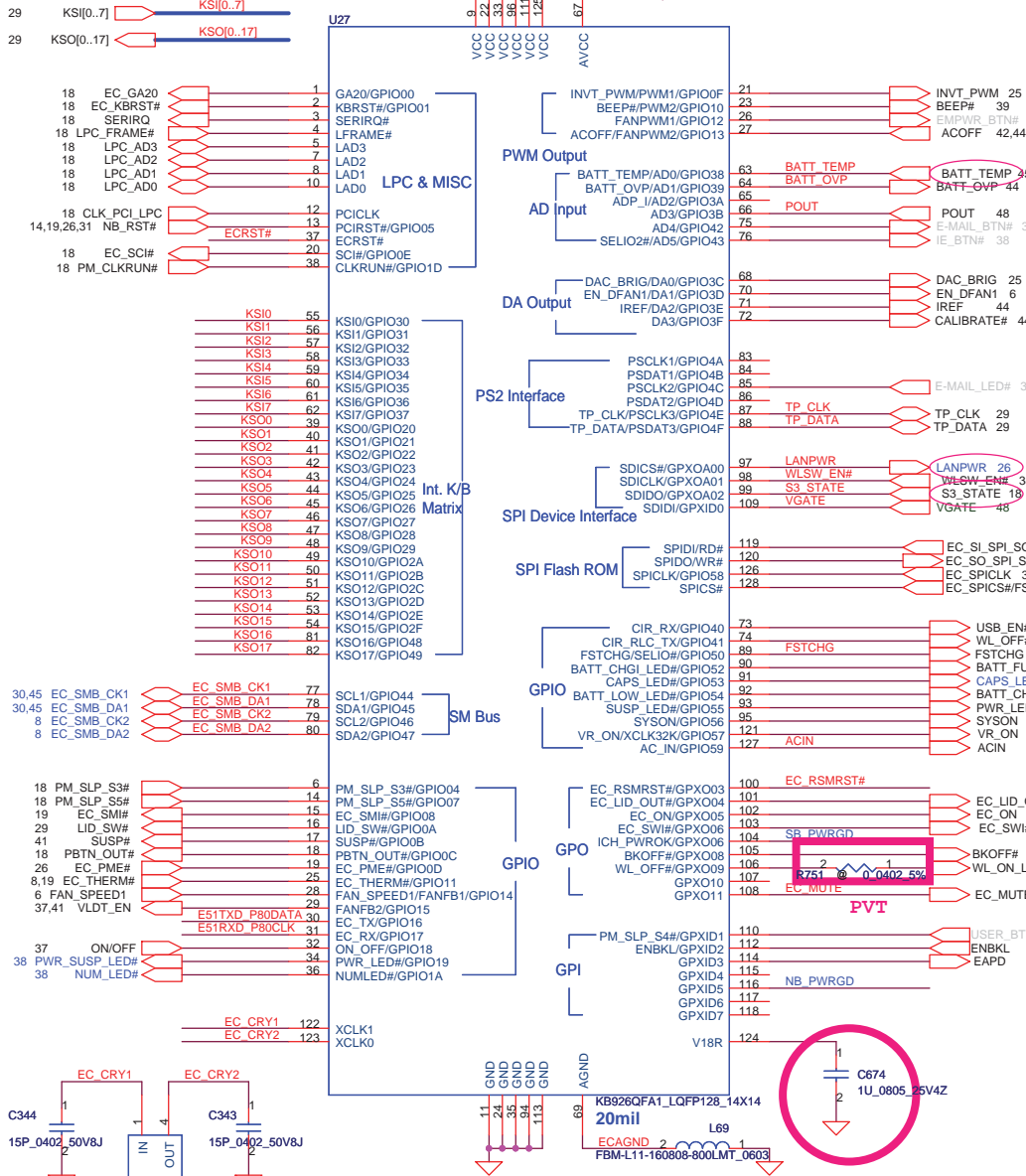
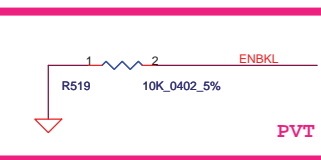
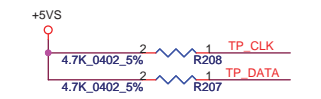
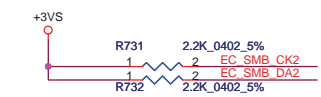
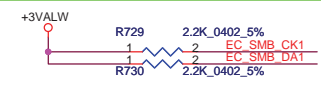
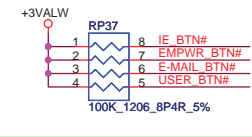
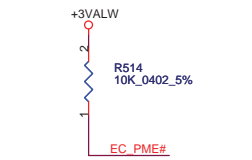
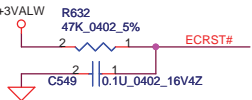
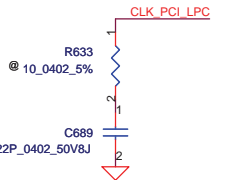
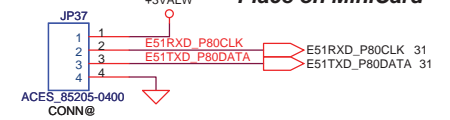
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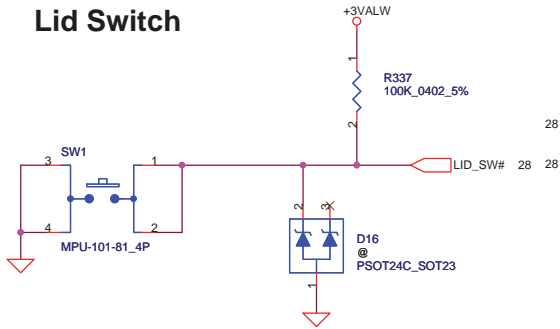
For EC Tools

Place on MiniCard

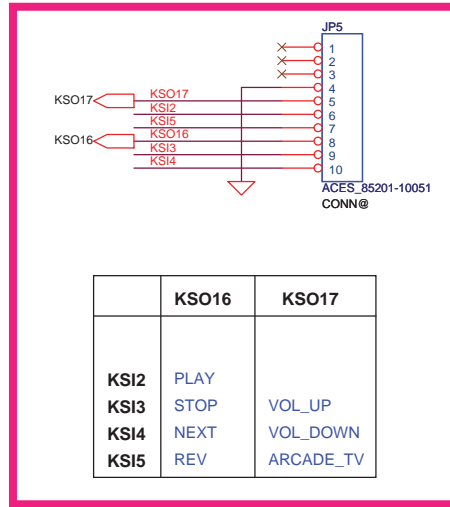


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Customer	KAW60 LA-4661P		Document Number	0.2	
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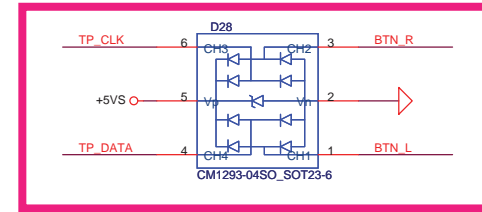
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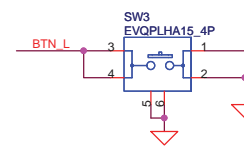
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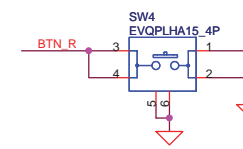
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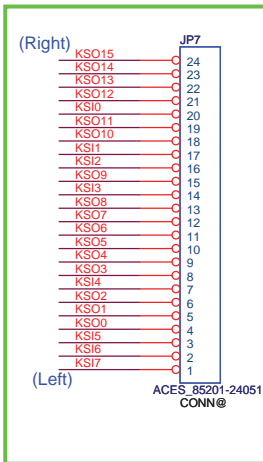
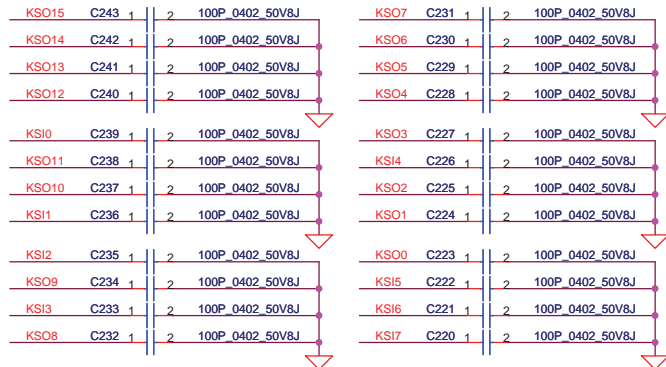
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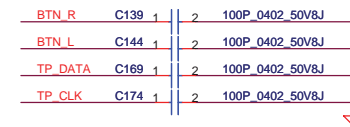
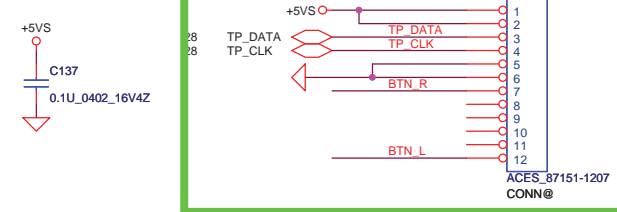
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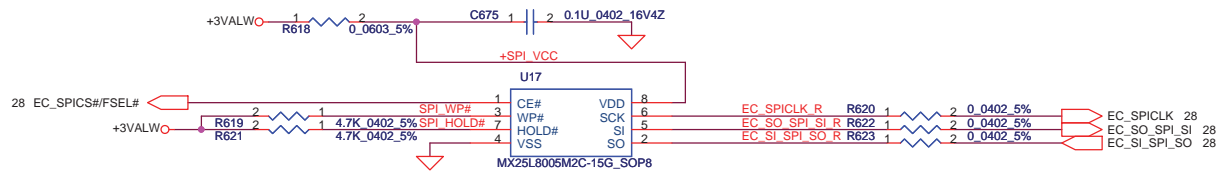
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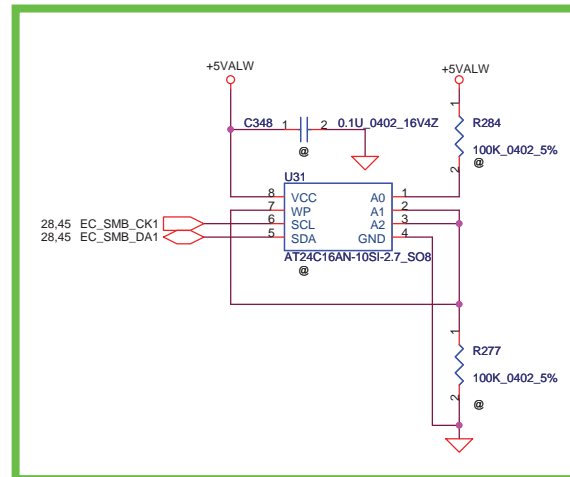
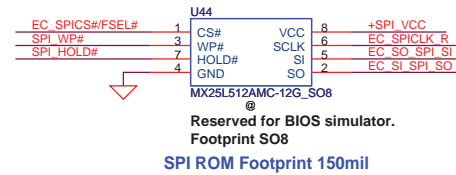
To TP/B Conn.



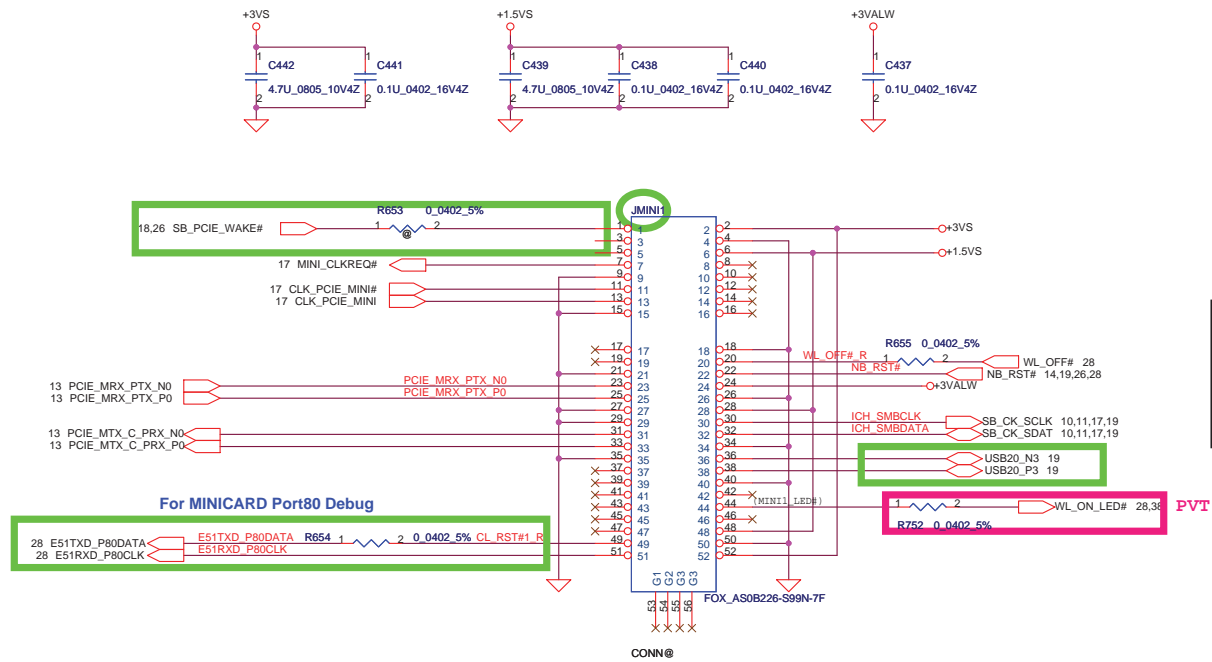
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SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

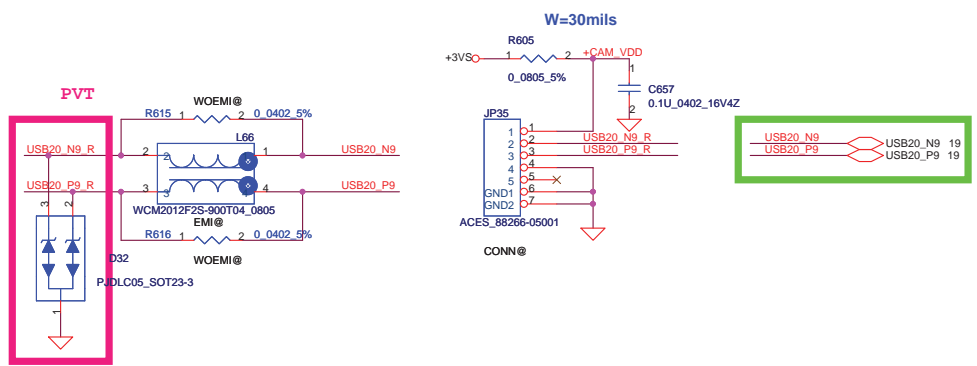


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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	Normal
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Camera



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		2006/06/20

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Compal Electronics, Inc.			
Title			
MINI Card & Camera			
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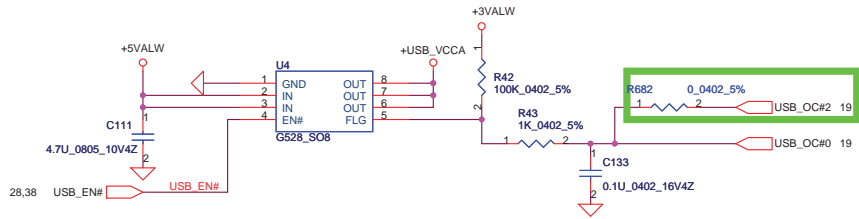
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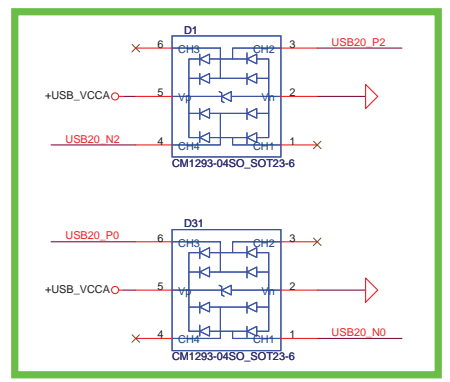
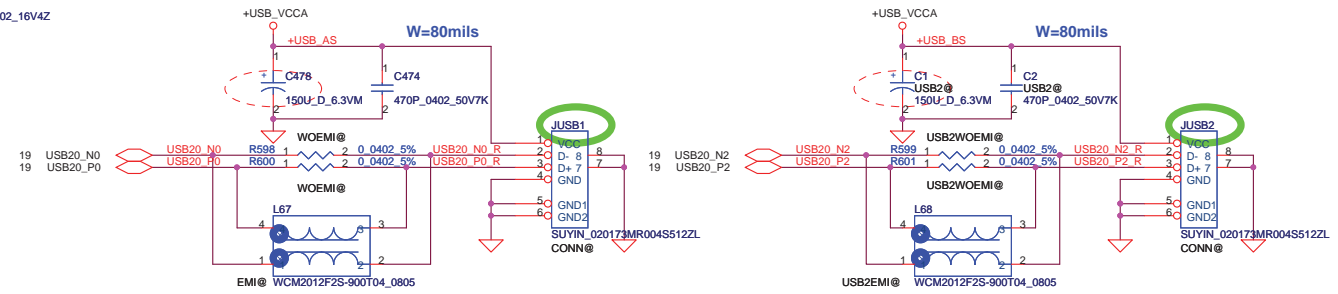
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USB CONN. 1 & 2



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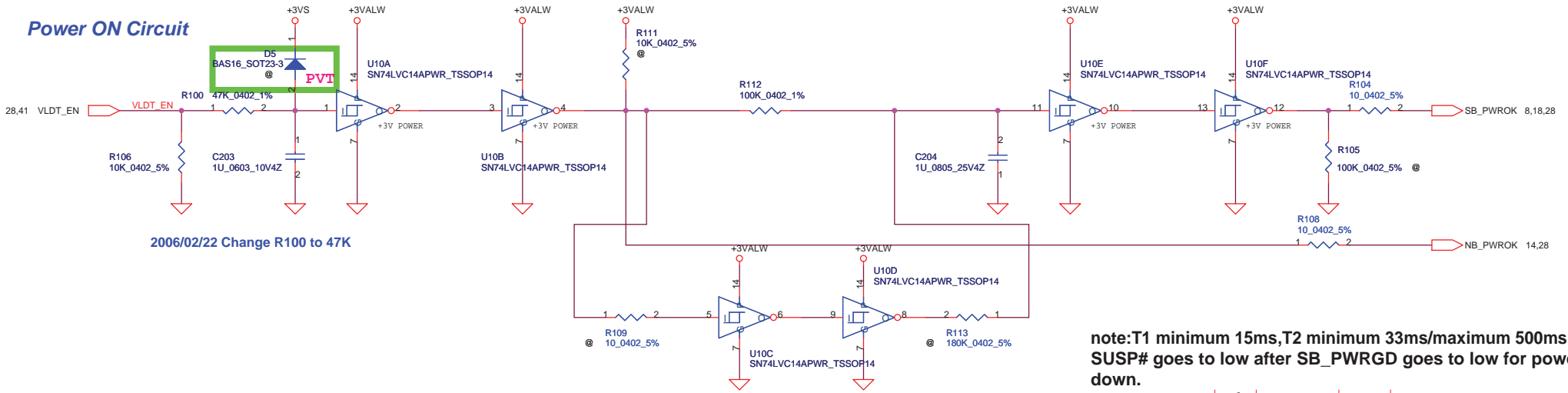
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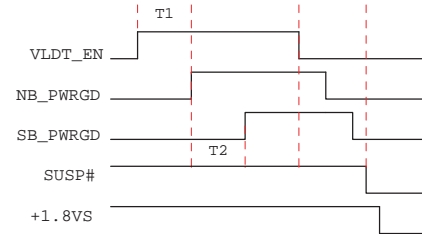
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Power ON Circuit

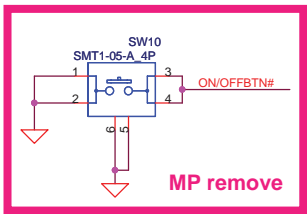
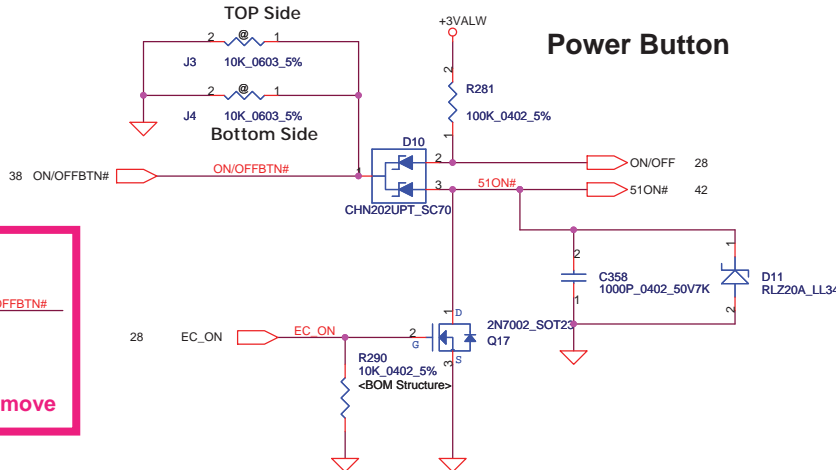


2006/02/22 Change R100 to 47K

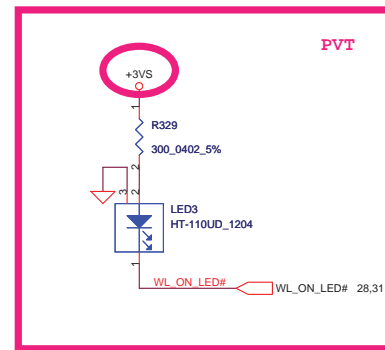
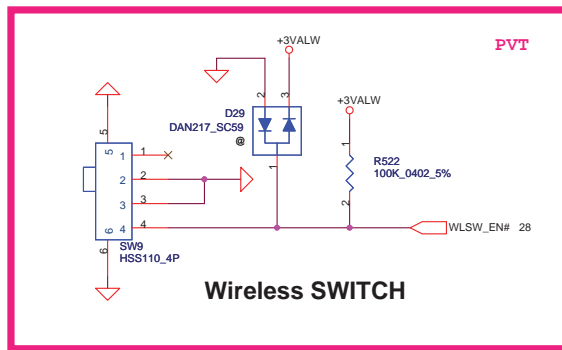
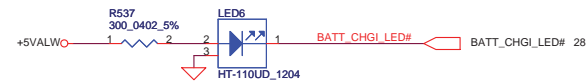
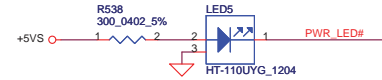
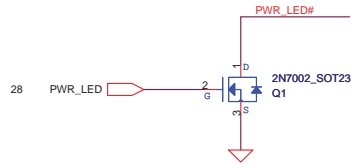
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power down.



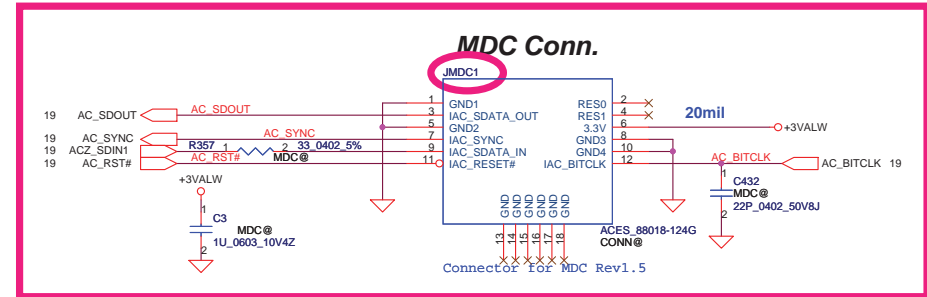
Power Button



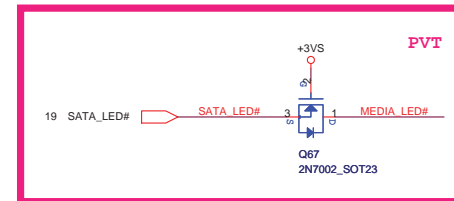
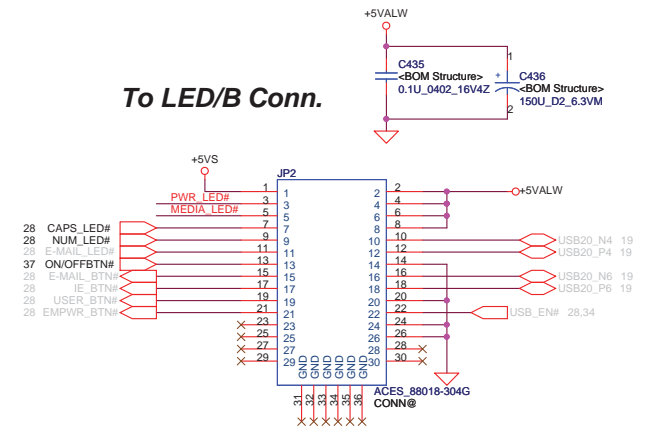
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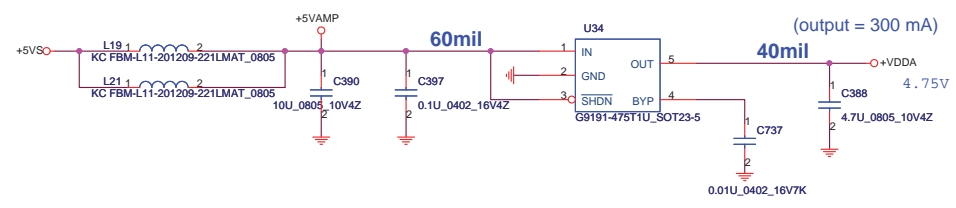
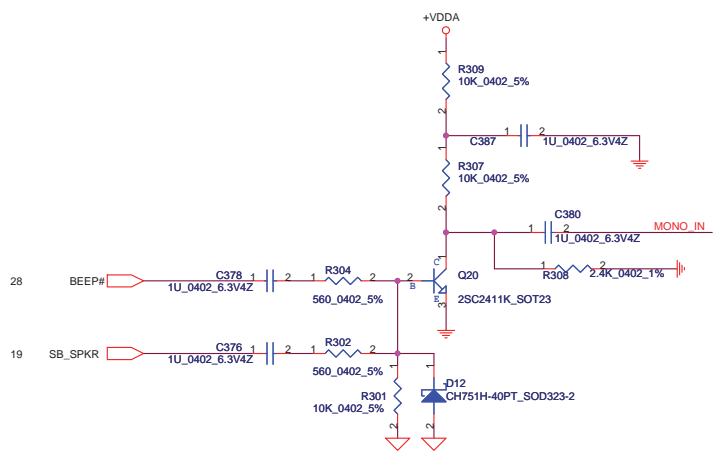
W/O Modem



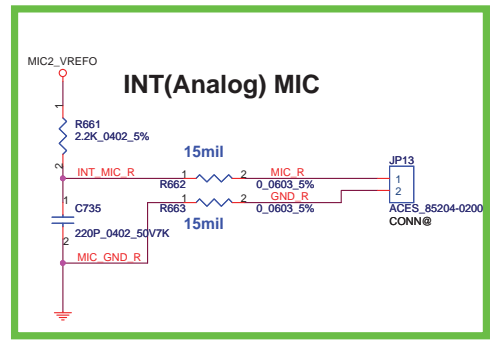
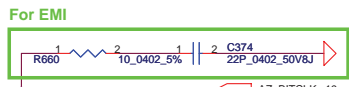
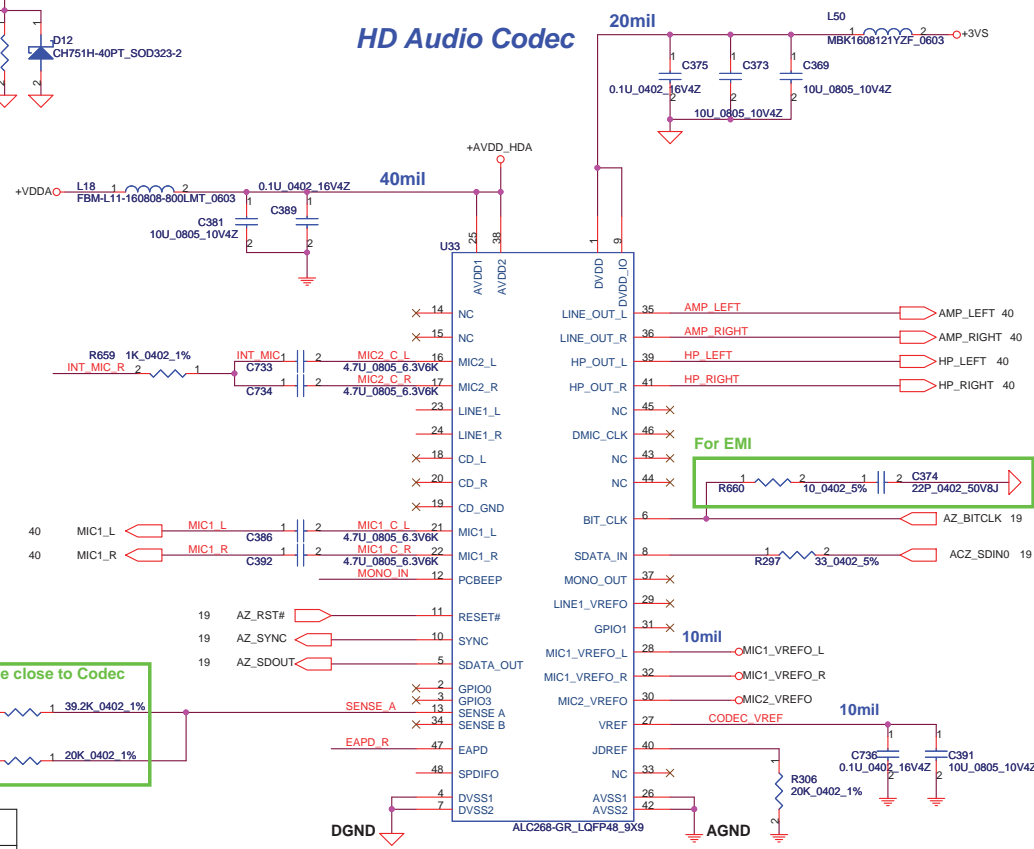
To LED/B Conn.



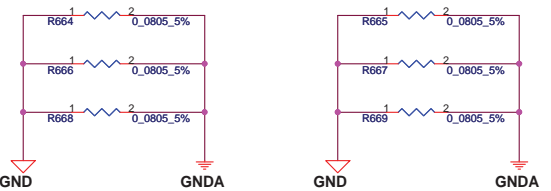
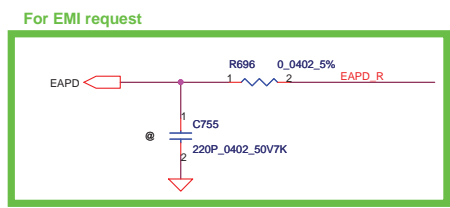
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HD Audio Codec

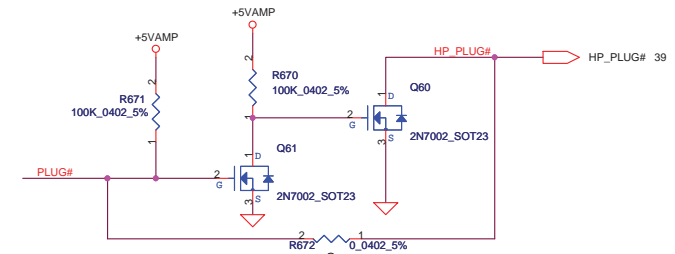
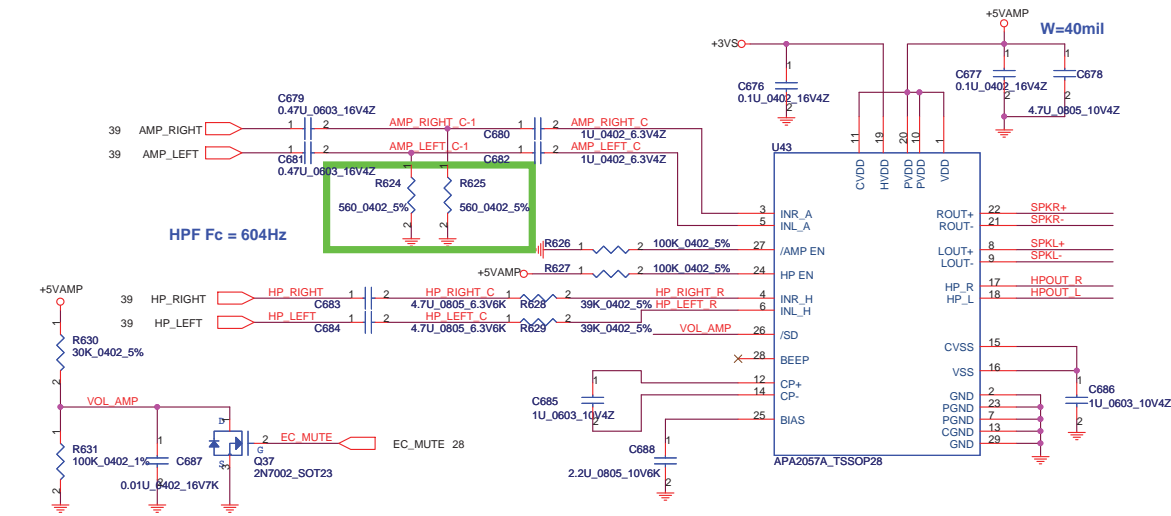


Place close to Codec

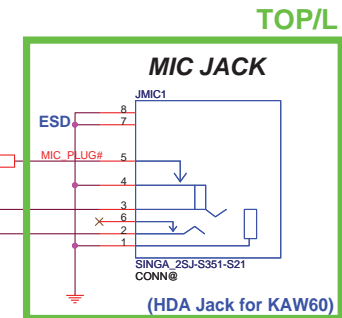
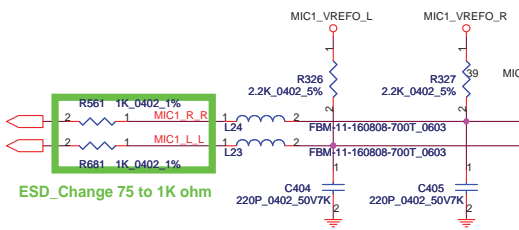
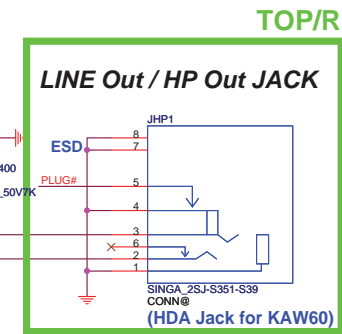
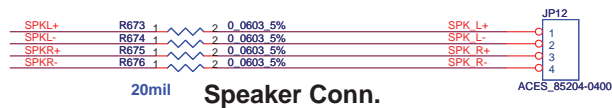


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

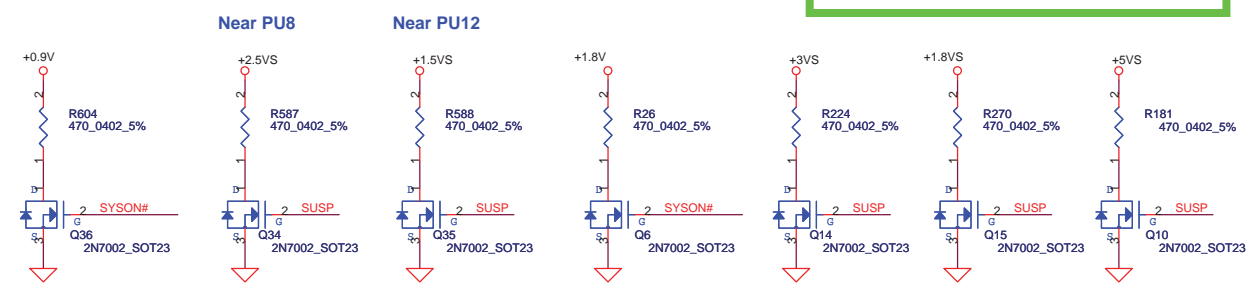
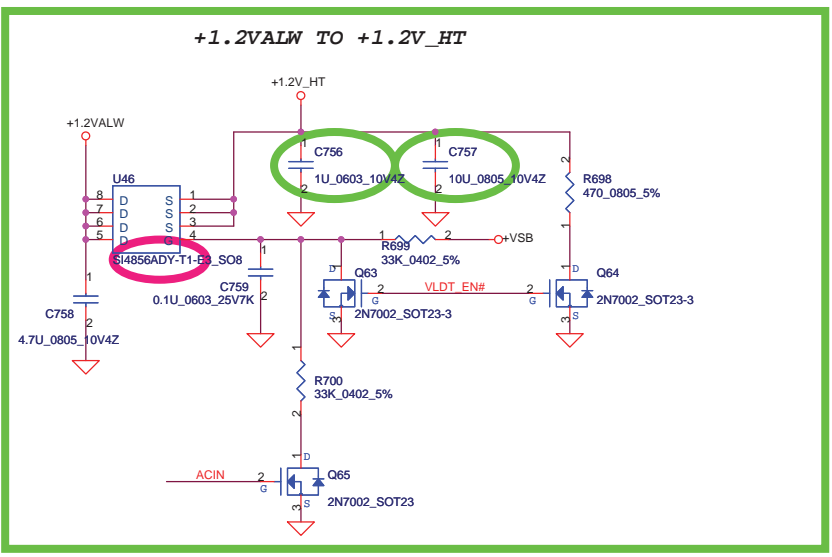
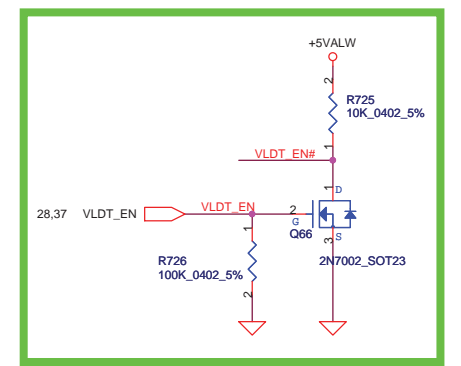
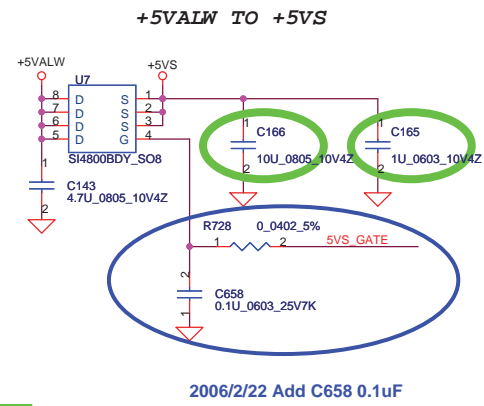
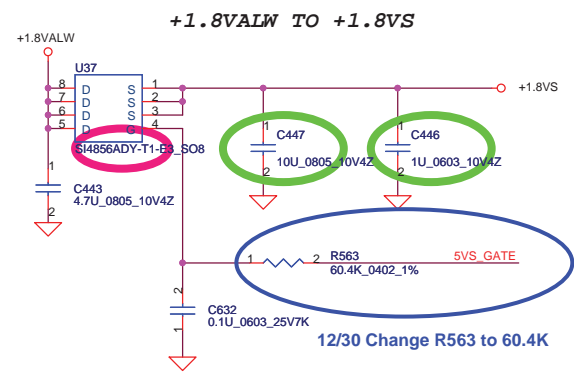
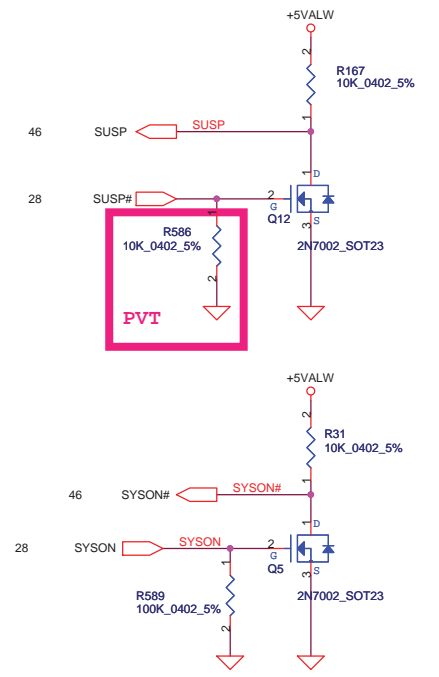
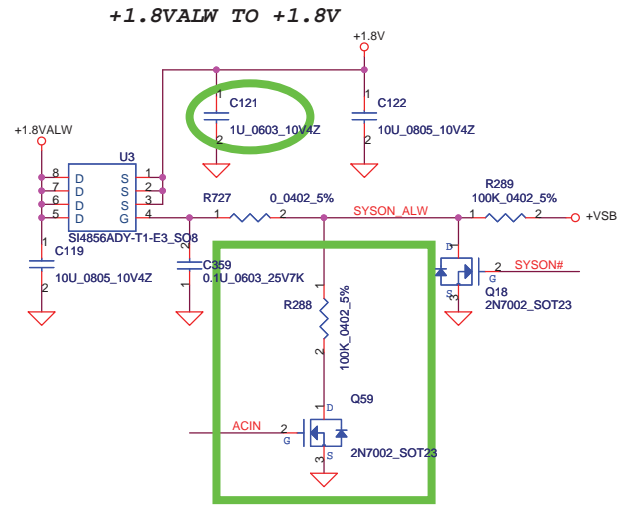
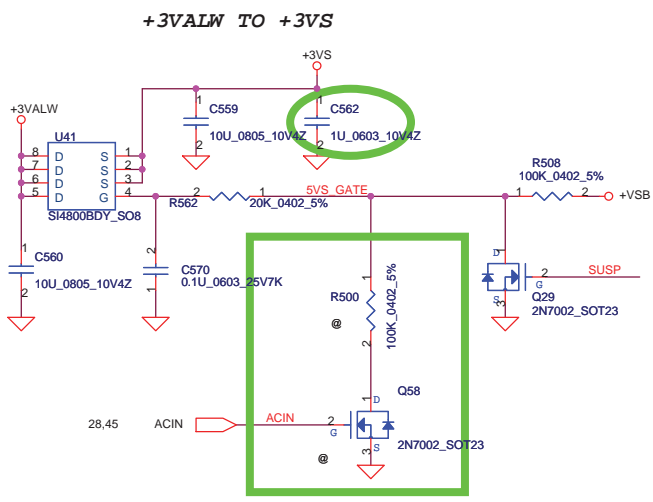
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	HDA Codec ALC268	
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				KAW60 LA-4661P	Rev 0.1
				Date: Friday, July 25, 2008	Sheet 39 of 50



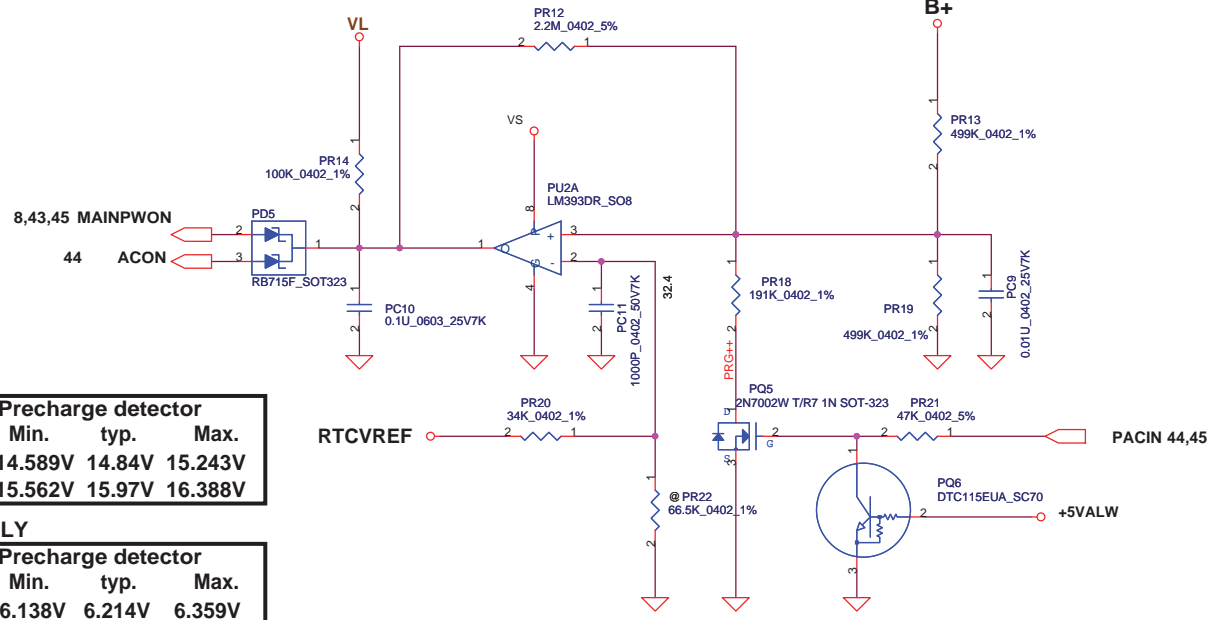
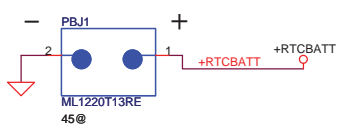
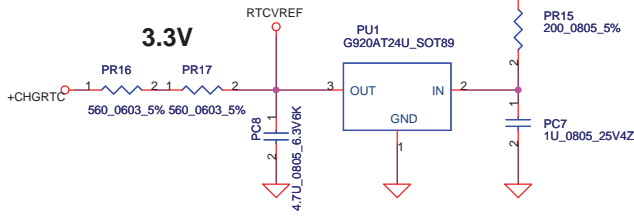
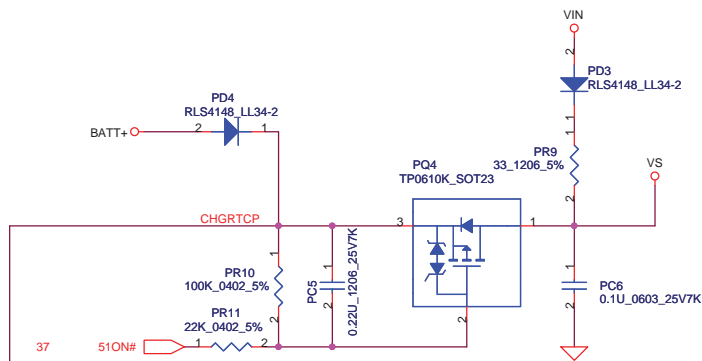
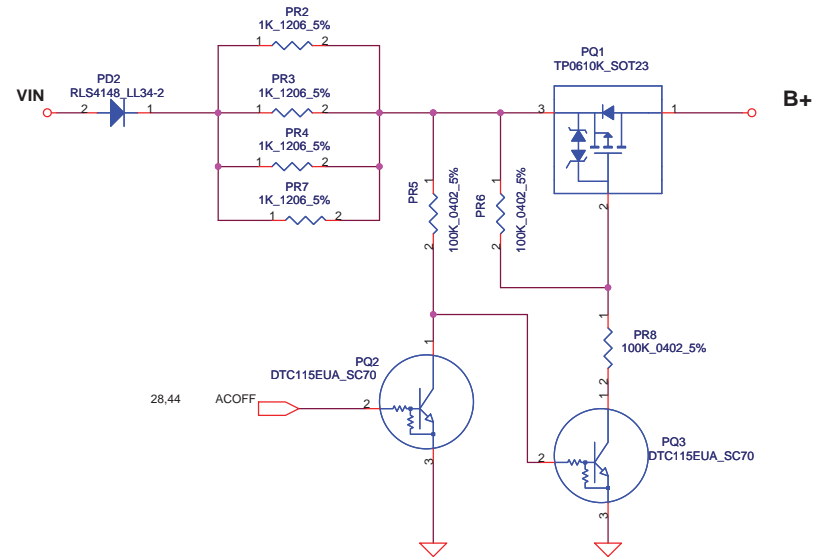
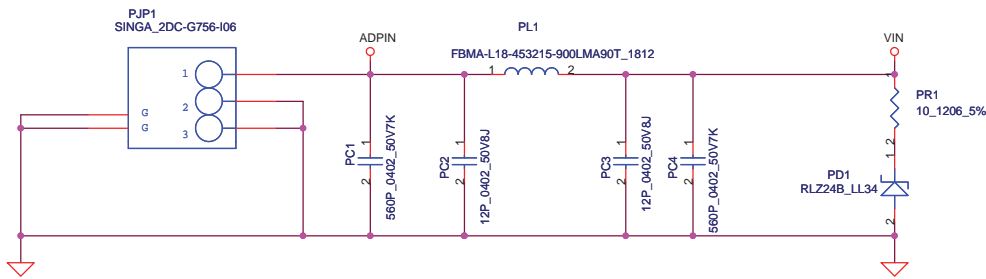
Gain= 14dB



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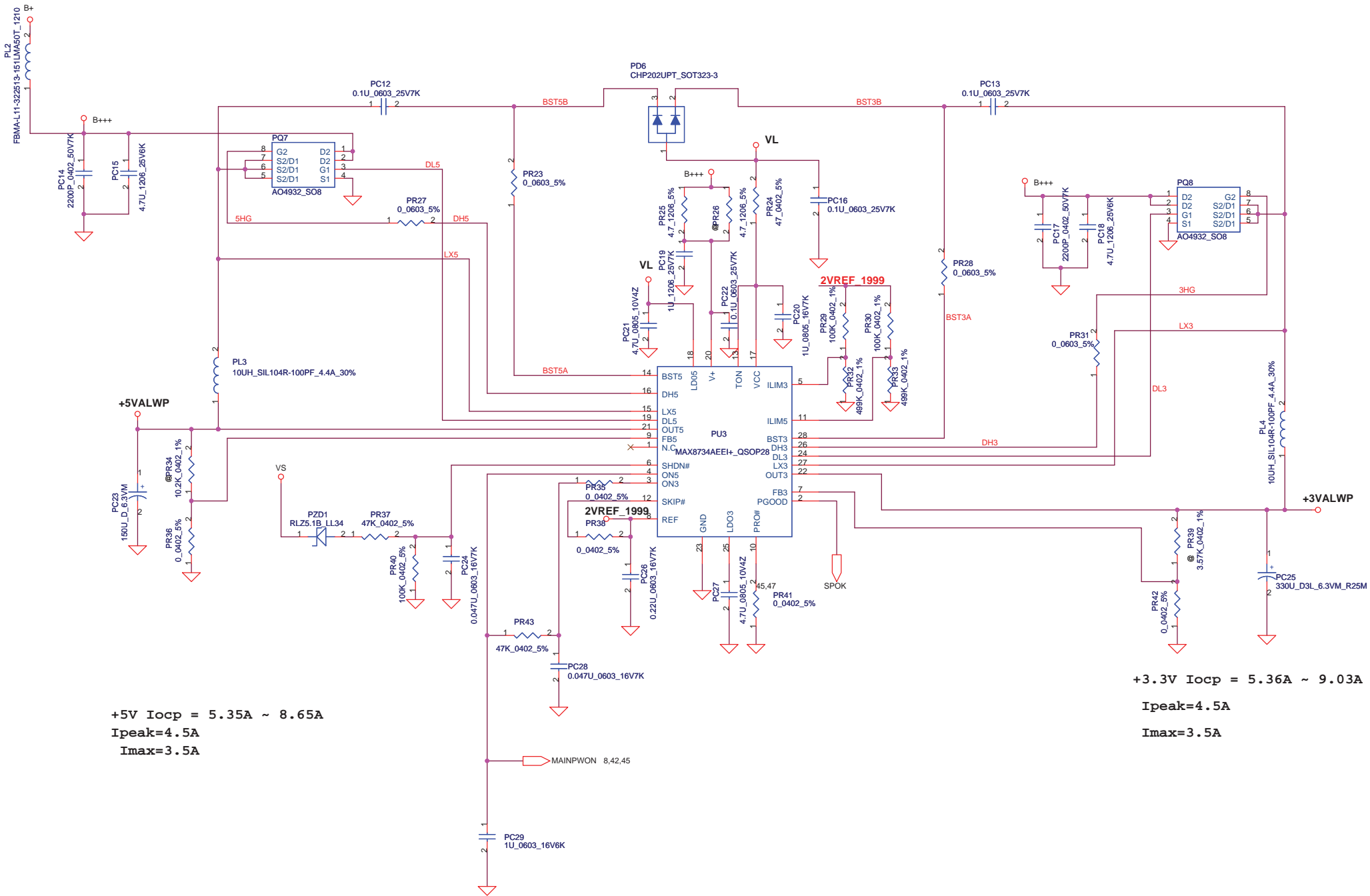
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/08	Deciphered Date	2006/03/08	DC INTERFACE	
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ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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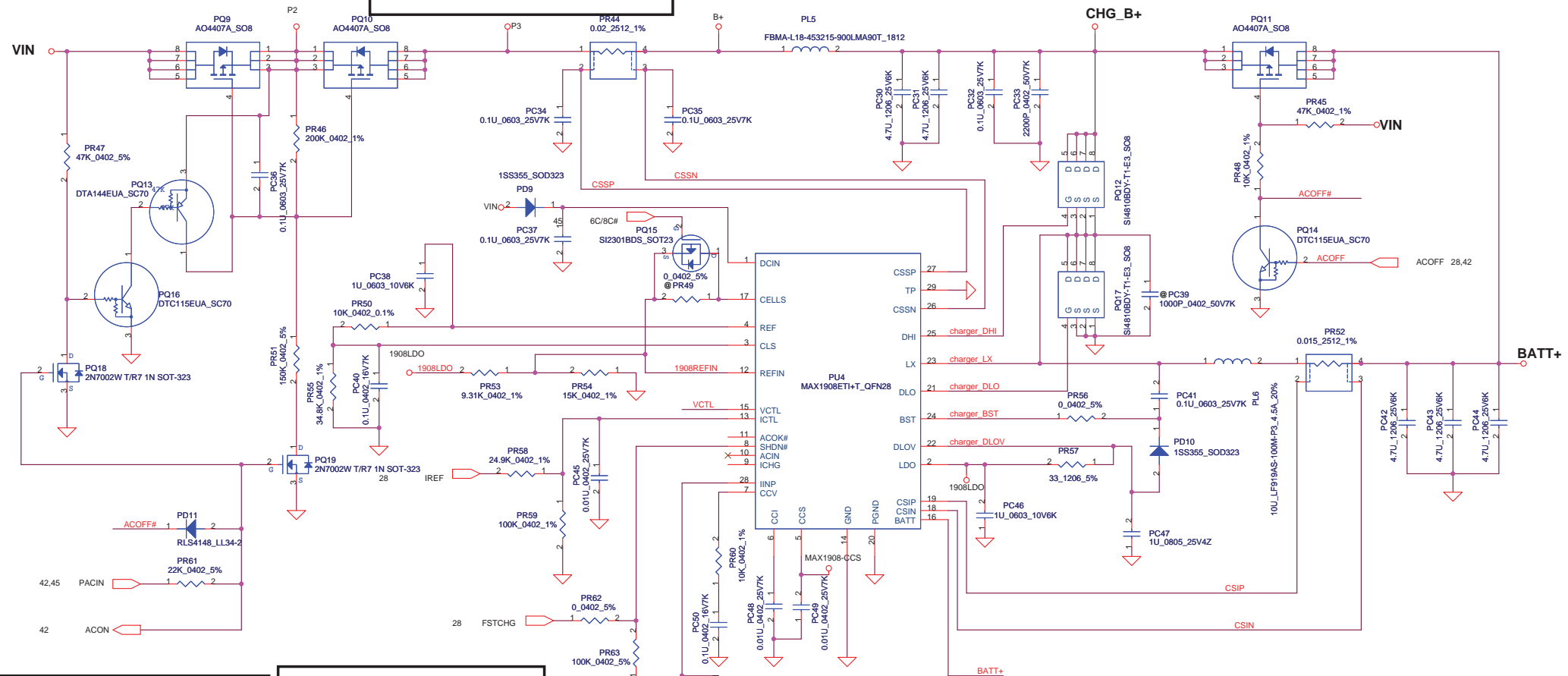
+5V Iocp = 5.35A ~ 8.65A
Ipeak=4.5A
Imax=3.5A

+3.3V Iocp = 5.36A ~ 9.03A
Ipeak=4.5A
Imax=3.5A

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I_{adp}=0~2.912A(65W)

CP Point:
 85% CP Point, 3.42A*0.85=2.907A~2.912A
 I_{input}=(34.8K/44.8K)*(75/20)=2.912A



Charger ADJ	Calibrate#	PR170	PR173
4.0V	L	@	@
4.1V	L	665K	221K
4.2V	H	@	@

$V_{refin} = V_{1908LDO} * (15K / (9.31K + 15K)) = 5.4V * (15K / (9.31K + 15K)) = 3.331V$
 $V_{vctl} = 3.331 * (221K / (221K + 665K)) = 0.83087V$
 $V_{batt} = CELLS * (4 + (0.4 * (V_{vctl} / V_{refin}))) = 3 * (4 + (0.4 * (0.83087 / 3.331))) = 12.29v$

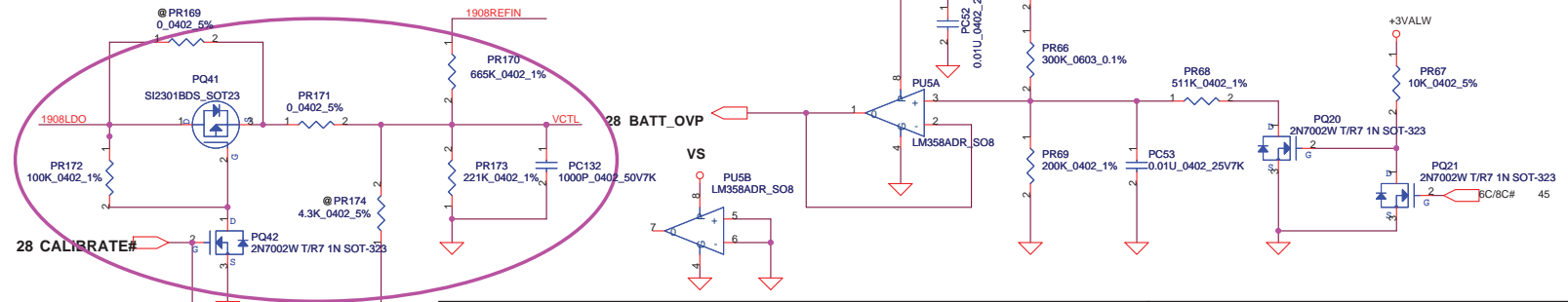
$I_{REF} = 0.832 * I_{charge}$
 $I_{REF} = 0.73 - 3.3V$

2P3S: 4400mAh
 0.8C = 3.52A

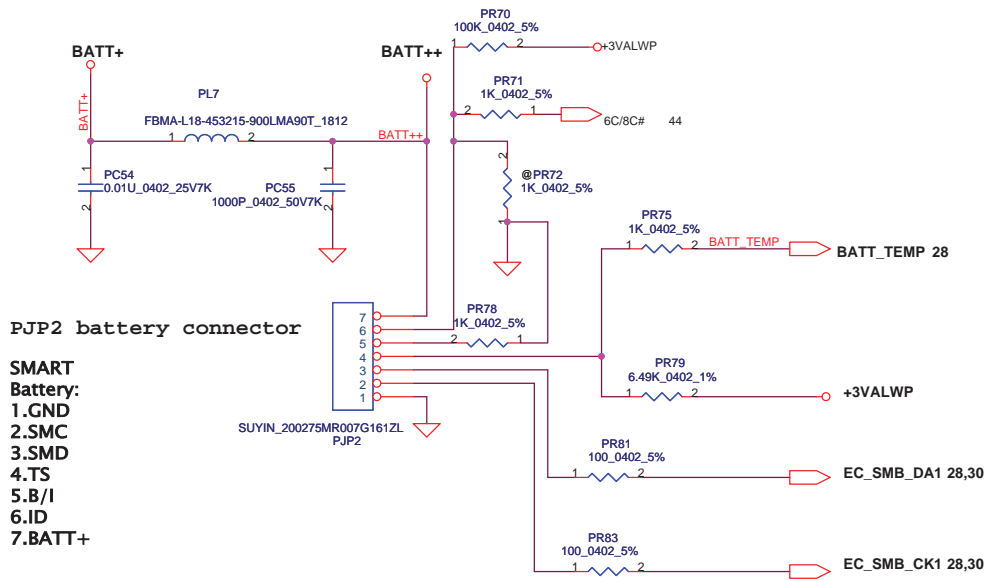
OVP-Voltage:
 LI-3S Battery Pack = 13.5V --- BATT-OVP = 2.0061V
 Battery-OVP = 0.1486 * BATT+

$V_{batt} = CELLS * (4V + (0.4 * (V_{vctl} / V_{refin})))$

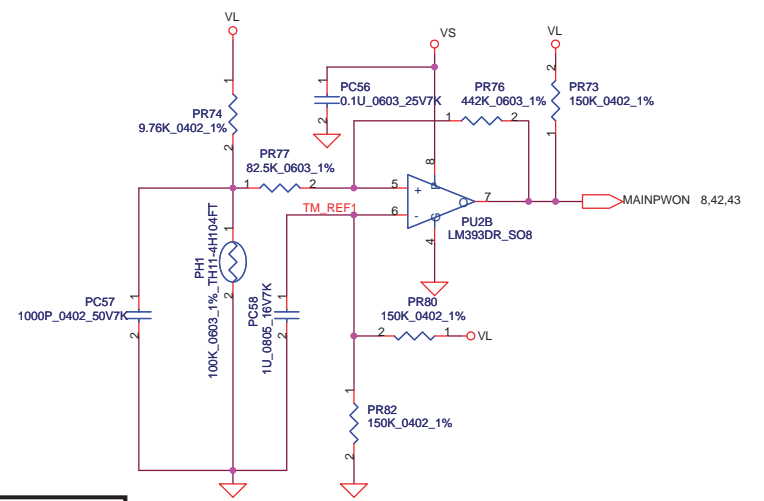
Charge voltage
 3S CC-CV MODE : 12.6V



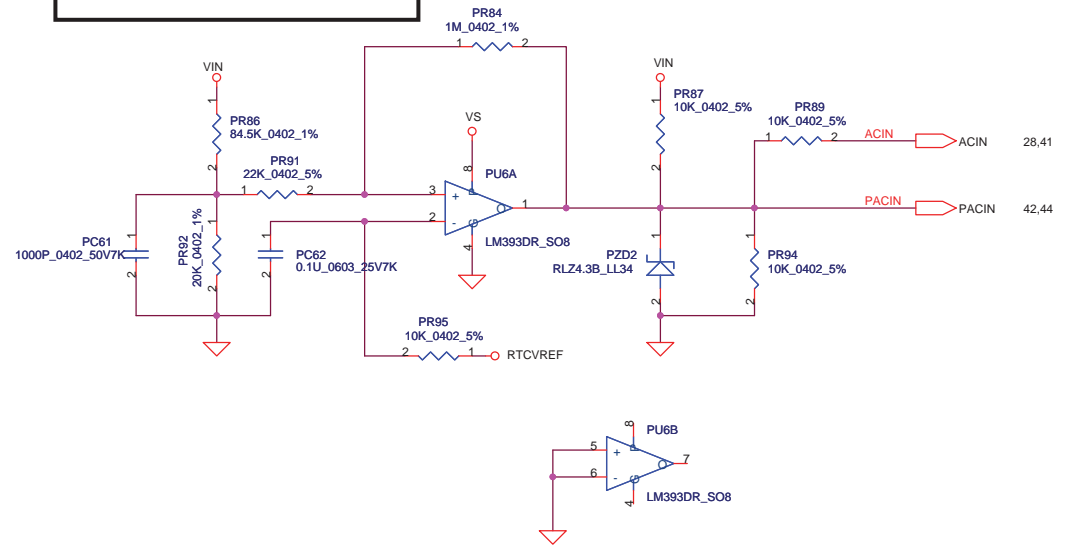
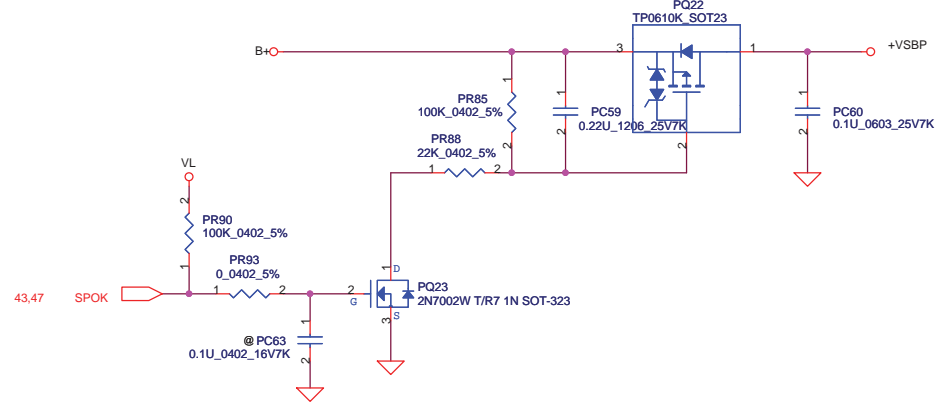
Security Classification	Compal Secret Data		Title	
Issued Date	2008/06/11	Deciphered Date	2009/06/11	Charger
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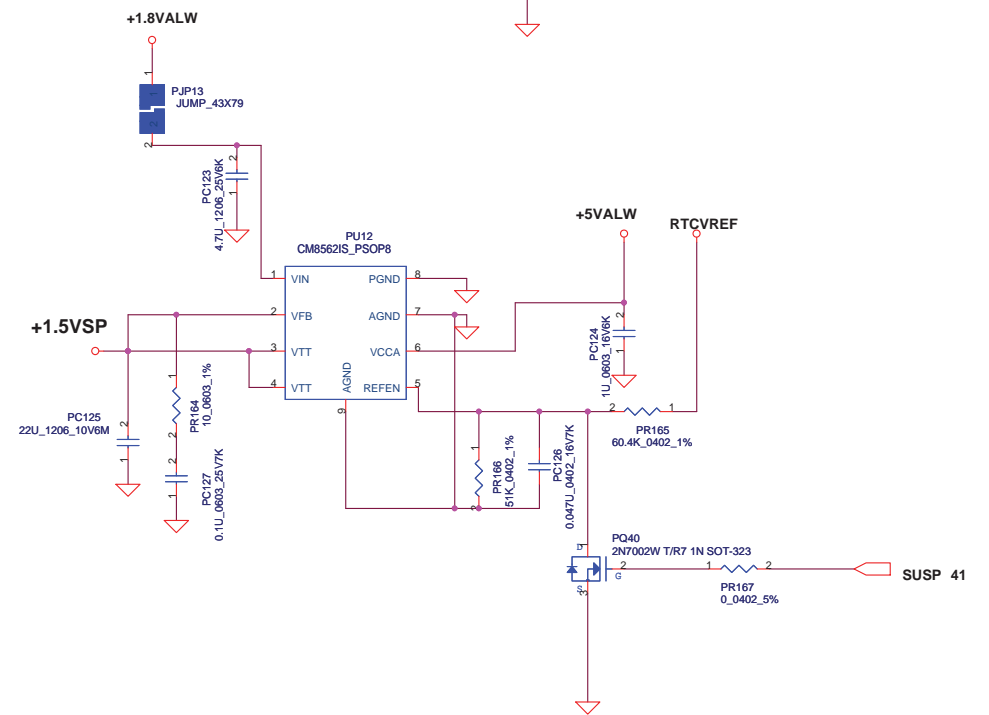
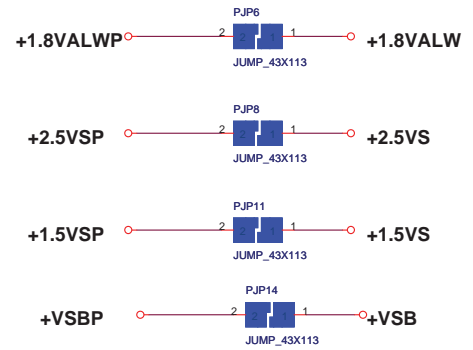
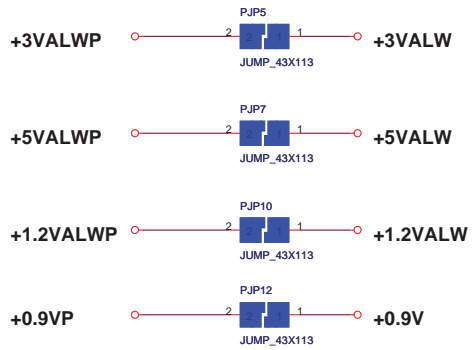
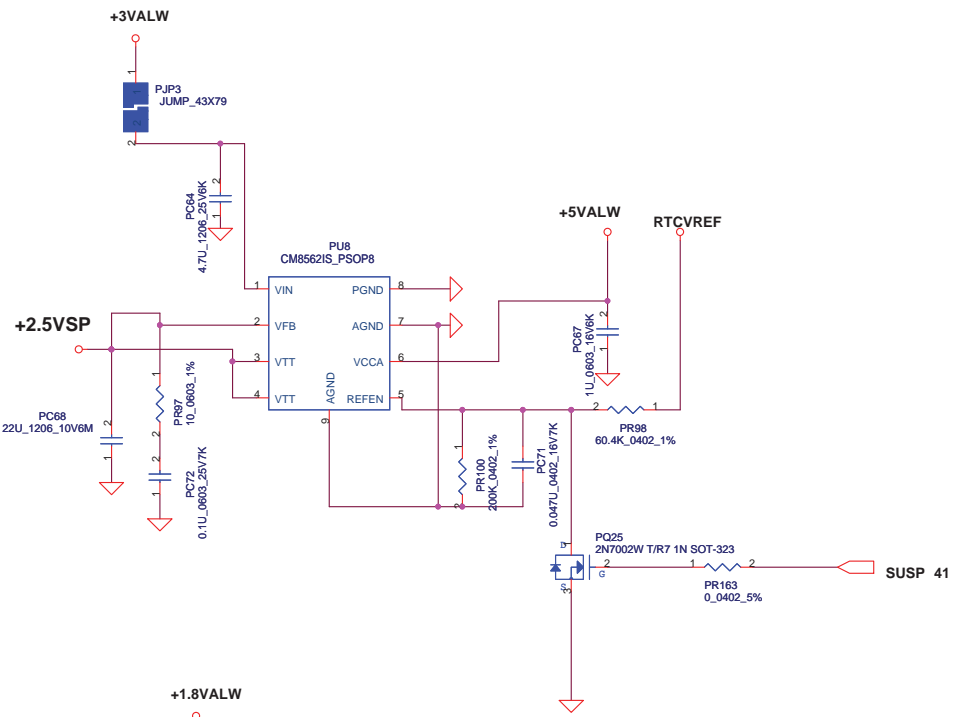
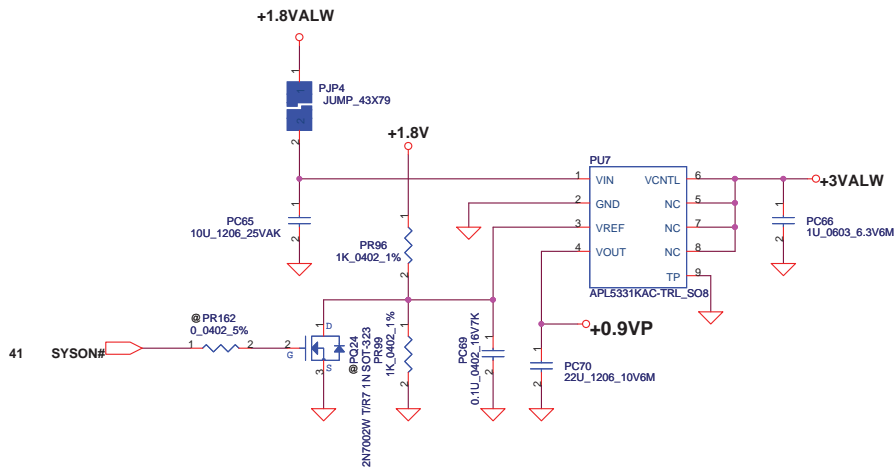
PH1 under CPU bottom side :
 CPU thermal protection at 90 degree C
 Recovery at 70 degree C



Vin Detector
 Min. typ. Max.
 H-->L 16.976V 17.257V 17.728V
 L-->H 17.430V 17.901V 18.384V



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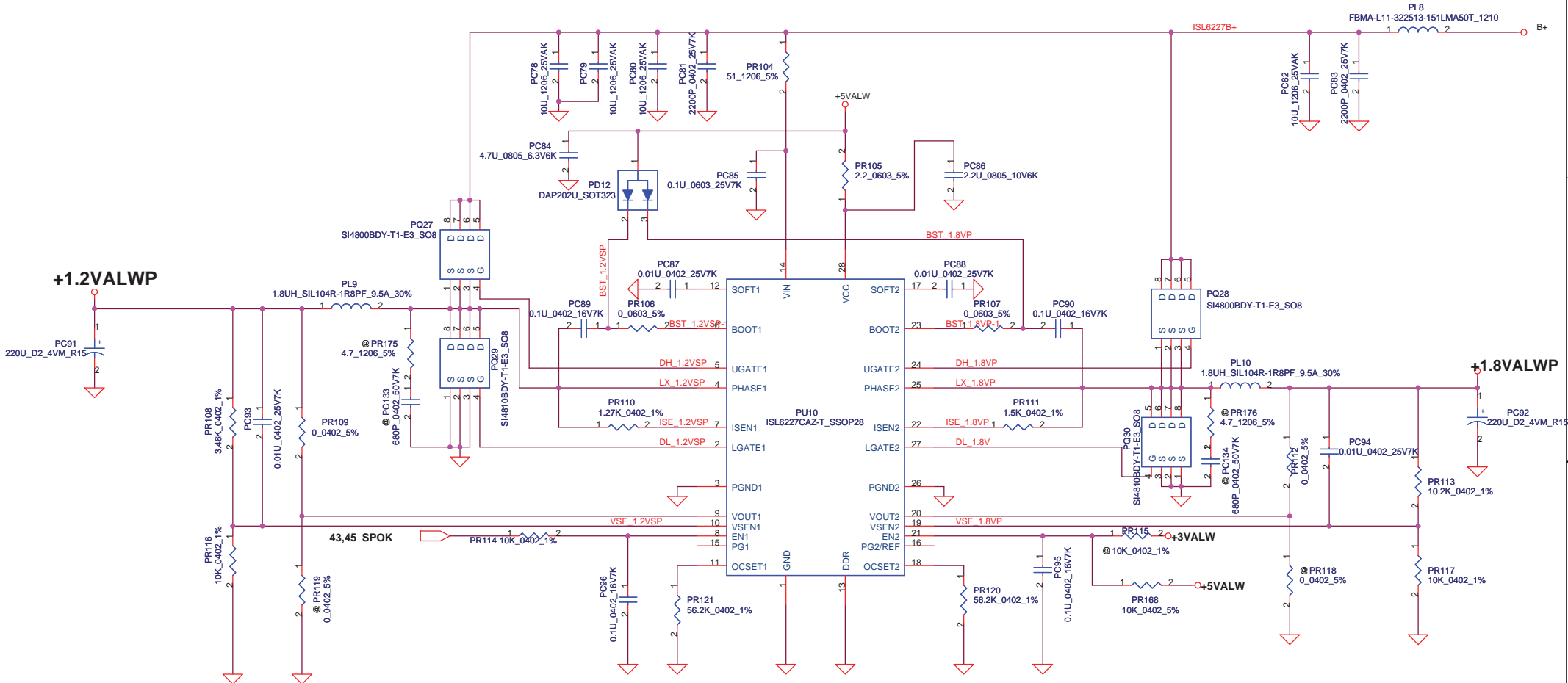


Security Classification	Compal Secret Data	
Issued Date	2008/06/11	Deciphered Date
		2009/06/11

Compal Electronics, Inc.		
Title	+0.9VSP/+1.5VSP/+2.5VSP	

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+1.2VALWP

+1.8VALWP

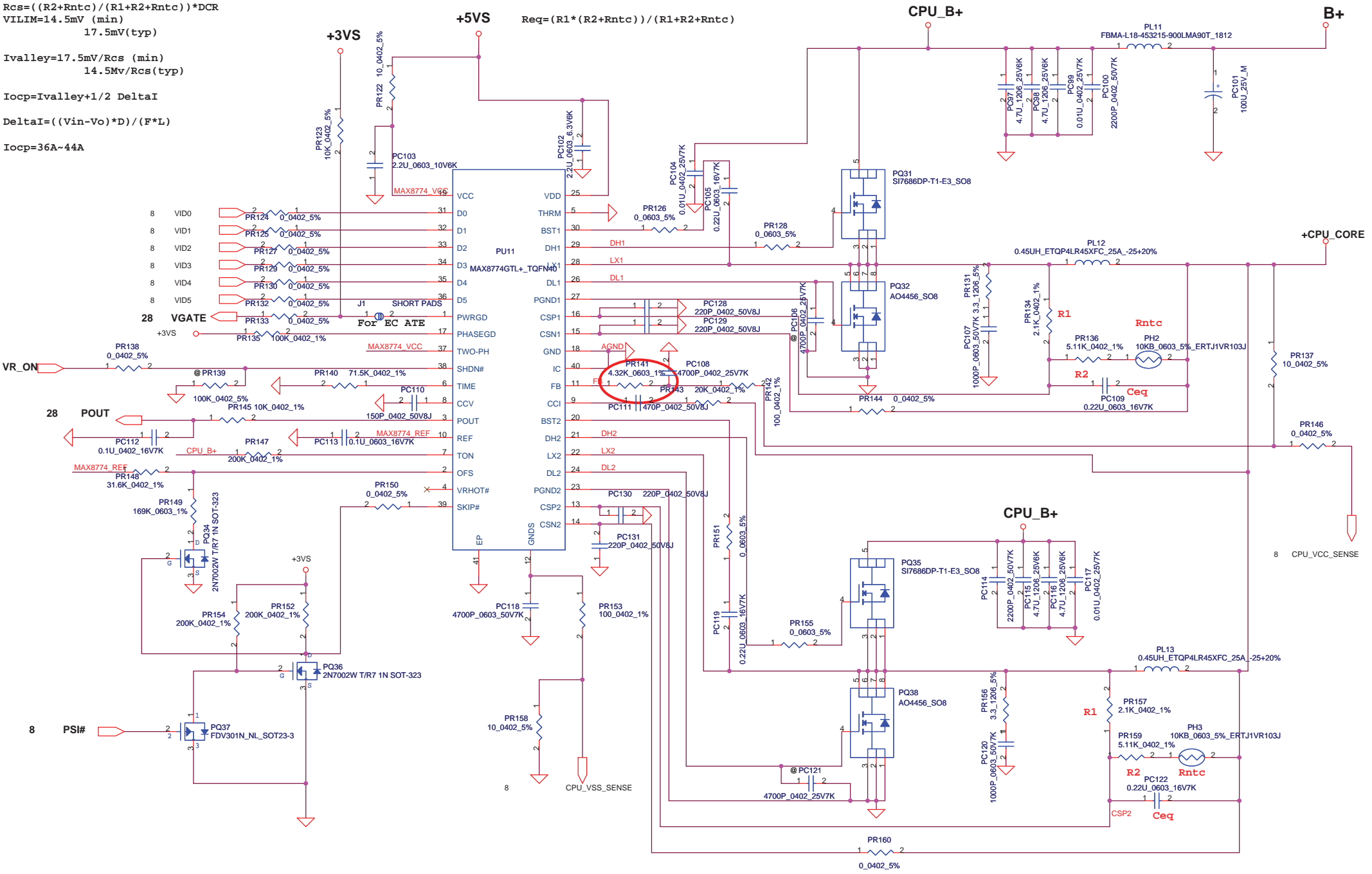
Ipeak=6.47A, Imax=6.47*0.7=4.53A
 Iocpmin=7.79A
 Iocpmax=11.83A

Ipeak=8.5A, Imax=6A
 Iocpmin=8.76A
 Iocpmax=13.46A

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OCp Setting:
 $Rcs = ((R2 + Rntc) / (R1 + R2 + Rntc)) * DCR$
 $VILIM = 14.5mV$ (min)
 $17.5mV$ (typ)
 $Ivalley = 17.5mV / Rcs$ (min)
 $14.5mV / Rcs$ (typ)
 $Iocp = Ivalley + 1/2 \Delta I$
 $\Delta I = ((Vin - Vo) * D) / (F * L)$
 $Iocp = 36A \sim 44A$

$Rcs * Ceq = L / Req$ must be satisfy!
 $Req = (R1 * (R2 + Rntc)) / (R1 + R2 + Rntc)$



<-BOM Structure>

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Issued Date	2008/06/11	Deciphered Date	2009/06/11	+CPU_CORE	
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Date:	Friday, July 25, 2008	Sheet	48	of	50

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	material issue.	Change to currently design	0.1	44	Change PQ9, PQ10, PQ11 from SB944070000(S TR AO4407 1P SO8 W/D) to SB00000DL00(S TR S TR AO4407A 1P SO8)	08,07/22	to PVT
2	material issue.	Change to currently design	0.1	48	Change PQ31 and PQ35 from SB578400080(S TR SI7840-T1 -E3 1N SO8) to SB000008L80(S TR SI7686DP-T1-E3 1N POWERPAK SO8)	08,07/22	to PVT
3	material issue.	AO4916 will be EOL, change to AO4932	0.1	43	Change PQ7 and PQ8 from SB000002W80(S TR AO4916 2N SO8) to SB00000BG00(S TR AO4932 2N SO8)	08,07/22	to PVT
4	BOM error	BOM error	0.1	48	Change PR141 from SD014200180(S RES 1/10W 2K 0603 1%) to SD014432180(S RES 1/10W 4.32K 0603 1%)	08,07/22	to PVT
5							
6							
7							
8							
9							
10							
11							
12							
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14							
15							
16							
17							
18							

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Issued Date	2008/06/11	Deciphered Date	2009/06/11	PIR(PWR)	
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				Date: Thursday, July 24, 2008	Rev 0.1
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PHASE	PAGE	MODIFICATION LIST	PURPOSE
PVT	P.19 & 24	Update CRT_DET & CRT_DET# net name	NA
	P.18 & 19	Change CRT_DET from GPIO61 to GPIO0 & reserved R741 , R742 , R743	For ACER AP test CRT detect feature
	P.20	Remove L71 , C694 & C697	For +3Vs (1.5V) , +5Vs (0.388V) , +1.8Vs (0.154V) on S5 leakage issue
	P.28	Change R519 from 100K to 10K	For RS690MC ENBKL had unexpected 3.3V pulse before normal display & white screen flash symptom appear
	P.14	Reserved U48 , U49 , R744 , R745 , R746 , R747 , C763	For RS690MC ENBKL , ENVDD if had unexpected 3.3V pulse before normal display
	P.28 & 31	Modify WL_ON_LED# from KB926 to JMINI1 control	WL LED activity behavior controlled by wireless mini card itself
	P.38	Update SW9 Footprint & P/N	NA
	P.41	Change R586 from 100K to 10K	For Susp# had 3V level glitch when G3 to S5 (Plug AC in) & caused +5Vs /+3Vs had leakage immediately
	P.6	Change D4 as SC1BAS16000(S DIO BAS16PT SOT-23)	Sourcer recommend
	P.26	Change U11 as SA000019910(S IC EE 1K CAT93C46VI-GT3 SOIC 8P)	SA093461070 (S IC EE 1K SO-8 I AT93C46-10SI-2.7) EOL
	P.50	Change T1 as SP050001210 / S X'FORM_ NS0013LF LAN (BOTHHAND)	MHPC X'form part not for ABO , Sourcer recommend
	P.18	Delete R695,R179,R484 for SB_TEST pin	AMD reference schematic
	P.20	Reserved C764 (1u_0402)	AMD reference schematic & design guide
	P.38	Modify WL_LED power rail as +3Vs	NA
	P.28 & 38	Modify LED control of SATA drive from EC to SB (Add Q67)	EC(media_led#/pin86 , reference sata_led# from SB) control behavior abnormal
	P.17	Change C510 , C511 of 14.318MHz as 27P from 22P	NA
	P.37 & 25	Change D5 , D21 as SC1BAS16000	NA
	P.26	Add L77 , C765 , C766 , C767 & change R645 / R647 as L78 / L79 , reserved C719 , C724	EMI request
	P.31 & 34	Stuff L66 , L67 , L68 & remove R615 , R616 , R598 , R599 , R600 , R601	EMI request
	P.29	Stuff D28	ESD request
	P.6	Update net EN_DFAN1_R	NA
	P.6	Update JCPU1 PCB footprint as SOC127MM48X51-948	NA
	P.26	Add R749 , R750 (300ohm_0402)	For LAN external EEPROM program issue
	P.31	Add D32 (SCA00000A00)	ESD request
	P.28 & 31	Reserved R751 & R752	Reserved WL_LED controlled by EC (Navarrow project)
	P.24	Change C411 & C412 PN from SE081680k80 to SE071680J80	AP Code
	P.6	Change U1 as SA00001Z900 (S IC APL5605KI-TRL SOP 8P)	(SA009930010) S IC G993P1UF SOP 8P FAN LDO EOL
	P.9	Change C504 & C505 as SGA19331D10	(SGA19331D00) S POLY C 330U ESR15 , but need ESR9 (SGA19331D10)

ZZZ



PCB 06B LA-4661P REV0 MB

LA4661MB Rev0 : DA600009Z00

LA4661MB Rev1 : DA6~

LA4661MB with Sub/B Rev1 : DAZ~

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