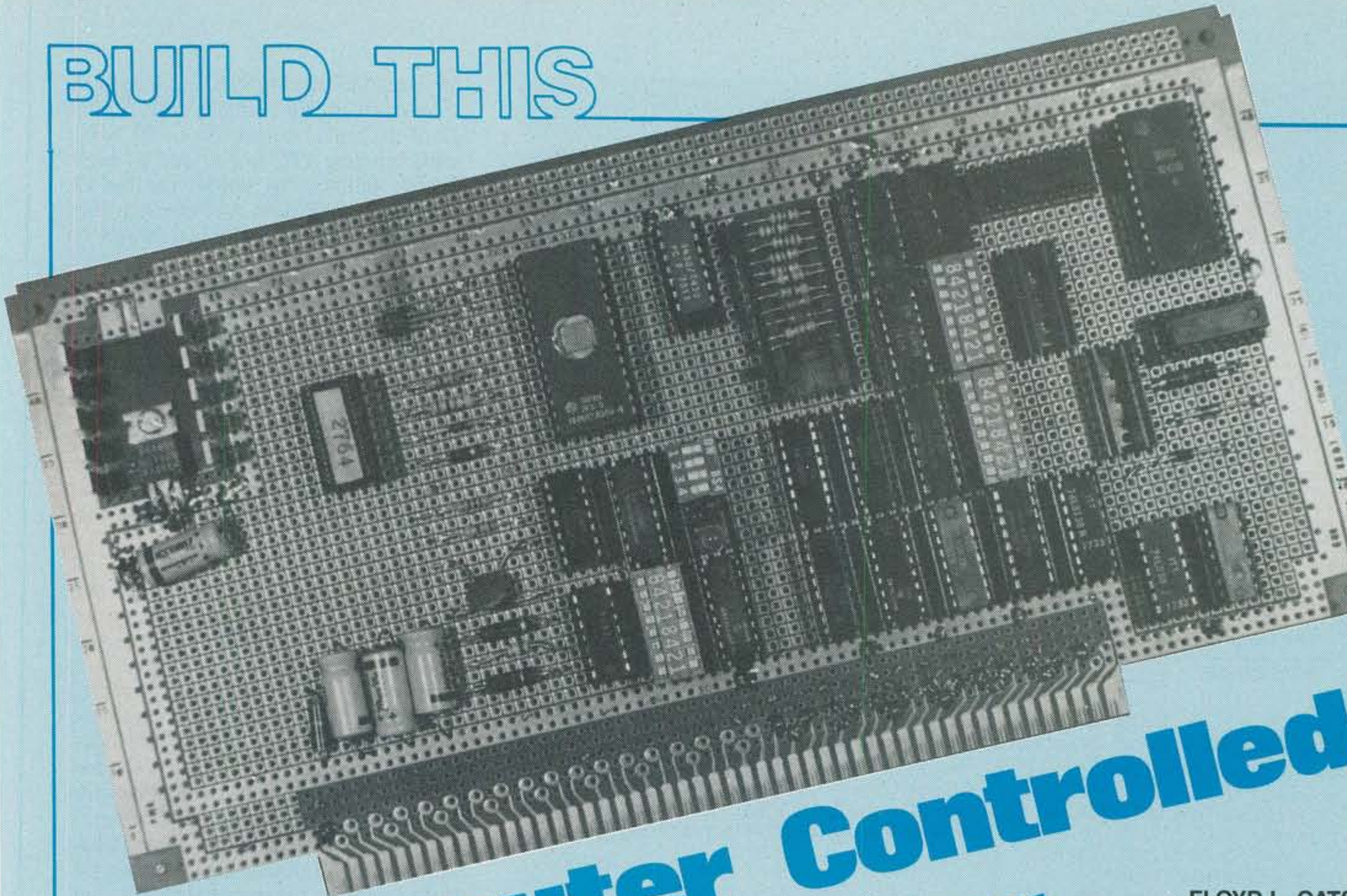

Computer Controlled IC Tester

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This month we'll test the IC tester and then we'll look at some options that you can add.

Part 2 LAST MONTH, WE DESCRIBED the IC-tester circuit and the theory behind how it works. Now it's time to make sure that it *does* work. After we do that, we'll look at some options that you can add to your tester. For example, we'll build a low-budget logic analyzer—it works by expanding your oscilloscope display to 16 traces.

Testing the tester

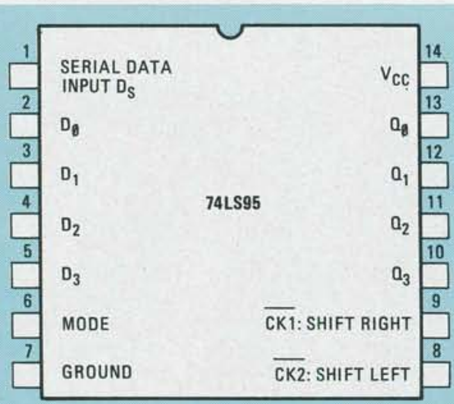
Most of the components and wiring are located in the data paths so the inherent self-diagnostic feature of the tester can be utilized as a debugging aid for the finished project. After the device is built and connected to the host computer, preliminary testing can begin.

For the purpose of discussion, we will assume that the device has been mapped into memory addresses CFØØH through CFFFH (as it is shown in the schematic). **Note:** An "H" indicates that a number is written in hexadecimal form.

Open all the isolation switches (S1–S16) and make sure that the test socket is empty and that there are no power-supply jumpers between SO3 and SO2. Read the sixteen response bits by performing memory reads on addresses CFØØH and CFØ1H. Both of those addresses should return FFH, indicating that the response is equal to sixteen "1" bits. Next, close all the isolation switches and write sixteen zeros in the stimulus latches by writing ØØ into address CFØØH. Read the response as before and look for sixteen zero bits. Now write all ones in the stimulus latches by writing FFH into memory address CFFFH and check for a response of all ones, as before. At this point, the tester is in a configuration where all stimulus information should be exactly duplicated on the response lines.

The next test will require a short program to send counting stimuli to the tester. After each stimulus is sent to the latches, the response is accepted and compared with the stimulus for equality. If single-bit failures are observed during the the test, the components and wiring associated with that particular bit should be checked carefully. If the bit patterns don't change or if they don't even resemble the correct patterns, the control circuitry might be at fault. Any discrepancies noted up to this point must be repaired before proceeding with further tests.

The final series of tests will verify the wiring of the isolation switches. Starting with all switches closed, open one switch and send a stimulus of all zeros. The response should be all zeros except for a single "1" bit, which should correspond to the open switch. Now close the switch just tested and open the next switch, then perform a similar stimulus/response test on this switch. Continue in this fashion until all sixteen switches have been tested. The final test is started with all switches open and is similar to the previous test in that one switch at a time is tested. This time the switches will be closed one at a time. Send test patterns of all zeros and



OPERATION	INPUTS: MODE	$\overline{CK1}$	$\overline{CK2}$	D_S	D_n	OUTPUTS: $Q_Ø$	Q_1	Q_2	Q_3
PARALLEL LOAD	H	X	↓	X	I	L	L	L	L
	H	X	↓	X	H	H	H	H	H
SHIFT RIGHT	L	↓	X	I	X	L	q0	q1	q2
	L	↓	X	H	X	H	q0	q1	q2
MODE CHANGE	↑	L	X	X	X	NO CHANGE			
	↑	H	X	X	X	UNDETERMINED			
	↓	X	L	X	X	NO CHANGE			
	↓	X	H	X	X	UNDETERMINED			

I: LOW VOLTAGE ONE SETUP TIME PRIOR TO HIGH-TO-LOW CLOCK TRANSITION
LOWER CASE LETTERS REPRESENT STATE OF REFERENCED OUTPUT ONE SETUP TIME PRIOR TO HIGH-TO-LOW CLOCK TRANSITION
↑: LOW-TO-HIGH TRANSITION
↓: HIGH-TO-LOW TRANSITION

FIG. 5—THE 74LS95. Before you test any IC, you have to prepare a function table. That's not only because you have to determine a valid and complete set of stimuli, but you also have to determine what kind of response you should expect.

look for a response of all ones except for the single closed switch.

Using the tester

In order to test an IC, the isolation switches and the power-supply jumpers must be configured for the specific circuit to be tested. The switches assigned to input pins of the test circuit must be closed and those assigned to output pins and power supply pins must be open. The actual test is done by comparing the set of test responses with a set of known good responses.

The best way to obtain a set of good responses is to issue stimuli to an IC (of the type you want to test) that you know to be good. You can save the responses for future comparison. Actually you should save both stimuli and responses since the patterns issued during the test must exactly match those used to create the initial patterns. A less attractive way of obtaining good response data is to issue patterns to a circuit thought to be good and then manually examine the response data to see if it is correct.

Let's consider the steps involved in testing the SN74LS95, a four-bit shift register with parallel-load capability. Figure 5 shows the pinout for that 14-pin IC along with a table that describes the circuit's functions. The MODE input (pin 6) determines the mode in which the circuit is operating (parallel load or shift), and also determines which of the two clocks is permitted to change the register contents. The function table reveals that there are edge transitions in the mode-change area that will cause indeterminate results. Those transitions should be avoided during the testing process because they represent invalid stimuli.

Fourteen-pin IC's should be mounted in the 16-pin socket such that pins 8 and 9 of the 16-pin socket are empty. (Consequently, pin 14 of the IC is connected to pin 16 of the test socket and to S16.) Figure 6 shows that and also indicates the required position of each isolation switch for that particular IC. The +5-volt power-supply jumper must be connected from SO3 pin 14 to SO2 pin 16. The ground jumper goes from SO3 pin 7 to SO2 pin 7. Set up the switches and power-supply jumpers, insert the IC into the test socket, and testing can begin.

The 74LS95 has multiple edge-sensitive inputs. As we mentioned previously, counting through the inputs does not generate suitable (complete and valid) stimuli for that IC. We shall use what amounts to a smaller and somewhat simpler set of test patterns as shown in Table 1.

Table 1 indicates that several patterns are issued to the 74LS95 before each response is read. For example, consider line 12 of the table. A stimulus of Ø228H is sent, bringing $\overline{CK2}$, MODE, and D_2 high. That is followed by ØØ68H on line 13, which brings $\overline{CK2}$ low. A response is then accepted; it and should equal 9Ø28H on line 14.

How does the host know when to accept a response? The software driver can take advantage of the fact that the isolation switches for the two power-supply pins are known to be open and that, consequently, those two pins are not sensitive to stimuli. Bits 7 and 16 can be used to imbed control-flag bits into the test data. Those can be used to tell the host whether to generate a stimulus, expect a response, call a subroutine, etc.

For example, when the ground line (bit 7) is made high, as on line 16, it indicates (to the author's test software) that a response is to be taken after the pattern is sent. When the +5-volt line is made high as on line 18, the software driver will call a subroutine to clear the 74LS95 before sending the test pattern on line 18. Notice that line 15 brings bits 16 and 7 of the test circuit low. The software driver writes that pattern and then proceeds to the next pattern on line 16. The pattern on line 16 has bit seven high (ground pin), causing the driver to accept a response (line 17) after sending the ØØ7ØH pattern. When both supply lines are high as on line thirty, it signifies "end of test." That use of power supply pins is one way, but not the only way, of simplify the passage of control parameters to the software.

Because the SN74LS95 does not have a separate CLEAR pin, the clear subroutine (Table 1, lines 1–4) must use the parallel-load capability of the circuit to load all zeros into the internal register. The response should be tested after the clear subroutine since a failure here will cause subsequent failures in the main body of the test. It is good general practice to flag the earliest possible failure in a series of tests, especially if the software is going to perform a complete and exhaustive failure analysis.

Options

If you build the tester on a prototyping board designed for your host system, you will almost certainly find that there is plenty of space left on the board for possible expansion. For example, an 18-pin socket may be added for the purpose of testing specific 18-pin circuits such as the popular 2114 RAM series. (The power supply pins would be permanently wired to the power-supply lines, while the other sixteen pins would be wired parallel to the sixteen test socket pins.) Pin correspondence between the test socket and the 18-pin socket can be assigned in any convenient order.

The addition of a PROM or EPROM

SN7495 PIN	14	13	12	11	10	9	8			7	6	5	4	3	2	1
FUNCTION	+5V	Q_0	Q_1	Q_2	Q_3	$\overline{CK1}$	$\overline{CK2}$	NC	NC	GD	MODE	D_3	D_2	D_1	D_0	D_S
SWITCH NUMBER	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
AND POSITION																

FIG. 6—SWITCH SETUP for testing the 7495 4-bit shift register.

programmer is practical because there are already sixteen latches on the board. If you add another SN74LS75, you'll have enough latches for the data and address lines of a 4K PROM. A square- or rectangular-wave generator may be added by selecting a bit and placing it under software control. Parameters describing the desired wave could be passed to software which would then compute the loop variables required to create the wave on the chosen bit line. Squarewave monitoring could be done by bringing the external wave into a bit line and letting the software sample the line. Those are just a few of the many ways to expand the IC tester.

Oscilloscope adapter

The logic analyzer is a very useful tool. But because it's also rather expensive, most hobbyists do not have access to one. However, we'll offer an alternative to the logic analyzer: an adapter for your oscilloscope that allows it to display 16 signals. Of course, its linearity and general quality of presentation won't match that of the logic analyzer. And it won't imitate the varied and complex functions of a logic analyzer. But it *can* be built from inexpensive, common logic-components. So for a very small expense, you can add a valuable tool for testing digital IC's to your testbench. Perhaps more important, the oscilloscope-adapter logic analyzer can be an excellent tutorial aid.

The author's display-adapter prototype was developed as an expansion of the digital IC tester that was presented last month, and it uses TTL IC's. However, the oscilloscope adapter can be built as a stand-alone unit, and the ideas can be applied to other logic families as well as TTL.

A look at the circuit

The oscilloscope adapter's circuit (its schematic is shown in Fig. 7) uses a counter/multiplexer/converter scheme to time-share sixteen digital signals onto a single oscilloscope channel.

The display counter, IC12 (a 74LS191 synchronous up/down counter), selects one of the sixteen channels for display. As it counts, each channel is selected in proper sequence—channel 1 is displayed on top, and channel 16 on the bottom.

A 74150 1-of-16 data selector/multiplexer, IC11 accepts the sixteen digital inputs from the tester. It selects one of them to pass to its output (pin 10). The selected input depends on the contents of the display counter.

The inverting buffer/drivers, IC13, along with its associated resistors, form a 5-bit 32-state digital-to-analog (D/A) converter. It combines the four display-counter bits and the single, selected channel bit into one of thirty-two discrete voltage steps—two voltage levels for each displayed channel. The output signal to the oscilloscope swings through more than four volts of the available 5-volt power-supply range.

TABLE 1

		SIGNAL TYPE	HEX VALUE	BIT VALUES 16..13	12..9	8..5	4..1	ACTION
CLEAR	01	Stimulus	0220	0000	0010	0010	0000	- Bring $\overline{CK2}$ and MODE high
	02	Stimulus	0020	0000	0000	0010	0000	- Drop $\overline{CK2}$ (load zeros)
	03	Stimulus	0040	0000	0000	0100	0000	- Drop MODE, then test
	04	Response	8000	1000	0000	0000	0000	- All pins low except V_{cc}
PARALLEL LOAD TEST	05	Stimulus	8020	1000	0000	0010	0000	- Clear, then bring MODE high
	06	Stimulus	0222	0000	0010	0010	0010	- Bring $\overline{CK2}$, MODE, D_0 high
	07	Stimulus	0062	0000	0000	0110	0010	- Drop $\overline{CK2}$, then test
	08	Response	C022	1100	0000	0010	0010	- V_{cc}, Q_0, MODE, D_0 high
	09	Stimulus	0224	0000	0010	0010	0100	- Bring $\overline{CK2}$, MODE, D_1 high
	10	Stimulus	0064	0000	0000	0110	0100	- Drop $\overline{CK2}$, then test
	11	Response	A024	1010	0000	0010	0100	- V_{cc}, Q_1, MODE, D_1 high
	12	Stimulus	0228	0000	0010	0010	1000	- Bring $\overline{CK2}$, MODE, D_2 high
	13	Stimulus	0068	0000	0000	0110	1000	- Drop $\overline{CK2}$, then test
	14	Response	9028	1001	0000	0010	1000	- V_{cc}, Q_2, MODE, D_2 high
	15	Stimulus	0230	0000	0010	0011	0000	- Bring $\overline{CK2}$, MODE, D_3 high
	16	Stimulus	0070	0000	0000	0111	0000	- Drop $\overline{CK2}$, then test
	17	Response	8830	1000	1000	0011	0000	- V_{cc}, Q_3, MODE, D_3 high
SHIFT TEST	18	Stimulus	8401	1000	0100	0000	0001	- Clear, then bring $\overline{CK1}$, D_s high
	19	Stimulus	0041	0000	0000	0100	0001	- Drop $\overline{CK1}$, then test
	20	Response	C001	1100	0000	0000	0001	- V_{cc}, Q_0, D_s high
	21	Stimulus	0400	0000	0100	0000	0000	- Bring $\overline{CK1}$ high D_s low
	22	Stimulus	0040	0000	0000	0100	0000	- Drop $\overline{CK1}$, then test
	23	Response	A000	1010	0000	0000	0000	- V_{cc}, Q_1 high
	24	Stimulus	0401	0000	0100	0000	0001	- Bring $\overline{CK1}$, D_s high
	25	Stimulus	0041	0000	0000	0100	0001	- Drop $\overline{CK1}$, then test
	26	Response	D001	1101	0000	0000	0001	- V_{cc}, Q_0, Q_2, D_s high
	27	Stimulus	0400	0000	0100	0000	0000	- CK_1 high and D_s low
	28	Stimulus	0040	0000	0000	0100	0000	- Drop $\overline{CK1}$, then test
	29	Response	A800	1010	1000	0000	0000	- V_{cc}, Q_1, Q_3 high
	30	Stimulus	8040	1000	0000	0100	0000	- END OF TEST

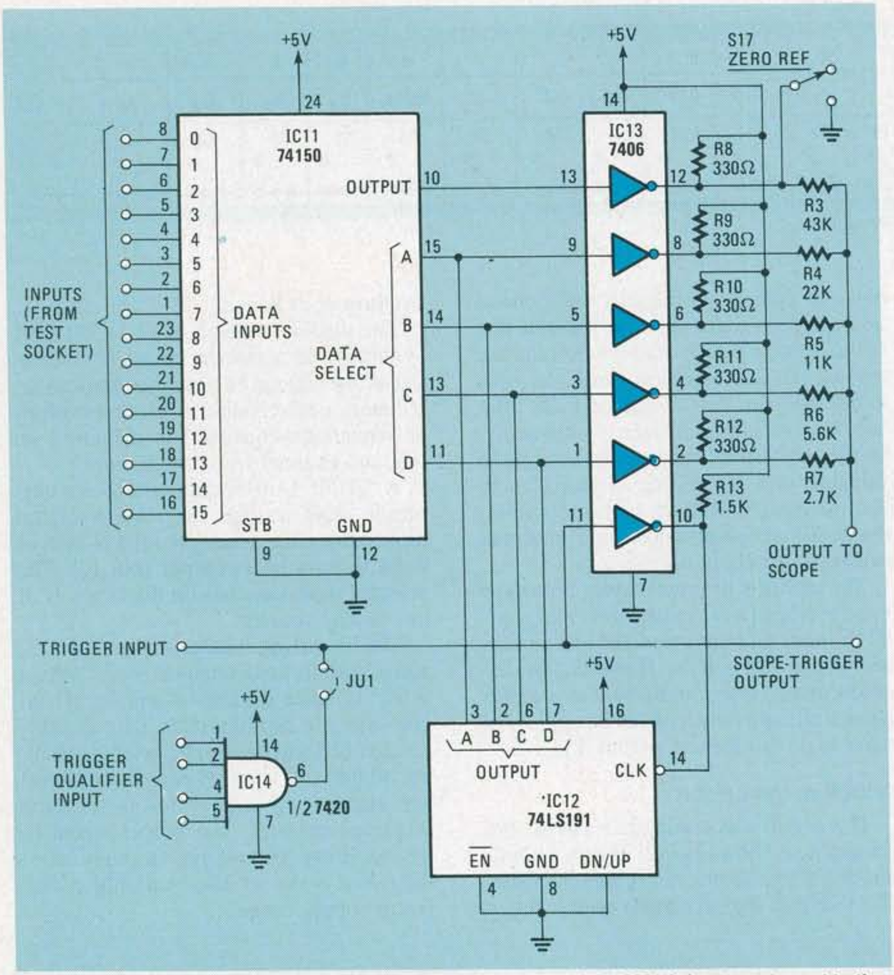


FIG. 7—OSCILLOSCOPE ADAPTER SCHEMATIC. IC12 selects which of IC11's inputs gets sent to the output buffer. The resistor network at the output of the buffer establishes 32 discrete voltage steps—two for each channel. IC14 is a trigger qualifier; it's optional, but suggested. Jumper JU1 is used to take the qualifier in and out of the circuit.

A trigger must be supplied by the logic system or device being observed. The trigger is needed both to act as a clock for the display counter and to initiate a horizontal oscilloscope sweep. The trigger signal is applied to pin 11 of IC13; sixteen of those trigger pulses are required to generate a complete 16-trace image on the scope. In complex digital systems, a single signal that can act as a suitable trigger is not always available—you may need an optional trigger qualifier so that you can create an acceptable trigger. A qualifier gate, such as what is shown for IC14, can be used. We recommend that you add such a qualifier gate along with a provision to enable it simply by the insertion of a jumper.

Switch S17 is an optional zero-reference switch. It is used to place a low logic-level on the least-significant input leg of the converter. When the switch is closed, the scope will display the 16 base lines. By momentarily closing the switch, you can quickly identify a steady-state channel as steady high or steady low. The switch is also useful in linearity tests.

Construction

You probably have enough room left on your original IC tester board to build the display adapter. Since the wiring or component layout is not critical, practically any construction technique may be used with good results.

There are many possible component substitutions that can be made in the TTL design. For example, the counter does not have to be a 74LS191: It can be another kind of synchronous counter like the 74LS163 or the 74LS193. Or it may be a standard (as opposed to low-power Schottky) TTL counter like the 74191. If substitutions are made, be sure to check the pinout of the new IC and document the changes where necessary. The use of ripple counters such as the 7493 is not recommended in this circuit—they tend to introduce excessive channel-switching transients. The 7406 may be substituted by other open-collector hex inverters including the 7416, and the 7405.

One final construction note: Assuming that you are building the circuit as an expansion of the IC tester, each display channel should be connected to its corresponding pin on the test socket. In other words, channel 1 should display the signal on pin 1 of test socket SO1 and so on. That makes using the analyzer easier.

Using the display adapter

For illustration purposes, let's set up the IC tester so that we can examine the waveshapes associated with the 74LS138 one-of-eight decoder. Table 2 lists the proper stimulus patterns. The trigger should be jumpered from the stimulus latch side of the isolation switch for pin 8 to pin 11 of IC13 in Fig. 7, and the scope should be set to trigger from the positive edge of an external signal. Isolation switches S1–S6 should be closed, and switches S7–S16 should be open.

Notice that the first two stimulus patterns will send a clock pulse to the display counter and trigger the oscilloscope, respectively. As shown in Fig. 8, the counter counts on the leading edge of the trigger pulse and the display begins on the trailing edge. That eliminates the channel-switching lines and lets us see a clean display.

Program your host computer to generate the looping stimulus patterns in Table 2 and run the test on a 74LS138. Connect the oscilloscope test leads to the adapter and, with the test running, we are ready to observe digital waveforms.

Set the vertical-sensitivity control to 1 volt/division and set the timebase to the fastest sweep. The exact sweep speed required for observation will depend on the speed at which the host system emits stimuli. Decrease the sweep speed and carefully observe the counting stimuli on channels one, two, and three, to determine when the proper speed is found. (It will probably be necessary to decalibrate the timebase to display the entire interval between triggers.) If the display shows four or eight traces with connecting steps, then the sweep is too slow but is close to the correct speed. If the display resembles multiple downward staircase waveforms, then the sweep is far too slow. Once the timebase is adjusted, the vertical sensitivity can be adjusted (and decalibrated) so that the sixteen channels cover the entire face of the scope, giving maximum channel separation. The display should resemble that shown in Fig. 9.

(continued on page 111)

TABLE 2

STIMULUS (HEX)	COMMENT
0020	Trigger low, count counter
00A0	Trigger high, trigger scope
00A1	
00A2	
00A3	Test patterns
00A4	
00A5	
00A6	
00A7	
	Loop back to first stimulus

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You can use the display adapter to view signals that originate outside of the tester. With the test socket empty and the power supply jumpers removed, open the isolation switches and jumper the system sig-

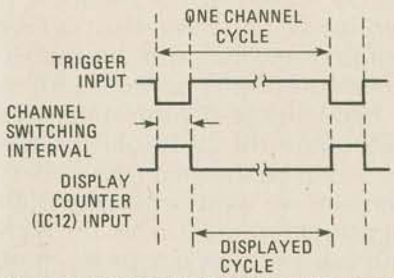

FIG. 8—THE COUNTER COUNTS on the leading edge of a logic trigger, but the scope triggers on the trailing edge. That eliminates the channel-switching lines from the display.

PARTS LIST

All resistors are ¼-watt, 5%
R3—43,000 ohms
R4—22,000 ohms
R5—11,000 ohms
R6—5600 ohms
R7—2700 ohms
R8–R12—330 ohms
R13—1500 ohms
Semiconductors
IC11—74150 1-of-16 selector/multiplexer
IC12—74LS191 binary synchronous up/down counter
IC13—7406 hex inverting buffer
IC14—7420 dual 4-input NAND gate
Other components
S17—SPST switch

should be evenly spaced, and all displayed signals should repeat themselves exactly between triggers. The qualifier can be useful in dealing with complex systems, but proper qualification hinges on your

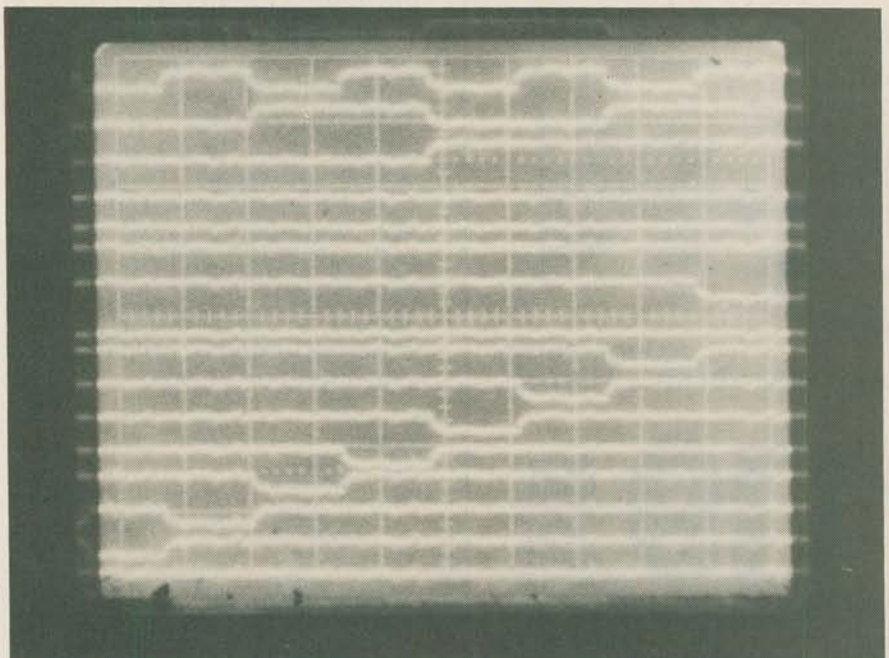

FIG. 9—THE OSCILLOSCOPE DISPLAY showing the waveforms generated by the 74LS138 test circuit. While it may not be the most eloquent logic analyzer, it can be an excellent teaching or learning tool.

nal(s) to the test socket pin(s). Bring in a suitable trigger, crank up the system, and you are ready to observe the chosen signals and their relationship to each other. Be aware that the displayed signals are now driving the additional load presented by the circuitry connected to the test socket—that includes the output drivers, the multi-channel adapter, and, perhaps, additional expansion hardware. System signals that are heavily loaded might not be able to drive that additional load.

The selection or generation of a trigger is most crucial in creating a stable and meaningful display. The trigger pulses

familiarity with the logic system. In general, under-qualified triggers tend to create brilliant but jittery displays. On the other hand, over-qualified triggers yield diminished or even non-existent displays.

In situations where trigger selection is relatively simple, the multi-channel adapter can become a tutorial aid. You can learn a lot by observing signals in a properly operating digital device. As you continue to use the adapter and really get a good "feel" for it, you will probably find many additional uses for the adapter. We'll find even more uses for the IC tester when we continue. **R-E**