More clock generators

In the last edition of Circuit File, Ray covered clock or square wave generators using transistors, op-amps and 555s. This time he covers the use of CMOS gates and the 4046B VCO chip.

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INEXPENSIVE CMOS logic ICs such as the 4001B and the 4011B can easily be used to make very inexpensive but highly versatile square-wave or 'clock' generator circuits. They can be designed to give symmetical or non-symmetrical outputs, and can be of the free-running or the gated types; in the latter case, they can be designed to turn on with either logic 0 or logic 1 gate signals, and to give either a logic 0 or a logic 1 output when in the 'off' mode. You can even use these 'cheapo' circuits as simple voltage-controlled oscillators (VCOs) or as frequency-modulated oscillators.

If you want really good VCO operation from a square-wave generator, with excellent linearity and versatility, you can turn to the slightly more expensive 4046B CMOS IC. We'll look at some applications of this chip later, but let's start by looking at some basic two-gate CMOS square-wave generator or astable circuits.

Basic two-gate astable circuits

The simplest way to make a CMOS astable circuit is to wire two CMOS inverter stages in series and use the C-R feedback network shown in Figure 1a. This circuit generates a decent square wave output and operates at about 1 kHz with the component values shown. The frequency is inversely proportional to the C-R time constant, so can be raised by lowering the values of either C1 or R1. C1 must be a non-polarised capacitor and can have any value from a few tens of pF to several uF, and R1 can have any value from about 4k7 to 22M; the operating frequency can vary from a frequency of 1 Hz to about 1 Mhz. For variable frequency operation, wire a fixed and a variable resistor in series in the R1 position.

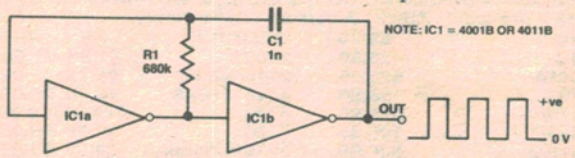

Figure 1(a). **Circuit of the basic two-gate CMOS astable. This operates at 1 kHz with the component values shown.**

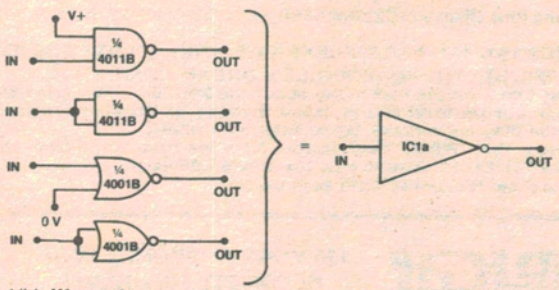

Figure 1(b). **Ways of connecting a two-input NAND (4011B) or NOR (4001B) gate for use as an inverter.**

Note at this point that each of the 'inverter' stages of the Figure 1a circuit can be made from a single gate of a 4001B quad two-input NOR gate or a 4011B quad two-input NAND gate by using the connections shown in Figure 1b. Thus each of these ICs can provide two astable circuits. Also note that the inputs to all unused gates in these ICs must be tied to one or other of the supply-line terminals; the Figure 1a astable (and all other astables shown in this feature) can be used with any supplies in the range 3 to 18 V; the 'zero volts' terminal goes to pin 7 of the 4001B or 4011B, and the '+ve' terminal goes to pin 14.

The output of the Figure 1b astable circuit switches (when lightly loaded) almost fully between the zero and positive supply rail values, but the C1-R1 junction is prevented from swinging below zero or above the positive rail levels by built-in clamping diodes at the input of IC1a. This characteristic causes the operating frequency of the circuit to be somewhat dependent on supply rail voltage. Typically, the frequency falls by about 0.8% for a 10% rise in supply voltage; if the frequency is normalised with a 10 volt supply, the frequency falls by 4% at 15 V or rises by 8% at 5 V.

Also, the operating frequency of the Figure 1a circuit is influenced by the 'transfer voltage' value of the individual IC1a gate that is used in the astable, and can be expected to vary by as much as 10% between individual ICs. The output symmetry of the waveform also depends on the 'transfer voltage' value of the IC and, in most cases, the circuit will give a non-symmetrical output. In most 'hobby' or other non-precision applications, these defects of the basic astable circuit are of little practical importance.

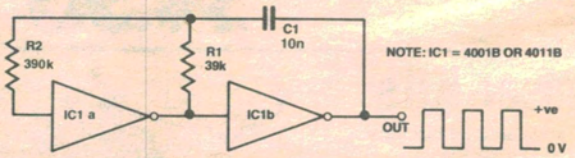

Figure 2. **This 'compensated' version of the 1 kHz astable has excellent frequency stability with variations in supply voltage.**

Some of the defects of the Figure 1a circuit can be minimised by using the 'compensated' astable of Figure 2, in which R2 is wired in series with the input of IC1a. This resistor must have a value that is large relative to R1, and its main purpose is to allow the C1-R1 junction to swing freely below the zero and above the positive supply rail voltages during circuit operation and thus improve the frequency stability of the circuit. Typically, when R2 is ten times the value of R1, the frequency varies by only 0.5% when the supply voltage is varied between 5 and 15 volts. An incidental benefit of R2 is that it gives a slight improvement in the symmetry of the output of the astable.

The basic and compensated astable circuits of Figures 1 and 2 can be built with a good number of detail variations, as shown in Figures 3 to 6. In the basic astable circuit, for example, C1 alternately charges and discharges via R1 and thus has a fixed symmetry. Figures 3 to 5 show how the basic circuit can be modified to give alternate C1 charge and discharge paths to thus allow the symmetry to be varied at will.

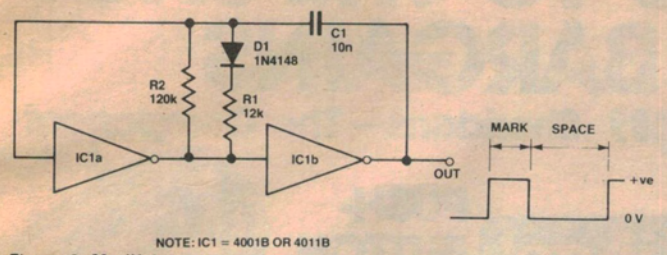

Figure 3. **Modifying the astable to give a non-symmetrical output: MARK is controlled by the parallel values of R1 and R2; SPACE is controlled by R2 only.**

The Figure 3 circuit is useful if you need a highly non-symmetrical waveform, equivalent to a fixed pluse delivered at a fixed 'timebase' rate. Here, C1 charges in one direction via R2 in parallel with the D1-R1 combination, to generate the mark or pulse part of the waveform, but discharges in the reverse direction via R2 only, to give the space between the pulses.

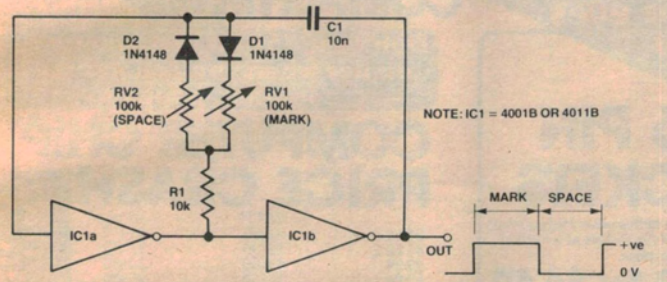

Figure 4. **This astable has independently variable MARK and SPACE times.**

Figure 4 shows the modifications for generating a waveform with independently variable mark and space times; the mark time is controlled by R1-RV1-D1, and the space time is controlled by R1-RV2-D2.

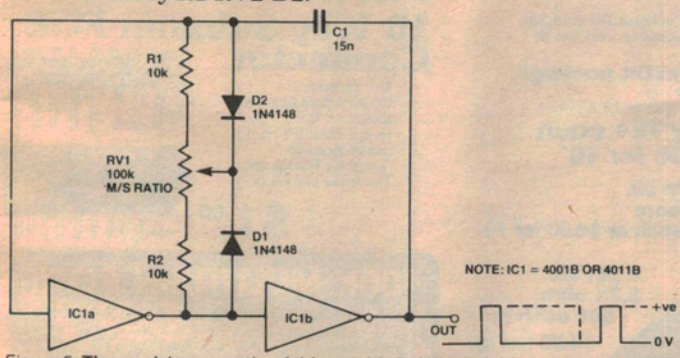

Figure 5. **The mark/space ratio of this astable is fully variable from 1:11 to 11:1 via RV1; frequency is almost constant at about 1 kHz.**

Figure 5 shows the modifications to give a variable symmetry or mark/space ratio output while maintaining a near-constant frequency. Here, C1 charges in one direction via D2 and the lower half of RV1 and R2, and in the other direction via D1 and the upper half of RV1 and R1. The M/S ratio can be varied over the range 1:11 to 11:1 via RV1.

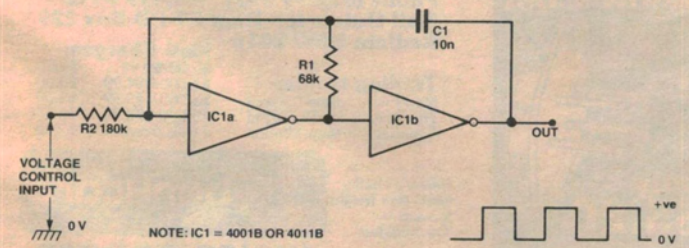

Figure 6. **Simple voltage-controlled oscillator (VCO) circuit.**

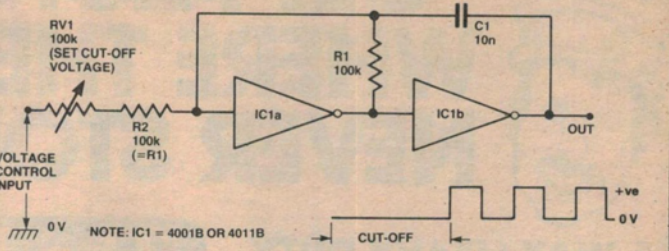

Figure 7. **Special effects VCO which cuts off when V_{in} falls below a preset value.**

Finally, Figures 6 and 7 show a couple of ways of using the basic astable circuit as a very simple VCO. The Figure 6 circuit can be used to vary the operating frequency over a limited range via an external voltage. R2 must be at least twice as large as R1 for satisfactory operation, the actual value depending on the required frequency shift range; a 'low' R2 value gives a large frequency shift range, and a 'large' R2 value gives a small frequency shift range. The Figure 7 circuit acts as a special-effects VCO in which the oscillator frequency rises with input voltage, but switches off completely when the input voltage falls below a value preset by RV1.

Gated astable circuits

All of the astable circuits of Figures 1 to 5 can be modified for gated operation, so that they can be turned on and off via an external signal, by simply using a two-input NAND (4011B) or NOR (4001B) gate in place of the inverter in the IC1a position, and by applying the input gate control signal to one of the gate input terminals. Note, however, that the 4001B and the 4011B give quite different types of gate control and output operation in these applications, as shown by the two basic versions of the gated astable in Figures 8 and 9.

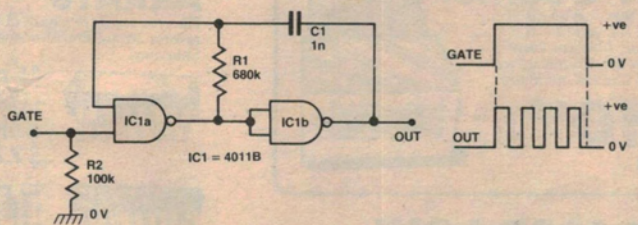

Figure 8. **This gated astable has a normally low output and is gated on by a high (logic 1) at the input.**

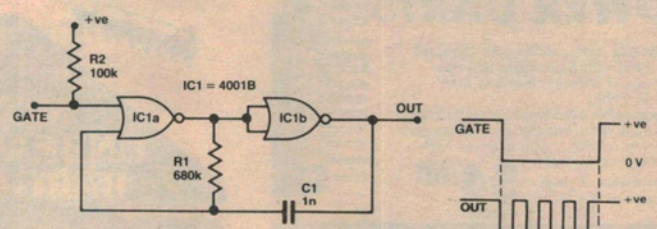

Figure 9. **This version of the gated astable has a normally high output and is gated on by a low (logic 0) at the input.**

Note specifically from these two circuits that the NAND version is gated on by a logic 1 input and has a normally low output, while the NOR version is gated on by a logic 0 input and has a normally high ouput. R2 can be eliminated from these circuits if the gate drive is direct-coupled from the ouput of a preceding CMOS logic stage, etc.

Note in the basic gated astable circuits of Figures 8 and 9 that the output signal terminates as soon as the gate drive signal is removed; consequently, any noise present at the gate terminal also appears at the outputs of these circuits. Fig- ▶

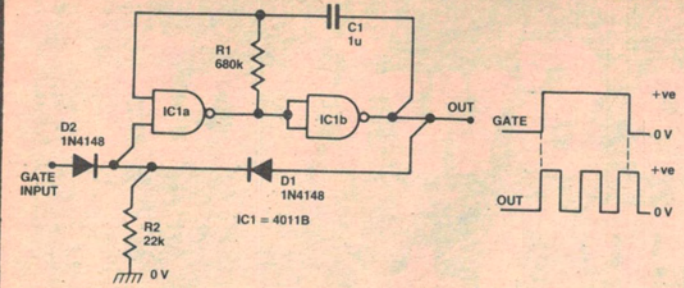

Figure 10. **Semi-latching or 'noiseless' gated astable circuit, with logic 1 gate input and normally zero output.**

ures 10 and 11 show how to modify the circuits to overcome this defect. Here, the gate signal of IC1a is derived from both the outside world and from the output of IC1b via diode OR gate D1-D2-R2. As soon as the circuit is gated from the outside world via D2 the output of IC1b reinforces or self-latches the gating via D1 for the duration of one half astable cycle, thus eliminating any effects of a noisy outside world gate signal. The outputs of the 'semi-latching' gated astable circuits are thus always complete numbers of half cycles.

'Ring of three' clock-generator circuits

The two-gate astable circuit is not generally suitable for direct use as a 'clock' generator with fast-acting counting and dividing circuits, since it tends to pick up and amplify any supply line noise during the 'transitioning' parts of its operating cycle and thus to produce square waves with 'glitchy' leading and trailing edges. A far better type of clock generator circuit is the 'ring of three' astable shown in Figure 12.

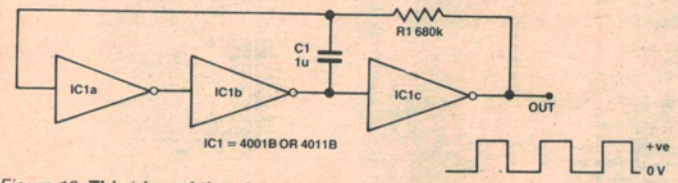

Figure 12. **This 'ring-of-three' astable makes an excellent clock generator.**

The Figure 12 'ring of three' circuit is similar to the basic two-gate astable, except that its 'input' stage (IC1a-IC1b) acts as an ultra-high gain non-inverting amplifier and its main timing components (C1-R1) are transposed (relative to the two-gate astable). Because of the very high overall gain of the circuit, it produces an excellent and glitch-free square wave output, ideal for clock-generator use.

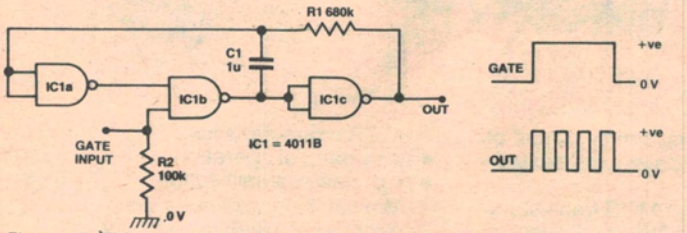

Figure 13. **This 'ring-of-three' astable is gated by a logic 1 input and has a normally low output.**

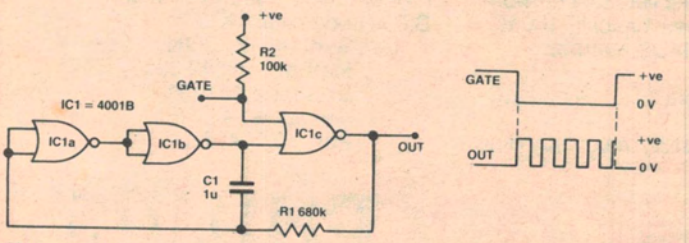

Figure 15. **Ring-of-three gated by a logic 0 input and having a normally low output.**

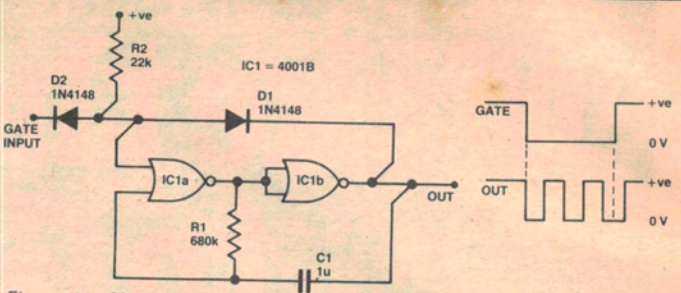

Figure 11. **Alternative semi-latching gated astable, with logic 0 gate and normally high output.**

The basic ring-of-three astable can be subjected to all the design modifications we've already looked at for the basic two-gate astable; e.g: it can be used in either basic or compensated form and can give either a symmetrical or non-symmetrical output, etc. The most interesting variations of the circuit occur, however, when it is used in the 'gated' mode, since it can be gated via either the IC1b or IC1c stages. Figures 13 to 16 show four variations on this 'gating' theme.

Thus the Figures 13 and 14 circuits are both gated on by a logic 1 input signal, but the Figure 13 circuit has a normally low output, while that of Figure 14 is normally high. Similarly, the Figures 15 and 16 circuits are both gated on by a logic 0 signal, but the output of the Figure 15 circuit is normally low, while that of Figure 16 is normally high.

4046B VCO circuits

To close this look at CMOS square wave generator circuits, let's look at some practical VCO applications of the 4046B phase-locked loop (PLL) IC. Figure 17 shows the internal block diagram and pinouts of this chip, which contains a couple of phase comparators, a VCO, a zener diode and a few other bits and pieces.

For our present purpose, the most important part of the chip is the VCO section. This VCO is a highly versatile device; it produces a well-shaped symmetrical square wave output, has a top-end frequency limit in excess of 1 MHz, has a voltage-to-frequency linearity of about 1% and can easily be 'scanned' through a 1 000 000:1 range by an external voltage applied to the VCO input terminal. The frequency of the oscillator is governed by the value of a capacitor (minimum value 50p) connected between pins 6 and 7, by the value of a resistor (minimum value 10k) wired between pin 11 and ground, and by the voltage (any value from zero to the supply voltage in use) applied to VCO-input pin 9.

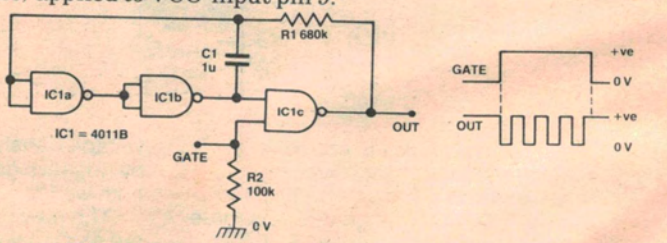

Figure 14. **This gated 'ring-of-three' astable is gated by a logic 1 input and has a normally high output.**

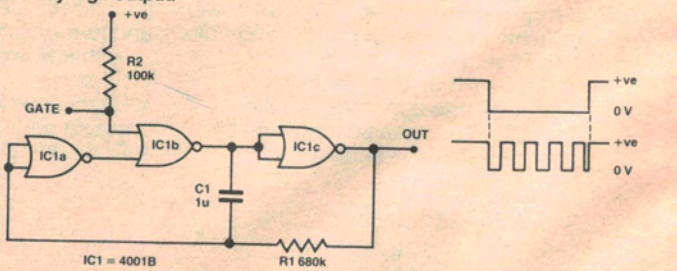

Figure 16. **Ring-of-three with normally high output and logic 0 gating.**

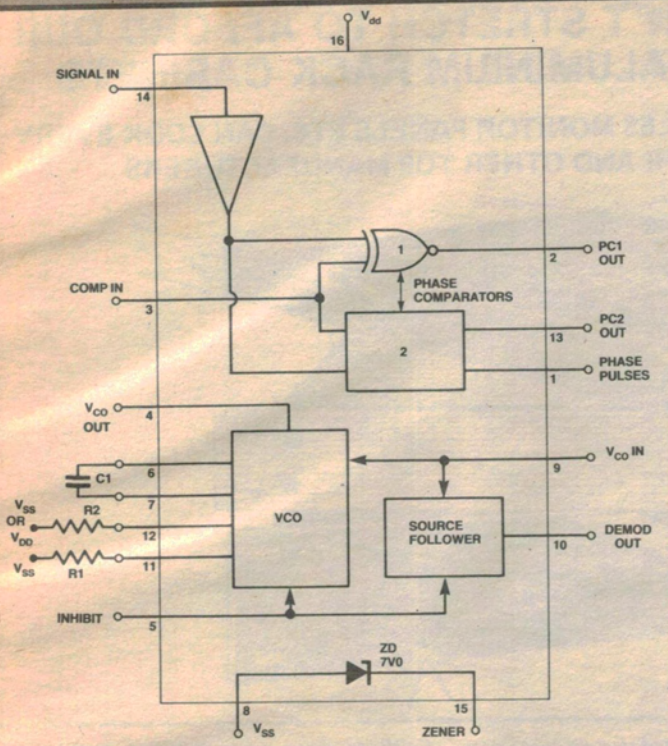

Figure 17. **Internal block diagram and pinouts of the 4046B.**

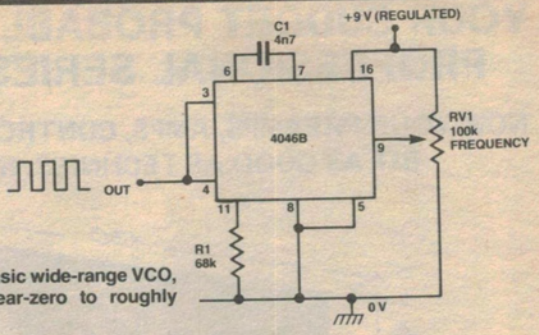

Figure 18. **Basic wide-range VCO, spanning near-zero to roughly 5 kHz.**

Figure 18 shows the simplest possible way of using the 4046B VCO as a voltage-controlled square wave generator. Here, C1-R1 determine the maximum frequency that can be obtained (with the pin 9 voltage at maximum) and RV1 controls the actual frequency by applying a control voltage to pin 9. The frequency falls to a very low value (a fraction of a Hz) with pin 9 at zero volts. The effective voltage-control range of pin 9 varies from roughly 1 V below the supply value to about 1 V above zero, and gives a frequency span of about 1 000 000:1. Ideally, the supply voltage to the circuit should be regulated.

We've said above that the frequency of the Figure 18 circuit falls to near-zero when the input voltage is reduced to zero. Figure 19 shows how the circuit can be modified so that the frequency falls all the way to zero with zero input, by wiring a high-value resistor (R2) between pins 12 and 16. Note here that when the frequency is reduced to zero, the VCO output randomly settles in either a logic 0 or a logic 1 state.

Figure 20 shows how the pin 12 resistor can alternatively be used to determine the minimum operating frequency of a restricted-range VCO. Here, f_{min} is determined by C1-R2 and f_{max} is determined by C1 and the parallel resistance of R1 and R2.

Figure 21 shows an alternative version of the restricted-range VCO, in which f_{max} is controlled by C1-R1 and f_{min} is determined by C1 and the series combination of R1 and R2. Note that by suitable choice of the R1 and R2 values, the circuit can be made to 'span' any desired frequency range from 1:1 to near-infinity.

Finally, it should be noted that the VCO section of the 4046B can be disabled by taking pin 5 of the package high (to logic 1 level) or enabled by taking pin 5 low. This feature makes it possible to gate the VCO on and off by external signals. Thus Figure 22 shows how the basic VCO circuit can be gated via a signal applied to an external inverter stage. Alternatively, Figure 23 shows how one of the internal phase comparators of the 4046B can be used to provide gate inversion, so that the VCO can be gated via an external voltage applied to pin 3. ●

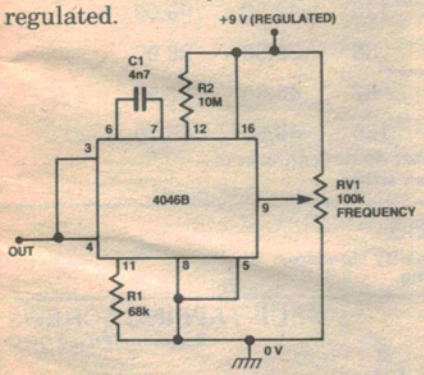

Figure 19. **Modification of the Figure 18 circuit takes it all the way down to zero.**

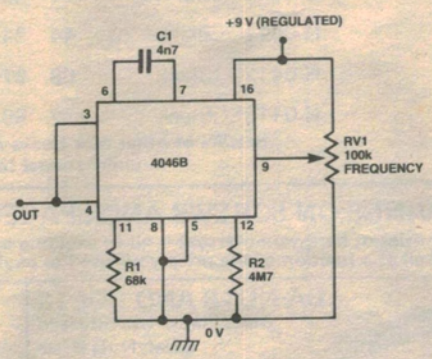

Figure 20. **Restricted-range VCO, with frequency variable from roughly 72 Hz to 5 kHz via RV1.**

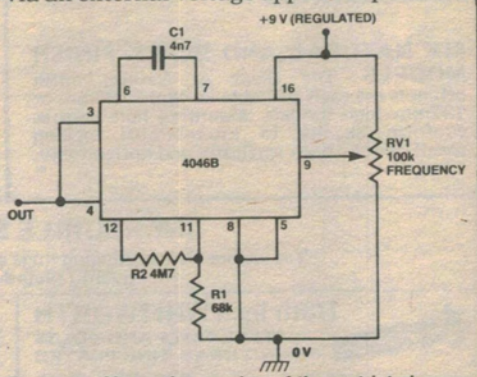

Figure 21. **Alternative version of the restricted-range VCO. Maximum frequency is controlled by C1-R1, minimum by C1-(R1+R2).**

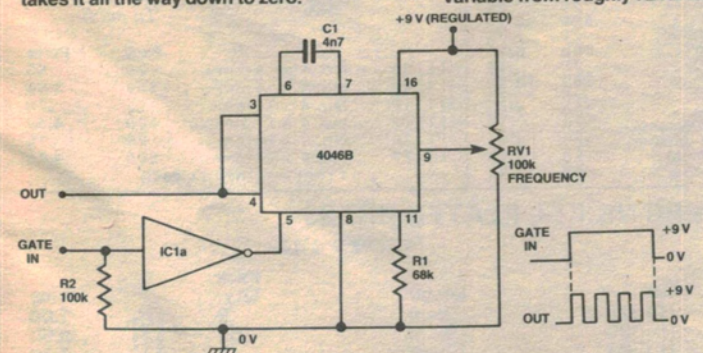

Figure 22. **Gated wide-range VCO using an external gate inverter.**

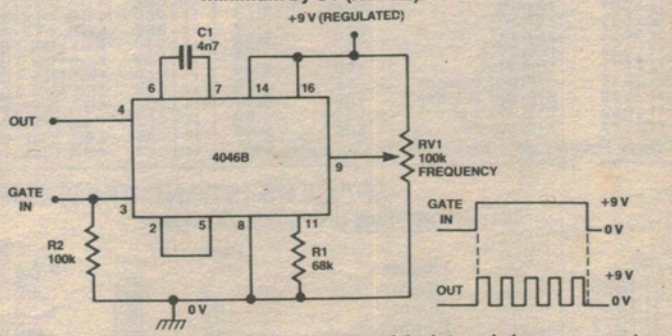

Figure 23. **Gated wide-range VCO using one of the internal phase comparators as a gate inverter.**