University of California at Berkeley

Physics 111 Laboratory
Basic Semiconductor Circuits (BSC)

Lab 5

JFET Circuits II

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References:

Hayes & Horowitz	Chapter 3
Horowitz & Hill	Chapter 3

In this lab you will investigate some more sophisticated JFET circuits, such as voltage amplifiers, differential amplifiers, attenuators, and modulators.

Before coming to class complete this list of tasks:

- Completely read the Lab Write-up
- Answer the pre-lab questions utilizing the references and the write-up
- Perform any circuit calculations or anything that can be done outside of lab.
- Plan out how to perform Lab tasks.

Pre-lab questions:

1. Explain in detail how a signal applied to the gate of one transistor in a differential amplifier can produce an output on the drain of the other transistor.
2. What are parasitic oscillations? How do you minimize them?

Do not forward bias the JFET gates. Forward gate currents larger than 50mA will burn out the JFETs Use a Heat Sink on the JFETs.

The Laboratory Staff will not help debug any circuit whose power supplies have not been properly decoupled!

Background
Voltage Amplifiers

Adding a drain resistor R_D to a source-follower turns it into a voltage amplifier, as shown to the right.
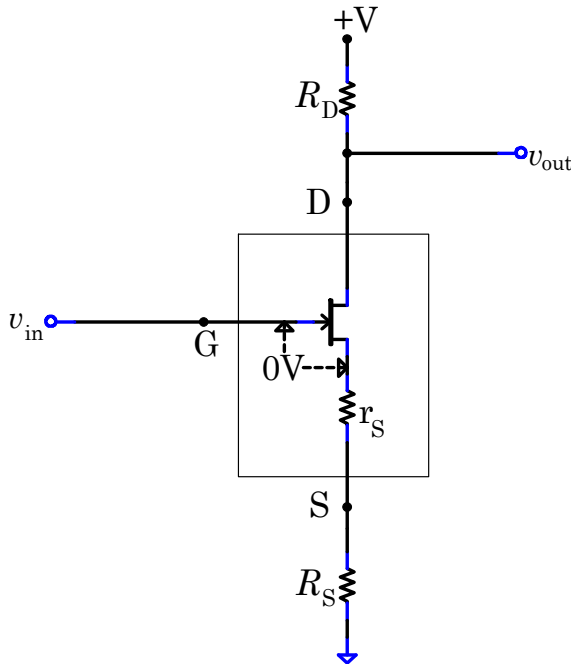
The equivalent small signal circuit for the amplifier is shown to the left and is most easily understood by remembering that the current in a source follower is given by

$$i = \frac{v_{in}}{R_S + r_S},$$

where $r_s = 1/g_m$. Since this current is unchanged by the addition of the drain resistor, the output voltage will be

$$v_{out} = -R_D i = -\frac{R_D}{R_S + r_S} v_{in}.$$

Thus the gain of the amplifier is

$$G = -R_D/(R_S + r_s) \approx -R_D/R_S, \qquad (1)$$

where the last equality assumes that the transconductance is high.

As with the source follower, the input current is given by the gate leakage current, so the amplifier's input impedance is extremely high. The output impedance of the amplifier equals the drain resistance R_D, and unlike the output impedance in the follower circuit, it is not low.
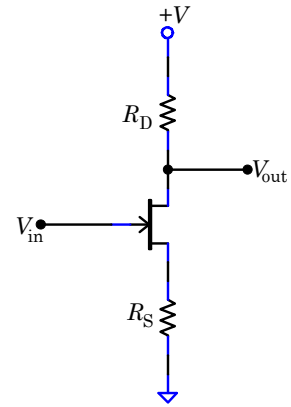
Differential Amplifiers

Differential amplifiers have two inputs, V_+ and V_-, and one or two outputs.

In an ideal differential amplifier, the amp's output depends solely on the difference between the two inputs, $V_\Delta = (V_+ - V_-)/2$. Thus $V_{out} = GV_\Delta$. Unfortunately, the output of any real differential amplifier also depends weakly on the average of the two inputs. This average, $V_C = (V_+ + V_-)/2$, is called the common mode of the amp.
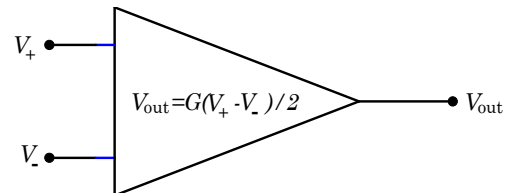
Differential amplifiers are one of the most common building blocks in analog circuit design. The front end of every op amp, for example, consists of a differential amplifier. Differential amplifiers are used whenever a desired signal is the difference between two signals, particularly when this difference is masked by common mode noise. A typical example is an electrocardiogram. The heart generates electrical signals, which can be detected by electrodes placed against the skin, but the signal from a single electrode would be swamped by background pickup. As you know from touching the oscilloscope input, the body is an excellent antenna for noise in frequencies ranging from 60Hz to 100MHz. Fortunately these undesired signals are nearly equal everywhere on the body. By using two pickups, placed so that the signal from the heart has opposite sign, and amplifying them in a differential amplifier, the desired signal from the heart can be preferentially amplified over the unwanted noise.

Differential amplifiers are constructed from a matched pair of transistors as shown to the lower left.

The drain of either transistor can be used as the output; in some cases both JFET drains are used to provide a differential output.[1]
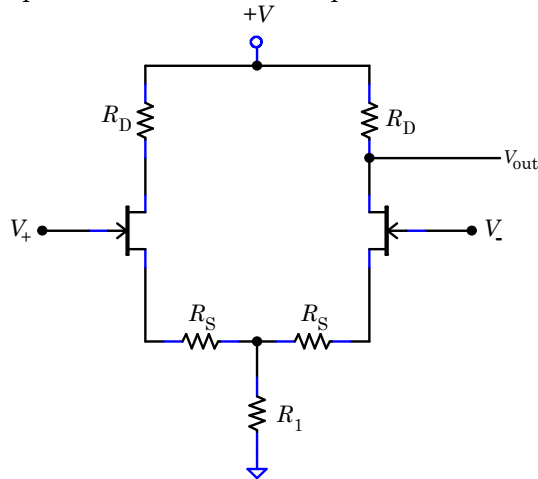
The amplifier's low common mode gain is immediately apparent by redrawing the circuit below:
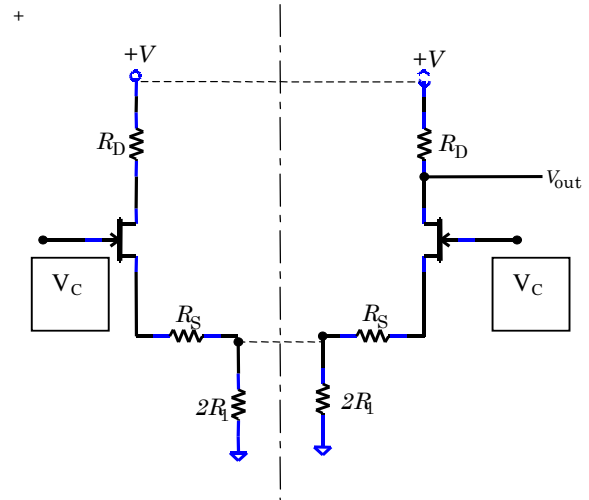
Since the transistors are identical, and since a common mode drive impresses the same signal on both transistors, both halves of the circuit will behave identically. Thus the common mode gain will be given by Eq. (1):

$$\frac{R_D}{2R_1 + R_S + r_S} .$$

(Note that the common resistor R_1 splits into two parallel resistors of twice the original value.) In practice, the common resistor R_1 is always made much greater than the source resistors, so the gain reduces to $R_D/2R_1$. As R_1 is also made much larger than the drain resistor R_D, common mode signals are strongly attenuated.

The response of the two transistors to a small differential signal V_Δ, on the other hand, will be equal and opposite. The net current flow I_o through, and voltage drop across, the common resistor will not change. Consequently the common resistor can be replaced with a voltage source of strength $R_1 I_o$:

Equation 1 yields the differential gain

$$\frac{R_D}{R_S + r_S} .$$

If R_D is chosen to be much greater than the source resistors, the differential gain can be quite large. The total V_{out} is the sum of V_{out-C} and $V_{out-\Delta}$.
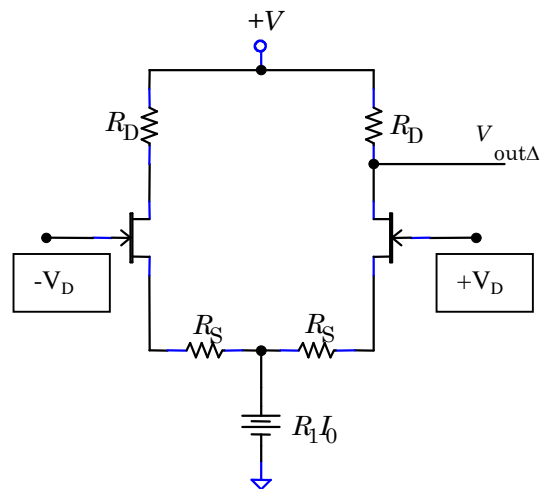
What happens if a signal is applied to just one input and the other is grounded? The signal can be decomposed into its common and differential components. For a signal applied solely to the V_+ input, the common mode signal will be $V_C = V_+/2$ and the differential signal will be $V_\Delta = V_+/2$. (Note how $V_- = V_C - V_\Delta = 0$.) The gain for this single input will be half the differential gain: $R_D/2(R_S + r_s)$.
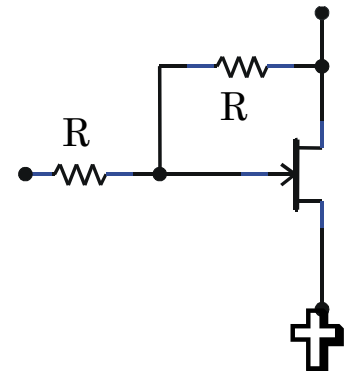
JFET Linearization

The linear-regime resistance R_{DS} between a JFET's drain and source is given by

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[1] Two outputs of opposite phase.

$$\frac{1}{R_{DS}} = 2k\left[\left(V_{GS} - V_P\right) - \frac{V_{DS}}{2}\right],$$

where k is a parameter that depends on the individual JFET, V_P is the voltage where the JFET first conducts (the pinch-off, or threshold voltage), and V_{DS} is the voltage between the drain and the source. This formula is derived in books on JFET physics.

The relationship between V_{DS} and I_D would be perfectly linear if it were not for the dependence of R_{DS} on V_{DS}. But linearity can be restored by adding a signal equal to $V_{DS}/2$ to the gate. This can be done by adding two resistors to the gate circuit as shown to the right.
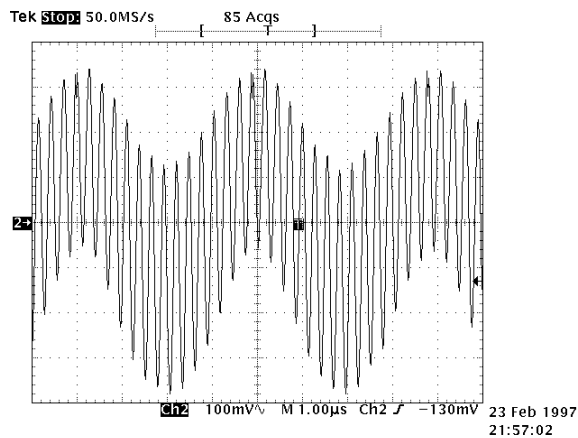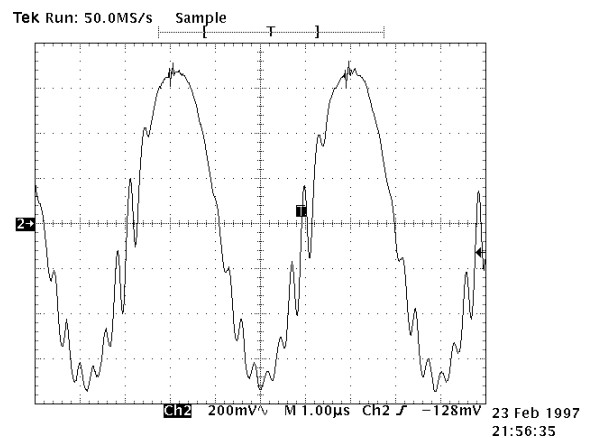
Parasitic Oscillations

Tek Run: 200MS/s ET Average

Ch2 100mV M 250ns Ch4 ƒ −130mV   23 Feb 1997
21:42:53
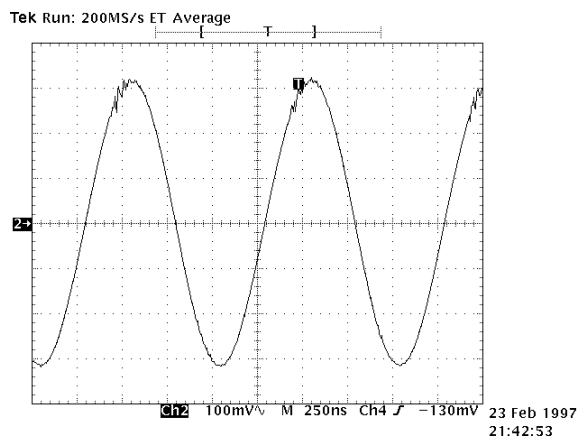
Parasitic oscillations are unwanted, high frequency oscillations caused by unintended positive-feedback loops. The loops are closed by unintended capacitive coupling between two neighboring wires. Because the oscillations normally occur at very high frequencies (1 to 100MHz), capacitances of only a few picofarads are sufficient to cause oscillations. Parasitic oscillations often first appear as "hair" on an otherwise undistorted signal. For example, in the scope trace on the left, the small oscillations at the top of the original sine wave are due to parasitic oscillations.

Larger parasitic oscillations may cover a substantial fraction of the signal, as shown to the right, or they may completely dominate the signal, as shown below.

Tek Run: 50.0MS/s   Sample

Ch2 200mV M 1.00µs Ch2 ƒ −128mV   23 Feb 1997
21:56:35

Tek Stop: 50.0MS/s   85 Acqs

Ch2 100mV M 1.00µs Ch2 ƒ −130mV   23 Feb 1997
21:57:02

Touching the circuit, or even waving your hand near the circuit, can either accentuate or suppress the os-
cillations.

There are no hard and fast rules for eliminating parasitic oscillations, but clean circuit layout goes a long way. Keep your leads short and un-jumbled. Lay your signals out from

left to right, and keep large[2] output signals away from small input signals. Believe it or not, beautifully wired circuits work better!

Unfortunately not even clean circuit layouts will always suppress the oscillations. At very high frequencies, the internal capacitances inside components, aided by the inductances formed by the component leads, can cause oscillations. An additional feedback route is through the power supplies themselves. ***Frequently parasitic oscillations can be tamed by liberally adding "decoupling" capacitors across the power supply.*** The decoupling capacitors function by providing a low impedance path to ground at high frequency, thereby shorting out the high frequency oscillations. To be effective, decoupling capacitors should placed close to the circuit components. Try placing 0.1µf capacitors between +12V and ground, –12V and ground, and between +12V and –12V. Vary the locations of the capacitors, and use more than one, until the oscillations go away. Don't be greedy; a 1 or 10µf capacitor will *not* work better than a 0.1µf capacitor. In fact, the larger internal inductances of large capacitors may well make them work worse than smaller capacitors.[3]

Packaging and Leads

Transistors are manufactured in many different packages and sizes. Ours come in a metal can. The leads are arranged in a triangle; the gate lead is the first lead clockwise from the tab when looking down (onto the can end, not the lead end) on the JFET.
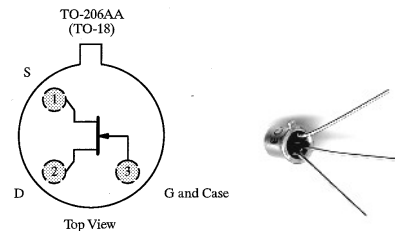
When inserting the JFET into the breadboard, there is not need to squash the leads out horizontally. In fact, doing so risks accidentally shorting the leads to the case. ***Instead, just bend them out gently so that they form a triangular pattern, which will insert into the transistor sockets on the breadboard.***

Many JFETs, including the 2N4392, are symmetrically constructed. The source and drain can be exchanged without changing the device behavior. But for simplicity, use the correct source and drain leads. Asymmetric JFETS, in which the source and drain cannot be exchanged, are normally drawn with an offset gate lead.
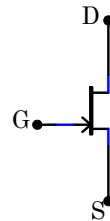
In the lab
(A) Amplifiers

5.1 ✍ Construct the amplifier below.

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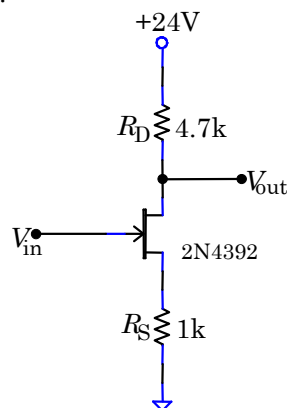
[2] Parasitic oscillations generally, but not always, require circuits with gain. The followers that we built in last week's lab were relatively immune from oscillating.

[3] This is particularly true of electrolytic capacitors.

What are the equilibrium voltages and currents in the circuit (V_{GS}, V_{DS}, V_{out}, I_{DS})? (Note no signal is applied for this) Drive the amplifier with a 10kHz, 1V p-p sine wave, and look at its output on the scope. What is the amp's gain? Does it agree with the predicted value? What is the maximum undistorted output amplitude? (Note: vary the input voltage for this) What limits the amplitude?
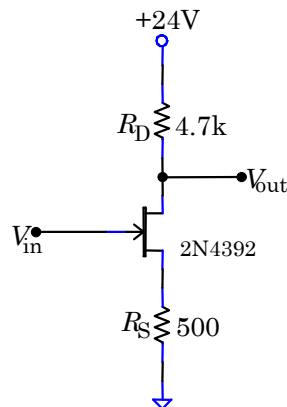
Cool the JFET with circuit cooler. How much does the gain change? Obtain four other JFETs. Measure and record the gain for each JFET.

5.2 The gain in 5.1 is low. A naïve application of the gain formula [Eq. (1)] would imply that the gain should increase substantially if the drain resistor is changed to 47k.
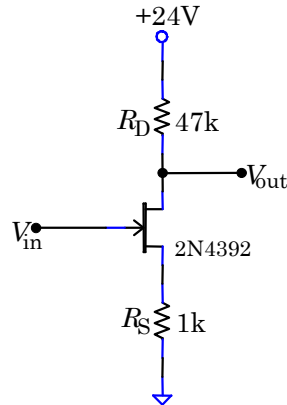
What actually happens? Why? (Hint: Look at V_{DS} again).

5.3 Equation (1) suggests that decreasing the source resistor will also increase the gain. Try the circuit below.


What is the gain now? What is the maximum undistorted output amplitude?

Cool the JFET with circuit cooler. How much does the gain change? Measure and record the gain for the other four JFETs. Why is the fractional variation in the gain larger for this circuit than for the circuit in 5.1?

The behavior of a well-designed circuit should not depend on temperature or on the parameters of its particular components. Consequently, 5.3's circuit is not very useful. The point of this section is to show you that circuit design is not as simple as plugging in to a formula and getting a useful circuit out. If you want more information on this subject, look under hybrid parameters and modular circuit design.
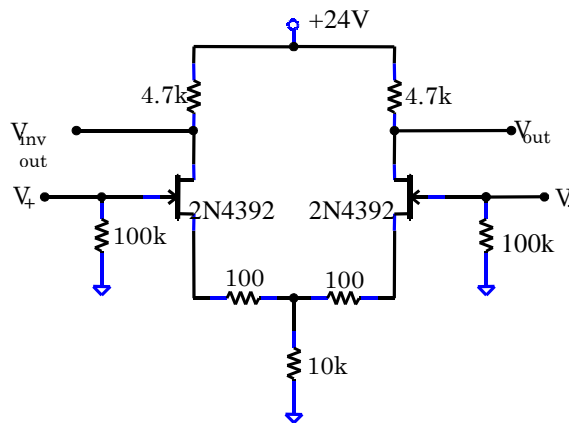
6.4 Bypassing the source resistor will also increase the gain.
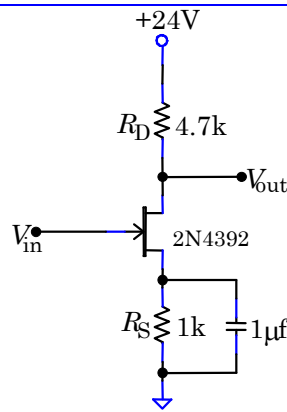
What is the gain now, experimentally, and theoretically? Is it frequency dependent? Why does the capacitor increase the gain? Is it as temperature dependent as the circuit in 5.3?

(B) Differential Amplifiers

**5.5** ✍ Build the differential amplifier below using your matched pair of JFETs from Lab 5.

Leaving the V_- input attached only to its 100k resistor, drive the V_+ input with a 1kHz, 0.1Vp-p sine wave. Measure the amplitude and phase of the output signal V_{out}. Look at V_{invout}; what is the signal there? Reverse the setup; drive the V_- input. What are the amplitude and phase at V_{out}? What about at V_{invout}?

Now drive V_+ and V_- with identical signals. What is the common mode gain?

If your circuit does not work, particularly if only one branch of the circuit works slightly and the other not at all, it is likely that the JFETs are not sufficiently well matched. Explore this effect by temporarily replace one of the JFETs with an unmatched JFET. Does the circuit still work? If it doesn't, why not? Hint-measure the voltage drop across both drain resistors.

5.6 Differential amplifier performance is vastly improved by replacing the common source resistor with a current source. Make all the measurements in 6.5 with the circuit below.
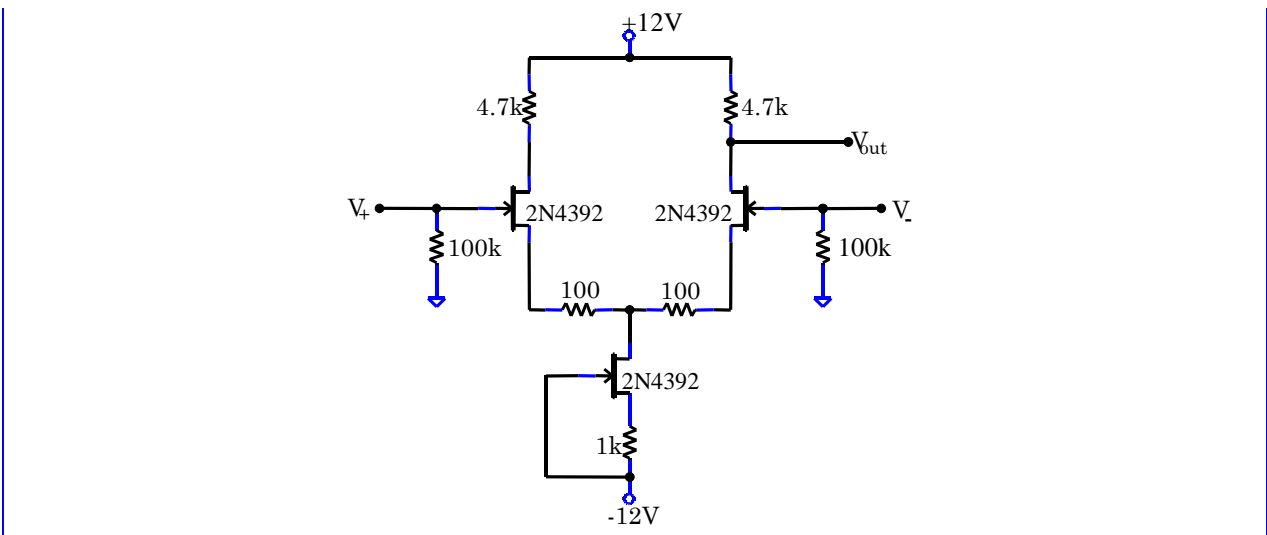
(C) JFET Attenuator

5.7 Build the JFET attenuator shown below.
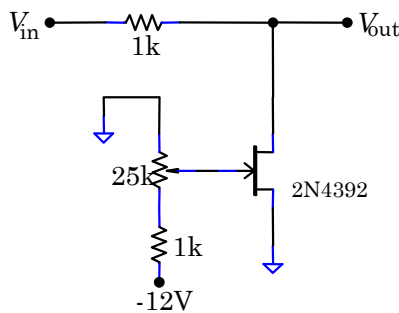
Drive the circuit with a 1kHz, 0.1Vp-p *triangle* wave. Vary the output amplitude with the potentiometer. Is the circuit linear (i.e. is the output still a triangle wave)? With the potentiometer set to produce a signal ¾ as large as the input, what is the largest input signal passed relatively undistorted?

5.8 Add two 100k resistors to linearize the attenuator.
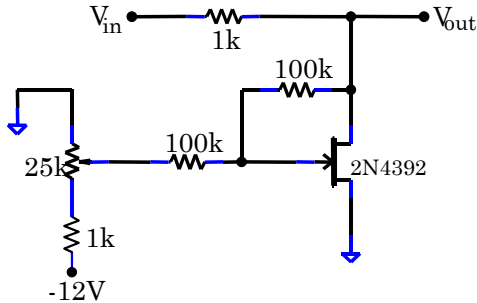
With the potentiometer set as described in **5.7**, what is the largest input signal passed relatively undistorted? Now set the potentiometer for the greatest attainable attenuation. Calculate the lowest possible JFET drain-source resistance corresponding to this setting.

(D) JFET Modulator

5.9 The circuit in 5.8 can be used to amplitude modulate (AM) a carrier wave. Use as an input carrier wave a 1Vp-p sine wave of about 1MHz with the circuit modification below.
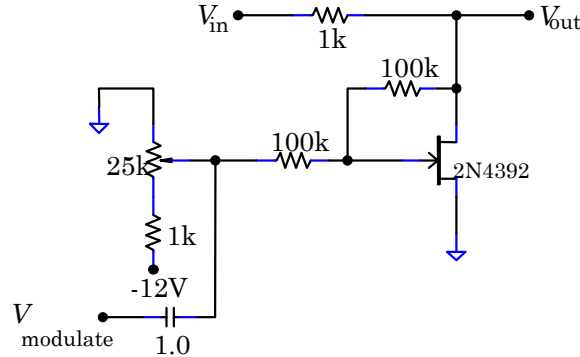
Add in a 1kHz 1Vp-p sine wave from another wave generator to the potentiometer signal through the V_{modulate} input. Set the potentiometer so that the carrier is modulated by the 1kHz wave. Sketch V_{out}.

5.10 ✎ Attach a 2-meter long wire to the output of the modulator. Obtain an AM radio, and tune it to a quiet frequency in the AM band. Adjust the high frequency carrier signal until you can hear the 1kHz tone coming from the radio. Then replace the modulating signal from the wave generator with the T1 audio signal from the distribution box. Listen to the radio. You have built a low power AM transmitter!

Analysis

5.11 What are the common mode and differential gains for a differential amplifier built with a current source? Hint-You will have to assume a stiffness (or Z_{out}) for the source.

(E) Surprise Circuit

5.12 Build the following circuit. What does it do and why?
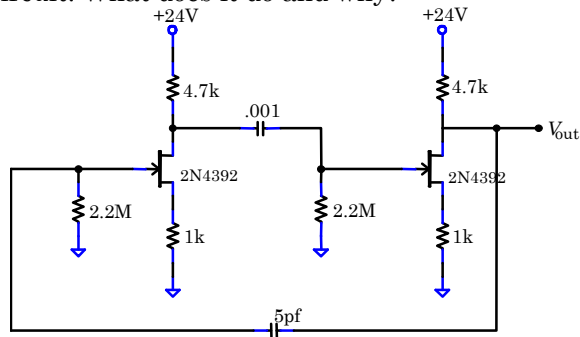

(F) Phase Splitter

5.13 Design and build a unity gain phase splitter: a circuit that splits an input signal into two signals of equal magnitude and opposite phase. Maximize the undistorted output amplitude of your circuit. Hint: there is an easier and more accurate way to construct this circuit than with a differential amplifier.

(G) High Gain Amplifier

5.14 With a careful design employing feedback, it is possible to make a high gain amplifier that is almost temperature and component independent. After completing 6.15, finish the design of the circuit below by specifying the values of all the resistors and capacitors.
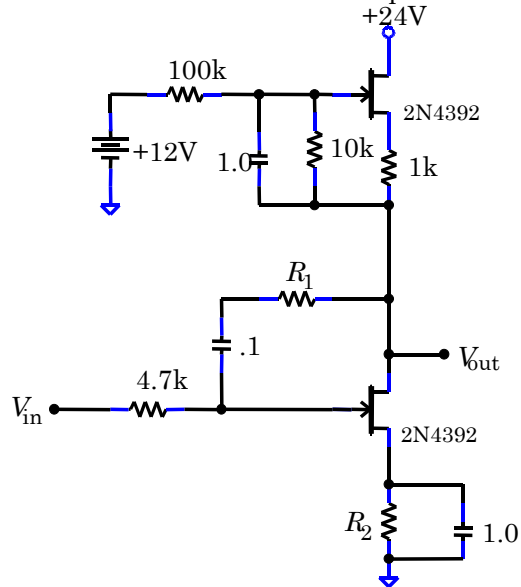
Aim for a feedback controlled gain of approximately 40.

Construct the circuit, and measure the gain. You will find that the gain is somewhat less than that predicted by the feedback ratio. Work out an expression for the gain that includes the transconductance of the JFET and the finite stiffness of the current source. Insert and measure the gain for several different JFETs. Is the circuit relatively independent of the particular JFET? Is the circuit temperature dependent?

5.15 In the circuit of 5.14, identify the components that perform the following functions, and explain how each function is accomplished:

1. Sets the gain through feedback.
2. Acts as a current source to increase the gain.
3. Increases the open-loop gain by providing an AC bypass.
4. Sets the current through the JFETs.
5. Assures that the drain source voltage across both JFETs is approximately 12V, independent of the particular parameters of each JFET.
6. Increases the stiffness of the current source by providing a bypass for AC signals.

The manual for Lab 6 may help you answer these questions.

Physics 111 ~ BSC   *Student Evaluation of Lab Write-Up*

Now that you have completed this lab, we would appreciate your comments. Please take a few moments to answer the questions below, and feel free to add any other comments. Since you have just finished the lab it is *your* critique that will be the most helpful. Your thoughts and suggestions will help to change the lab and improve the experiments.

Please be specific, use references, include corrections when possible, and *turn this in with your lab report*. Thank you!

Lab Number: _____ Lab Title: _____ Date: _____

Which text(s) did you use?

How was the write-up for this lab? How could it be improved?

How easily did you get started with the lab? What sources of information were most/least helpful in getting started? Did the pre-lab questions help? Did you need to go outside the course materials for assistance? What additional materials could you have used?

What did you like and/or dislike about this lab?

What advice would you give to a friend just starting this lab?

The course materials are available over the Internet. Do you (a) have access to them and (b) prefer to use them this way? What additional materials would you like to see on the web?