JFET AC Analysis

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Nov 17, 2001, Sept. 22, 2008

Introduction

This note will discuss AC analysis using the g_m JFET model shown in Figure 1 for the three types of amplifiers: common-source, common-gate, and common-drain. For each type of amplifier the goal is to determine the input resistance, r_{in}, output resistance, r_o, and voltage gain. The voltage gain may be either the unloaded stage gain, the loaded stage gain, or the net voltage gain depending on what is needed. The analysis is simplified by first developing general equations for the AC terminal resistances of the JFET and then using this result to compute the input and output resistances of each of the three amplifier types.

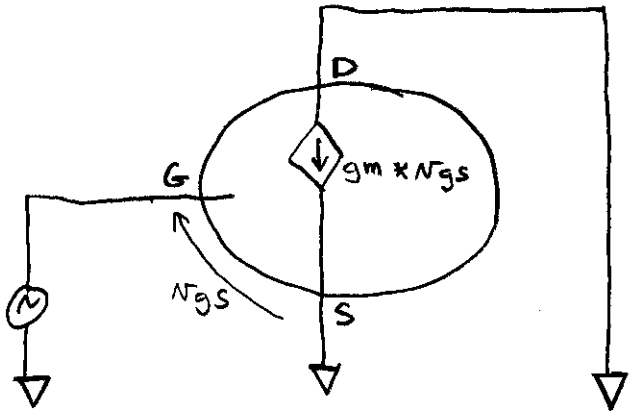

Figure 1: Simple AC model for JFET

Before proceeding with AC analysis, we must have a value for g_m. The transconductance, g_m, of the JFET is determined by first performing a bias analysis to calculate the drain current, I_D for a given I_{DSS} and V_P for the JFET. Note that the parameters, I_{DSS} and V_P, vary widely for any given type of JFET so both the bias analysis and AC analysis must be performed for each set of I_{DSS} and V_P of interest.

The g_m of a JFET is calculated by

$$g_m = | 2 * \text{sqrt}(I_D * I_{DSS}) / V_P| \qquad \text{Eq. 1}$$

Note the absolute value is used to make the calculation independent of whether an N-channel or P-channel JFET is being used since g_m is always a positive quantity.

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AC terminal resistances

The first step in AC analysis is to develop equations that give us the AC resistance looking into each transistor terminal. The result of these calculations will enable us to easily calculate the input and output resistances of transistor amplifiers including the bias circuit. The g_m model and standard circuit is shown in Figure 2. We define one set of AC resistances looking out of the transistor terminals and another set of AC resistances looking into the transistor terminals. Each of these is easy to calculate.

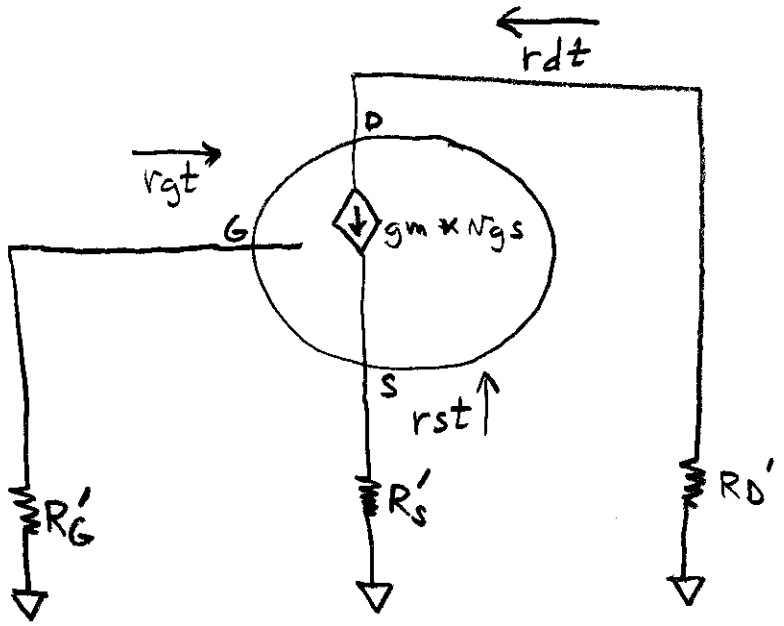

Figure 2: JFET AC terminal resistances

Any combination of resistances can be reduced to a single resistor. In order that we do not have to be concerned about the specific resistors in the external circuit for our analysis, the external circuit is reduced to three resistances, R_G', R_S', and R_D'. These are the external AC resistances seen looking out of the particular terminal of the transistor.

For the three types of amplifiers, R_G', R_S', and R_D' will consist of external resistance combinations different for each amplifier type. In all cases, it should be obvious how to compute these resistances. Simply imagine yourself looking out of the specific transistor terminal and seeing the net AC resistance to ground. For example, for the common-source amplifier, R_G' may be R_G (or the parallel combination of the voltage divider bias resistors, R_{G1} and R_{G2}) also in parallel with R_A since the coupling capacitor is an AC short. R_S' may be R_S in parallel with R_{S1} for a common-source circuit or R_S in parallel with R_L in a common-drain circuit. R_D' may be R_D in parallel with R_L for common-source and common-gate circuits. For the common-gate circuit, R_S' is generally just R_S. The point is that no matter what the external circuit, it will be reduced to a single resistance representing the AC resistance. For this process, all coupling and bypass capacitors are treated as short circuits to AC which in fact they are at the signal frequencies we are using.

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The AC resistances looking into the terminals of the transistor are called r_{gt}, r_{st}, and r_{dt}. Just to clarify the nomenclature, r_{gt} is the AC **r**esistance looking into the **g**ate **t**erminal. Note that r_{gt} does not include R_G', r_{st} does not include R_S', and that r_dt does not include R_D'.

Calculation of r_{gt}

Since the gate to channel junction is reversed biased the impedance seen looking into the gate terminal is extremely high. For all practical purposes, we take this impedance to be infinity. In reality, it may be in the region of $1x10^8$ to over $1x10^{10}$ Ohms.

r_{gt} = infinity Eq. 2

Calculation of r_{st}

$r_{st} = v_s / (-i_d)$ By Ohm's law. Negative because i_d is defined as positive for current leaving the source. We are looking in. Eq. 3

$r_{st} = 1/g_m$ Since g_m is i_d/v_s Eq. 4

Calculation of r_{dt}

$r_{dt} = v_d / i_d$ By Ohm's law Eq. 5

$i_d = 0$ We note that $i_d = 0$ because $v_{gs} = 0$ Eq. 6

r_{dt} = infinity This should not be surprising since we are looking into a current source. A more complete model of the JFET would show that r_{dt} is generally between about 30,000 and 1,000,000 Ohms. Eq. 7

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Calculation of Input Resistance, Output Resistance, and Voltage Gain

We are now ready to use r_{gt}, r_{st}, and r_{dt} to perform specific AC analysis for each of the three types of amplifiers. Note that the impedance calculations can now be performed by inspection.

Common-Source analysis

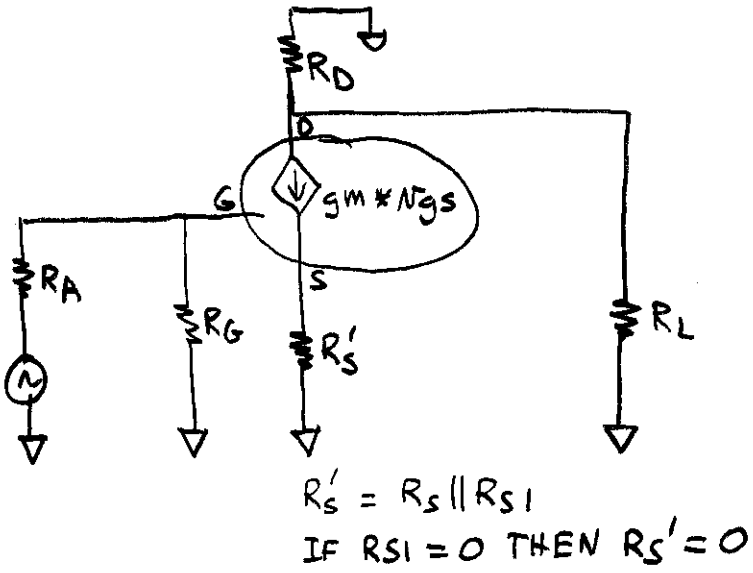

Figure 3: Common-source AC model

$r_{in} = R_G \| r_{gt} = R_G$ since r_{gt} = infinity Eq. 8

$r_o = R_D \| r_{dt} = R_D$ since we are taking r_{dt} to be infinity Eq. 9

To find the voltage gain, we note that:

$v_d = -i_d * R_D = -g_m * v_{gs} * R_D$ Eq. 10

$v_s = i_d * R_S' = g_m * v_{gs} * R_S'$ Eq. 11

$$v_g = v_s + v_{gs}$$
$$= g_m * v_{gs} * R_S' + v_{gs}$$
$$= v_{gs} * (1 + g_m * R_S')$$ Eq. 12

Noting that voltage gain is v_d/v_g, then from Equations 10 and 12 we can write:

$$Av = \frac{-g_m * R_D}{1 + g_m * R_S'}$$ Eq. 13

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The voltage gain is negative because the output signal is inverted from the input signal.

The output voltage division factor is $R_L / (r_o + R_L)$. Using $r_o = R_D$, the load gain is

$$Avl = \frac{-g_m * R_D}{1 + g_m * R_S'} * \frac{R_L}{R_D + R_L} \qquad \text{Eq. 14}$$

The input voltage division factor is $r_{in} / (R_A + r_{in})$. For most JFET amplifier circuits this voltage division factor is practically 1 since R_G is usually much greater than R_A. The net voltage gain from the source to the load is:

$$Avn = \frac{R_G}{R_A + R_G} * \frac{-g_m * R_D}{1 + g_m * R_S'} * \frac{R_L}{R_D + R_L} \qquad \text{Eq. 15}$$

Common-Gate Analysis

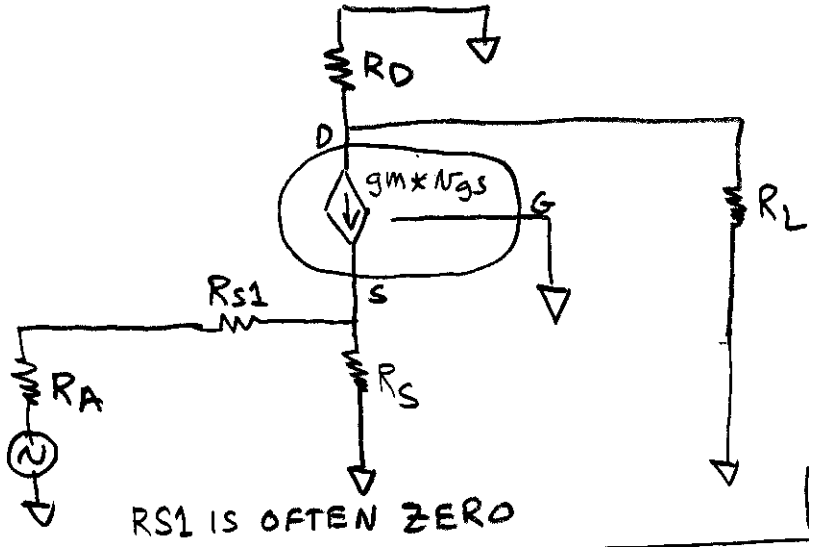

Figure 4: Common-gate AC model

$$r_{in} = R_S \| r_{st} = R_S \| (1/g_m) = R_S / (1 + g_m * R_S) \qquad \text{Eq. 16}$$

$$r_o = R_D \| r_{dt} = R_D \qquad \text{Eq. 17}$$

To find the gain we note that:

$$v_{gs} = -v_{in} \qquad \text{Eq. 18}$$

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$v_o = v_d = -i_d * R_D$ Eq. 19

$i_d = g_m * v_{gs}$ Eq. 20

$v_o = g_m * v_{gs} * R_D$ Eq. 21

Thus, noting that gain is v_o/v_{in} we can write:

$Av = g_m * R_D$ Eq. 22

Considering the output voltage division we can write:

$$Avl = \frac{g_m * R_D}{1} * \frac{R_L}{R_D + R_L}$$ Eq. 23

Including the input voltage division factor, the net gain from signal source to output is:

$$Avn = \frac{r_{in}}{R_A + r_{in}} * \frac{g_m * R_D}{1} * \frac{R_L}{R_D + R_L}$$ Eq. 24

Common-Drain analysis

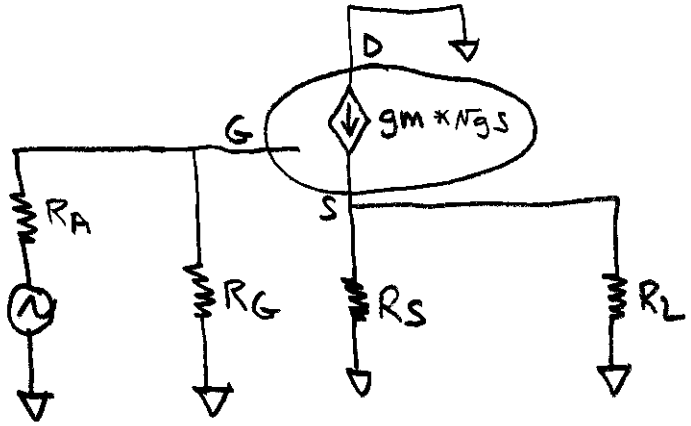

Figure 5: Common-drain AC model

$r_{in} = R_G || r_{gt} = R_G$ since r_{gt} = infinity Eq. 25

$r_o = R_S || r_{st}$
$= R_S || (1/g_m)$
$= R_S / (1 + g_m * R_S)$ Eq. 26

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To calculate gain we note that:

$$v_o = v_s = i_d * R_S = g_m * v_{gs} * R_S \qquad \text{Eq. 27}$$

$$\begin{aligned} v_{gs} &= v_{in} - v_o \\ &= v_{in} - i_d * R_S \\ &= v_{in} - g_m * v_{gs} * R_S \end{aligned} \qquad \text{Eq. 28}$$

Thus,

$$v_{in} = v_{gs} * (1 + g_m * R_S) \qquad \text{Eq. 29}$$

Noting that voltage gain is v_o/v_{in} we can write:

$$Av = \frac{g_m * R_S}{1 + g_m * R_S} \qquad \text{Eq. 30}$$

Including the output voltage division factor we can write:

$$Avl = \frac{g_m * R_S}{1 + g_m * R_S} * \frac{R_L}{r_o + R_L} \qquad \text{Eq. 31}$$

By factoring in the output impedance, Equation 31 can also be written as

$$Avl = \frac{g_m * R_S||R_L}{1 + g_m * R_S||R_L} \qquad \text{Eq. 32}$$

The net loaded gain from signal source to load is:

$$Avn = \frac{R_G}{R_A + R_G} * \frac{g_m * R_S||R_L}{1 + g_m * R_S||R_L} \qquad \text{Eq. 33}$$