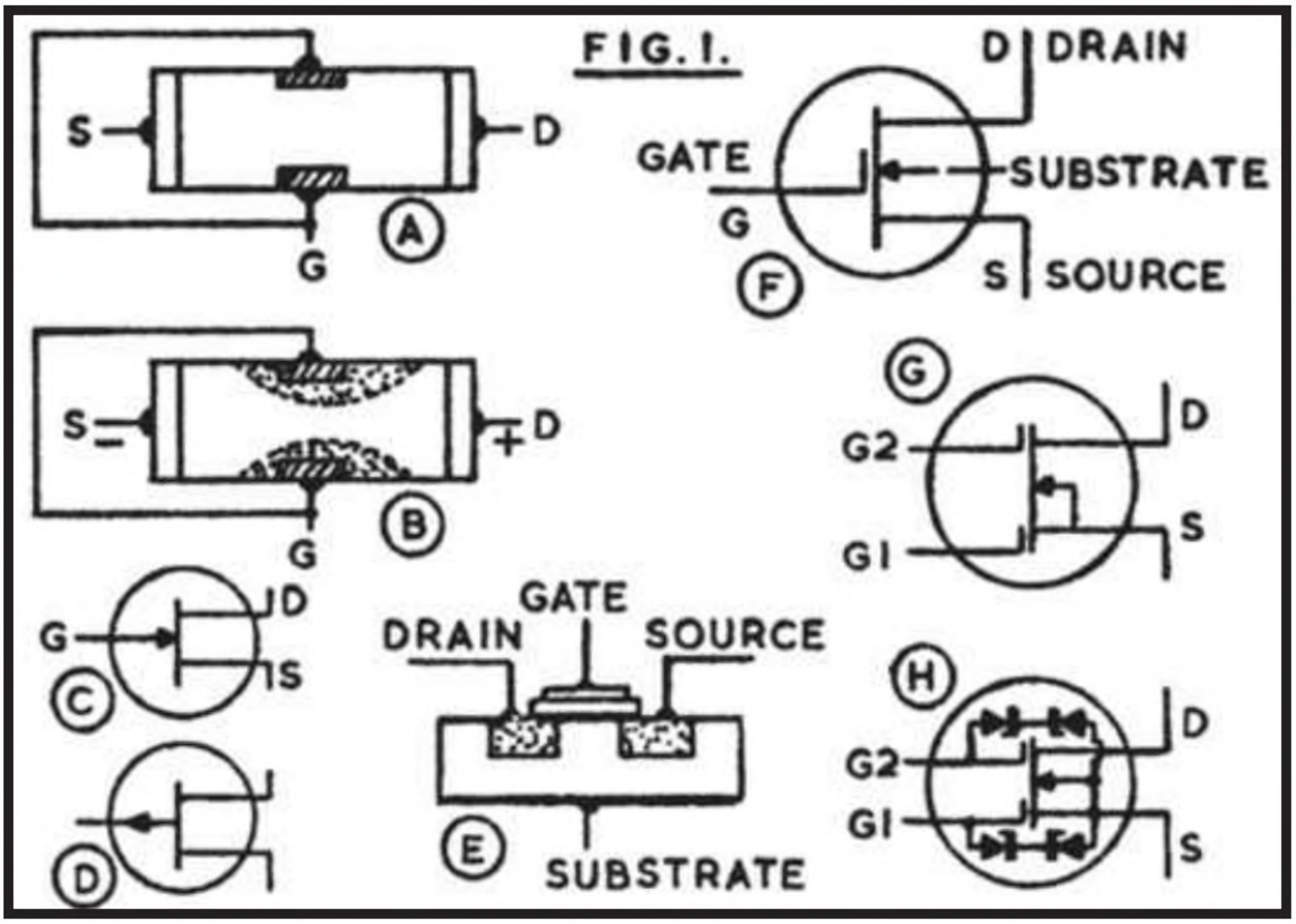
FET Operation

Figure 1 will help clarify the working of the field effect transistor. "A" represents the essential elements of the device, which has Source lead 5, Gate lead G, and Drain connection D. The path for current is from Source to Drain through the semiconductor material, this path being termed the channel. With the N-channel FET, the carriers are electrons. The Source is connected to negative of the supply, and Drain to positive.

P-type gates are formed on the N-type channel, providing PN junctions. When these junctions receive reverse bias, areas surrounding them are emptied of electron carriers. These "depletion areas" reduce the width of the carrier channel as at B. As a result there is a drop in the passage of current carriers from Source to Drain. Increasing the bias causes the depleted regions to extend, and the channel grows smaller, reducing current even further. Eventually the gate can be made so negative that the channel is virtually closed. This is the pinch off region, and current is practically zero. The current from source to drain, and through external circuit items, can there fore be controlled by adjusting



the gate voltage. Since the gate to channel junction area is reverse biassed gate current is extremely small, and thus the gate input Impedance is very high. Generally, the gate current is negligible.

"C" is the symbol for this FET, with S indicating Source (negative), G for Gate, and D for Drain (positive). Such N-channel FETs are conveniently operated with a negative ground or source line. "D" is the symbol for a P-channel FET. Typical types and leadouts are shown later.

"E" represents an insulated gate FET. The gate is insulated from the channel by an extremely thin dielectric so that there is no junction in the way described for "A". The substrate is P-type material with positive hole carriers. When the gate is made negative, positive charges move from the substrate towards the gate, so that the width of the conducting channel reduced, and thus also the current from drain to source.

The gate input impedance is extremely high, as the gate is insulated, and may in fact be many hundreds of megohms. This

type of FET is thus very useful where a high input impedance is wanted.

"F" is the symbol for an insulated gate FET. The insulated gate FET is readily available with two gates, as at "G". Signal input is to Gate 1, and Gate 2 may be used to control gain, or for the oscillator input when employing the transistor as a mixer.

The extremely high gate impedance of the transistor renders it somewhat liable to damage, and for this reason protected gate types are popular. As shown at "H" diodes are provided from the gates to the substrate and source, which are normally joined at "G". These diodes conduct if more than a few volts potential should arise between gate and source circuits, and this prevents destruction of the gate insulation, which would make the device useless. Generally the protective diodes shown at "H" are omitted from the symbol of a protected insulated gate FET.

Using FETs

Soldering precautions which are employed with the bipolar junction transistor will also avoid damage to the FET from heating. The essential is to avoid lengthy cooking of the joint near to the transistor. If the iron has obtained its correct heat, and surfaces to be soldered are clean, it is generally necessary only to apply the iron and solder for two or three seconds, and in the so circumstances no heat sink clips or similar precautions are necessary. Remove the iron as soon as the joint is properly formed.

It will often prove helpful to identify leads by colour coding, especially when using JFETs with different lead positions. With the usual N-channel FET "C" (Figure 1) it is convenient to place a short piece of black sleeeving on the source lead, with red on the drain. These indications will then also agree with circuit polarity. The gate can be left bare. With devices having two gates, green can be used for Gate 1, and blue for Gate 2, or as wished. Such coding will also greatly simplify checking connections when the FET has been wired into position.

Particular care is required with the insulated gate FET "G" which has no protection. Because of the extremely high gate impedance, this FET can be damaged by static charges which would be of no importance at all when handling junction devices. Touching the gate leads with the fingers, or a plastic tool, or any metal object, may destroy the insulation. Such FETs are supplied with a shorting collar - generally a small spring which passes round the leads, joining them electrically. This is not removed until the FET has been soldered into position. In most applications, an inductor, or resistor of up to a few hundred k will be present from G1 to negative line, with a lower value resistor from negative to source, and a gain control or resistor network to G2. Once these components have been connected, an external path is formed from G1 and G2 to source, and this protects the FET against static charges. The shorting ring can thus be removed. It must be replaced, or the leads bound with bright, thin wire, if it is necessary to unsolder any item which would interrupt the protecting G1-G2-Source circuit.

This particular precaution is not required with protected gate FETs "H". However, the unprotected type is quite often used, and will be satisfactory when handled correctly.

FET Types

Many FETs are interchangeable in the circuits given here, but it is necessary to check that essential characteristics are suitable. General purpose and audio devices intended only for lower frequencies cannot be used in VHF circuits. All are low power devices, and for a maximum supply voltage of 20v to 30v. It is impracticable to list all types, but those in the table will easily fill the circuit needs of the projects described.

Figure 2 shows the leads of the types most generally required. Viewing the small plastic type from below, "1" has Drain, Gate and Source leads in this order, while "2" has Gate, Source and Drain leads as shown, and so on. "4" is a metal cased dual gate FET, while "5" has a separate substrate lead, and "7" a separate shield Sh. "6" has source, gate and drain leads.

The reference number following each FET shows that it has leads identified from the positions as in Figure 2.

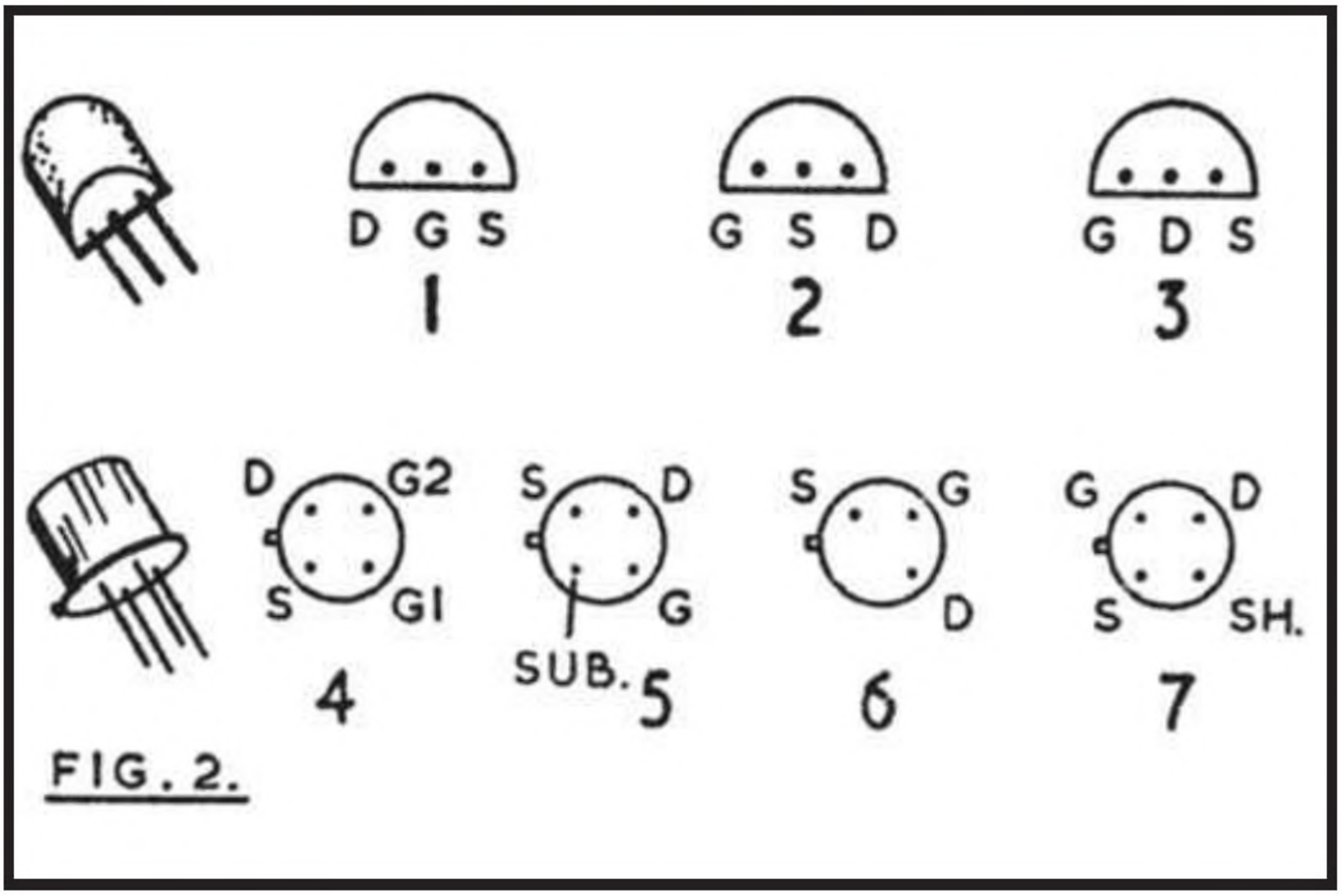


FIG. 2.

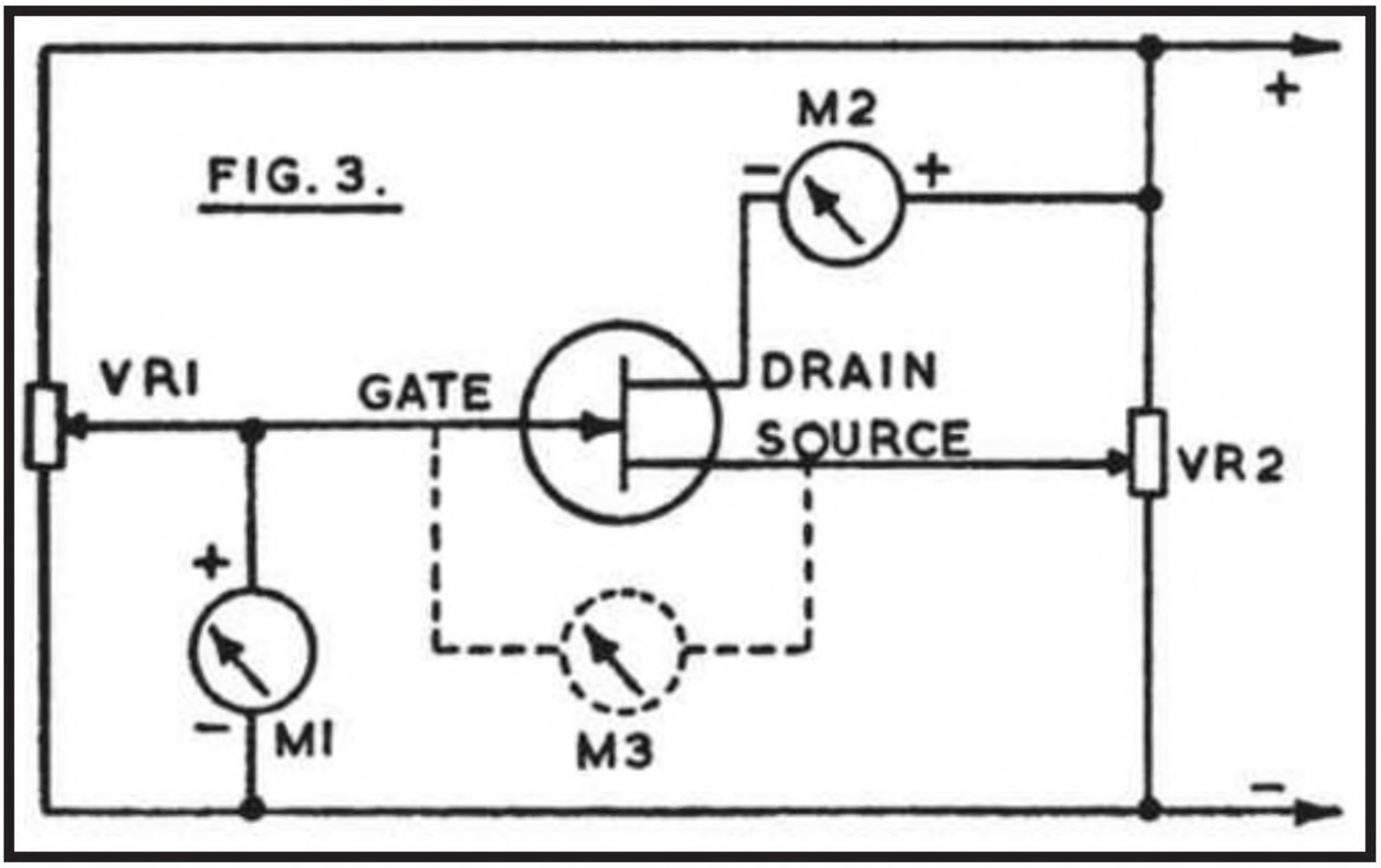
FET Testing

Tests which will show whether or not a field effect transistor is in working condition are readily made with a circuit which can be hooked up in a few minutes and operated from a 9v battery. This can be useful when dealing with surplus or other FETs of doubtful origin, or as a test for the FET in a circuit which does not function. It can usually be assumed that a new FET, purchased from a reliable source, will be in working order.

Two meters are required to show the relationship between gate voltage and drain current with the minimum difficulty. Any ordinary voltmeter with a scale of about 0-10v, 0-5v, or less, will be satisfactory, and it need not be an expensive meter with high resistance. A milliammeter reading about 0-10mA is also necessary. Single range meters, or multirange test meters on suitable ranges, can be used. In Figure 3, M1 is the voltmeter, and M2 the meter to show drain current. The potentiometers VR1 and VR2 are in no way critical, but can best be about 500 ohm or 1k linear

Type No.	Base	Maximum Ratings	Other Information
2N3819	1	200mW 25v	General purpose AF and RF. N-channel.
2N5457/ MPF 103	2	310mW 25v	General purpose AF. N-channel.
2N54581 MPF104 2N5459/ MPF105	2 2	200mW 25v	General purpose AF and RF. N-channel.
BF244	1	200mW 25v	VHF. N-channel.
7644/ BF244	5	200mW 25v	VHF. N-channel. (Sub. lead omitted)
MPF 102	2	200mW 25v	VHF. N-channel.
2N5450/5	3	310mW 25v	General purpose AF. P-channel.
40602/ MEM618	4	330mW 20v	Dual-gate VHF amp. and mixer.
40673	4	330mW 20v	Dual-gate VHF amp. and mixer.
2N3823	5	300mW 30v	VHF amp./mixer. N-channel.
2N2497/ 500	6	500mW -	Low noise. P-channel.
80111	7	100mW 20v	RF amp. N-channel.

components. VR2 ought not to be over 1k, as source current passes through part of the element, so there would be a substantial voltage drop here for other than low source-drain current levels.



With M1 connected as in Figure 3, and VR2 set so that the source is at 1v above negative, the gate/source potential will be zero when VR1 is also set so that M1 reads 1v. If VR1 is now adjusted so that M1 shows less than lv, the gate is negative relative to the source, and the current shown by M2 fails. On the other hand, making the gate more positive causes the drain current to rise.

The relationship between gate and source voltages is readily shown by connecting the voltmeter at M3. A centre zero 1-0-1v instrument is ideal here, but an ordinary meter is suitable, with the leads to it reversed when the gate is more negative than the source.

A typical general purpose FET gave the following readings:

Gate/Source Voltage	Drain Current
0.4 negative	1.6mA
0.2 negative	2.2mA
0	3mA
0.2 positive	3.8mA
0.4 positive	5mA

Thus, over this range, a change of 0.8v in gate voltage has caused a change of 3.4mA in drain current.

Exact results will depend on the individual transistor and other circumstances, but the control of drain current by the gate voltage in this way will be absent with a faulty FET.