# A Practical Guide to Modern Digital ICs

by Ray Marston

Part 5

The best way to learn about modern CMOS is by experimenting with the inexpensive 4007UB IC. The 4007UB houses little more than two pairs of complementary MOSFETs and one simple CMOS inverter stage; all of these elements are independently accessible, and can be configured in a variety of ways. The 4007UB is thus a very versatile IC, and is ideal for demonstrating CMOS principles to students, technicians, and engineers. It can be readily configured to act as a multiple digital inverter, a NAND or NOR gate, a transmission gate, or a uniquely versatile 'micropower' linear amplifier or oscillator, etc. This part presents a selection of practical circuits of these types.

## 4007UB Basics

Figure 1(a) shows the functional diagram and pin numbering of the 14-pin 4007UB, which houses two complementary pairs of independently-accessible MOSFETs, plus a third complementary pair that is connected in the form of a basic CMOS inverter stage. Each of the three independent input terminals of the IC is internally connected to the standard CMOS protection network shown in Figure 1(b). All MOSFETs in the 4007UB are enhancement-mode devices; Q1, Q3 and Q5 are p-channel types, and Q2, Q4 and Q6 are n-channel types. Figure 1(c) shows the terminal notations of the two MOSFET types; note that the 'B' terminal represents the bulk substrate. All modern '4000B-series' and fast '74-series' CMOS ICs are designed around the basic elements shown in Figure 1, and thus it is useful to get a good basic understanding of both the digital and the linear characteristics of these elements, starting off with those of the basic MOSFETs.

## Digital Operation

The input (gate) terminal of a MOSFET presents a near-infinite impedance to DC voltages, and the magnitude of an external voltage applied to the gate controls the magnitude of the MOSFET's source-to-drain current flow. The basic characteristics of the enhancement-mode n-channel MOSFET are such that the source-to-drain path is open circuit when the gate is at the same potential as the source, but becomes a near short-circuit (a low-value resistance) when the gate is heavily biased *positive* to the source. Thus, the n-channel MOSFET can be used as a digital inverter by wiring it as shown in Figure 2; with a logic-0 (zero volts) input, the MOSFET is cut off and the output is at logic-1 (the positive rail voltage), but with a logic-1 input, the MOSFET is driven on and the output is at logic-0.

The basic characteristics of the enhancement-mode p-channel MOSFET are such that the source-to-drain path is open when the gate is at the same potential as the source, but becomes a near-short when the gate is heavily biased *negative* to the source. The p-channel MOSFET can thus be used as a digital inverter, by wiring it as shown in Figure 3.

Note that in the Figure 2 and 3 inverter circuits, that the ON currents of the MOSFETs are determined by the R1 value, and these circuits thus draw a significant quiescent current when their MOSFETs are driven ON. This snag can be overcome by connecting the complementary pair of MOSFETs in the classic CMOS inverter configuration shown in Figure 4(a).

In Figure 4(a), with a logic-0 input applied, Q1 is driven fully on and the output is thus firmly tied to the logic-1 (positive rail) state, but Q2 is cut off and the inverter thus passes zero quiescent current via this MOSFET. With a logic-1 input applied, Q2 is driven on and the output is firmly tied to the logic-0 (zero volt) state, but Q1 is cut off and the circuit again passes zero quiescent current. This 'zero quiescent current' characteristic of the complementary MOSFET inverter is one of the most important features of the CMOS digital inverter, and the Figure 4(a) circuit forms the basis of the entire CMOS family of digital ICs. Q5 and Q6 of the 4007UB are fixed-wired in this CMOS inverter configuration.

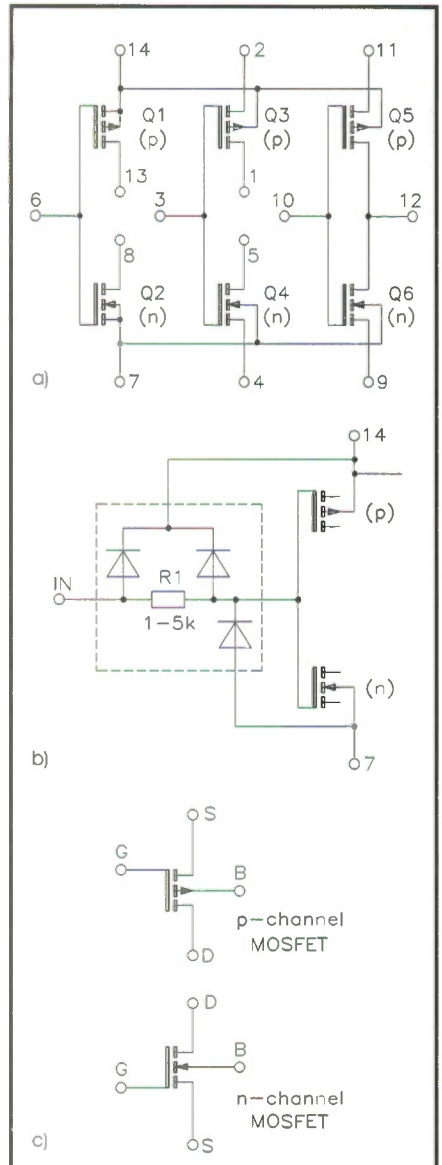



**Figure 1. (a) Functional diagram of the 4007UB dual CMOS pair plus inverter. (b) Internal input-protection network (within dotted lines) on each input of the 4007UB. (c) MOSFET terminal notations; G=Gate, D=Drain, S=Source, B=Bulk substrate.**

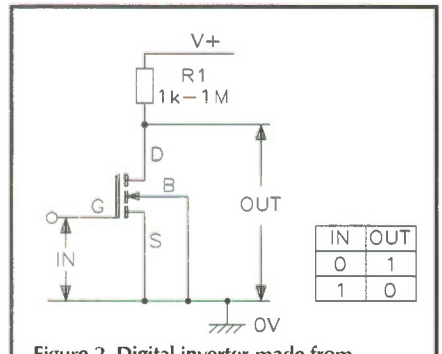
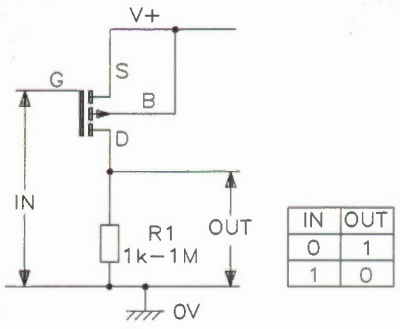



**Figure 2. Digital inverter made from n-channel MOSFET.**

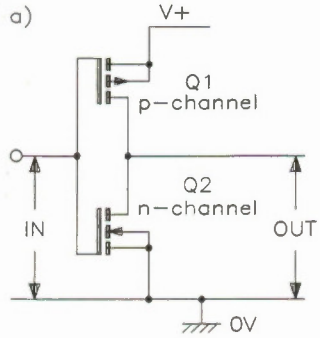
## Linear Operation

To fully understand the operation and vagaries of CMOS circuitry, it is necessary to understand the linear characteristics of basic MOSFETs. Figure 5 shows the typical gate-voltage/drain-current graph of an n-channel enhancement mode MOSFET. Note that negligible drain current flows until the gate voltage rises to a 'threshold' value of about 1·5 to 2·5V, but that the drain current then increases almost linearly with further increases in gate voltage.




| IN | OUT |
|---|---|
| 0 | 1 |
| 1 | 0 |

Figure 3. Digital inverter made from p-channel MOSFET.




b)

| IN | OUT |
|---|---|
| 0 | 1 |
| 1 | 0 |

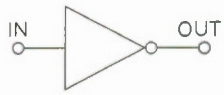



Figure 4. (a) Circuit, (b) Truth Table and (c) standard symbol of the CMOS digital inverter.

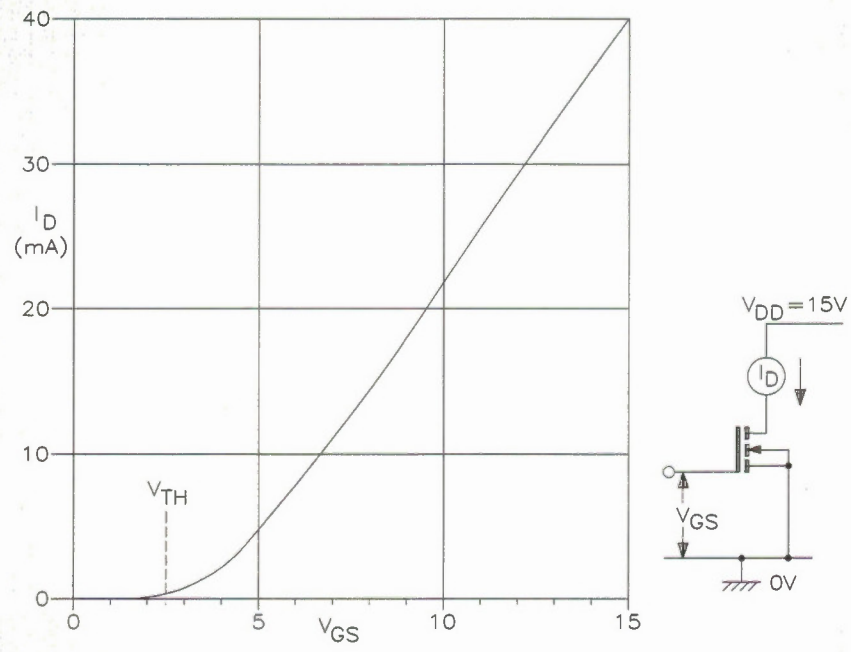



Figure 5. Typical gate-voltage/drain-current characteristics of an n-channel MOSFET.

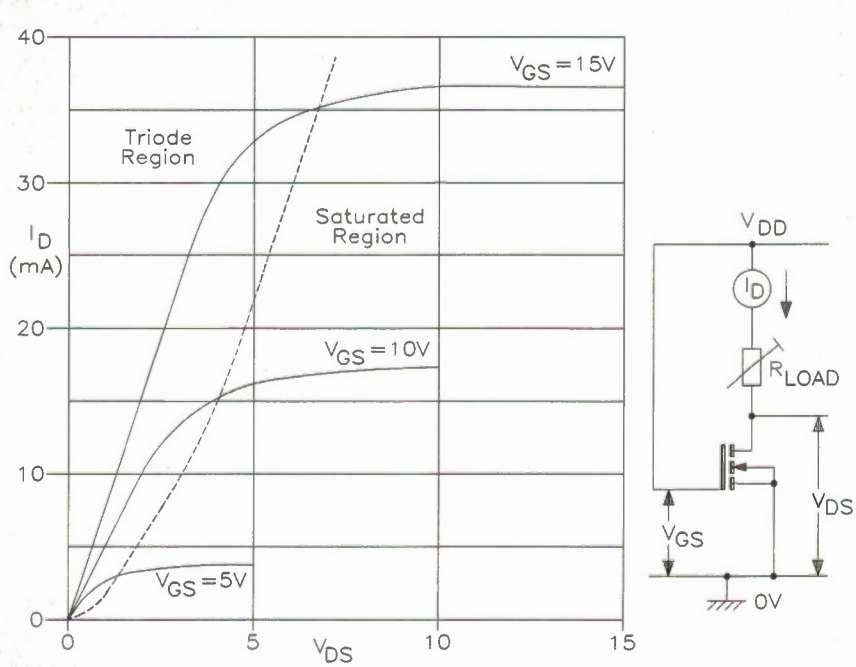



Figure 7. Typical $I_D$ to $V_{DS}$ characteristics of the n-channel MOSFET at various fixed values of $V_{GS}$.

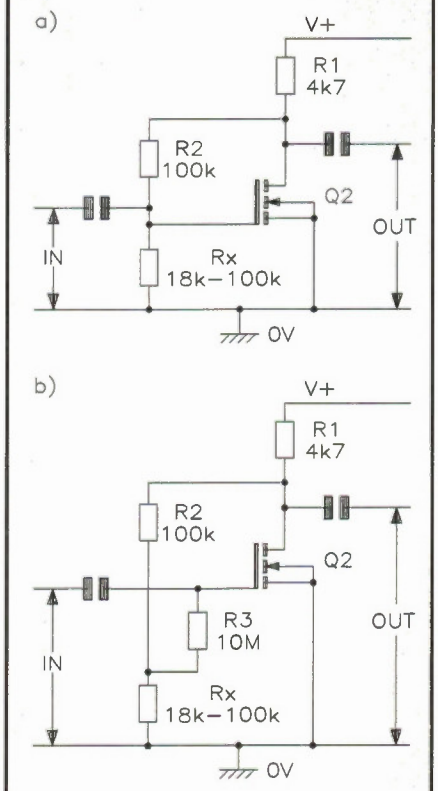



Figure 6. Methods of biasing an n-channel MOSFET as a linear inverting amplifier.

Figure 6 shows how to connect an n-channel 4007UB MOSFET as a linear inverting amplifier. R1 serves as the drain load of Q2, and R2-Rx bias the gate so that the device operates in the linear mode. The Rx value must be selected to give the desired quiescent drain voltage, but is normally in the range 18 to 100kΩ. The amplifier can be made to give a very high input impedance, by wiring a 10MΩ isolating resistor between the R2-Rx junction and the gate of Q2, as shown in Figure 6.

Figure 7 shows the typical $I_D/V_{DS}$ characteristics of an n-channel MOSFET at various fixed values of gate-to-source voltage. Imagine here that, for each set of curves, $V_{GS}$ is fixed at the $V_{DD}$ voltage, but that the $V_{DS}$ output voltage can be varied by altering the value of drain load, $R_L$. The graph can be divided into two characteristic regions, as indicated by the dotted line, these being the *triode* region and the *saturated* region.

When the MOSFET is in the saturated region (with $V_{DS}$ at some value in the nominal range 50 to 100% of $V_{GS}$), the drain acts like

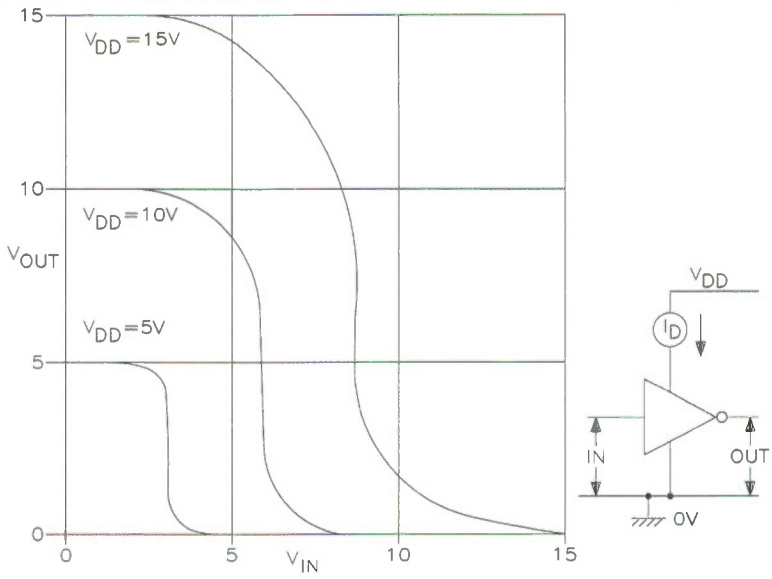
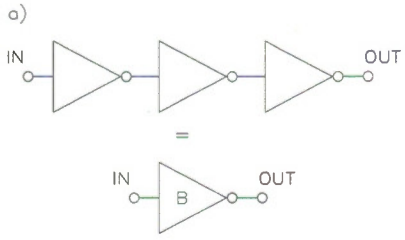
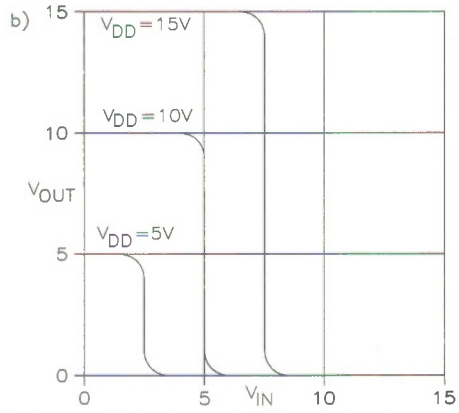



Figure 8. Typical voltage transfer characteristics of the 4007UB simple CMOS inverter.

Figure 10. Wiring three simple CMOS inverters in series (a) gives the equivalent of a B-series 'buffered' CMOS inverter, which has the transfer characteristics shown in (b).



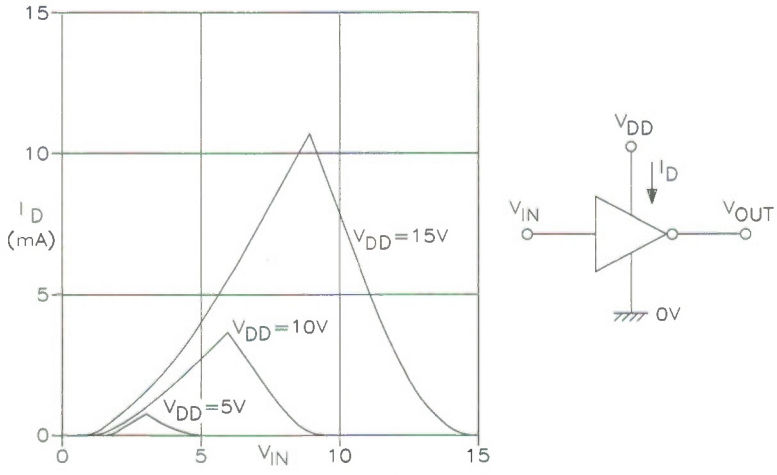




Figure 11. Drain-current transfer characteristics of the simple CMOS inverter.

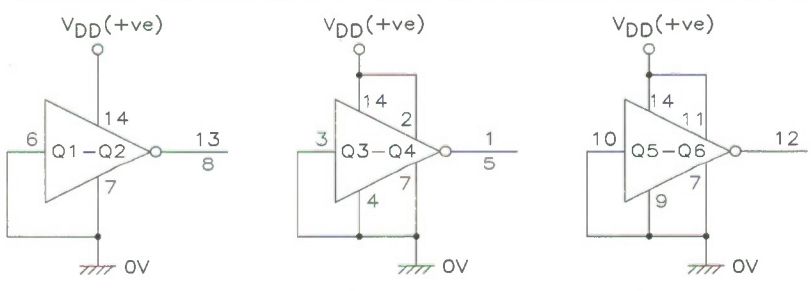



Figure 12. Individual 4007UB complementary MOSFET pairs can be disabled by connecting them as CMOS inverters and grounding their inputs.

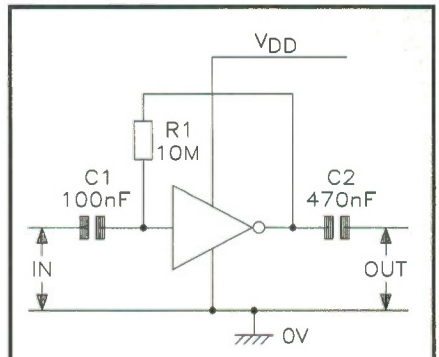



Figure 9. Method of biasing the simple CMOS inverter for linear operation.

a constant current source, with its current value controlled by $V_{GS}$: a low $V_{GS}$ value gives a low constant-current value, and a high $V_{GS}$ value gives a high constant-current value. These saturated constant-current characteristics provide CMOS with an output 'short-circuit proof' feature, and also determine its operating speed limits at different supply voltage values.

When the MOSFET is in the triode region (with $V_{DS}$ at some value in the nominal range 1 to 50% of $V_{GS}$), the drain acts like a voltage-controlled resistance, with the resistance value increasing approximately as the square of the $V_{GS}$ value.

The p-channel MOSFET has an $I_D/V_{DS}$ characteristics graph that is complementary to that of Figure 7. Consequently, the action of the standard CMOS inverter of Figure 4 (which uses a complementary pair of MOSFETs) is such that its current-drive capability into an external load, and its operating speed limits also increase in proportion to the supply rail voltage.

Figure 8 shows the typical voltage-transfer characteristics of the 4007UB's standard CMOS inverter at different supply voltage values. Note (on the 15V $V_{DD}$ line, for example) that the output voltage changes by only a small amount when the input voltage is shifted around the $V_{DD}$ and 0V levels, but that when $V_{in}$ is biased at roughly half-supply volts, a small change of input voltage causes a large change of output voltage: typically, the inverter gives a voltage gain of about 30dB when used with a 15V supply, or 40dB at 5V. Figure 9 shows how to connect the CMOS inverter as a linear amplifier; the circuit has a typical bandwidth of 710kHz at 5V, or 2·5MHz at 15V.

Wiring three simple CMOS inverter stages in series as in Figure 10(a) gives the direct equivalent of a modern '4000B-series' 'buffered' CMOS inverter stage, which has the overall voltage transfer graph of Figure 10(b). The B-series inverter typically gives about 70dB of linear voltage gain, but tends to be grossly unstable when used in the linear mode.

Finally, Figure 11 shows the drain-current transfer characteristics of the simple CMOS inverter. Note that the drain current is zero when the input is at either zero of full supply volts, but rises to a maximum value (typically 0·5mA at 5V supply, or 10·5mA at 15V) when the input is at roughly half-supply volts, under which condition, both MOSFETs of the inverter are biased on. In the 4007UB, these ON currents can be reduced by wiring extra resistance in series with the source of each MOSFET of the CMOS inverter; this technique is used in the 'micropower' circuits shown later in this article.

## Using the 4007UB

The 'usage' rules of the 4007UB are quite simple. In any specific application, all unused elements of the device must be disabled; complementary pairs of MOSFETs can be disabled by connecting them as standard CMOS inverters and tying their inputs to ground, as shown in Figure 12; individual MOSFETs can be disabled by tying their source to their substrate (B), and leaving the drain open circuit.

In use, the input terminals must not be allowed to rise above $V_{DD}$ (the supply voltage) or below $V_{SS}$ (0V). To use an n-channel MOSFET, the source must be tied to $V_{SS}$, either directly or via a current-limiting resistor. To use a p-channel MOSFET, the source must be tied to $V_{DD}$, either directly or via a current-limiting resistor.

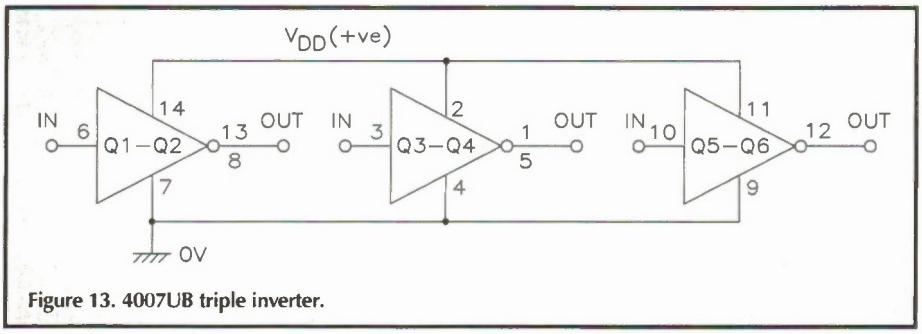



**Figure 13. 4007UB triple inverter.**

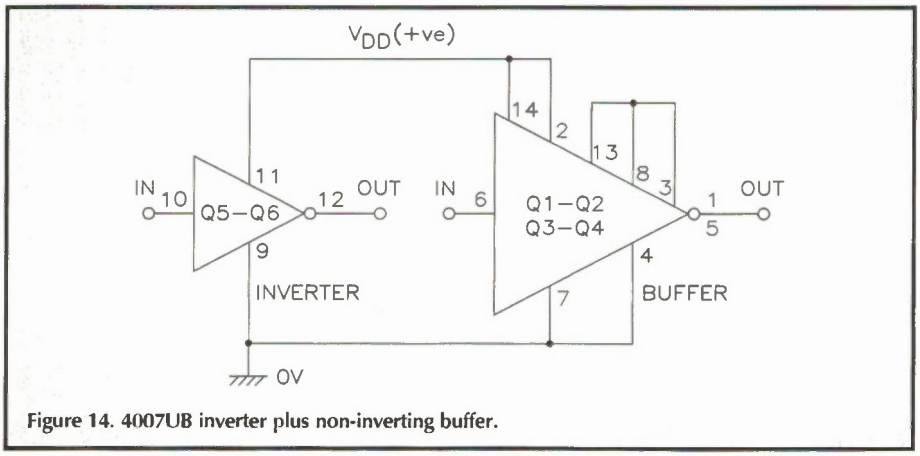



**Figure 14. 4007UB inverter plus non-inverting buffer.**

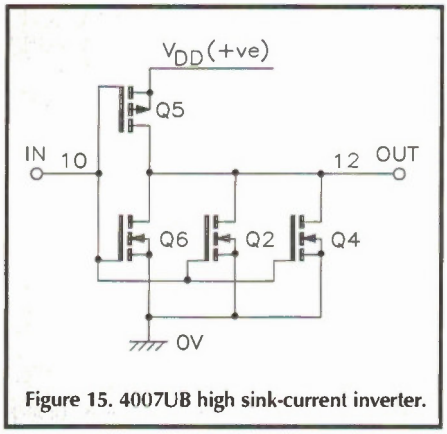



**Figure 15. 4007UB high sink-current inverter.**

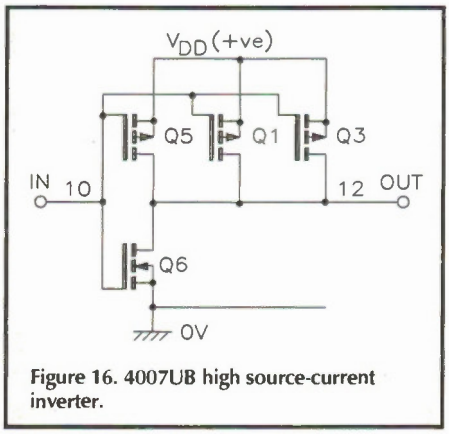



**Figure 16. 4007UB high source-current inverter.**

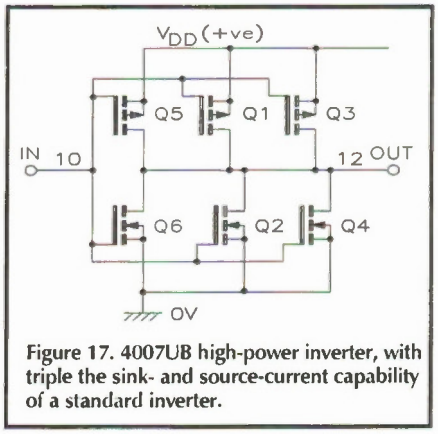



**Figure 17. 4007UB high-power inverter, with triple the sink- and source-current capability of a standard inverter.**

## Practical Circuits

### Digital

The 4007UB elements can be configured to act as any of a variety of standard digital circuits. Figure 13 shows how to wire the IC as a triple inverter, using all three sets of complementary MOSFET pairs. Figure 14 shows the connections for making an inverter plus non-inverting buffer; here, the Q1-Q2 and Q3-Q4 inverter stages are simply wired directly in series, to give an overall non-inverting action.

The maximum source (load-driving) and sink (load-absorbing) output current of a simple CMOS inverter stage self-limits at about 10 to 20mA as one or other of the output MOSFETs turns fully on. Higher sink currents can be obtained by simply wiring n-channel MOSFETs in parallel in the output stage. Figure 15 shows how to wire the 4007UB so that it acts as a high-sink-current inverter that will absorb triple the current of a normal inverter. Similarly, Figure 16 shows how to wire the 4007UB to act as a high-source-current inverter, and Figure 17 shows the connections for making a single inverter that will sink or source three times more current than a standard inverter stage.

The 4007UB is a perfect device for demonstrating the basic principles of CMOS logic gates. Figure 18 shows the basic connections for making a 2-input NOR gate. Note that the two n-channel MOSFETs are wired in parallel so that either can pull the output to ground from a logic-1 input, and the two p-channel

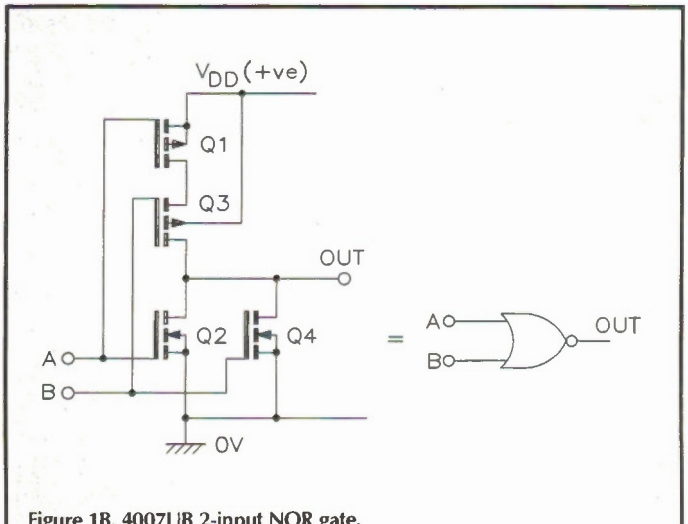



**Figure 18. 4007UB 2-input NOR gate.**

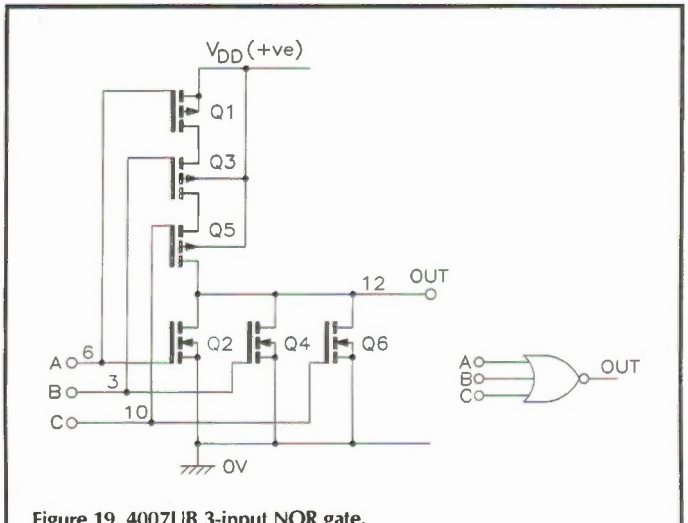
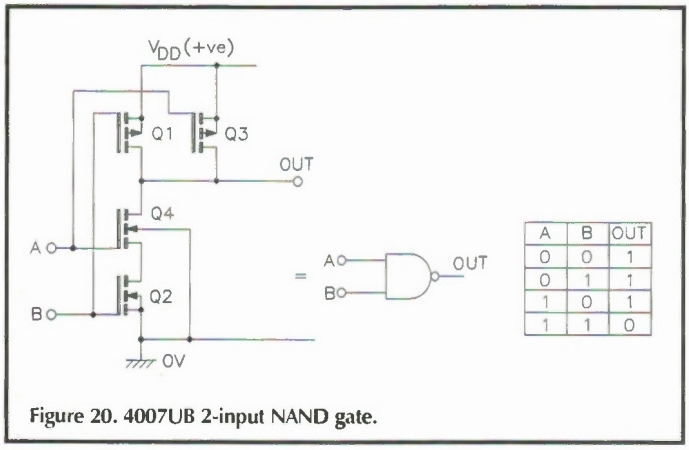



**Figure 19. 4007UB 3-input NOR gate.**




| A | B | OUT |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Figure 20. 4007UB 2-input NAND gate.**

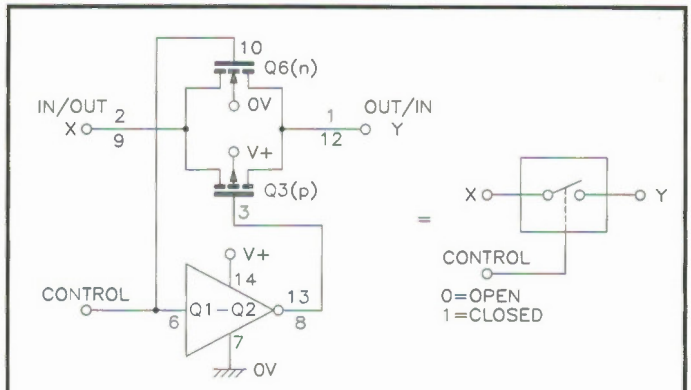



**Figure 21. 4007UB transmission gate or bilateral switch.**

MOSFETs are wired in series so that both must turn on to pull the output high from a logic-0 input. The truth table shows the logic of the circuit. A 3-input NOR gate can be made by simply wiring three p-channel MOSFETs in series and three n-channel MOSFETs in parallel, as shown in Figure 19.

Figure 20 shows how to wire the 4007UB as a 2-input NAND gate. In this case, the two p-channel MOSFETs are wired in parallel and the two n-channel MOSFETs are wired in series. A 3-input NAND gate can be made by similarly wiring three p-channel MOSFETs in parallel and three n-channel MOSFETs in series.

Figure 21 shows the basic way of using the 4007UB to make another important CMOS element, the transmission gate or bilateral switch, which acts like a near-perfect switch that can conduct signals in either direction and can be turned on (closed) by applying a logic-1 to its control terminal or turned off (open) via a logic-0 control signal. In Figure 21, an n-channel and a p-channel MOSFET are wired in parallel (source-to-source and drain-to-drain), but their gate signals are applied in antiphase via the Q1-Q2 inverter. To turn the Q3-Q6 transmission gate on (closed), Q6 gate is taken to logic-1 and Q3 gate to logic-0 via the inverter; to turn the switch off, the gate polarities are simply reversed. The 4007UB transmission gate has a near-infinite OFF

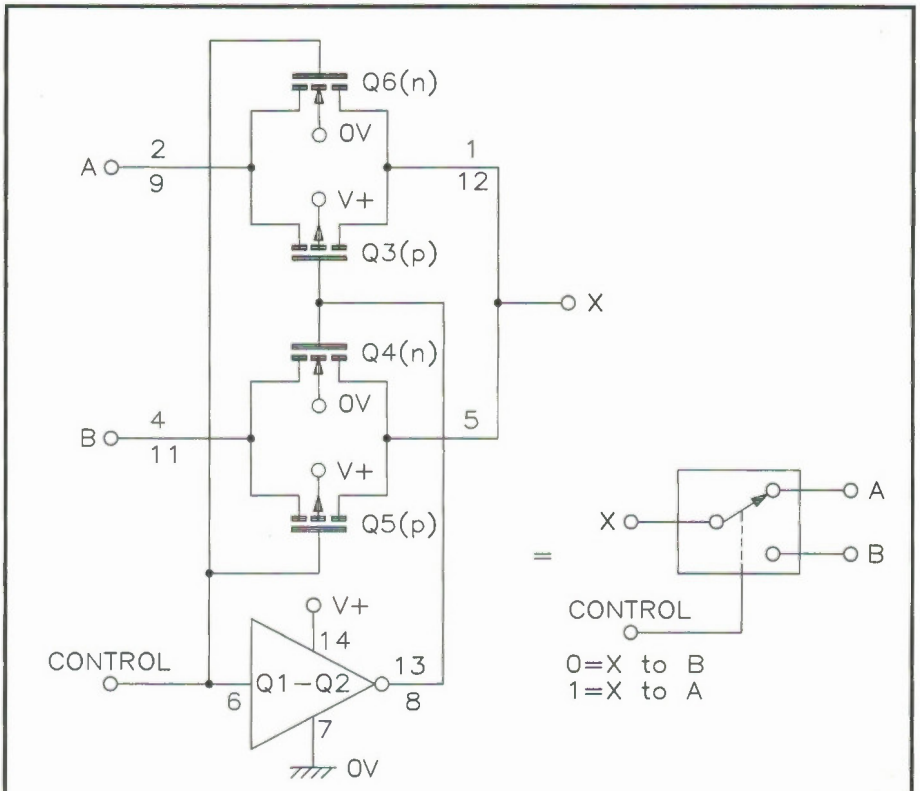



**Figure 22. 4007UB 2-way transmission gate.**

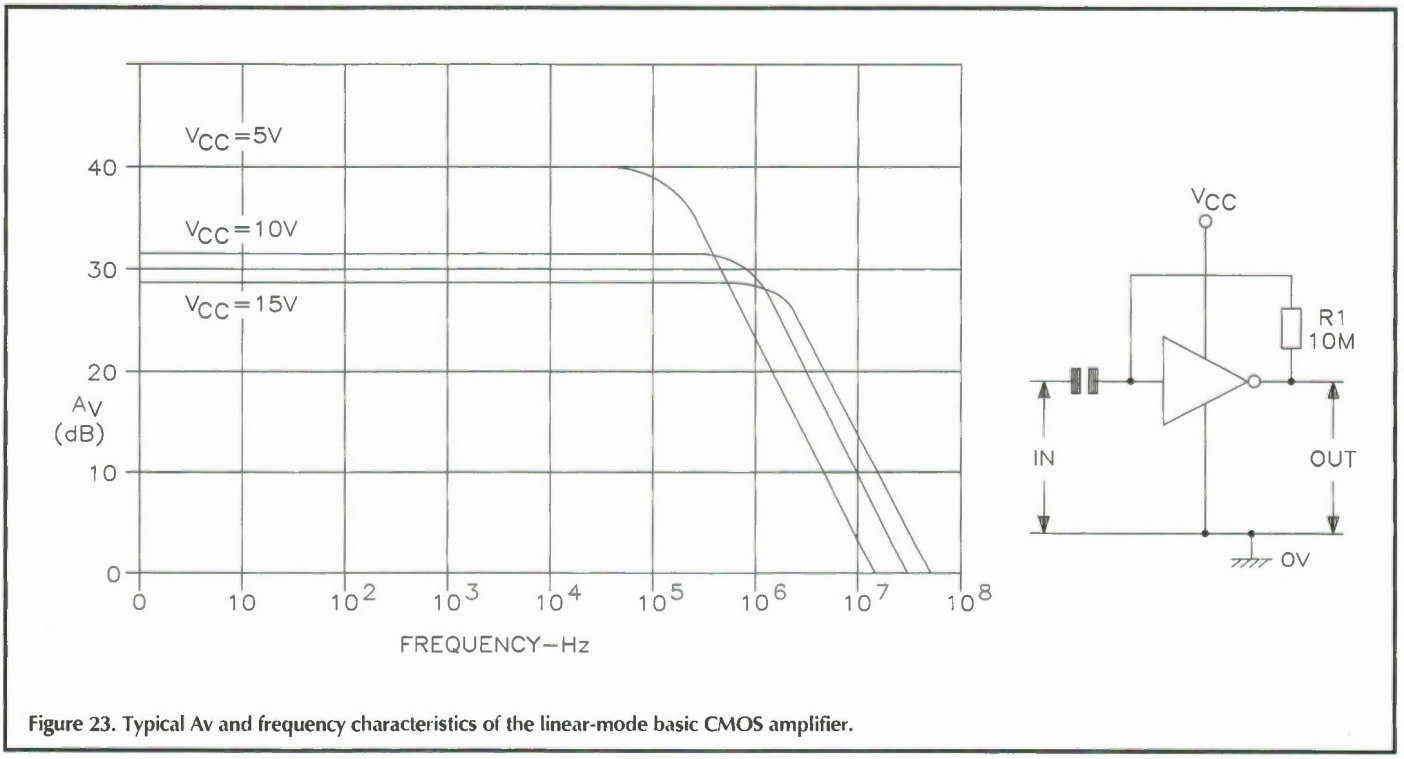



**Figure 23. Typical Av and frequency characteristics of the linear-mode basic CMOS amplifier.**

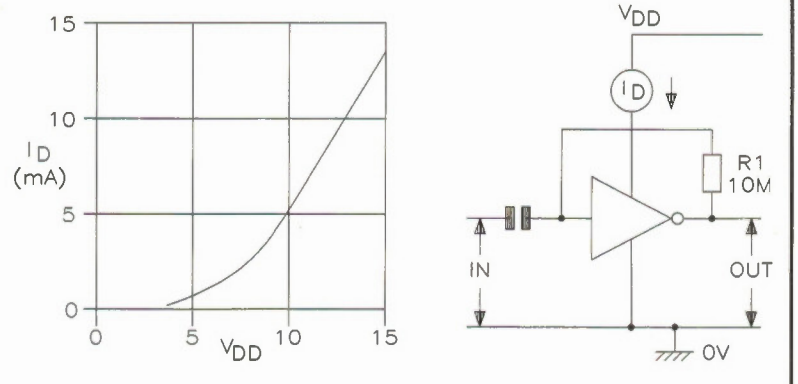



Figure 24. Typical $I_D/V_{DD}$ characteristics of the linear-mode CMOS amplifier.

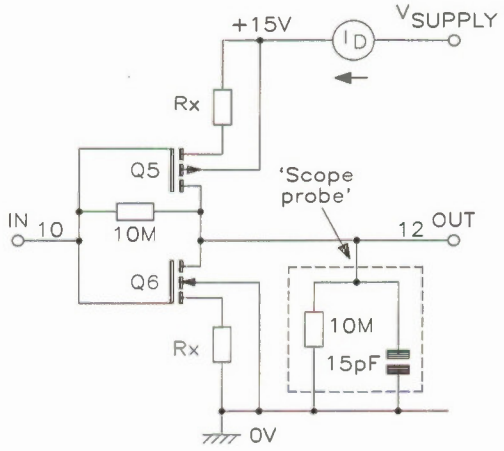



Figure 25. 'Micropower' 4007UB CMOS linear amplifier, showing method of reducing ID, with measured performance details.

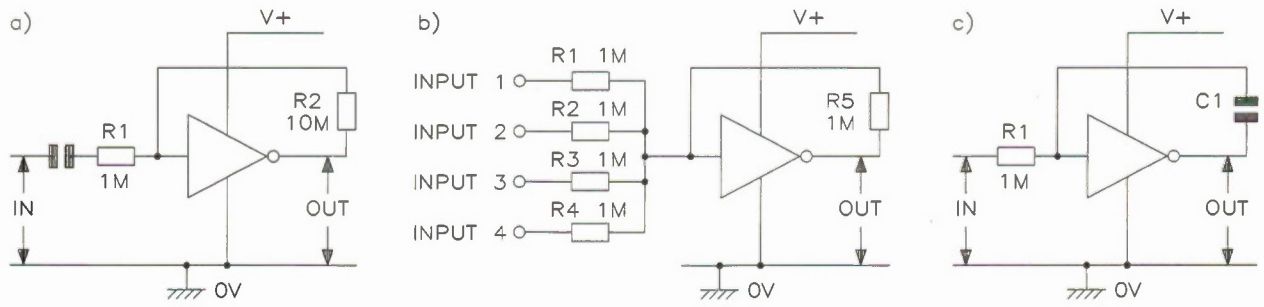



Figure 26. The CMOS amplifier can be used in a variety of linear inverting amplifier applications. Three typical examples are shown here.

resistance and an ON resistance of about 600Ω. It can handle all signals between 0V and the positive supply rail value. Note that, since the gate is bilateral, either of its main terminals can function as an input or output.

Finally, Figure 22 shows how the 4007UB can be wired as a dual transmission gate that functions like a single-pole double-throw (SPDT) switch. In this case, the circuit uses two transmission elements, but their control voltages are applied in anti-phase, so that one switch opens when the other closes, and vice versa. The 'X' sides of the two gates are shorted together to give the desired SPDT action.

## Practical Circuits

### Linear

Figures 6 to 9 have already shown that the basic 4007UB MOSFETs and the CMOS inverter can be used as linear amplifiers.

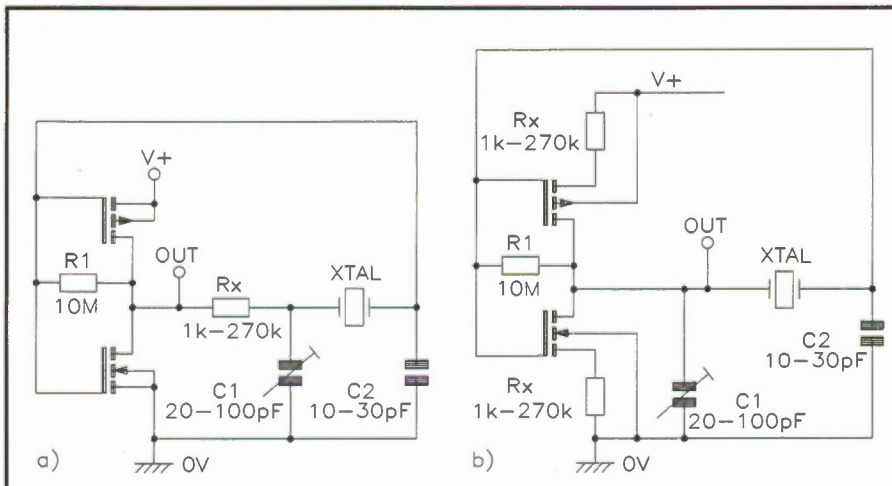



Figure 27. Crystal oscillator using (a) standard and (b) micropower 4007UB CMOS linear inverter.

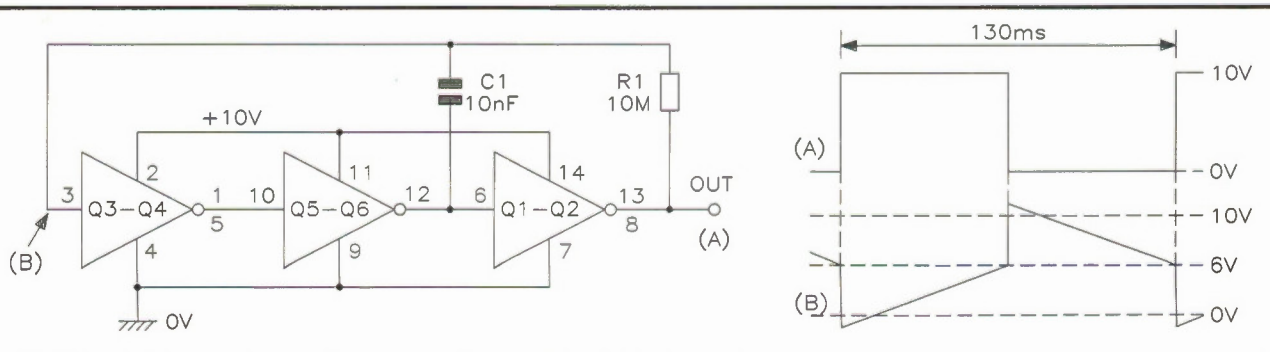



Figure 28. This 4007UB ring-of-three astable consumes 280μA at 6V, and 1·6mA at 10V.

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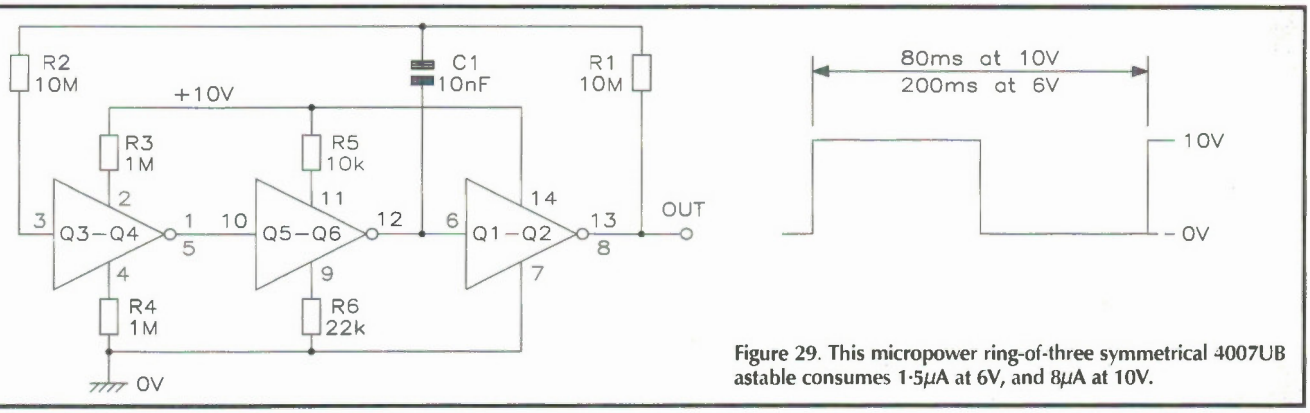


**Figure 29. This micropower ring-of-three symmetrical 4007UB astable consumes 1·5μA at 6V, and 8μA at 10V.**

Figure 23 shows the typical voltage gain and frequency characteristics of the linear CMOS inverter when operated from three alternative supply rail values (this graph assumes that the amplifier output is feeding into the high impedance of a 10MΩ/15pF oscilloscope probe). The output impedance of the open-loop amplifier typically varies from 3kΩ at 15V supply, to 5kΩ at 10V, or 22kΩ at 5V, and it is the product of the output impedance and output load capacitance that determines the bandwidth of the circuit; increasing the output impedance or load capacitance reduces the bandwidth.

As you would expect from the voltage transfer graph of Figure 8, the distortion characteristics of the CMOS linear amplifier are not very good. Linearity is fairly good for small-amplitude signals (output amplitudes up to 3V Pk-to-Pk with a 15V supply), but the distortion then increases progressively as the output approaches the upper and lower supply limits. Unlike a bipolar transistor circuit, the CMOS amplifier does not 'clip' excessive sine wave signals, but progressively rounds off their peaks. Figure 24 shows the typical drain-current/supply-voltage characteristics of the basic CMOS linear amplifier. Note that the supply current typically varies from 0·5mA at 5V to 12·5mA at 15V.

## 'Micropower' Circuits

In many applications, the quiescent supply current of the 4007UB CMOS linear amplifier can be usefully reduced, at the expense of reduced amplifier bandwidth, by wiring external resistors in series with the source terminals of the two MOSFETs of the CMOS stage, as shown in the 'micropower' circuit of Figure 25. Table 1 shows the effect that different resistor values have on the drain current, voltage gain and bandwidth of the amplifier when it is operated from a 15V supply and has its output feeding to a 10MΩ/15pF oscilloscope probe.

| R1 | $I_D$ | AV ($V_{OUT}/V_{IN}$) | Upper 3dB Bandwidth |
|---|---|---|---|
| 0 | 12·5mA | 20 | 2·7MHz |
| 100Ω | 8·2mA | 20 | 1·5MHz |
| 560Ω | 3·9mA | 25 | 300kHz |
| 1kΩ | 2·5mA | 30 | 150kHz |
| 5k6Ω | 600μA | 40 | 25kHz |
| 10kΩ | 370μA | 40 | 15kHz |
| 100kΩ | 40μA | 30 | 2kHz |
| 1MΩ | 4μA | 10 | 1kHz |

**Table 1. Measured performance details of the 'micropower' 4007UB linear amplifier shown in Figure 25.**

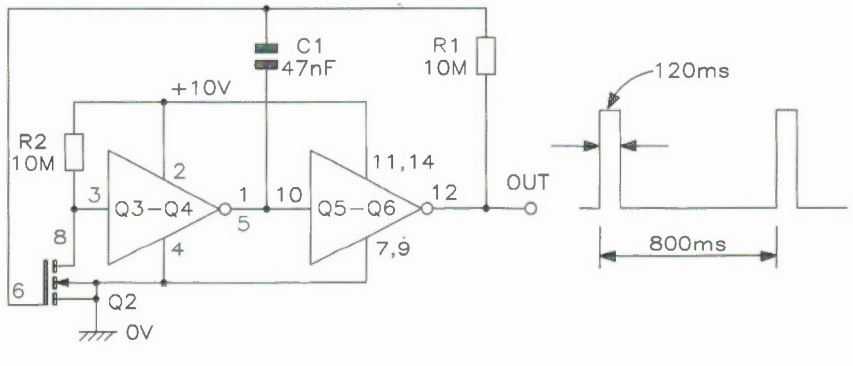


**Figure 30. This 4007UB asymmetrical ring-of-three astable consumes 2μA at 6V, and 5μA at 10V.**

It is important to appreciate in the Figure 25 circuit, that these additional resistors add to the output impedance of the amplifier (the output impedance roughly equals the R1-Av product), and this impedance and the external load resistance/capacitance has a great effect on the overall gain and bandwidth of the circuit. When using 10kΩ values for R1, for example, if the load capacitance is increased to 50pF, the bandwidth falls to about 4kHz, but if the capacitance is reduced to a mere 5pF, the bandwidth increases to 45kHz. Similarly, if the resistive load is reduced from 10MΩ to 10kΩ, the voltage gain falls to unity. Thus, for significant gain, the load resistance must be large relative to the output impedance of the amplifier.

The basic (unbiased) CMOS inverter stage has an input capacitance of about 5pF and an input resistance of near-infinity. Thus, if the output of the Figure 25 circuit is fed directly to such a load, it will show a voltage gain of about ×30 and a bandwidth of 3kHz when R1 has a value of 1MΩ; it will even give useful gain and bandwidth when R1 has a value of 10MΩ, but will consume a quiescent current of only 0·4μA! The CMOS linear amplifier can be used, in either its standard or micropower forms, to make a variety of fixed-gain amplifiers, mixers, integrators, active filters and oscillators, etc. Three typical basic applications are shown in Figure 26.

One attractive 4007UB linear application is as a crystal oscillator, as shown in Figure 27(a). Here, the CMOS amplifier is linearly biased via R1 and provides 180° phase shift, and the Rx-C1-XTAL-C2 pi-type crystal network gives an additional 180° of phase shift at the crystal resonant frequency, thereby causing the circuit to oscillate. If this circuit is needed to provide a frequency accuracy within only 0·1% or so, Rx can be replaced by a short and C1-C2 can be omitted; for ultra-high accuracy, the correct values of Rx-C1-C2 must be individually determined (Figure 27 shows the typical range of values). In micropower applications, Rx can be incorporated in the CMOS amplifier, as shown in Figure 27b. If desired, the output of the crystal oscillator can be fed directly to the input of an additional CMOS inverter stage, for improved waveform shape/amplitude.

## Practical Circuits

### Astables

One of the most useful applications of the 4007UB, is as a ring-of-three astable multivibrator; Figure 28 shows the basic configuration of the circuit. Waveform timing is controlled by the values of R1 and C1, and

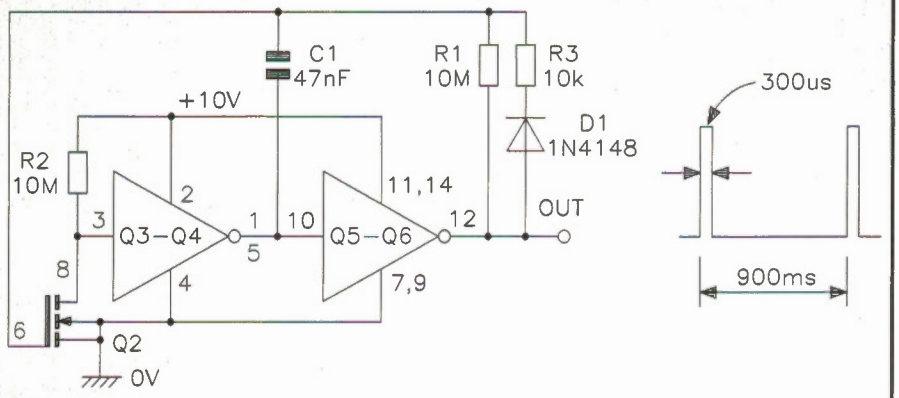


**Figure 31. This dual time-constant version of the 4007UB astable generates a very narrow output pulse.**

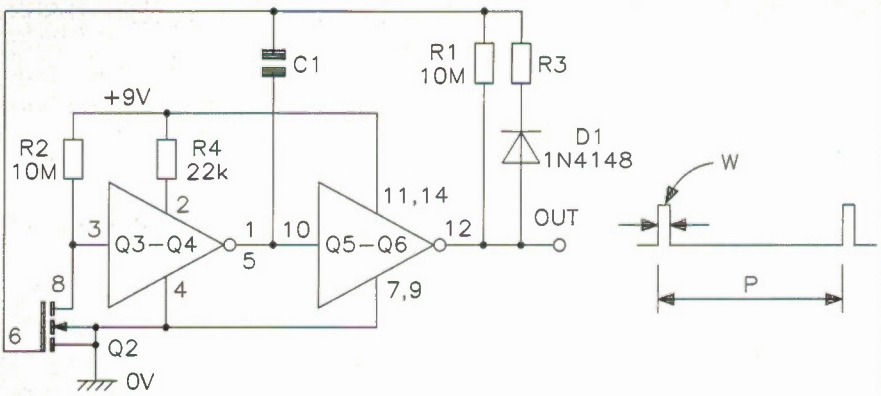


**Figure 32. This micropower version of the 4007UB dual time-constant astable consumes absolutely minimal currents.**

| C1/R3 Values | $I_{mean}$ @ 9V (μA) | W (μs) | P (ms) |
|---|---|---|---|
| 47nF/10kΩ | 1·5 | 300 | 900 |
| 10nF/33kΩ | 3·5 | 160 | 180 |

**Table 2. Effects of C1 and R3 values on the astable circuit of Figure 32.**

the output waveform (A) is approximately symmetrical. Note that for most of the waveform period, the front-end (waveform B) part of the circuit operates in the linear mode, so the circuit consumes a significant running current.

In practice, the running current of the Figure 28 4007UB astable circuit is higher than that of an identically configured B-series 'buffered' CMOS IC such as the 4001B, the comparative figures being 280μA at 6V or 1·6mA at 10V for the 4007UB, against 12μA at 6V or 75μA at 10V for the 4001B. The 4007UB circuit, however, has far lower propagation delays than the 4001B and typically, has a maximum astable operating speed that is three times higher than that of the 4001B.

The running current of the 4007UB astable can be greatly reduced by operating its first two stages in the 'micropower' mode, as shown in Figure 29. This technique is of particular value in low-frequency operation, and the Figure 29 circuit in fact, consumes a mere 1·5μA at 6V or 8μA at 10V, these figures being far lower than those obtainable from any other IC in the CMOS range. The frequency stability of the Figure 29 circuit is not, however, very good, the period varying from 200ms at 6V to 80ms at 10V.

Figure 30 shows the 4007UB configured as an asymmetrical ring-of-three astable, with the 'input' of the circuit applied to n-channel MOSFET, Q2. The circuit consumes a mere 2μA at 6V or 5μA at 10V. Figure 31 shows how the symmetry of the above circuit can be varied by shunting R1 with the D1-R3 network, so that the charge and discharge times of C1 are independently controlled. With the component values shown, the circuit produces a 300μs pulse once every 900ms, and consumes a mere 2μA at 6V or 4·5μA at 10V.

Finally, to complete this look at the 4007UB IC, Figure 32 shows how the current consumption of the above circuit can be even further reduced by operating the Q3-Q4 CMOS inverter in the micropower mode. Table 2 gives details of circuit performance with alternative C1 and R3 values. This circuit can give years of continuous operation from one 9V battery. E