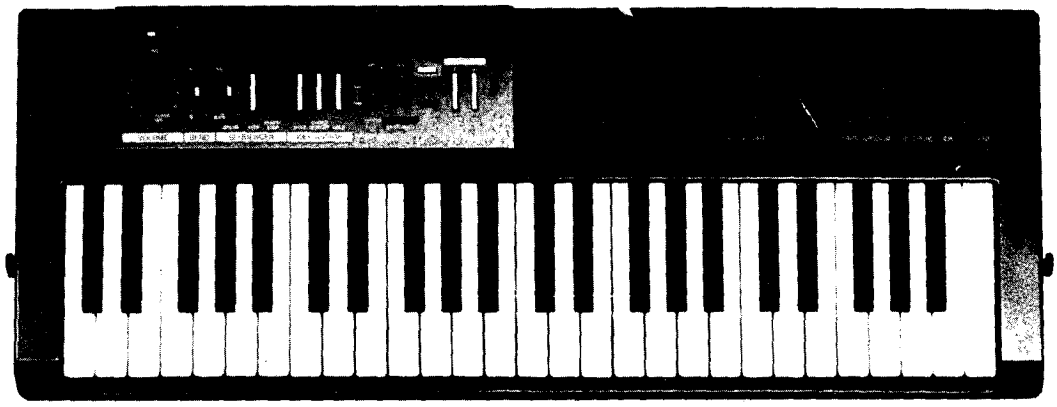
KORG®



*KORG PROGRAMMABLE POLYPHONIC SYNTHESIZER*

# SERVICE MANUAL POLY-800

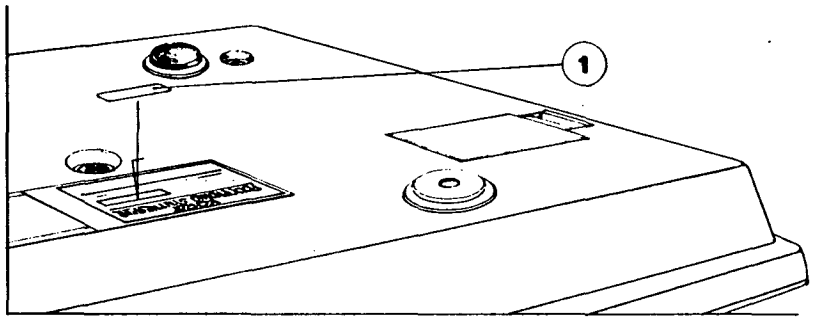
CONTENTS

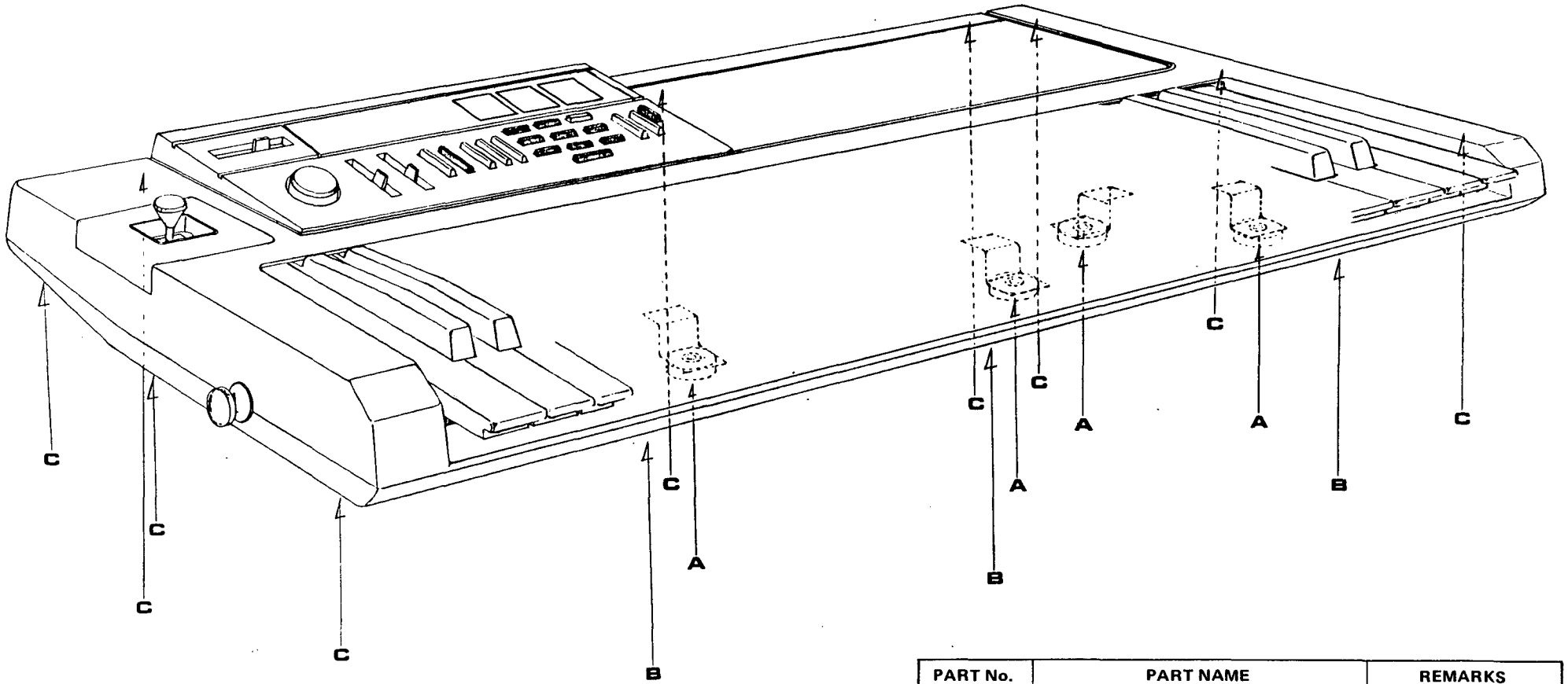

1. SPECIFICATIONS . . . . . 1
2. STRUCTURAL DIAGRAM . . . . . 2
3. BLOCK DIAGRAM. . . . . 5
4. CIRCUIT DIAGRAM. . . . . 7
5. PC BOARD . . . . . 10
6. CIRCUIT DESCRIPTIONS . . . . . 14
7. TROUBLESHOOTING TABLE. . . . . 20
8. CHECK AND ADJUSTMENT PROCEDURE . . . . . 21
9. REFERENCE DATA. . . . . 23
10. PARTS LIST . . . . . 32



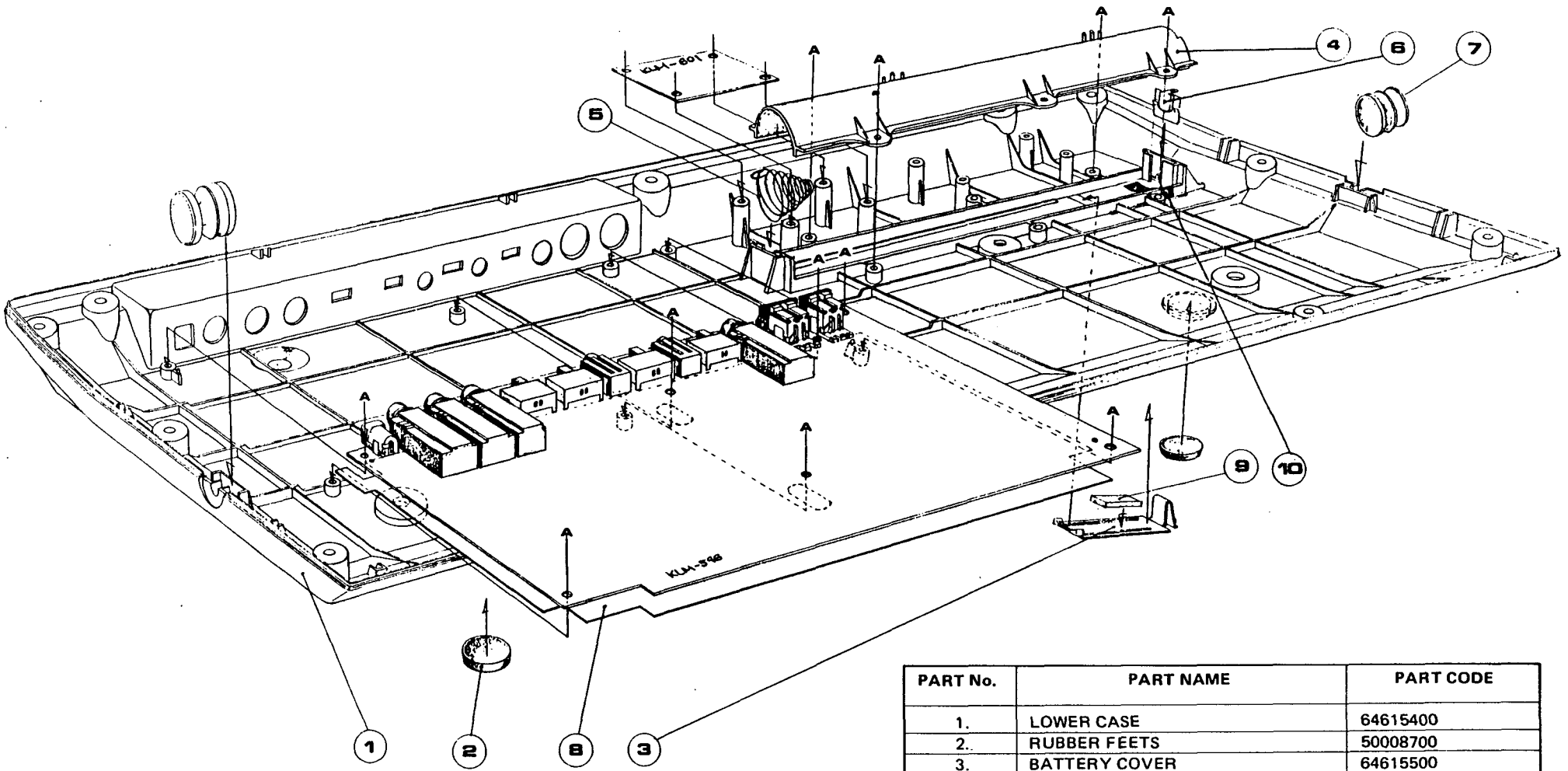
KEIO ELECTRONIC LABORATORY CORPORATION
TOKYO/JAPAN

# 2. STRUCTURAL DIAGRAM

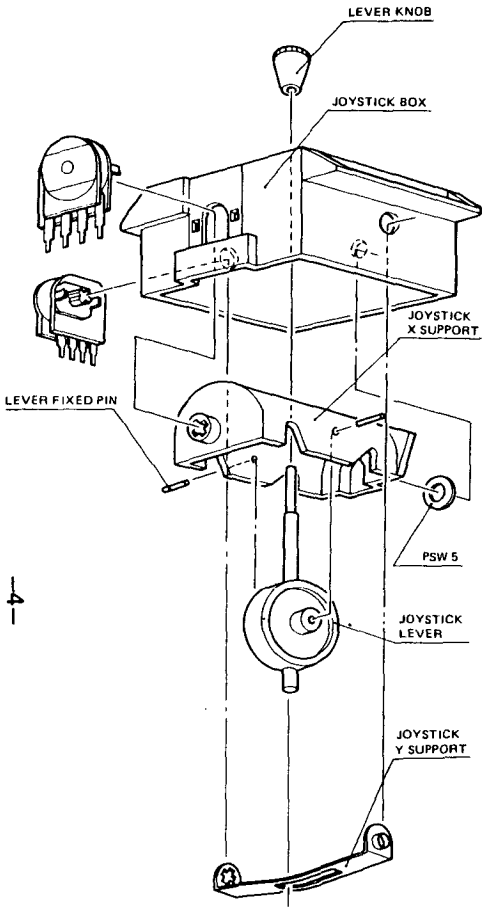


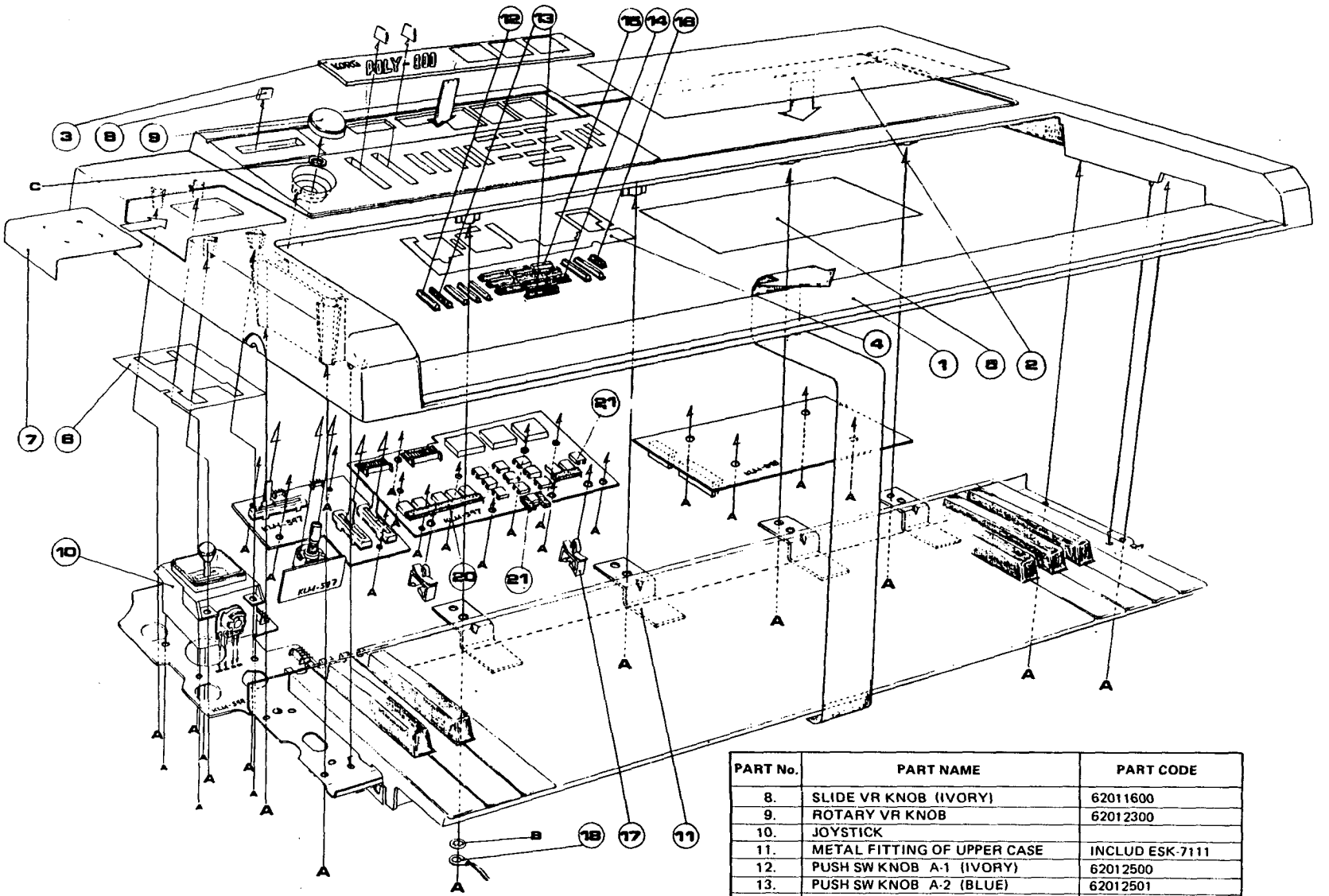




| PART No. | PART NAME | REMARKS |
|---|---|---|
| 1. | SERIAL NUMBER SEAL | KOC-F40050 |
| | | |
| A | SCREWS | FE B ZMC 5 x 8 |
| B | SCREWS | PLAX B ZMC 4 x 8 |
| C | SCREWS | PLAX B ZMC 4 x 12 |




| PART No. | PART NAME | PART CODE |
|---|---|---|
| 1. | LOWER CASE | 64615400 |
| 2. | RUBBER FEETS | 50008700 |
| 3. | BATTERY COVER | 64615500 |
| 4. | BATTERY HOLDER | 64615600 |
| 5. | BATTERY TERMINAL (SPRING) | 64058100 |
| 6. | BATTERY TERMINAL | 64058101 |
| 7. | STRAP PEG | 64402200 |
| 8. | SHIELDING SHEET | 58018004 |
| 9. | CUSHION FOR BATTERY | 50008800 |
| 10. | RIBBON | 54008100 |
| | | |
| A | SCREWS | PLAX B ZMC 3 x 8 |

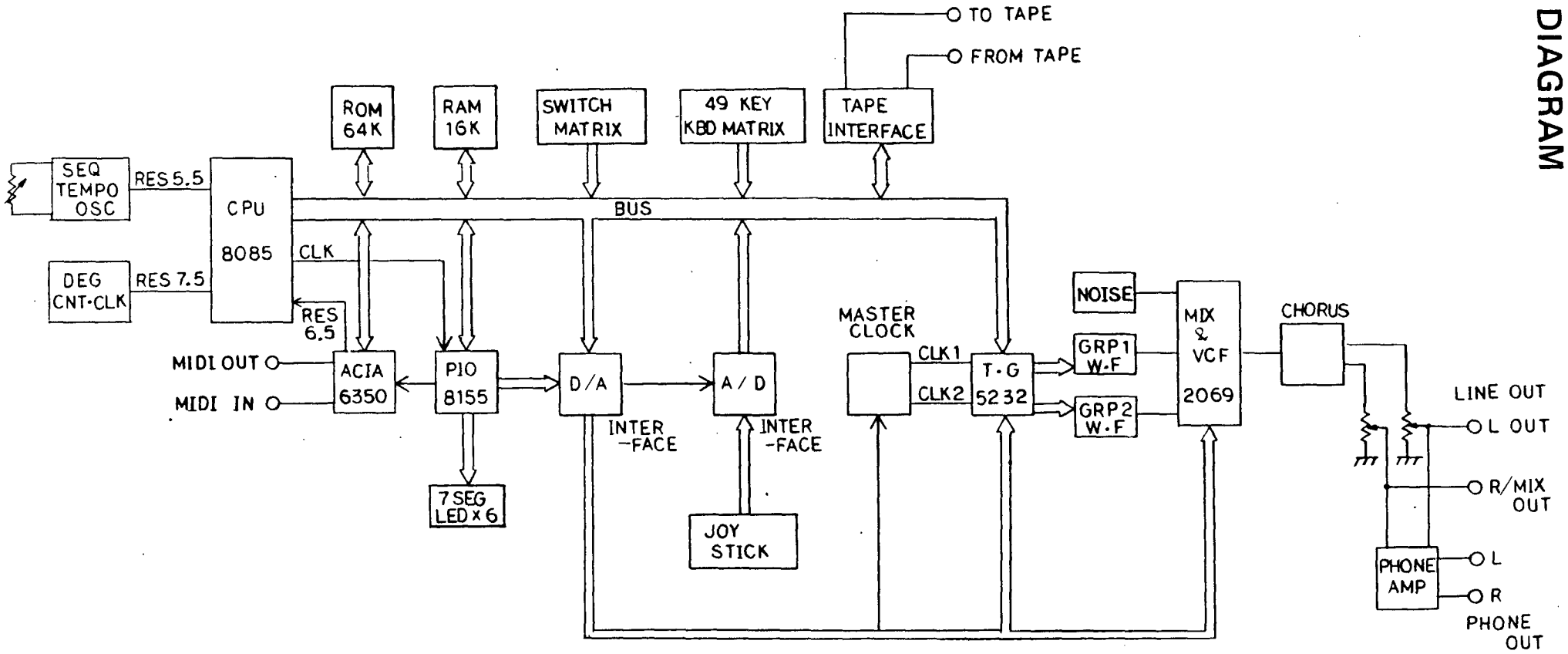


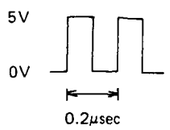

| PART No. | PART NAME | PART CODE |
|---|---|---|
| 1. | UPPER CASE | 64615300 |
| 2. | PARAMETER INDEX PANEL | 64905100 |
| 3. | DISPLAY COVER | 64905200 |
| 4. | SHIELDING PLATE FOR PANEL | 64063000 |
| 5. | SHIELDING PLATE FOR KLM-598 | 64062800 |
| 6. | SHIELDING PLATE FOR JOYSTICK | 64062900 |
| 7. | JOYSTICK PLATE | 64062600 |

| PART No. | PART NAME | PART CODE |
|---|---|---|
| 8. | SLIDE VR KNOB (IVORY) | 62011600 |
| 9. | ROTARY VR KNOB | 62012300 |
| 10. | JOYSTICK | |
| 11. | METAL FITTING OF UPPER CASE | INCLUD ESK-7111 |
| 12. | PUSH SW KNOB A-1 (IVORY) | 62012500 |
| 13. | PUSH SW KNOB A-2 (BLUE) | 62012501 |
| 14. | PUSH SW KNOB B-1 (BLUE) | 62012400 |
| 15. | PUSH SW KNOB B-2 (IVORY) | 62012401 |
| 16. | PUSH SW KNOB B-3 (RED) | 62012402 |
| 17. | HARNESS STOPPER WS-1NA | 54009400 |
| 18. | LUG 3φ | 67200100 |
| 20. | PUSH SW CUSHION A | 50008900 |
| 21. | PUSH SW CUSHION B | 50009000 |
| | | |
| A | SCREWS | PLAX B ZMC 3 x 8 |
| B | WASHERS | TWU ZMC 3 |
| C | NUT | VN ZMC 7 |

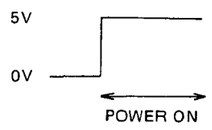
# 3. BLOCK DIAGRAM



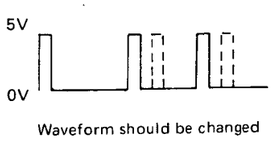
**A** CPU CLOCK



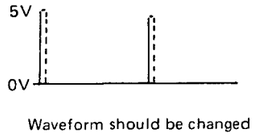

**B** CPU RESET



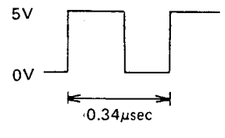

**C** CPU RES 6.5



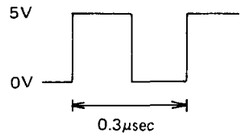

**D** CPU RES 5.5



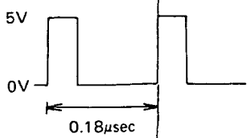

**E** CPU RES 7.5



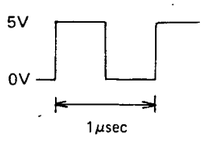

**F** CPU CLOCK OUT




**G** CPU ALE



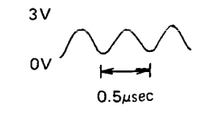

**H** TIMER OUT



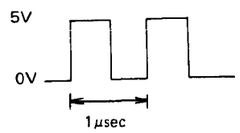

When using 74LS74

Tab this side.

**I** OSC CLOCK




**J** **K** CLOCK1, 2



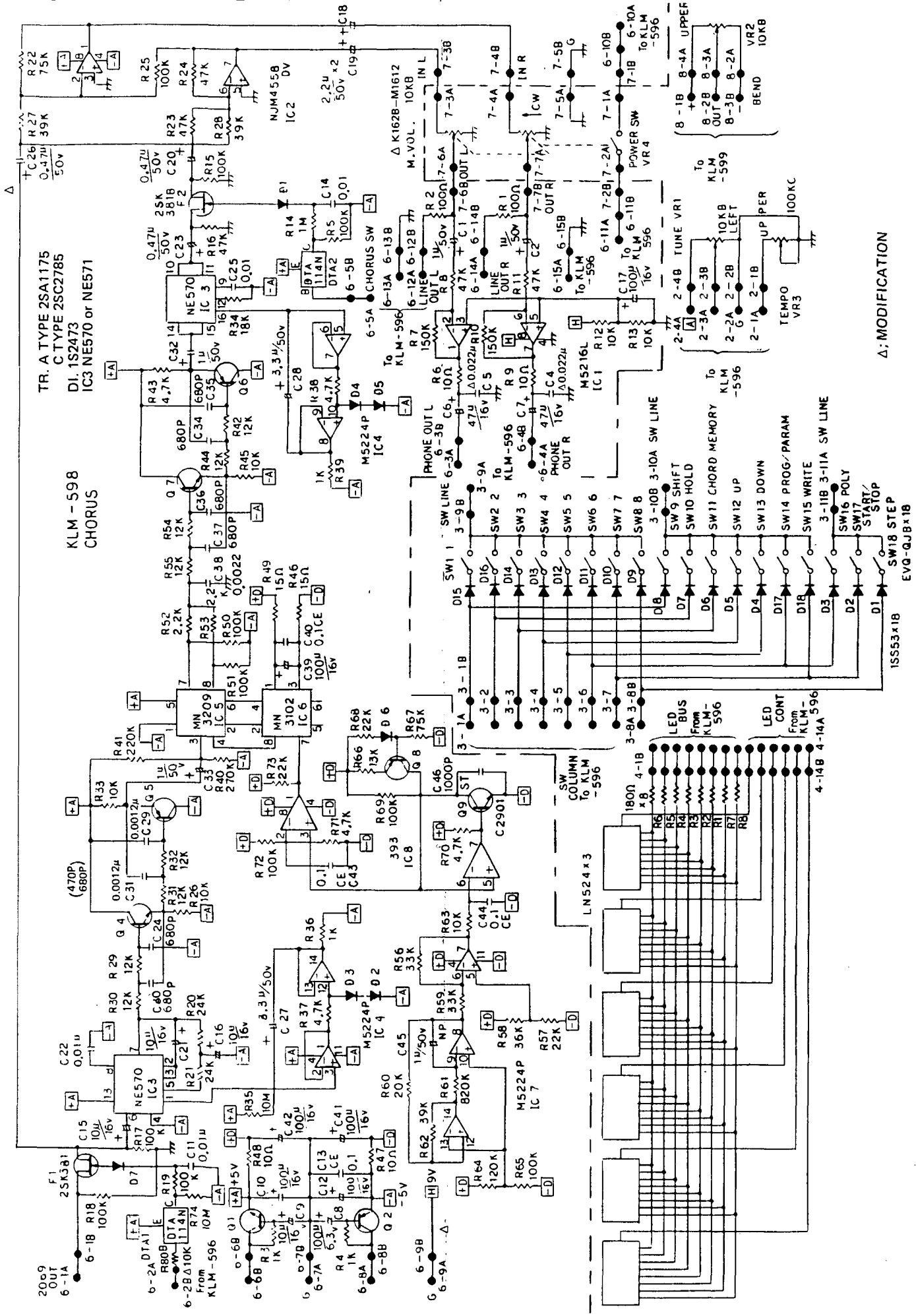

**L** WHITE NOISE


△; MODIFICATION

Value in bracket was used for Old production

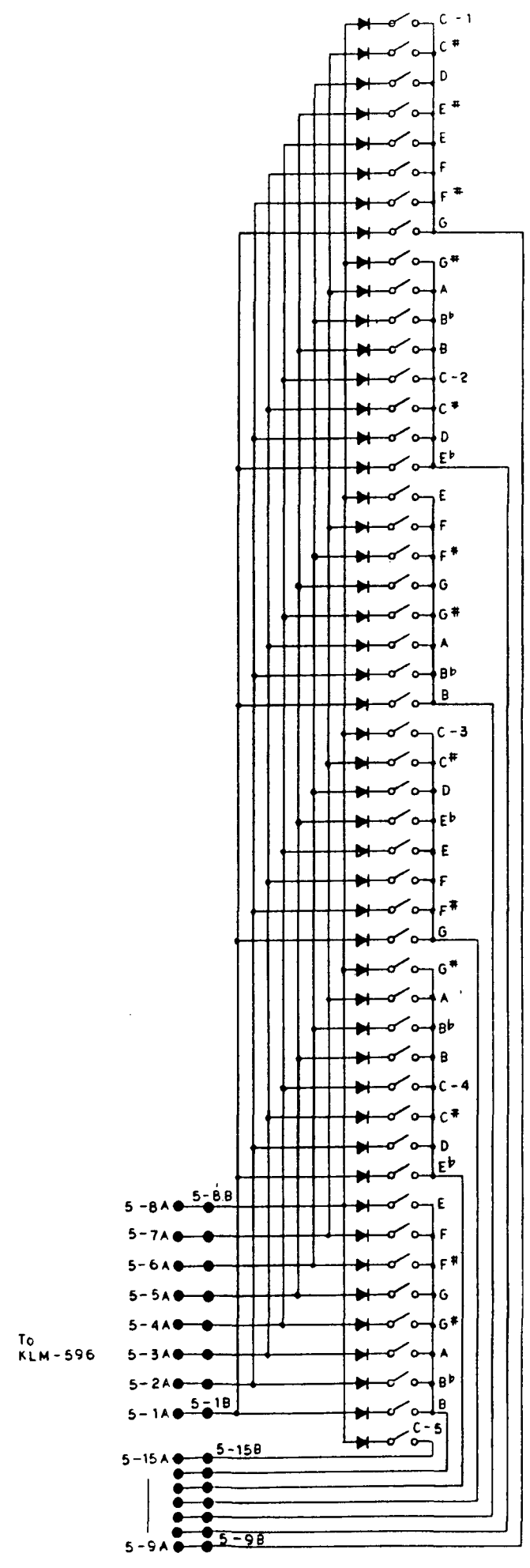
| IC-8 | | IC-12 | |
|---|---|---|---|
| OUTPUT | FUNCTION | OUTPUT | FUNCTION |
| X0 | DC01 LEVEL | X0 | Each EG signal of 8voice is coming out. |
| X1 | DC02 LEVEL | X1 | |
| X2 | RESO | X2 | |
| X3 | | X3 | |
| X4 | CUT OFF | X4 | |
| X5 | MG | X5 | |
| X6 | VIB | X6 | |
| X7 | BEND | X7 | |

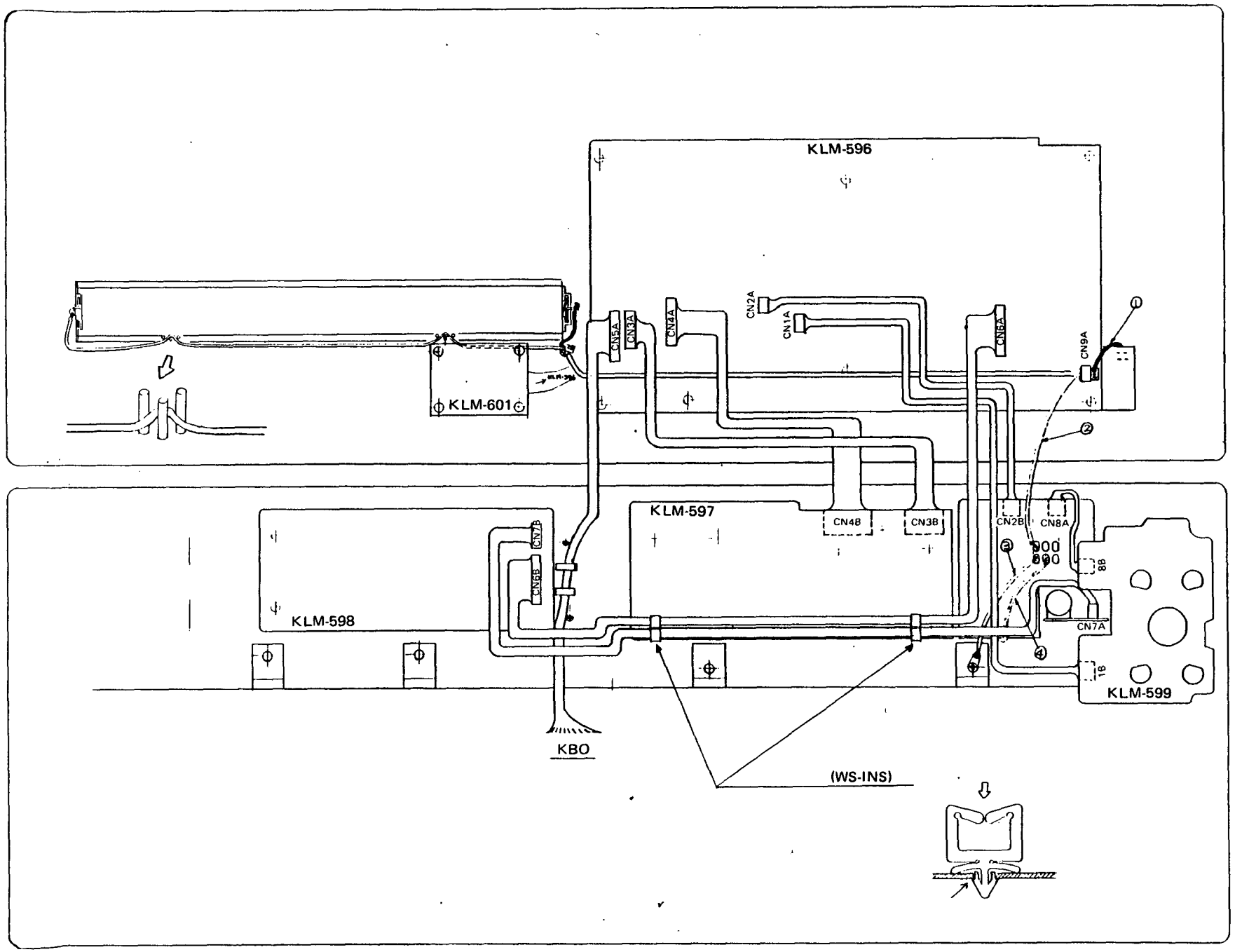
# 4. CIRCUIT DIAGRAM



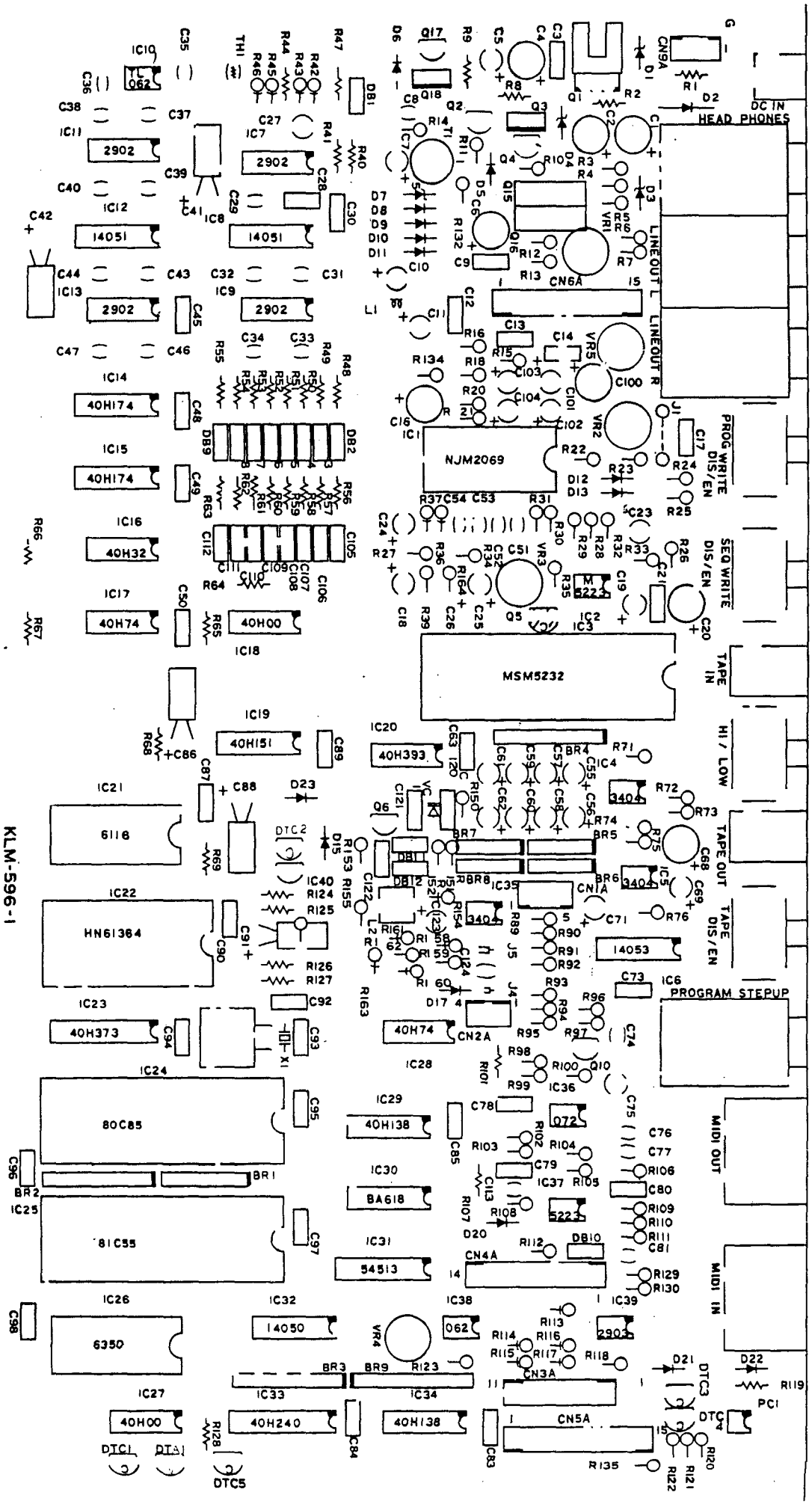


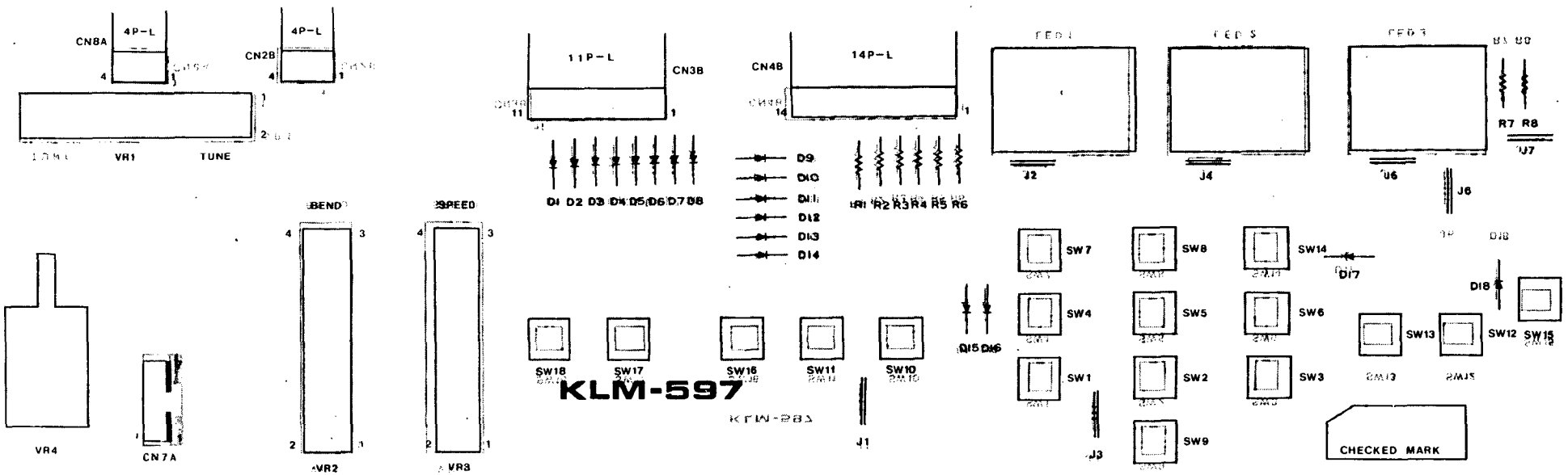

## KEY BOARD SWITCH MATRIX (49 Key)




KLM-596
KLM-601
CN5A
CN3A
CN4A
CN2A
CN1A
CN6A
CN9A
KLM-597
CN4B
CN3B
CN2B
CN8A
CN7B
CN6B
KLM-598
8B
CN7A
1B
KLM-599
KBO
(WS-INS)

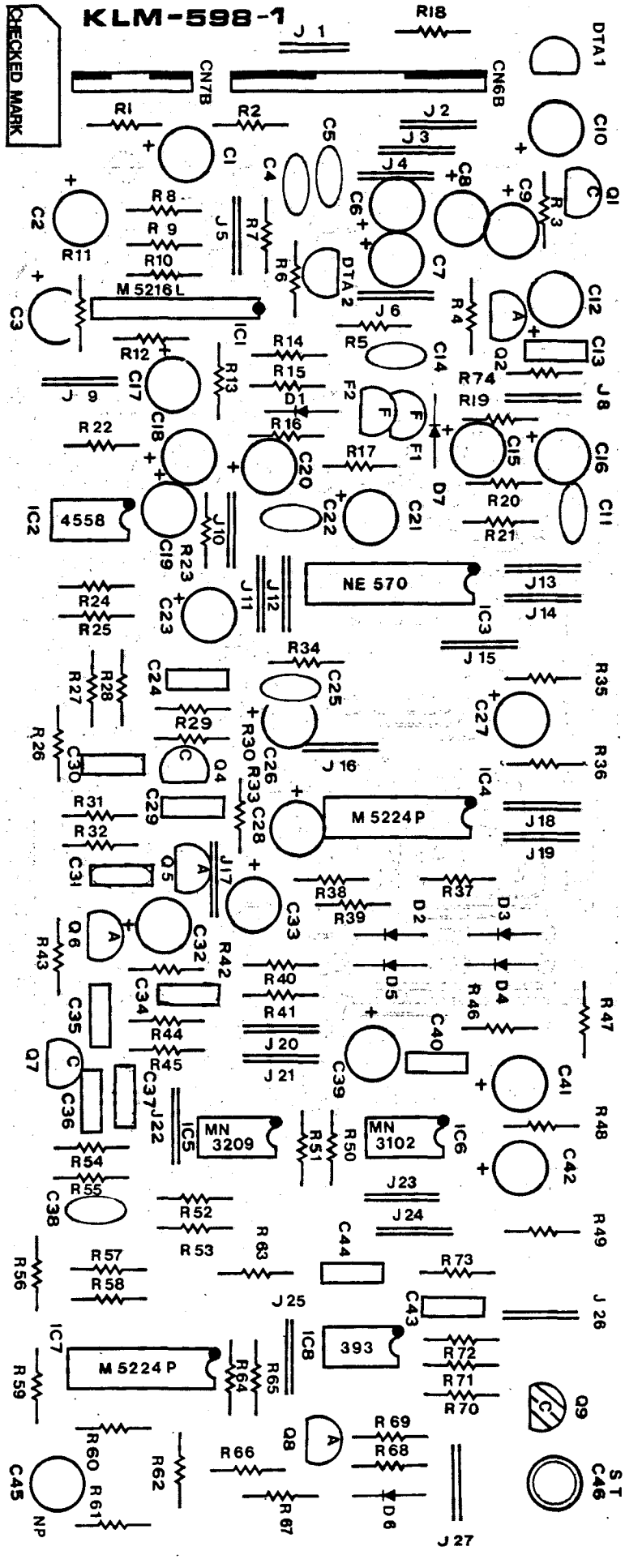
# 5. PC BOARD

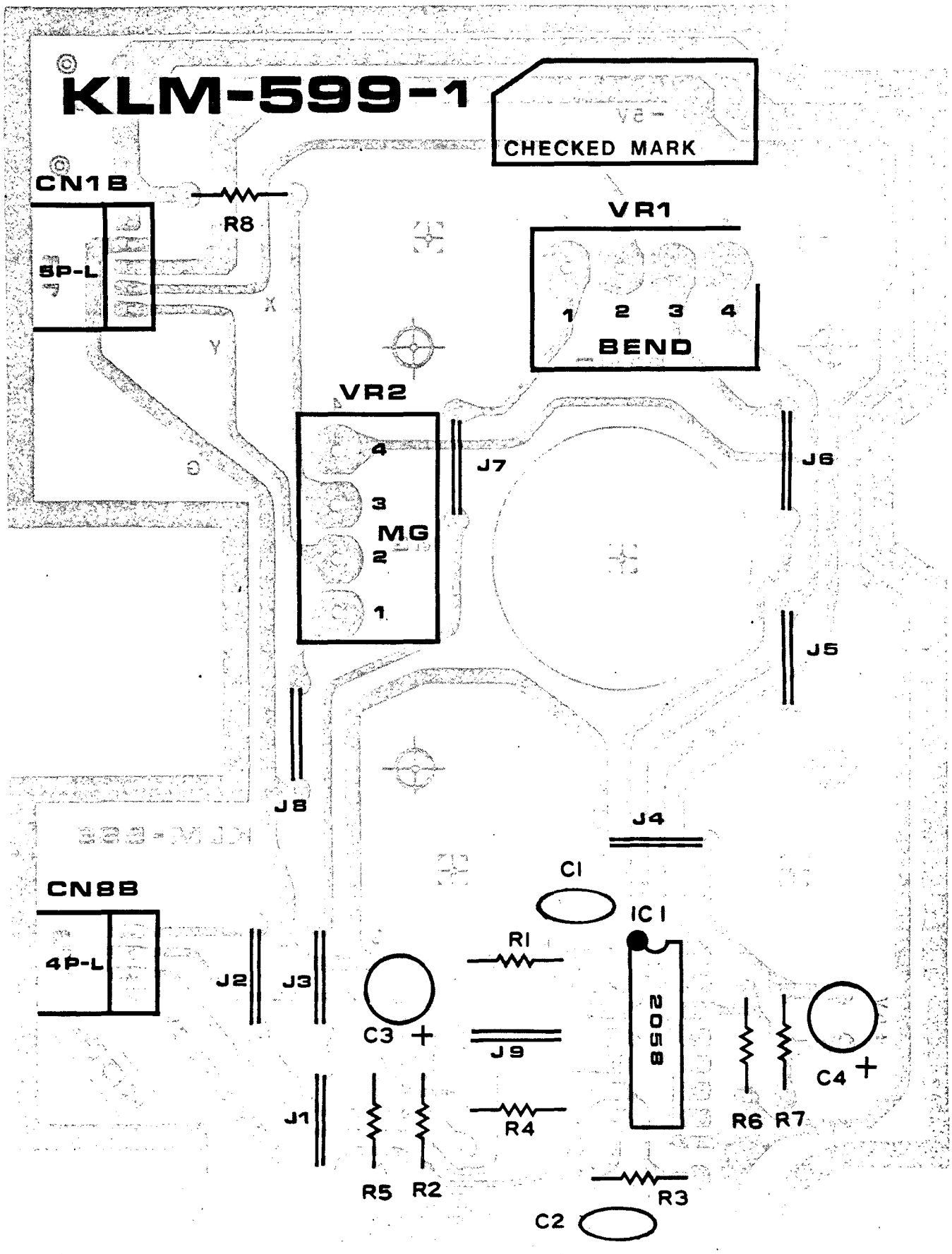

KLM-596-1
HEAD PHONES
DC IN
LINE OUT L
LINE OUT R
PROG WRITE DIS/EN
SEQ WRITE DIS/EN
TAPE IN
HI / LOW
TAPE OUT
TAPE DIS/EN
PROGRAM STEPUP
MIDI OUT
MIDI IN
NJM2069
MSM5232
HN61364
80C85
81C55
6118
6350
BA618
54513
14053
14050
40H00
40H32
40H74
40H138
40H151
40H240
40H373
40H393
14051
2902
3404
5223
2903
062
TL
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
IC11
IC12
IC13
IC14
IC15
IC16
IC17
IC18
IC19
IC20
IC21
IC22
IC23
IC24
IC25
IC26
IC27
IC28
IC29
IC30
IC31
IC32
IC33
IC34
IC35
IC36
IC37
IC38
IC39
IC40
CN1A
CN2A
CN3A
CN4A
CN5A
CN6A
CN9A
PC1


CN8A
4P-L
CN2B
4P-L
VR1
TUNE
11P-L
CN3B
CN4B
14P-L
D1 D2 D3 D4 D5 D6 D7 D8
D9
D10
D11
D12
D13
D14
R1 R2 R3 R4 R5 R6
J2
J4
J6
R7 R8
U7
U6
SW7
SW8
SW14
SW4
SW5
SW6
SW1
SW2
SW3
SW9
SW18
SW17
SW16
SW11
SW10
SW13
SW12
SW15
D15 D16
D17
D18
J1
J3
VR4
CN7A
BEND
SPEED
VR2
VR3
CHECKED MARK

KLM-597

104 B


KLM-598-1
CHECKED MARK
M 5216 L
4558
NE 570
M 5224 P
MN 3209
MN 3102
M 5224 P
393


KLM-599-1
CHECKED MARK
CN1B
5P-L
R8
VR1
1 2 3 4
BEND
VR2
4
3
MG
2
1
J7
J6
J5
J8
J4
CN8B
4P-L
J2
J3
C1
IC1
R1
C3 +
J9
J1
R4
R5
R2
R3
C2
2058
R6
R7
C4 +

# 6. CIRCUIT DESCRIPTIONS

## Introduction

The POLY-800 is an eight voice, programmable polyphonic synthesizer disigned, among other things, to be battery operated and thus portable, (It weighs less than 10 lbs with batteries included.) It features 64 programs with Edit and Tape Interface, MIDI (Musical Instrument Digital Interface) capabilities, built-in Noise Generator, Chorus and an all-digital programming system called the "DAC" (Digital Access Control) System.

## KEYBOARD DATA PROCESSING AND PANEL SWITCH OPERATION

There are six 8-tone keyboard buses (plus 1 tone for high C). IC34 decodes addresses for CPU bus line supply.
Key on/off data is read by the CPU via the IC33 buffer.
When the CPU receives key data, it instantly outputs pitch data to the TG. (Tone Generator)
**Note:** If IC34 (TC40H138) fails, then there will be no sound for some or all groups of eight notes. If IC33 (TC40H240) fails then sound will not be heard for every eighth note.
Switch operation is exactly the same as the keyboard.
DC01 and DC02 octave switching is read by the CPU via a matrix circuit and performed by IC3 (MSM5232) itself. The MSM5232 output goes through a waveform synthesis circuit (which includes IC's 4, 5, and 6) and is input to the filter chip IC1 (NJM2069).
Likewise, EG (DEG1, DEG2, DEG3), LEVEL1, LEVEL2, CUTOFF, and other switching is read by the CPU via the same matrix. The CPU processes the data and controls IC2069 via a D/A converter and time sharing CV circuit.
Data for sounds created by the user is stored in static RAM IC21 (HM6116). Therefore, to maintain all program data when the unit is turned off, it is necessary for this type of memory to have a battery back-up. Six size "C" 1.5V batteries provide backup power for RAM, as well as power the unit when the AC adaptor is not in use. A charged capacitor keeps RAM memory in tact for a short period of time if the batteries are weak or are removed. When replacing batteries, the user must be careful not to take more than four minutes, because contents of program memory will be erased if beyond that time, or if the battery voltage drops below the required level ( about 6 volts ).

## ABOUT MIDI

1. MIDI (Musical Instrument Digital Interface) is a hardware and software set of standards agreed on by many synthesizer manufacturers. It allows the interconnection of synthesizers, sequencers, computers, and rythm machines, 5-Pin DIN cords are used for connection between instruments and other devices. Maximum cable length is 15meters (50 feet).
The POLY-800 can be connected to other MIDI eauipped units for transmission and reception of the following data.

1) Key data [keyboard, sequencer]
2) Joystick
3) Sequencer clock & stop/start control
4) Program change

**Note:** Some instruments may not be able to process certain data. For example, if you connect the POLY-800 to a unit that does not have a pitch bending function, that unit will not be affected by POLY-800 pitch bending joystick movement.

### 2. Data format

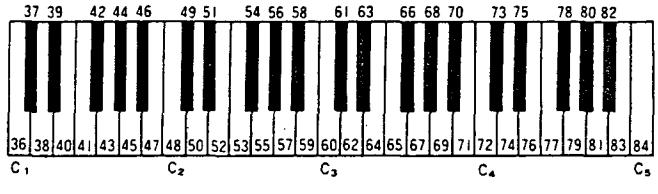
MIDI data transmission is in the form of messages of several bytes. Except for real time messages, a message always includes 1 status byte followed by 1 or 2 data bytes.

1) Key data consists of 3 bytes.

| STATUS | SECOND | THIRD | DESCRIPTION |
|---|---|---|---|
| 1001nnnn | 0KKKKKKK | 0VVVVVV | |

nnnn is the channel number. During transmission the keyboard channel is 0000 (channel 1), the sequencer is 0001 (channel 2). During reception it varies from 1 ~ 16. (depending on the channel the user selects)

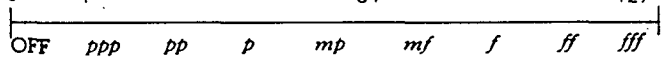
KKKKKKK determines keyboard pitch (0 ~ 127). For example, KKKKKKK=60 means the middle C key. See chart below.




If the POLY-800 receives keyboard data that is above or below its octave range, it shifts the octave and sounds the note within its keyboard range.
For example, when the POLY-800 is connected to a five octave keyboard and the DCO octave is programmed for 16', the upper four octaves of the five octave keyboard will respond just like the POLY-800's keyboard. Notes that are played in the fifth octave will repeat the notes in the fourth octave.

VVVVVVV is key velocity. On the POLY-800 this is either 0 or 64.
VVVVVVV = 64 if no velocity sensors.
VVVVVVV = 0 *means note off, with velocity* = 64

KEY VELOCITY



2) Joystick

Joystick X axis movement (bend) and Y axis movement (modulation) should be considered separately.

Joystick (bend) sensitivity is determined by the receiving side. Center values are sent as 00H, 40H.

| STATUS | SECOND | THIRD |
|---|---|---|
| 11100000 | 0VVVVVVV(LSB) | 0VVVVVVV(MSB) |

| LOW | CENTER | HIGH |
|---|---|---|
| LSB MSB<br>00H 00H | LSB MSB<br>00H 40H | LSB MSB<br>00H 7FH |

JOYSTICK (MODULATION MG)

| STATUS | SECOND | THIRD | DESCRIPTION |
|---|---|---|---|
| 10110000 | 00000001 | 0nnnn000 | +Y, DCO MG |
| 10110000 | 00000010 | 0nnnn000 | −Y, VCF MG |

3) Sequencer Clock & start/stop control.

The above are defined by 1 byte (real time messages).

(1) Sequencer clock (F8H)

| STATUS | DESCRIPTION |
|---|---|
| 11111000 | Synchronization is achieved by using 24 clock pulses per quarter note. |

(2) Start (FAH)

| STATUS | DESCRIPTION |
|---|---|
| 11111010 | Sent when start switch is pressed on sequencer or rhythm machine. |

(3) Stop (FCH)

| STATUS | DESCRIPTION |
|---|---|
| 11111100 | Sent when stop switch is pressed. Stops sequence. |

4) Program change [CnH; (Tx n=0 RX n=0~15)]

Consists of 1 status byte and 1 data byte.

| STATUS | DATA |
|---|---|
| 1100nnnn | 0PPPPPPP |

nnnn is the channel number which is 0000 for transmission and can be changed from 0~15 for reception.

PPPPPPP is the program number which for the POLY-800 is as shown in the chart below. (64 possible combinations from 00H~3FH)

| 2nd No. / 1st No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| 1 | 00H (0) | 01H (1) | 02H (2) | 03H (3) | 04H (4) | 05H (5) | 06H (6) | 07H (7) |
| 2 | 08H (8) | 09H (9) | 0AH (10) | 0BH (11) | 0CH (12) | 0DH (13) | 0EH (14) | 0FH (15) |
| 3 | 10H (16) | 11H (17) | 12H (18) | 13H (19) | 14H (20) | 15H (21) | 16H (22) | 17H (23) |
| 4 | 18H (24) | 19H (25) | 1AH (26) | 1BH (27) | 1CH (28) | 1DH (29) | 1EH (30) | 1FH (31) |
| 5 | 20H (32) | 21H (33) | 22H (34) | 23H (35) | 24H (36) | 25H (37) | 26H (38) | 27H (39) |
| 6 | 28H (40) | 29H (41) | 2AH (42) | 2BH (43) | 2CH (44) | 2DH (45) | 2EH (46) | 2FH (47) |
| 7 | 30H (48) | 31H (49) | 32H (50) | 33H (51) | 34H (52) | 35H (53) | 36H (54) | 37H (55) |
| 8 | 38H (56) | 39H (57) | 3AH (58) | 3BH (59) | 3CH (60) | 3DH (61) | 3EH (62) | 3FH (63) |

## TRANSMITTED DATA

| STATUS | SECOND | THIRD | DESCRIPTION |
|---|---|---|---|
| 1001000* | 0KKKKKKK | 01000000 | NOTE ON |
| 1000000* | 0KKKKKKK | 01000000 | NOTE OFF |
| 10110000 | 00000001 | 0nnnn000 | JOYSTICK (DCO) |
| 10110000 | 00000010 | 0nnnn000 | JOYSTICK (VCF) |
| 1011000* | 01111100 | 00000000 | MODE CHANGE OMNI OFF |
| 1011000* | 01111101 | 00000000 | MODE CHANGE OMNI ON |
| 1011000* | 01111111 | 00000000 | MODE CHANGE POLY ON |
| 11000000 | 000PPPPP | ——— | PROGRAM CHANGE (0~63) |
| 11100000 | 00000000 | 0bbbbbbb | PITCH BENDER (0~40H~7FH) |

NOTES:
1. The * can be 0 or 1. If 1, it becomes an exclusive seq data channel.
2. Pitch range (0KKKKKKK) is 24 ~ 54H.
3. Joy stick range (0nnn000)
   4-bit resolution.
4. Pitch bender range (0bbbbbbb)
   7-bit resolution; MSB only.
5. Mode change is sent with seq start/stop.
   For start, omni off, poly on: for stop, omni ON, poly on, to ch1 and ch2 respectively.
6. Real time messages are only sent during seq operation.

## RECOGNIZED RECEIVE DATA 1

| STATUS | SECOND | THIRD | DESCRIPTION |
|---|---|---|---|
| 1001**** | 0KKKKKKK | 0VVVVVVV | NOTE ON (V>0)<br>NOTE OFF (V=0)<br>VELOCITY IGNORED |
| 1000**** | 0KKKKKKK | 0VVVVVVV | NOTE OFF<br>VELOCITY IGNORED |
| 1011**** | 00000001 | 0nnnnnnn | MG1 (DCO)<br>bit 2 ~ bit 0 IGNORED<br>4 bit RESOLUTION |
| 1011**** | 00000010 | 0nnnnnnn | MG2 (VCF)<br>bit 2 ~ bit 0 IGNORED<br>4 bit RESOLUTION |
| 1011**** | 0xxxxxxx | 00000000 | MODE CHANGE<br>(SECOND BYTE)<br>7C; OMNI OFF<br>7D; OMNI ON<br>(REFER TO NOTE 8) |
| 1100**** | 0PPPPPPP | ——— | PROGRAM CHANGE<br>(EXAMPLE 70 → 06)<br>(EXAMPLE 64 → 00) |
| 1110**** | 0——— | 0bbbbbbb | PITCH BENDER<br>SECOND IGNORED<br>ONLY THIRD RECOGNIZED |

NOTES:
1. If omni is off, then only channel specified in parameter will be received.
   If omni is on, then everything will be received but mode change commands will only be obeyed for specified channel.
2. Pitch range (0KKKKKKK) is 24H ~ 54H. Other values will be transposed to nearest octave.
3. All Omni on/off commands will be interpreted as being accompanied by poly on.

## RECOGNIZED RECEIVE DATA 2

| STATUS | |
|---|---|
| 11111000 | TIMING CLOCK |
| 11111010 | START |
| △ ~~11111011~~ | ~~CONTINUE START (=START)~~ △ ; MODIFICATION |
| 11111100 | STOP |

NOTE: Timing clock is only received between start and stop. Continue start functions like start.

## PANEL CONTROL

| PARAMETER | | |
|---|---|---|
| 86 | RCV CH; | RECEIVE CHANNEL 1 ~ 16<br>BACK UPPED<br>ONLY EFFECTIVE AFTER OMNI OFF OR MODE CHANGE COMMAND. |
| 87 | PROG CHANGE; | 0 = DISABLE<br>1 = ENABLE<br>ONLY FUNCTIONS FOR RECEPTION. ALWAYS USED IN TRANSMISSION.<br>DISABLE DEFAULT |
| 88 | SEQ CLK; | 1 = INTERNAL; SEQ PERFORMED BY INTERNAL CLOCK.<br>2 = EXTERNAL, SEQ PERFORMED ACCORDING TO RECEIVED MIDI CLOCK. NOT TRANSMITTED.<br>INTERNAL DEFAULT |

## MAIN CIRCUIT DESCRIPTIONS

Below are simple descriptions of each circuit block.
Refer to circuit diagram for number.

1) Tape interface input circuit:
Consists of amplifier and comparator. When command is executed, data on this line is input to the CPU accumulator's 7th bit.

2) CPU:
A CMOS 8-bit microprocessor IC24 (80C85) featuring low power consumption. Virtually all POLY-800 functions are handled by this CPU.

3) Reset circuit:
IC40 (PST518) is a 3-pin IC used for reset. It generates an initial reset voltage of about 4.2V.

4) Sequencer tempo clock oscillator circuit
The tempo circuit includes IC28 (TC40H074) and 1/2 of IC36 (which is 1/2 of a TL072).
The tempo control is connected to CN2 pin 1 providing 10Hz±20% at the knob's 0 position and 100Hz±20% at the 10 position for CPU interrupts. If this circuit fails, then there will be no sound from the sequencer section.

5) Interrupt oscillator circuit:
This oscillator cycle is used for the EG, MG, LED displays, and S/H time division processing. Oscillator frequency is 2400Hz ~ 3600Hz. Interrupt order is by priority. If this circuit fails, EG operation and LED indication may become erratic.

6) Address Decoder:
TTL circuit decodes addresses for RAM and other ICs.

7) ROM (8192 words x 8bit PROM)

8) RAM (2048 words x 8bit static RAM)

9) Address latch:
IC latches according to CPU ALE (Address Latch Enable) terminal output signal since CPU uses address LSB 8bits together with data bus 8bit input.

10) Peripheral I/O:
PA, PB, and PC ports are all used for output. The internal timer is used for the interface IC26 (63B50) reference clock. The CPU 3MHz clock frequency is divided by 6 to obtain 500kHz. RAM is used for the program working area.

11) LED display drive circuit:
IC30 (BA618) and IC31 (M54513) form a 6 x 8 matrix for time sharing indication by the panel's 7-segment LED display.

12) 8-bit D/A converter:
Uses CMOS noninverting buffer IC32 (HD14050 or "4050"), and BR9 (RKM10L253F or "BR9") a 10-pin (R=25kohm) R-2R ladder resistor in D/A converter with output of 0V ~ 4V.

13) External DC power supply ripple filter:
Diode D2 is used to protect the circuit in case of reverse AC adapter polarity.

14) LED display power supply:
Circuit is designed so that LEDs become dim when battery voltage drops below rated level. (about 6V)

15) +5V power supply:
This circuit design is employed because it maintains normal operation up until just before the batteries drop below rated voltage of Volts (about 6V)

16) -5V power supply:
A type of DC-DC converter.

17) Bend depth circuit (KLM-599 PCB):
Because MIDI is used, R6 and R7 assure correct joystick center values.

18) A/D converter comparator.

19) Master oscillator:
Varactor VC1 and coil KL-003 are used in the oscillator circuit. This generates a frequency of about 2MHz at the tune knob's center position. This is divided down (to about 1MHz) to supply the TG. (CL1, CL2)
Bend and vibrato control voltages are D/A converted by IC35 (3404) and applied to the oscillator.

20) EG S/H circuit:
EG values calculated by the CPU are output by time sharing and input to the TG.
LED diodes for each voice are there to smooth the stepped transition.

21) Keyboard panel switch input circuit:
A 9 x 8 matrix is formed by DTC5, IC34 (TC40H138), and IC33 (TC40H240). This handles keyboard and panel switch outputs as well as output from the comparator in circuit diagram (18).

22) Detune circuit:
Lowers frequency by thinning out clock pulses.

23) Tape interface output circuit.

24) CV circuit:
Performs time division output and S/H on CV for VCF and master oscillator.

25) 6-bit latch circuit:
A 6-bit control output circuit with 2 bits for detune, 2 bits for DCO waveform switching, 1 bit for A/D converter, X-Y switching, and 1 bit for noise gate control.

26) 6-bit latch circuit:
A 6-bit control output circuit with 5 bits for S/H control and 1 bit for chorus on/off switching.

27) VCA + VCF circuit:
The IC1 (NJM2069) has three internal VCAs and one internal 24dB/oct VCF (LPF). SIG1 and SIG2 respectively receive mixed DCO1 and DCO2 inputs from the TG; LEVEL1 and LEVEL2 are control input terminals.
The other VCA is for noise only. The 9pin (VCA LIN IN) is its control terminal.
MG, EG INT and CUTOFF, KBD TRACK are controlled separately and input to VCF LOG.
See REFERENCE DATA for details.

28) Analog switch circuit:
Performs DCO waveform switching and joystick A/D converter input switching.

29) Noise generator.

30) MIDI interface circuit:
This is a standard type MIDI interface circuit employing the MIDI interface IC26 (ACIA63B50) and high processing speed photocoupler PC-1. (PC-900)
D22 is used to prevent destruction of the photocoupler LED in case a reverse voltage is applied. R119 (220 ohm) and R121 (220 ohm) resistors are for prevention of damage in case of excessive current.
The circuit is designed to provide a data transmission rate of 31.25 k baud (±1%).

31) Waveform synthesis circuit:
Using the TG's various foot outputs (16', 8', 4', and 2'), this produces 2-waveforms, one by addition on a 1=1=1=1 basis and the other using the ratio 1=1/2=1/4=1/8.
The block resistor BR5 (RKC 1/8 B4 33K) is made up of four 1/8W 33k resistors (1=1=1=1). BR6 (RMO0470) is 10K ohms using R, 2R, 4R, 8R (1=1/2=1/4=1/8).

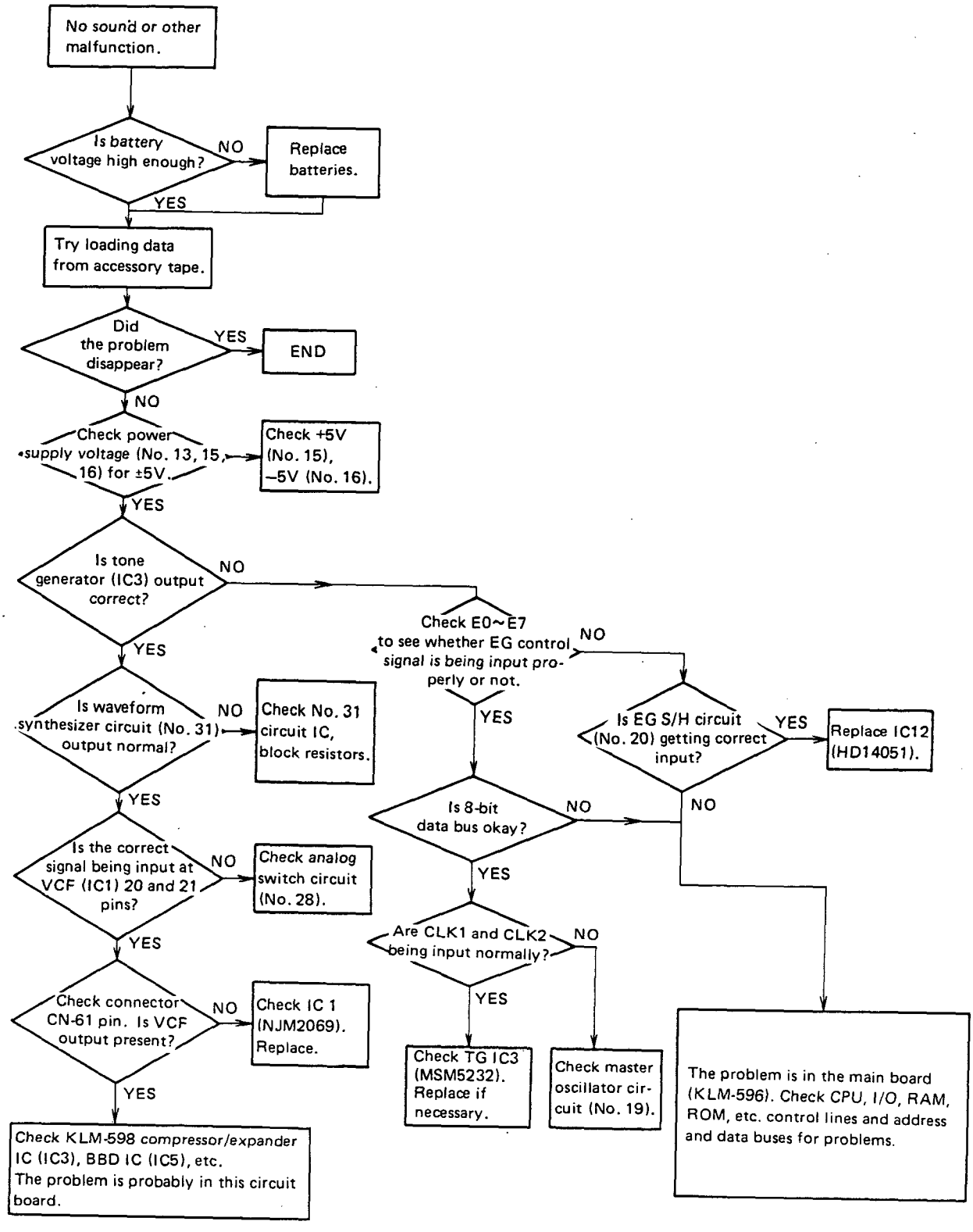
32) TG (Tone Generator):
An IC having eight sets of dividers and VCAs. See REFERENCE DATA for details.

## KLM-597, 598

KLM-598 consists of the chorus circuit and headphone amp circuit. The VCF output signal transits noise gate F1 (2SK381) and is input to compressor IC3 (NE570); then IC4 (M5224P) detects the envelope.
The clock generator circuit which drives the BBD IC makes IC7 (M5224P) generate a triangle wave which comparator IC8 (393) converts to a sawtooth wave with a change of pitch for a more natural chorus effect.
F2 (2SK381B) at the output is an FET for chorus on/off switching.
KLM-597 includes the panel section LED display and switch matrix circuitry.

# 7. TROUBLESHOOTING TABLE

The order in which things should be checked naturally coincides with the signal path in the POLY-800. Please refer to this flow chart to help you pinpoint sources of malfunctions. Remember to save user programs to tape before beginning service procedures.



# 8. CHECK AND ADJUSTMENT PROCEDURE

## ADJUSTMENT PROCEDURE

**Caution:** This product has been thoroughly adjusted at the factory before shipment. Therefore do not adjust anything other than those VRs required for servicing.

BEFORE making any calibration adjustments, Be sure test data is loaded into POLY-800.
The following setting chart shows the program data used for service testing. After inputting the data, save it on tape for future time saving convenience.

---

PROGRAM no. 11 (noise level):

| Parameter: | 17 | 18 | 33 | 41 | 43 | 45 | 48 | 71 | 72 | 73 | 74 | 75 | 76 | 83 | 84 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Value: | 0 | 1 | 15 | 99 | 0 | 0 | 0 | 0 | 0 | 31 | 0 | 31 | 0 | 0 | 0 |

PROGRAM no. 12 (master oscillator):

| Parameter: | 11 | 12 | 13 | 14~16 | 17 | 18 | 41 | 42 | 43 | 45 | 48 | 51 | 52 | 53 | 54 | 55 | 56 | 83 | 84 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Value: | 2 | 2 | 1 | 0 | 30 | 1 | 60 | 0 | 0 | 0 | 0 | 0 | 0 | 31 | 0 | 31 | 0 | 0 | 0 |

PROGRAM no. 13 (cutoff):

| Parameter: | 11 | 12 | 13 | 14~16 | 17 | 18 | 41 | 42 | 43 | 45 | 48 | 51 | 52 | 53 | 54 | 55 | 56 | 83 | 84 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Value: | 2 | 1 | 1 | 0 | 30 | 1 | 12 | 15 | 2 | 0 | 0 | 0 | 0 | 31 | 0 | 31 | 0 | 0 | 0 |

PROGRAM no. 14 (resonance):

| Parameter: | 11 | 12 | 13 | 14~16 | 17 | 18 | 41 | 42 | 43 | 45 | 48 | 51 | 52 | 53 | 54 | 55 | 56 | 83 | 84 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Value: | 1 | 1 | 1 | 0 | 31 | 1 | 59 | 15 | 0 | 0 | 0 | 0 | 0 | 31 | 0 | 31 | 0 | 0 | 0 |

**1. Power supply circuit (KLM-596, circuit no. 15):**

Be sure that the specified AC adapter is being used: 9V, 300mA,

1) +5V check and adjustment:
Use DVM (digital voltmeter) to check KLM-596 connector CN6 Pin 6 and confirm +5V (±0.005V). Adjust VR1 if necessary.

2) -5V check:
Use DVM to check KLM-596 connector CN6 Pin 8 and confirm −5V (within −4.7V ~ −5.7V)

**2. D/A converter check and adjustment (KLM-596, circuit no. 12):**

With joystick bend control at center position:
connect DVM to KLM-596 IC10 (TL062) Pin 7 and confirm 1.986V ±0.005V. Adjust VR4 if necessary.

Also confirm:
3.929V for an upward pitch bend and
0.076V for a downward pitch bend.

**Note:** Adjustment is easiest in the joystick circuit although the idea is to obtain a 4V output from IC 38 (TL062) by adjusting the D/A converter when IC 81C55 port A output is all high.

**3. Noise level check and adjustment:**

1) Select program no. 11.
2) Depress C3 key and set to HOLD.
3) Connect oscilloscope to KLM-596 CN6A 3 pin and confirm noise level of 0.3Vp-p (± 20%).
4) Adjust VR3 if necessary.

**4. Master oscillator check and adjustment:**

Set tune knob to center and bend intensity to maximum. Connect AT-12 to line out jack.
1) Select program no. 12.
2) Depress C3 key and set to HOLD.
3) Confirm AT-12 indication of −1 OCT, C, 0 cent. If necessary, adjust by turning KL-003 coil.
4) Next, push joystick to maximum upward pitch bend position and confirm AT-12 reading of −1 OCT, G, +35 cents. Adjust KLM-601 VR2 if necessary.
5) At maximum joystick downward pitch bend AT-12 indication should be −2 OCT, D, −35 cents. Adjust KLM-601 VR1 if necessary.

Δ; MODIFICATION

Δ; VR3 is a semi-fixed resistor to fix range of tune VR on front panel.
Confirm +40 ~ +70 cents when tune VR is at # max position.
Confirm −40 ~ −70 cents when tune VR is at b max position.
If necessary, Adjust VR3.

**5. Cutoff check and adjustment:**

1) Select program no. 13.
2) Play C3 and set to HOLD.
3) Connect oscilloscope to CN6A pin 3 and observe waveform as in figure 1.
4) Adjust VR2 to obtain maximum waveform amplitude.

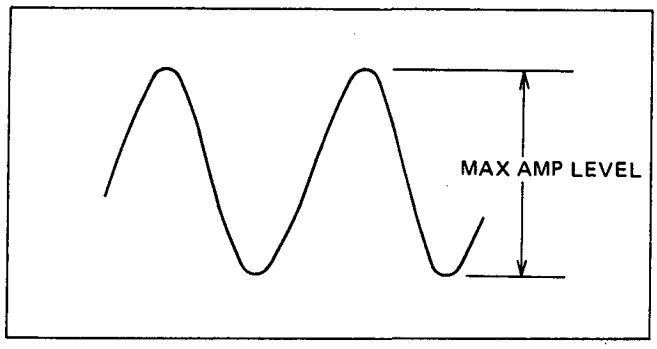



Fig. 1

**6. Resonance check and adjustment:**

1) Select program no. 14.
2) Play G4 and set to HOLD.
3) Confirm no oscillation and confirm that waveform is as shown in figure 2.
4) Adjust VR5 if necessary to prevent oscillation or to correct waveform deviation from figure 2 example.

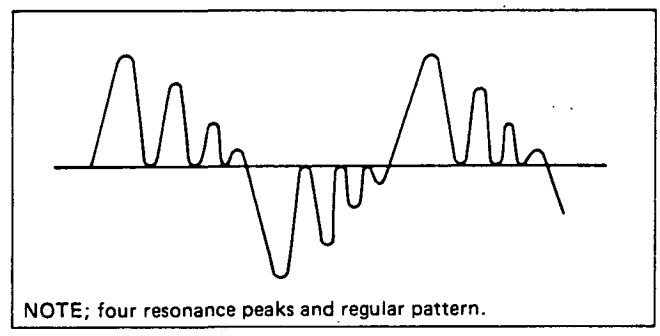


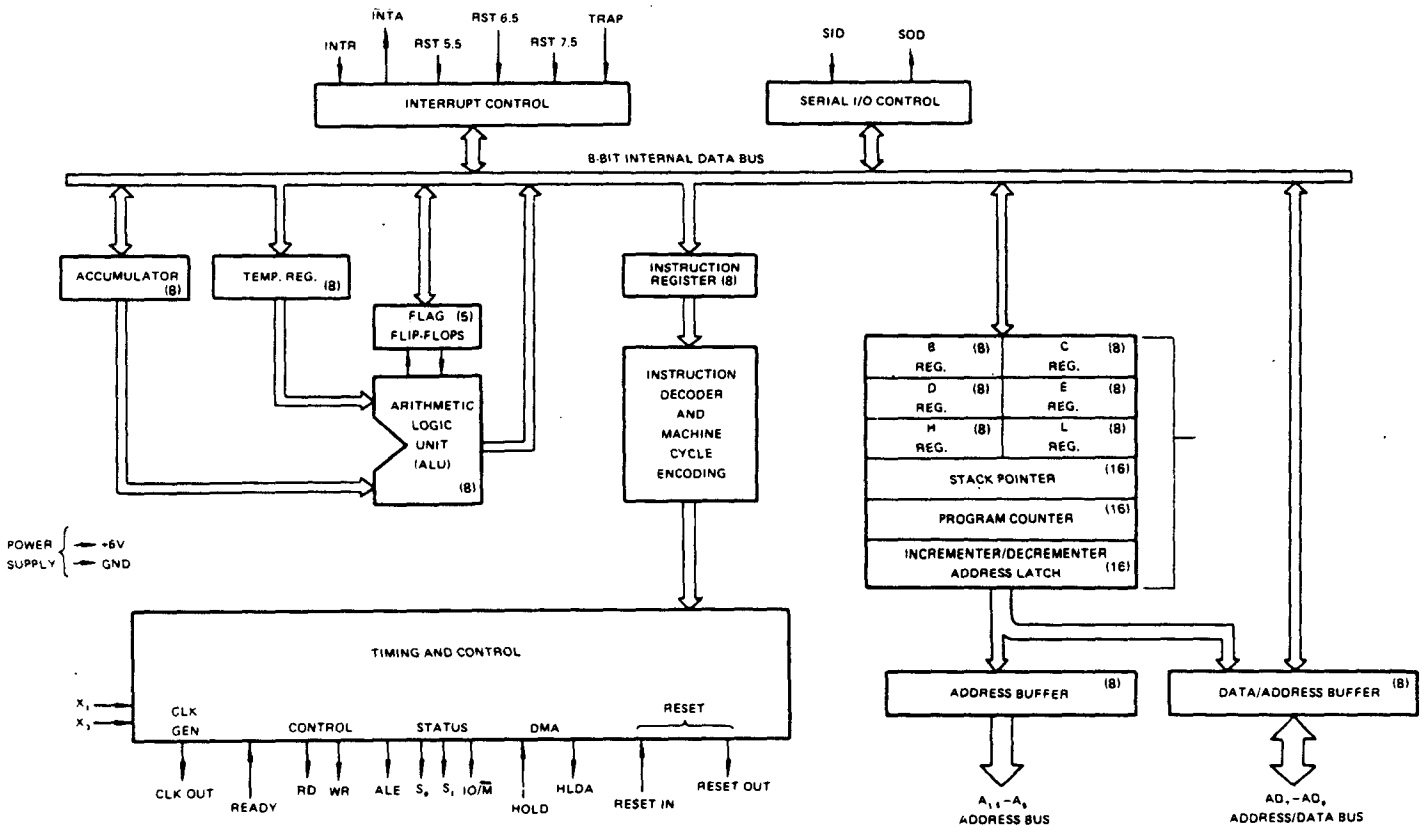

Fig. 2

# 9. REFERENCE DATA

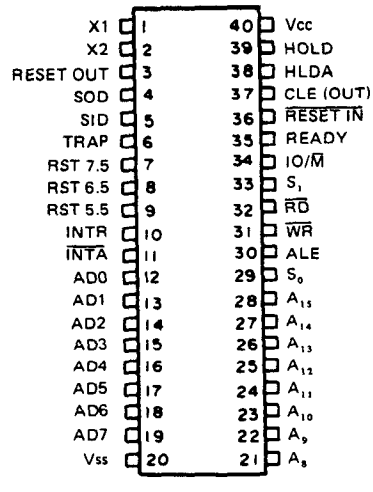
## 80C85A SINGLE CHIP 8-BIT CMOS MICROPROCESSORS

- Single +5V Power Supply
- 100% Software Compatible with 8080A
- 1.3$\mu$s Instruction Cycle (8085A); 0.8$\mu$s (8085A-2)
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is non-Maskable) Plus an 8080A-compatible interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64k Bytes of Memory

### BLOCK DIAGRAM




### PIN CONFIGURATION



## FUNCTIONAL PIN DEFINITION

The following describes the function of each pin;

**Symbol** — **Function**

$A_8$-$A_{15}$ (Output, 3-state)

Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

$AD_{0-7}$ (Input/Output, 3-state)

Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.

ALE (Output)

Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.

$S_0$, $S_1$, and IO/$\overline{M}$ (Output)

Machine cycle status:

| IO/$\overline{M}$ | $S_1$ | $S_0$ | Status |
|---|---|---|---|
| 0 | 0 | 1 | Memory write |
| 0 | 1 | 0 | Memory read |
| 1 | 0 | 1 | I/O write |
| 1 | 1 | 0 | I/O read |
| 0 | 1 | 1 | Opcode fetch |
| 1 | 1 | 1 | Interrupt Acknowledge |
| * | 0 | 0 | Halt |
| * | X | X | Hold |
| * | X | X | Reset |

* = 3-state (high impedance)
X = unspecified

$S_1$ can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, $S_0$ and $S_1$ become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.

**Symbol** — **Function**

$\overline{RD}$ (Output, 3-state)

READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.

$\overline{WR}$ (Output, 3-state)

WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.

READY (Input)

If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.

HOLD (Input)

HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.

HLDA (Output)

HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.

INTR (Input)

INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

## FUNCTIONAL PIN DESCRIPTION (Continued)

| Symbol | Function |
|---|---|
| $\overline{INTA}$ (Output) | INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an $\overline{INTR}$ is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port. |
| RST 5.5<br>RST 6.5<br>RST 7.5<br>(Inputs) | RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.<br><br>The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction. |
| TRAP (Input) | Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 1.) |
| $\overline{RESET\ IN}$ (Input) | Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flaps may be altered by RESET with unpredictable results. $\overline{RESET\ IN}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{RESET\ IN}$ is applied. |
| RESET OUT (Output) | Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods. |
| $X_1, X_2$ (Input) | $X_1$ and $X_2$ are connected to a crystal, LC, and RC network to drive the internal clock generator. $X_1$ can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency. |
| CLK (Output) | Clock Output for use as a system clock. The period of CLK is twice the $X_1$, $X_2$ input period. |
| SID (Input) | Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed. |
| SOD (Output) | Serial output data line. The output SOD is set or reset as specified by the SIM instruction. |
| Vcc | +5 volt supply. |
| Vss | Ground Reference. |

**TABLE 1** **INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY**

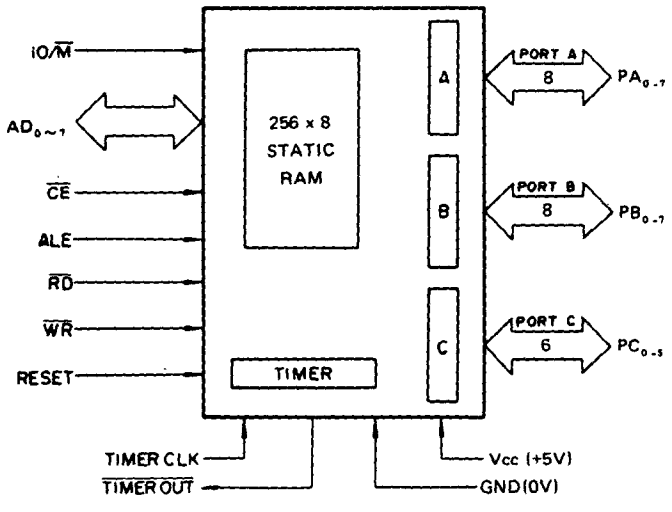
| Name | Priority | Address Branched To (1) When Interrupt Occurs | Type Trigger |
|---|---|---|---|
| TRAP | 1 | 24H | Rising edge AND high level until sampled. |
| RST 7.5 | 2 | 3CH | Rising edge (latched). |
| RST 6.5 | 3 | 34H | High level until sampled. |
| RST 5.5 | 4 | 2CH | High level until sampled. |
| INTR | 5 | See Note (2). | High level until sampled. |

NOTES:
(1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depend on the instruction provided to the cpu when the interrupt is acknowledged.

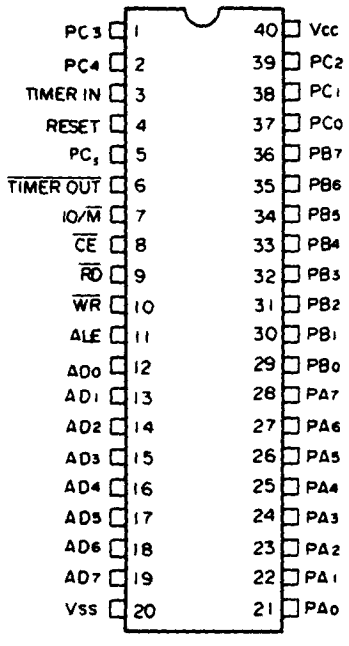
# MSM81C55RS 2048-BIT CMOS STATIC RAM WITH I/O PORTS AND TIMER

- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Compatible with 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

## BLOCK DIAGRAM




## PIN CONFIGURATION

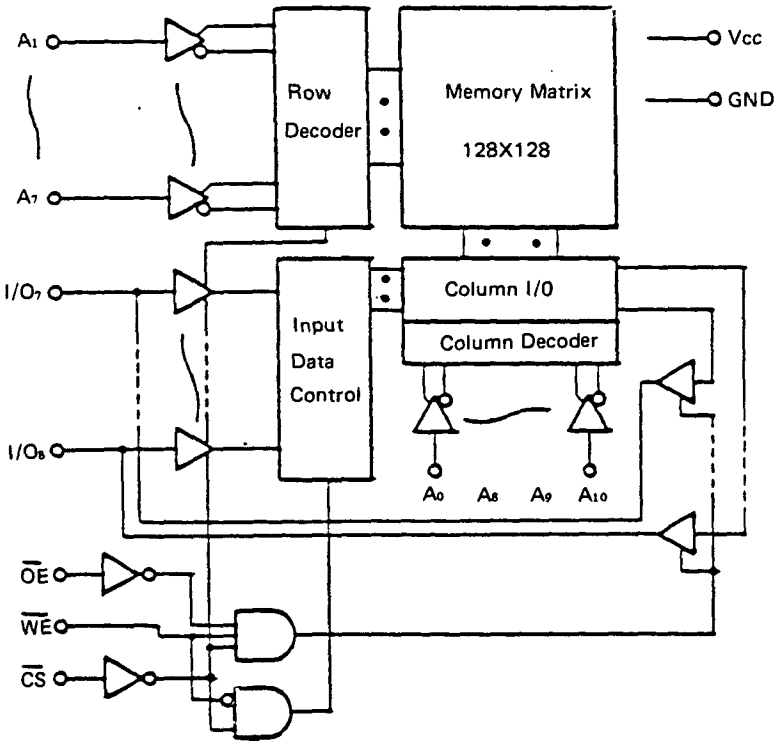



## PIN FUNCTIONS

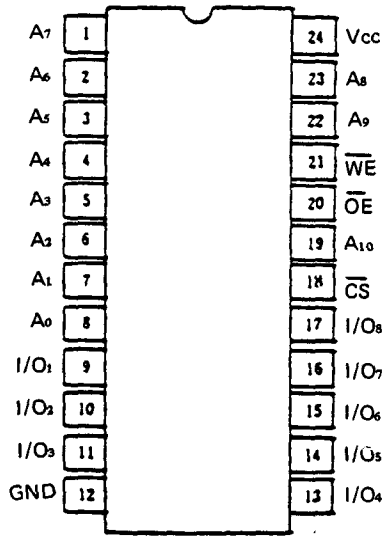
| Symbol | Function |
|---|---|
| RESET (Input) | Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085A clock cycle times. |
| $AD_{0-7}$ (Input/Output) | 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal. |
| CE or $\overline{CE}$ (Input) | Chip Enable: On the 8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH. |
| $\overline{RD}$ (Input) | Read control: Input low on this line with the Chip Enable active enables and $AD_{0-7}$ buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus. |
| $\overline{WR}$ (Input) | Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/$\overline{M}$. |
| ALE (Input) | Address Latch Enable: This control signal latches both the address on the $AD_{0-7}$ lines and the state of the Chip Enable and IO/M into the chip at the falling edge of ALE. |
| IO/M (Input) | Selects memory if low and I/O and command/status registers if high. |
| $PA_{0-7}$ (8) (Input/Output) | These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register. |
| $PB_{0-7}$ (8) (Input/Output) | These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register. |
| $PC_{0-5}$ (6) (Input/Output) | These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When $PC_{0-5}$ are used as control signals, they will provide the following:<br>$PC_0$ – A INTR (Port A Interrupt)<br>$PC_1$ – ABF (Port A Buffer Full)<br>$PC_2$ – A $\overline{STB}$ (Port A Strobe)<br>$PC_3$ – B INTR (Port B Interrupt)<br>$PC_4$ – B $\overline{BF}$ (Port B Buffer Full)<br>$PC_5$ – B STB (port B Strobe) |
| TIMER IN (Input) | Input to the counter-timer. |
| $\overline{TIMER\ OUT}$ (Output) | Timer output. This output can be either a square wave or a pulse depending on the timer mode. |
| Vcc | +5 volt supply. |
| Vss | Ground Reference. |

## 3. HM6116 2048-WORD × 8-BIT HIGH SPEED STATIC CMOS RAM

### BLOCK DIAGRAM

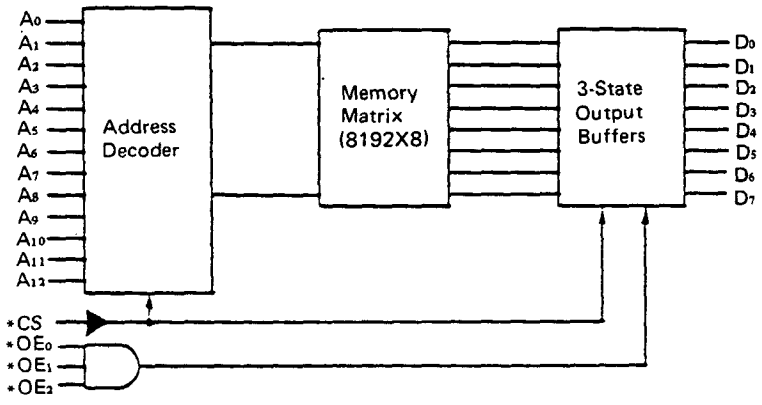



### PIN CONFIGURATION

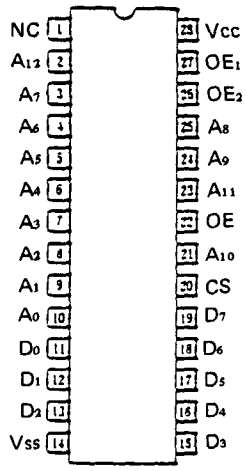



## 4. HN61364 8192-WORD × 8-BIT MASK PROGRAMMABLE READ ONLY MEMORY

### BLOCK DIAGRAM

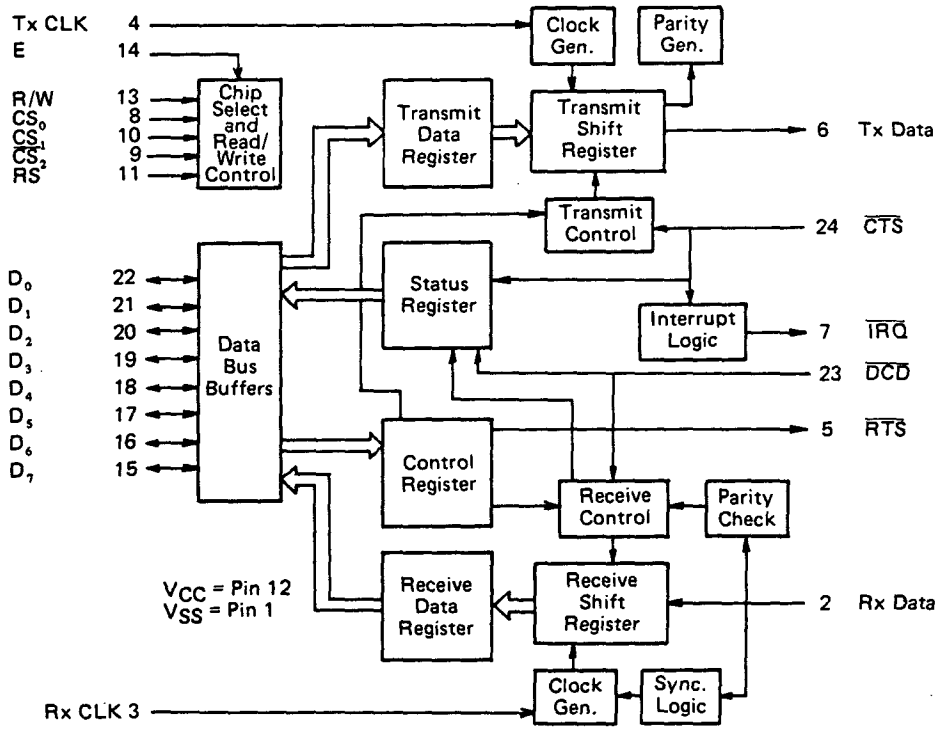



### PIN CONFIGURATION

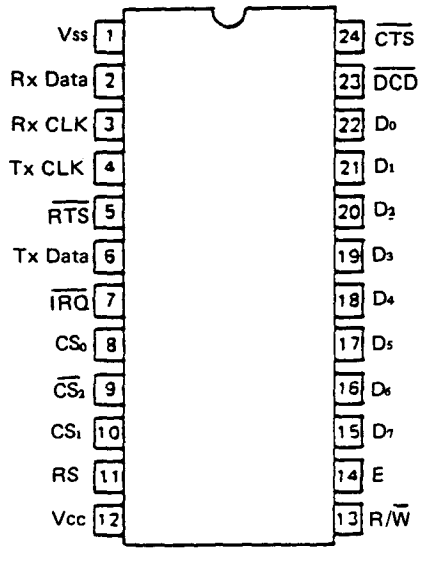


## 5. HD63B50 CMOS ACIA (CMOS ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER)

### BLOCK DIAGRAM

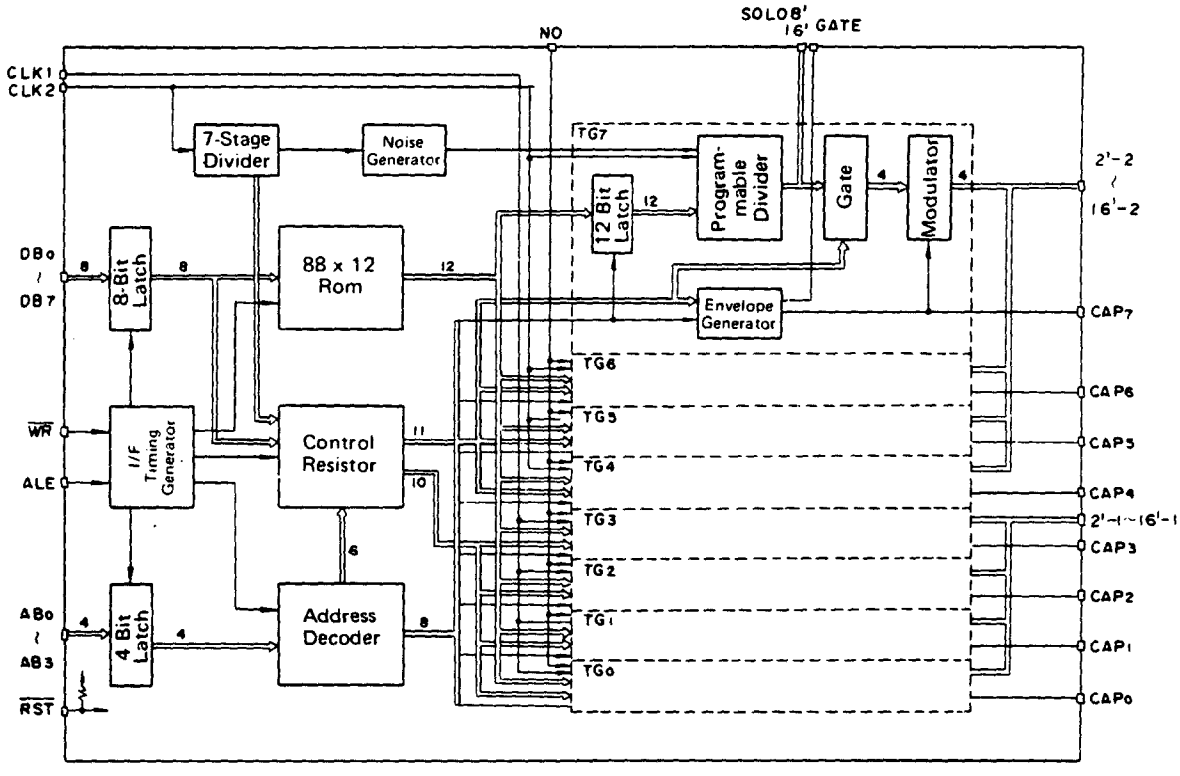



### PIN CONFIGURATION

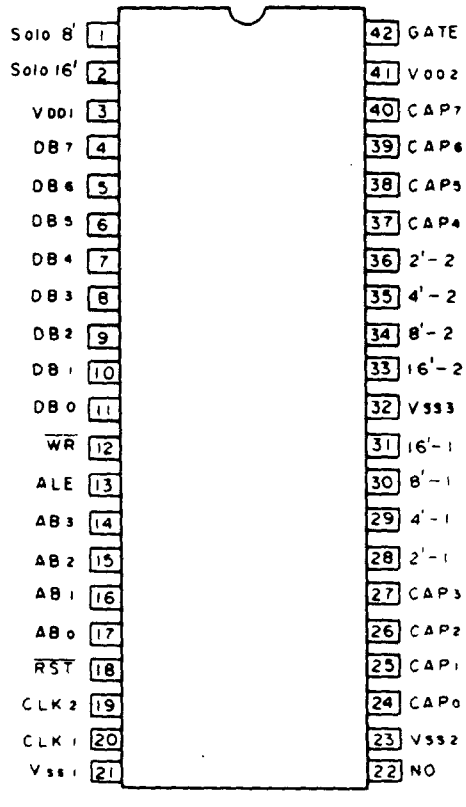


# IC MSM5232RS 8CHANNELS MUSICAL INSTRUMENT TONE GENERATOR

## BLOCK DIAGRAM




## PIN CONFIGURATION



## IC MSM5232RS SPECIFICATIONS

The MSM5232RS is a musical instrument tone generator IC that includes eight sets of scale generating frequency dividers and envelope generators with an 8-bit bus interface integrated on a single chip. It can simultaneously output eight sounds over a seven octave range under microprocessor control.

## CHARACTERISTICS

- 2-group 4+4–tone polyphonic output.
  Each group has its own clock input, output bus, and control register, enabling rich, variegated sound operation.
- 7-octave range, plus noise output capability.
- Four foot length outputs: 2', 4', 8' and 16'.
- Built-in envelope generator.
  Sustained and attenuated envelope waveforms and variable attack and delay time constants.
- Interface for 8-bit microprocessor control.
- Built-in scale generating ROM converts key number into frequency divider data.
- CMOS IC means low power operation.

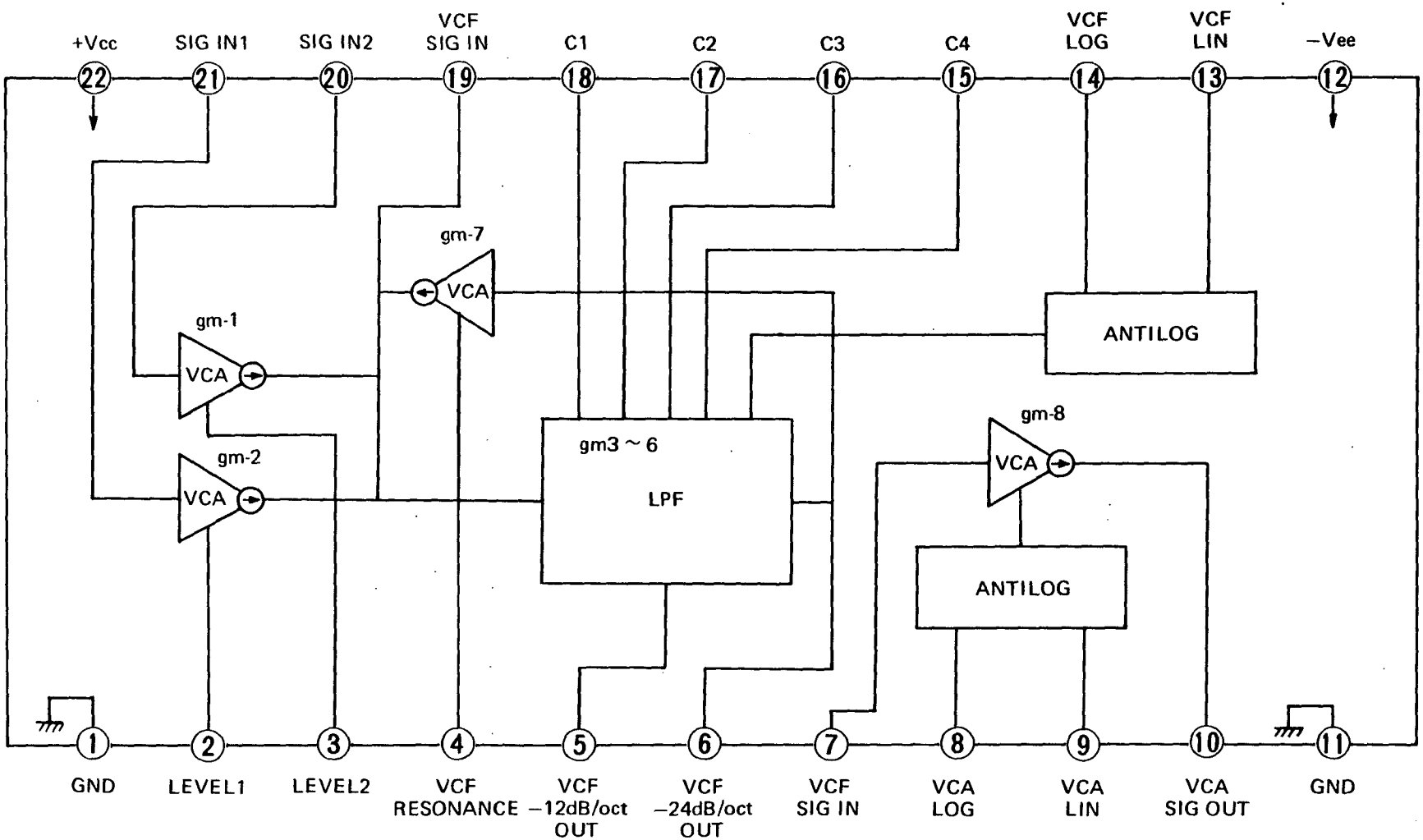
## PIN FUNCTIONS

| Symbol | Function |
|---|---|
| DB0 ~ B7 | Data input terminals. Connected to CPU data bus, so all data is input through these terminals. |
| AB0 ~ AB3 | Address input terminals. These inputs select data write registers. |
| ALE | When this input is at "H", trailing edge is latched and signals applied to AB0-AB3 are input to address register. |
| WR | When this input is at "L", trailing edge is latched and signals applied to DB0-DB7 are input to data latch. |
| CLK1, CLK2 | Reference clock input. Output scale is obtained by frequency division of this input. CLK1 is the reference frequency for tone generators TG0-TG3 (group 1), while CLK2 is for TG4-TG7 (group 2). |
| RST | Internal initialization input terminal. Pull-up resistor is built in. |
| CAP0-CAP7 | Envelope generator capacitor connection terminals. Envelopes are generated by charging and discharging of this capacitance through internal resistance. Furthermore, if envelope generator operation is prohibited, a high impedance state will be created and external envelope waveform input will become possible. |

| Symbol | Function |
|---|---|
| 2'-1 ~ 16'-1, 2'-2 ~ 16'-2 | Tone bus output terminals. Divided into group 1 and group 2. Each is made up of four registers: 2', 4', 8', and 16'. Four tone generators are connected to each tone bus, and are mixed by current adding. Therefore this output must be fed to a low impedance. |
| SOLO8', SOLO16' | Solo sound source output terminals. TG7, 8' and 16' pitched rectangle waves are always available at these outputs. |
| GATE | On/off signal output for solo outputs. In the solo mode, TG7 GF is output. It becomes "L" level when solo mode is prohibited. |
| NO | Noise output terminal. Internal simulated random noise generator provides noise which is available at this output at all times. |
| VDD1, VSS1 | 5 V power supply terminal. |
| VDD2, VSS2, VSS3 | 5 ~ 15 V power supply terminal. |

**NOTE:** Please connect VDD1 and VDD2 as well as VSS2 and VSS3, each externally.

## BLOCK DIAGRAM AND PIN CONFIGURATION



# 10. PARTS LIST

| PART CODE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| | **CARBON RESISTORs** | | | |
| 10013710 | S1/4JY 1M | | | 2 |
| 10016610 | 1/6JY 100K | KLM-601 | | 1 |
| 10016615 | 1/6JY 150K | | | 1 |
| 10016722 | 1/6JY 2.2M | | | 1 |
| 10113747 | S1/4JT 4.7M | KLM-596 | | 1 |
| 10413210 | S1/4JYTP 10Ω | KLM-598 | | 4 |
| 10413215 | S164JYTP 15Ω | | | 2 |
| 10413247 | S1/4JYTP 47Ω | KLM-596 | | 2 |
| 10413310 | S1/4JYTP 100Ω | KLM-598 | | 2 |
| 10413318 | S1/4JYTP 180Ω | KLM-597 | | 8 |
| 10413322 | S1/4JYTP 220Ω | KLM-596 | | 2 |
| 10413333 | S1/4JYTP 330Ω | | | 1 |
| 10413347 | S1/4JYTP 470Ω | | | 1 |
| 10413410 | S1/4JYTP 1K | | | 8 |
| | | KLM-598 | | 4 |
| 10413422 | S1/4JYTP 2.2K | KLM-596 | | 1 |
| | | KLM-598 | | 2 |
| | | KLM-599 | | 1 |
| 10413439 | S1/4JYTP 3.9K | | | 1 |
| 10413447 | S1/4JYTP 4.7K | KLM-598 | | 5 |
| 10413510 | S1/4JYTP 10K | KLM-596 | | 8 |
| | | KLM-598 | | 6 |
| 10413512 | S1/4JYTP 12K | | | 8 |
| 10413513 | S1/4JYTP 13K | | | 1 |
| 10413518 | S1/4JYTP 18K | | | 1 |
| 10413520 | S1/4JYTP 20K | | | 1 |
| 10413522 | S1/4JYTP 22K | | | 3 |
| 10413524 | S1/4JYTP 24K | | | 2 |
| 10413533 | S1/4JYTP 33K | KLM-596 | | 1 |
| | | KLM-598 | | 2 |
| 10413536 | S1/4JYTP 36K | | | 1 |
| 10413539 | S1/4JYTP 39K | KLM-596 | | 8 |
| | | KLM-598 | | 3 |
| 10413547 | S1/4JYTP 47K | | | 5 |
| 10413562 | S1/4JYTP 62K | KLM-596 | | 1 |
| 10413575 | S1/4JYTP 75K | KLM-598 | | 2 |
| 10413610 | S1/4JYTP 100K | KLM-596 | | 3 |
| | | KLM-598 | | 11 |
| | | KLM-599 | | 4 |
| 10413612 | S1/4JYTP 120K | KLM-598 | | 1 |
| 10413615 | S1/4JYTP 150K | | | 2 |
| 10413622 | S1/4JYTP 220K | | | 2 |
| 10413627 | S1/4JYTP 270K | | | 1 |
| 10413682 | S1/4JYTP 820K | | | 1 |
| 10413710 | S1/4JYTP 1M | KLM-596 | | 1 |
| | | KLM-598 | | 1 |
| 10413810 | S1/4JYTP 10M | | | 2 |
| 10416000 | 1/6JTP 0Ω | KLM-596 | | 1 |
| 10416210 | 1/6JTP 10Ω | | | 1 |
| 10416215 | 1/6JTP 15Ω | | | 1 |
| 10416247 | 1/6JTP 47Ω | | | 3 |
| 10416310 | 1/6JTP 100Ω | | | 3 |
| 10416315 | 1/6JTP 150Ω | | | 2 |
| 10416322 | 1/6JTP 220Ω | | | 3 |
| 10416336 | 1/6JTP 360Ω | | | 1 |
| 10416347 | 1/6JTP 470Ω | | | 1 |
| 10416410 | 1/6JTP 1.0K | | | 7 |
| 10416422 | 1/6JTP 2.2K | | | 2 |
| 10416433 | 1/6JTP 3.3K | | | 1 |
| 10416439 | 1/6JTP 3.9K | | | 1 |
| 10416447 | 1/6JTP 4.7K | | | 2 |
| 10416468 | 1/6JTP 6.8K | KLM-596 | | 3 |
| 10416482 | 1/6JTP 8.2K | | | 1 |
| 10416510 | 1/6JTP 10K | | | 16 |
| 10416512 | 1/6JTP 12K | | | 1 |
| 10416515 | 1/6JTP 15K | | | 1 |
| 10416516 | 1/6JTP 16K | | | 1 |
| 10416522 | 1/6JTP 22K | | | 1 |
| 10416533 | 1/6JTP 33K | | | 2 |
| 10416547 | 1/6JTP 47K | | | 1 |
| 10416556 | 1/6JTP 56K | | | 1 |
| 10416562 | 1/6JTP 62K | | | 2 |
| 10416568 | 1/6JTP 68K | | | 3 |
| 10416582 | 1/6JTP 82K | | | 2 |
| 10416591 | 1/6JTP 91K | | | 1 |
| 10416610 | 1/6JTP 100K | | | 8 |
| 10416620 | 1/6JTP 200K | | | 1 |
| 10416633 | 1/6JTP 330K | | | 1 |
| 10416647 | 1/6JTP 470K | | | 1 |
| 10416710 | 1/6JTP 1.0M | | | 1 |
| | **METAL FILM RESISTORs** | | | |
| 12512261 | 1/6TP 26.1Ω SN14K2CT26F | | | 1 |
| 12514100 | 1/6TP 1.00K SN14K2CT26F | | | 2 |
| 12514604 | 1/6TP 6.04K SN14K2CT26F | | | 1 |
| 12515100 | 1/6TP 10.0K SN14K2CT26F | KLM-599 | | 1 |

| PART CODE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| 12515118 | 1/6TP 11.8K SN14K2CT26F | KLM-596 | | 1 |
| 12515147 | 1/6TP 14.7K SN14K2CT26F | KLM-599 | | 1 |
| 12515249 | 1/6TP 24.9K SN14K2CT26F | KLM-596 | | 1 |
| 12515499 | 1/6TP 49.9K SN14K2CT26F | | | 1 |
| 12515511 | 1/6TP 51.1K SN14K2CT26F | | | 1 |
| 12515845 | 1/6TP 84.5K SN14K2CT26F | KLM-596 | | 1 |
| 12516100 | 1/6TP 100K SN14K2CT26F | | | 5 |
| 12516200 | 1/6TP 200K SN14K2CT26F | | | 1 |
| | **BLOCK RESISTORs** | | | |
| 13504533 | RKC1/8B4J 33K | KLM-596 | BR5, BR7 | 2 |
| 13506510 | RKC1/8B6J 10K | | BR1 | 1 |
| 13508410 | RKC1/8B8J 1K | | BR4 | 1 |
| 13508510 | RKC1/8B8J 10K | | BR2, BR3 | 2 |
| 13810525 | RKM10K253F 25K | | BR9 | 1 |
| 13890470 | RM 0470 | | BR6, BR8 | 2 |
| | **THERMISTOR** | | | |
| 18032310 | TD5-A110DA | | | 1 |
| | **MYLAR CAPACITORs** | | | |
| 20402410 | 50V 0.001UF K AMZV | KLM-596 | | 5 |
| | | KLM-599 | | 2 |
| 20402412 | 50V 0.0012UF K AMZV | KLM-598 | | 4 |
| 20402415 | 50V 0.0015UF K AMZV | KLM-596 | | 2 |
| 20402422 | 50V 0.0022UF K AMZV | KLM-598 | | 3 |
| 20402447 | 50V 0.0047UF K AMZV | KLM-596 | | 1 |
| 20402510 | 50V 0.01UF K AMZV | | | 1 |
| | | KLM-598 | | 4 |
| 20402547 | 50V 0.047UF K AMZV | KLM-596 | | 16 |
| | **STYROL CAPACITOR** | | | |
| 20503410 | 50V JT 1000PF | KLM-598 | | 1 |

| PART CODE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| | **CERAMIC CAPACITORs** | | | |
| 21442220 | 50V 22PF RTHE40TKSL220J | KLM-596 | | 2 |
| 21443100 | 50V 100PF RTHE50TKSL101J | | | 2 |
| 21443680 | 50V 680PF RTHE40TKYB681K | KLM-598 | | 4 |
| 21443820 | 50V 820PF RTHE40TKYB821K | KLM-596 | | 1 |
| 21446100 | 250V 0.1UF | | | 37 |
| | RTDSFC80TKY5U104M | KLM-598 | | 4 |
| | **TANTALUM CAPACITOR** | | | |
| 22005247 | 10V 47UFM | KLM-596 | | 1 |
| | **ELECTROLYTIC CAPACITORs** | | | |
| 25401310 | 6.3V 100UF RE.T2 | | | 6 |
| | | KLM-598 | | 1 |
| 25401322 | 6.3V 220UF RE.T2 | KLM-596 | | 1 |
| 25403210 | 16V 10UF RE.T2 | KLM-596 | | 11 |
| | | KLM-598 | | 4 |
| | | KLM-599 | | 1 |
| 25403247 | 16V 47UF RE.T2 | KLM-598 | | 2 |
| 25403310 | 16V 100UF RE.T2 | KLM-596 | | 4 |
| | | KLM-598 | | 6 |
| 25406047 | 50V 0.47UF RE.T2 | KLM-596 | | 2 |
| | | KLM-598 | | 3 |
| 25406110 | 50V 1UF RE.T2 | KLM-596 | | 11 |
| | | KLM-598 | | 4 |
| 35406122 | 50V 2.2UF RE.T2 | | | 2 |
| 25406133 | 50V 3.3UF RE.T2 | | | 2 |
| 25423247 | 16V 47UF RB-LL.T2 | KLM-596 | | 1 |
| 25426110 | 50V 1UF RB-LL.T2 | | | 1 |
| 25463210 | 16V 10UF RBP.T2 | | | 2 |
| 25466047 | 50V 0.47UF RBP.T2 | | | 1 |
| 25466110 | 50V 1UF RBP.T2 | KLM-598 | | 1 |
| | **TRANSISTORs** | | | |
| 30100328 | TR 2SB744 A P/Q | KLM-596 | Q3 | 1 |
| 30100700 | TR2SB731 | | Q1 | 1 |
| 30201107 | TR 2SC1583 G | | Q15, Q16 | 2 |
| 30202299 | TR 2SC2785 K Selected for noise (white) | | Q5 | 1 |

| PART CODE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| 30300528 | TR 2SD794A P/Q | | Q18 | 1 |
| 30400020 | TR 2SA1175 K TN | | | 3 |
| | | KLM-598 | | 4 |
| 30420020 | TR 2SC2785 K TN | KLM-596 | | 2 |
| | | KLM-598 | | 3 |
| 30420030 | TR 2SC2901 K TN | | | 1 |
| **DIGITAL TRANSISTORs** | | | | |
| 30430010 | TR DTA-114N T-93 | KLM-596 | DTA1 | 1 |
| | | KLM-598 | DTA1, DTA2 | 2 |
| 30430020 | TR DTC-114N T-93 | KLM-596 | DTC1 ~ 5 | 5 |
| **FET** | | | | |
| 30460020 | FET 2SK381-34-B | KLM-598 | F1, F2 | 2 |
| **DIODEs** | | | | |
| 31000800 | 1S2473 | KLM-601 | | 1 |
| 31001100 | 1SS-53 | KLM-596 | D1 | 1 |
| 31001500 | SR1K-2 | | D2 | 1 |
| 31400100 | 1S1555 TP-3 | KLM-596 | | 1 |
| | | KLM-598 | | 7 |
| 31400300 | 1S-2473 T-77 | KLM-596 | | 13 |
| | | KLM-597 | | 18 |
| **VARACTOR** | | | | |
| 31020400 | 1SV-149 B | | | 1 |
| **LED** | | | | |
| 31201500 | LT-8001P | | DB2 ~ 9 | 16 |
| 31203200 | LED LN524RA | KLM-597 | | 3 |
| **ZENER DIODEs** | | | | |
| 31422300 | HZ-6B1L-TD | KLM-596 | D7 | 1 |
| 31422400 | HZ-3ALL-TD | | D3 | 1 |
| 31422500 | HZ-5CLL-TD | | D1 | 1 |
| 31422700 | HZ-11A3-TD | | D4 | 1 |

| PART COCE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| **DOUBLE DIODE** | | | | |
| 31430100 | MC-931 TP | KLM-596 | DB10 ~ 13 | 4 |
| **ICs** | | | | |
| 32002021 | MN-3209 | KLM-598 | BBD | 1 |
| 32002022 | MN-3102 | | BBD driver | 1 |
| 32003011 | TC-40H000 P | KLM-596 | Quand 2-input nand gate | 2 |
| 32003021 | TC-40H074 P | | Dual D-type positive edge-triggered flip flop with set, reset | 2 |
| 32003026 | TC-40H138 P | | 3 to 8 demultiplexer | 2 |
| 32003030 | TC-40H151 P | | 8 to 1 data selector/multiplexer with strobe | 1 |
| 32003041 | TC-40H174 P | | Hex D-type flip flop with reset | 2 |
| 32003043 | TC-40H032 P | | Quad 2-input positive or gate | 1 |
| 32003047 | TC-40H240 P | | Octal buffer/line driver with 3-state output | 1 |
| 32003058 | TC-40H373 P | | Octal D-type transparent latch with 3-state output | 1 |
| 32003063 | TC-40H393 P | | Dual 4-bit binary counter | 1 |
| 32004016 | HD-14050 BP | KLM-596 | Hex buffer | 1 |
| 32004017 | HD-14051 BP | | 8-Channel analog multiplexer/ demultiplexer | 2 |
| 32004028 | HM-6116LP-4 | | 2048-Word x 8 bit static CMOS RAM | 1 |
| 32004039 | HD-14053 BP | | Triple 2-channel analog multiplexer/ demultiplexer | 1 |
| 32004063 | HD 63B50P | | CMOS asynchronous communica-tions interface adaptor | 1 |
| 32006009 | MSM-5232RS | | 8-Channel tone generator | 1 |
| 32006010 | MSM-80C85ARS | | CPU | 1 |
| 32006011 | MSM-81C55RS | | 2048 bit CMOS static RAM with I/O ports and timer | 1 |
| 32007003 | BA-618 | | LED driver | 1 |
| 32009001 | NJM-4558D-V | KLM-598 | OP amp | 1 |
| 32009007 | NJM-2902 N | KLM-596 | | 4 |
| 32009015 | NJM-2903 D | | | 1 |
| | | KLM-598 | | 1 |
| 32009027 | NJM-20690 | | 3-VCA and 1-VCF | 1 |
| 32009028 | NJM-3404AD | KLM-596 | | 3 |
| 32009029 | NJM-2058 D | KLM-599 | | 1 |
| 32011020 | M5224 P | KLM-598 | | 2 |
| 32011024 | M-5223 | KLM-596 | | 2 |
| 32011025 | M-54513 | | | 1 |

| PART CODE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| 32011026 | M-5216 L | KLM-598 | Head phone amp | 1 |
| 32012005 | MBM-2764-30Z | | 8K byte prom | 1 |
| 32013001 | PST-518 | KLM-596 | System reset | 1 |
| 32021011 | TL-072 | | Dual BI FET OP amp | 1 |
| 32021022 | TL-062 | | Dual BI FET OP amp | 2 |
| 32025002 | NE-571 | KLM-598 | | 1 |
| | **PHOTO COUPLER** | | | |
| 33000900 | PC-900 | KLM-596 | | 1 |
| | **CERAMIC OSCILLATOR** | | | |
| 33500900 | EF0-A6ROMO1 | | | 1 |
| | **P.C. BOARDs (without parts)** | | | |
| 34059600 | KLM-596 | | MAIN BOARD | 1 |
| 34059700 | KLM-597 | | PANEL BOARD | 1 |
| 34059800 | KLM-599 | | JOYSTICK BOARD | 1 |
| 34060000 | KLM-600 | KLM-597 | VR BOARD | 3 |
| 34060100 | KLM-601 | | SUB BOARD | 1 |
| | **SEMI-FIXED RESISTORs** | | | |
| 35201215 | H1051A 1.5KB | KLM-596 | VR1, +5V ADJ | 1 |
| 35201310 | H1051A 10KB | | VR5, RESONANCE ADJ | 1 |
| 35201322 | H1051A 22KB | | VR4, D/A ADJ | 1 |
| 35201410 | H1051A 100KB | | | 1 |
| | | KLM-601 | VR2, PITCH BEND ADJ (UP) | 1 |
| 35201468 | H1051A 680KB | | VR1, PITCH BEND ADJ (DOWN) | 1 |
| 35201510 | H1051A 1MB | KLM-596 | VR3, NOISE GAIN ADJ | 1 |
| 35201515 | H1051A 1.5MB | KLM-601 | | 1 |
| | **ROTARY VRs** | | | |
| 36016900 | K16200009 10KB | | JOYSTICK VR | 2 |
| 36204300 | K162B-5M1612-10KB | KLM-597 | VR with POWER SW | 1 |
| | **SLIDE VRs** | | | |
| 36504000 | S3018P-613-10KB | | BEND INT, TUNE | 2 |
| 36504100 | S3018P-613-100KC | | SEQUENSER SPEED | 1 |
| | **SLIDE SW** | | | |
| 37303900 | R-S47836 | KLM-596 | TAPE, WRITE E/D | 4 |

| PART CODE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| | **PUSH SW** | | | |
| 37505700 | EVQQJBO4K | KLM-597 | PANEL SWITCH | 18 |
| | **COILs** | | | |
| 40201200 | KD-4 | KLM-596 | DC-DC CONVERTER | 1 |
| 40201300 | ELEY-471KA | | DC-DC CONVERTER | 1 |
| 40201400 | KL-003 | | OSC | 1 |
| | **AC ADAPTERs** | | | |
| 40502700 | KAC-302 UNI/117V | | UNI | 1 |
| | | | 117 2P | 1 |
| 40502800 | KAC-303 JAM/CSA | | JAM | 1 |
| 40503000 | KAC-305 240AU | | 240 AU | 1 |
| 40503100 | KAC-306 240GE | | 240 GE | 1 |
| 40503200 | KAC-307 240AF | | 240 AF | 1 |
| 40503300 | KAC-308 220GE/ | | 220GE | 1 |
| | SCHANDINAVIA | | 220 SE | 1 |
| | | | DEMKO | 1 |
| | | | SEMKO | 1 |
| | | | NEMKO | 1 |
| | | | 220 FR | 1 |
| | | | FEMKO | 1 |
| | **KEY BOARDs** | | | |
| 42002500 | ESK-7111 | | NORMAL | 1 |
| 42002600 | ESK-7112 | | REVERSE | 1 |
| | C | | | 4 (4) |
| | D | | | 4 (4) |
| | E | | | 4 (4) |
| | F | | | 4 (4) |
| | G | | | 4 (4) |
| | A | | | 4 (4) |
| | B | | | 4 (4) |
| | H.C. | | | 1 (1) |
| | BLACK KEY | | | 20 (20) |
| | | | ( ): REVERSE | |
| | CONTACT STRIPS | | 6 groups | 7 |
| | SPRING | | 7 groups | 49 |

| PART CODE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| **PHONE JACKs** | | | | |
| 45001400 | SG-4611 #01 | KLM-596 | 3P with SWITCH | 3 |
| 45001700 | SG-4612 #01 | KLM-596 | STEREO | 1 |
| **DC INPUT JACK** | | | | |
| 45400300 | HEC-0470-01-230 | | POWER JACK | 1 |
| **MINI-PHONE JACK** | | | | |
| 45400900 | HSJ-0786-01-010 3.5φ | | TAPE I/O | 2 |
| **HARNESSes** | | | | |
| 47040100 | HNS-301 | | | 1 |
| 47040200 | HNS-302 | | | 1 |
| 47040300 | HNS-303 | | | 1 |
| 47040400 | HNS-304 | | | 1 |
| 47040600 | HNS-306 | | | 1 |
| 47040700 | HNS-307 | | | 1 |
| 47040800 | HNS-308 | | | 1 |
| 47040900 | HNS-309 | | | 1 |
| **CONNECTORs** | | | | |
| 47408004 | S4P W-P2604 #51 | KLM-596 | | 2 |
| 47408805 | S5P W-P2605 #51 | | | 1 |
| 47408807 | S7P W-P2607 #51 | KLM-597 | | 1 |
| | | KLM-598 | | 1 |
| 47408811 | S11P W-P2611 #51 | KLM-596 | | 1 |
| 47408814 | S14P W-P2614 #51 | | | 1 |
| 47408815 | S15P W-P2615 #51 | | | 2 |
| | | KLM-598 | | 1 |
| 47408904 | L4P W-P2804 #51 | KLM-597 | | 2 |
| | | KLM-599 | | 1 |
| 47408905 | L5P W-P2805 #51 | | | 1 |
| 47408911 | L11P W-P2811 #51 | KLM-597 | | 1 |
| 47408914 | L14P W-P2814 #51 | | | 1 |
| **IC SOCKETs** | | | | |
| 48001282 | 28P DICA-28CTI | KLM-596 | | 1 |
| 48005222 | 22P C472211 | | | 1 |

| PART CODE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| **DIN JACK** | | | | |
| 45403100 | DINJACK 5PIN TCS-5350-01-1011 | | MIDI I/O | 2 |
| **RUBBER FEET** | | | | |
| 50008700 | KOC-F40272 | | | 2 |
| **CUSHION FOR BATTERY** | | | | |
| 50008800 | 16x30x4 KOC-F40280 | | | 1 |
| **PUSH SW CUSHION A** | | | | |
| 50008900 | KOC-F40282 | | | 1 |
| **PUSH SW CUSHION B** | | | | |
| 50009000 | KOC-F40283 | | | 3 |
| **BATTERY** | | | | |
| 52001100 | SUM2DGB | | | 6 |
| **RIBBON** | | | | |
| 54008100 | KOC-F40224 | | | 1 |
| **HARNESS STOPPER** | | | | |
| 54009400 | WS-1NA | | | 2 |
| **SHIELDING SHEET** | | | | |
| 58018004 | KOC-F40275 | | | 1 |
| **CONNECTION CORD** | | | | |
| 60201300 | 6.3φ PLUG 2.5M | | | 1 |
| **SLIDE VR KNOB (IVORY)** | | | | |
| 62011600 | KOC-E40121 | | | 3 |

| PART CODE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| | **JOYSTICK LEVER KNOB** | | | |
| 62012200 | KOC-E40149 | | | 1 |
| | **ROTARY VR KNOB** | | | |
| 62012300 | KOC-E40151 | | VR with POWER SW KNOB | 1 |
| | **PUSH SW KNOBs** | | | |
| 62012400 | B-1 (TURQUOISE) KOC-E40153 | | L = 13mm | 8 |
| 62012401 | B-2 (IVORY) KOC-E40153 | | L = 13mm | 1 |
| 62012402 | B-3 (RED) KOC-E40153 | | L = 13mm | 1 |
| 62012500 | A-1 (IVORY) KOC-E40152 | | L = 25.5mm | 6 |
| 62012501 | A-2 (TORQUOISE) KOC-E40152 | | L = 25.5mm | 2 |
| | **BATTERY TERMINALs (SPRING)** | | | |
| 64058100 | KOC-C40438 | | | 1 |
| 64058101 | KOC-C40437 | | | 1 |
| | **JOYSTICK Y SUPPORT** | | | |
| 64058400 | KOC-C40446 | | | 1 |
| | **JOYSTICK PLATE** | | | |
| 64062600 | KOC-C40500 | | | 1 |
| | **SHIELDING SHEET FOR KLM-598** | | | |
| 64062800 | KOC-C40509 | | | 1 |
| | **SHIELDING SHEET FOR JOYSTICK** | | | |
| 64062900 | KOC-C40510 | | | 1 |
| | **SHIELDING SHEET FOR PANEL** | | | |
| 64063000 | KOC-C30211 | | | 1 |

| PART CODE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| | **STRAP PEG** | | | |
| 64402200 | KOC-C40505 | | | 2 |
| | **JOYSTICK BOX** | | | |
| 64610100 | KOC-E30036 | | | 1 |
| | **JOYSTICK X SUPPORT** | | | |
| 64610101 | KOC-E40114 | | | 1 |
| | **UPPER CASE** | | | |
| 64615300 | KOC-E10014 | | | 1 |
| | **LOWER CASE** | | | |
| 64615400 | KOC-E10013 | | | 1 |
| | **BATTERY COVER** | | | |
| 64615500 | KOC-E30056 | | | 1 |
| | **BATTERY HOLDER** | | | |
| 64615600 | KOC-E30057 | | | 1 |
| | **LEVER FOR JOYSTICK** | | | |
| 64616100 | KOC-E40150 | | | 1 |
| | **PARAMETER INDEX PANEL** | | | |
| 64905100 | KOC-E30058 | | | 1 |
| | **DISPLAY COVER** | | | |
| 64905200 | KOC-E30060 | | | 1 |
| | **LUG** | | | |
| 67200100 | 3$\phi$ | | | 1 |

| PART CODE | SPECIFICATIONS | P.C. BOARD | IDENTIFICATION NO. FUNCTION | Q'TY |
|---|---|---|---|---|
| | | SERIAL NO. SEAL | | |
| 68599999 | | | | 1 |
| | | SCREWS, NUTS, WASHERS (Please refer to structural diagram) | | |
| 70560508 | FE B BZMC 5x8 | | | 4 |
| 74530308 | PLAX B ZMC 3x8 | | | 46 |
| 74560408 | PLAX B BZMC 4x8 | | | 3 |
| 74560412 | PLAX B BZMC 4x12 | | | 9 |
| 78430300 | TWU ZMC 3 | | | 1 |
| 78690500 | PSW 5 | | | 1 |

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