Service Manual

CP-3

Digital
Surround
Processor

lexicon

Safety Suggestions

Read Instructions Read all safety and operating instructions before operating the unit.

Retain Instructions Keep the safety and operating instructions for future reference.

Heed Warnings Adhere to all warnings on the unit and in the operating instructions.

Follow Instructions Follow operating and use instructions.

Heat Keep the unit away from heat sources such as radiators, heat registers, stoves, etc., including amplifiers which produce heat.

Ventilation Make sure that the location or position of the unit does not interfere with its proper ventilation. For example, the unit should not be situated on a bed, sofa, rug, or similar surface that may block the ventilation openings; or, placed in a cabinet which impedes the flow of air through the ventilation openings.

Wall or Ceiling Mounting Do not mount the unit to a wall or ceiling except as recommended by the manufacturer.

Power Sources Connect the unit only to a power supply of the type described in the operating instructions, or as marked on the unit.

Grounding or Polarization* Take precautions not to defeat the grounding or polarization of the unit's power cord.

*Not applicable in Canada.

Power Cord Protection Route power supply cords so that they are not likely to be walked on or pinched by items placed on or against them, paying particular attention to cords at plugs, convenience receptacles, and the point at which they exit from the unit.

Nonuse Periods Unplug the power cord of the unit from the outlet when the unit is to be left unused for a long period of time.

Water and Moisture Do not use the unit near water — for example, near a sink, in a wet basement, near a swimming pool, near an open window, etc.

Object and liquid entry Do not allow objects to fall or liquids to be spilled into the enclosure through openings.

Cleaning The unit should be cleaned only as recommended by the manufacturer.

Servicing Do not attempt any service beyond that described in the operating instructions. Refer all other service needs to qualified service personnel.

Damage requiring service The unit should be serviced by qualified service personnel when:

the power supply cord or the plug has been damaged,

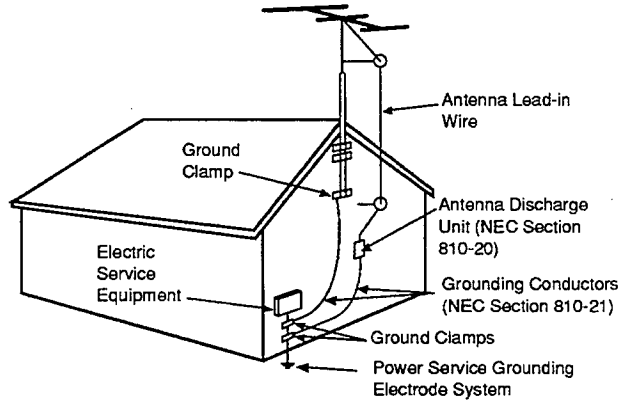
objects have fallen, or liquid has been spilled into the unit,

the unit has been exposed to rain,

the unit does not appear to operate normally or exhibits a marked change in performance,

the unit has been dropped, or the enclosure damaged.

Outdoor Antenna Grounding If an outside antenna is connected to the receiver, be sure the antenna system is grounded so as to provide some protection against voltage surges and built-up static charges. Section 810 of the National Electrical Code, ANSI/NFPA No. 70-1984, provides information with respect to proper grounding of the mast and supporting structure, grounding of the lead-in wire to an antenna-discharge unit, size of grounding conductors, location of antenna-discharge unit, connection to grounding electrodes, and requirements for the grounding electrode. See figure below.



NEC — National Electrical Code

Power Lines An outside antenna should be located away from power lines.

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service and repair of this instrument. Failure to comply with these precautions, or with specific warnings elsewhere in these instructions violates safety standards of design manufacture and intended use of the instrument. Lexicon assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT

To minimize shock hazard the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor AC power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing and adjusting.

SAFETY SYMBOLS

General definitions of safety symbols used on equipment or in manuals.

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage. (Terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)

WARNING — The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION — The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like which is essential to highlight.

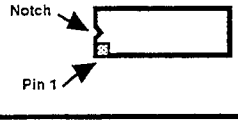
CAUTION

Electrostatic Discharge (ESD) Precautions

The following practices minimize possible damage to ICs resulting from electrostatic discharge or improper insertion.

- Keep parts in original containers until ready for use.
- Avoid having plastic, vinyl or styrofoam in the work area.
- Wear an anti-static wrist-strap.
- Discharge personal static before handling devices.
- Remove and insert boards with care.
- When removing boards, handle only by non-conductive surfaces and never touch open-edge connectors except at a static-free workstation.*
- Minimize handling of ICs.
- Handle each IC by its body.
- Do not slide ICs or boards over any surface.
- Insert ICs with the proper orientation, and watch for bent pins on ICs.
- Use anti-static containers for handling and transport.

*To make a plastic-laminated workbench anti-static, wash with a solution of Lux liquid detergent, and allow to dry without rinsing.



CAUTION

ICs inserted backwards will be destroyed. Incorrect insertion of ICs is also likely to cause damage to the board.

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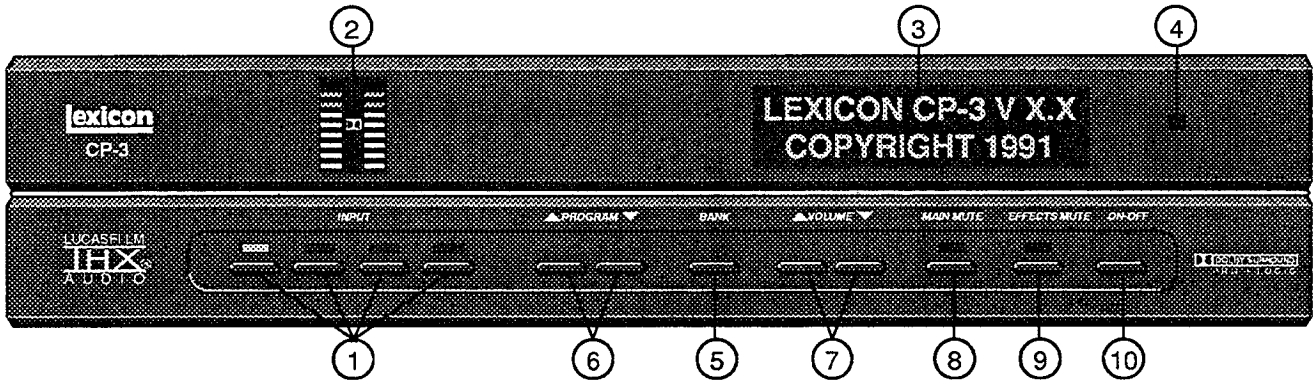
1

Controls and Connectors

The Front Panel



1. Input
The four INPUT buttons are used to select which input is processed by the CP-3. Pressing any one of these buttons will select that input and light the LED above it. The CP-3 can be programmed to engage a specific operating mode for each input, so changing inputs may change the mode being used.

2. Input Level Display
The INPUT LEVEL display monitors the level in the CP-3's digital encoding circuits and is used to indicate the correct Dolby level for video sound sources (marked by the double-D symbol between the LEDs.) When correctly set, the loudest passages will light the entire row of green LEDs, the two yellow ones, and occasionally flash the red peak LEDs at the top. (The input level meters can be turned off to eliminate distraction — See Owner's Manual.)

3. Alphanumeric Display
The alphanumeric LCD (liquid crystal display) shows both the mode that is running and its modifiable parameters. The contrast of the LCD can be adjusted for optimum visibility. See Owner's Manual.)

4. Infrared Receiver
The small unlabeled window to the right of the LCD houses the infrared receiver used by the CP-3 to detect signals from the remote controls.

5. Bank
In Expanded operation, the BANK button cycles through the Preset bank and two User banks (A&B) where customized modes can be stored. The mode number doesn't change: if you are using Preset 9, pressing BANK once switches to User A9, pressing it again switches to User B9, pressing it again switches back to Preset 9. In Standard operation, the BANK button is inoperative.

6. Program
The PROGRAM button steps through the modes of the bank currently in use. Using its Expanded modes, the CP-3 can have as many as 45 operating modes: Presets 1-15 are configured at the factory, those labeled User A1-15 and User B1-15 are available for storage of modes customized by the user.

In Standard operation, 5 modes are available.

7. Volume
The VOLUME buttons adjust the level of all channels simultaneously. These buttons assume the function of the volume control on your preamp or receiver.

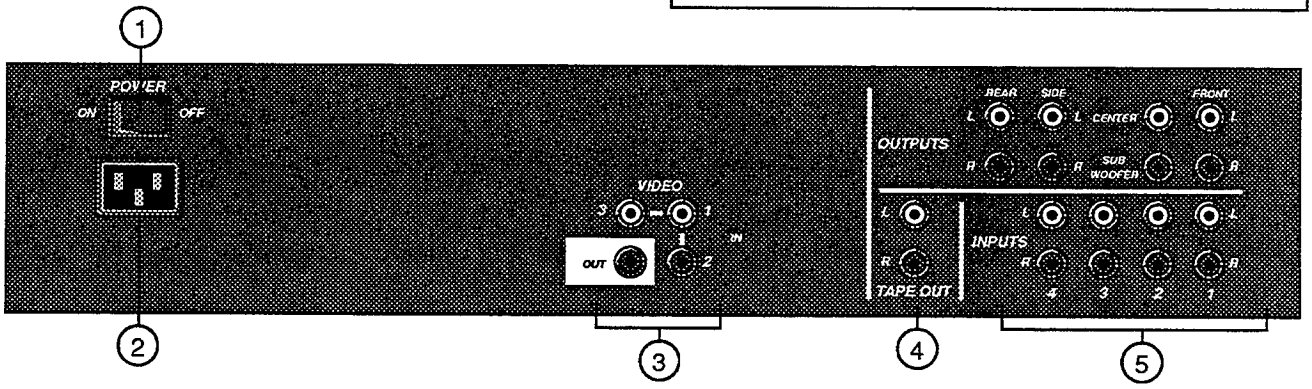
8. Main Mute
MAIN MUTE turns off all outputs and lights both MAIN and EFFECTS MUTE LEDs.

9. Effects Mute
EFFECTS MUTE turns off all signals added by the CP-3, lights the yellow EFFECTS MUTE LED on the front panel, and displays "EFFECTS MUTED." This bypasses all signal processing in the CP-3 except level control, and is the simplest way to play "normal" two-speaker stereo. Pressing again will restore normal operation.

10. On/Off
ON/OFF alternately puts the CP-3 into and out of standby mode. Although this switch may be used to turn the CP-3 off, it is important that the CP-3 be turned on with the remote control that will be used during each session. If the front panel switch is used to turn on the CP-3, it will resume operation in whichever mode (Standard or Expanded) it was last in.

The Rear Panel

CAUTION: Never make or break any connections to the CP-3 with the rear-panel power ON. Make sure any associated amplifiers have been turned off for at least one minute before turning this master power switch on or off.



1. Power On/Off
The master power switch should be left ON when the unit is in regular use. When the CP-3 will not be used for an extended period of time, or whenever you are connecting or disconnecting any cables to the unit, this switch should be turned OFF.

2. Power Connector
Connect the supplied AC power cord here, then plug the cord into an unswitched outlet. Be sure that the power cord is firmly seated in this connector.

3. Video In and Video Out
The three video inputs are switched with their corresponding audio inputs and fed to VIDEO OUT. VIDEO OUT should be connected to a video input on your monitor for the On Screen display to work. The CP-3 will generate a blue background field if there is no video signal in the selected input. If the CP-3 is turned off via the front panel or either remote, the last input selected will continue to be passed to the video output. If the rear-panel master power switch is turned off, or if AC power is removed from the unit, the video output will default to Input 1.

4. Tape Out
This provides an unprocessed, buffered audio output of whatever input has been selected. This output will be active if the CP-3 is turned off via remote, or front panel, but is shut off when the rear-panel master power switch is turned off.

5. Audio Inputs and Outputs
There are four stereo audio inputs on the CP-3. Input 4 is audio only; it uses the video signal from Video Input 1.

Stereo outputs are provided for Front, Side, and Rear amplifiers, as well as single monaural outputs for the Center speaker amplifier and the Subwoofer amp.

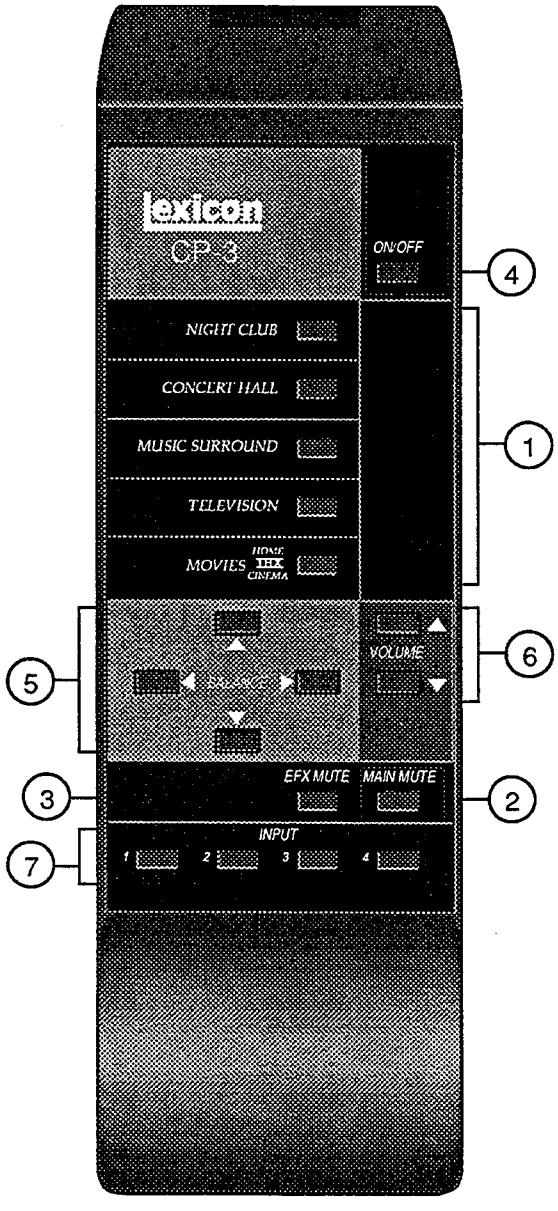
The Standard Remote

1. The Operating Modes
The five operating mode buttons on the Standard Remote can be customized to load any of 45 operating modes.

2. Main Mute
Turns off all outputs, lights both MAIN and EFX MUTE LEDs and displays "SYSTEM MUTED." Pressing again will restore normal operation. (Because it is possible to alter the setting of the volume while Main Mute is on, check the volume before you turn the mute off again.)

3. EFX Mute (Effects Mute)
Turns off all signals added by the CP-3, lights the yellow EFFECTS MUTE LED on the front panel, and displays "EFFECTS MUTED." This bypasses all signal processing in the CP-3 except level control, and is the simplest way to play "normal" two-speaker stereo. Pressing again will restore normal operation.

Pressing EFX MUTE after the MAIN MUTE (which mutes the main and effect outputs) has been engaged will turn the effect mute off while leaving the main speakers muted. This allows you to hear the effect the CP-3 is adding without the main channels on. Operation depends on the mode in use.



4. On/Off
Puts the CP-3 into standby.

The CP-3 uses this button's signal to differentiate between the remotes. Therefore it is important that the CP-3 be turned on with the remote control that will be used during each session.

5. Balance
These four buttons adjust the level of the sound relative to the other channels. For instance, pressing the left arrow will turn down the level of all the right channels. The effect of the Front/Back control on the side channels will depend on speaker configuration and operating mode.

6. Volume
These buttons simultaneously adjust the level of all channels.

The first push of either of these buttons displays the current value for 2 seconds; another push during that time increases or decreases the displayed value. Holding the button down for 1 second changes values rapidly.

7. Input
Buttons 1-4 select the input source and can be programmed to automatically engage the desired operating mode.

The Expanded Remote

1. The Modes
The CP-3 can operate in one of four modes (PANORAMA, AMBIENCE, REVERB, or SURROUND). Each of these modes has a set of preset variations as listed on the Expanded remote (1-15). As many as 30 customized versions of these presets can be stored in User Registers.

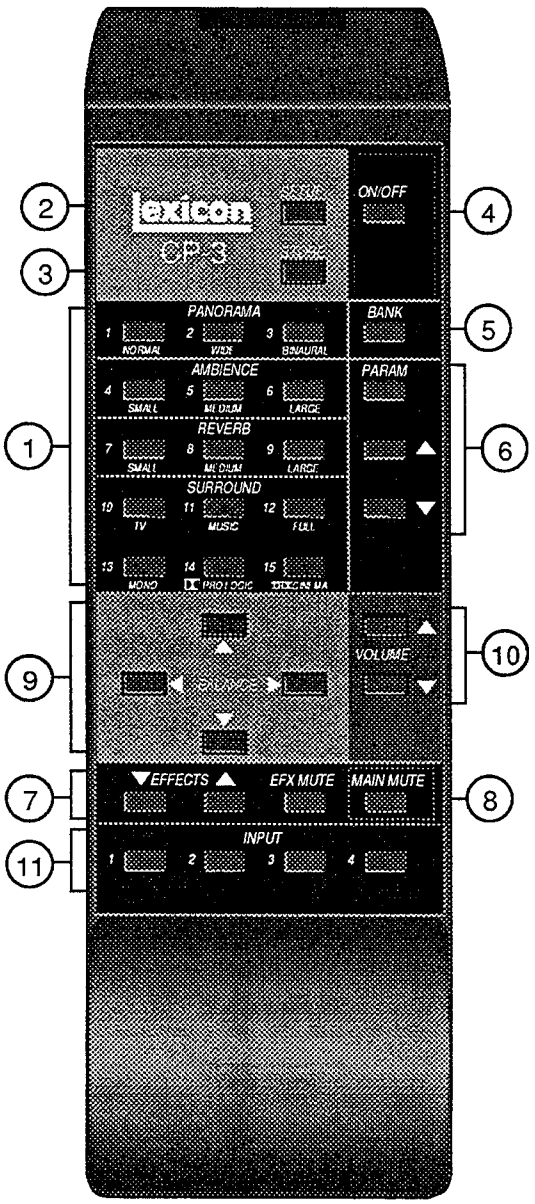
2. Setup
Allows selection and adjustment of all the interface functions of the CP-3 including Input and Output levels, visual displays, speaker configurations, etc.

3. Store
Saves in memory the settings from the SETUP mode and is used to memorize and store any customized operating modes.

4. On/Off
Puts the CP-3 into standby.

The CP-3 uses this button's signal to differentiate between the remotes. Therefore it is important that the CP-3 be turned on with the remote control that will be used during each session.

5. Bank
Switches between 3 register banks: the Presets and 2 User register Banks (A & B) where customized modes may be stored. The mode number doesn't change: if you are using Preset 9, pressing BANK once switches to User A9, pressing BANK again switches to USER B9, and pressing BANK once more selects Preset 9.



6. Parameter
The three parameter buttons allow selection and adjustment of variable parameters within each mode. Pushing PARAM displays the parameter menu with a moveable cursor for 5 seconds; pushing it again before the display changes moves the cursor to the next parameter.

Pressing PARAM ▲ or ▼ will display and adjust the current parameter (whether or not PARAM has been pushed.) A single push of either of these buttons displays the parameter; another push changes the parameter by one unit. Holding PARAM ▲ or ▼ for more than 1 second causes the values to change rapidly.

7. Effects*
▲ and ▼ adjust the level of all signals added by the CP-3.

8. Mutes
MAIN MUTE turns off all outputs and lights both MAIN and EFX MUTE LEDs. Pushing EFX MUTE while in system-mute mode turns the effects alone back on. EFX MUTE alternately turns off and on all signals added by the CP-3. Use it to compare the sound with and without CP-3 processing, or as a simple way to play normal two-speaker stereo.

9. Balance*
BALANCE: The four balance buttons adjust the levels of the rear speakers relative to the sides and fronts, and the left/right balance of all speakers: front, sides and rear. It should be used instead of the balance control on your preamp or receiver.

10. Volume*
▲ and ▼ simultaneously adjust the level of all channels. These should be used instead of the volume control on your preamp or receiver.

11. Input
INPUT buttons 1-4 select the input source and can be programmed to automatically engage the desired operating mode.

**The first push of either of these buttons displays the current value for 2 seconds; another push during that time increases or decreases the displayed value. Holding the button down for 1 second changes values rapidly.*

Periodic Maintenance

Under normal conditions the CP-3 requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners.

Avoid using abrasive materials such as steel wool or metal polish. If the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the CP-3 exterior.

Obtaining Factory Parts and Service

Ordering Parts

When ordering parts, identify each part by type, value and Lexicon Part Number. Replacement parts can be ordered from:

Lexicon Inc.
100 Beaver Street
Waltham MA 02154
Telephone: 617-736-0300
Fax: 617-891-0340

ATT: Customer Service

Returning units for service

Before returning a unit, consult with Lexicon to determine the extent of the problem. No equipment will be accepted without Return Authorization from Lexicon.

If you choose to return a CP-3 to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured, and consigned to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company name
- Street address
- City, State, Zip Code, Country
- Telephone number (including Area Code)
- Serial number of unit
- Preferred method of return shipment

Please include a brief note labeled with your Return Authorization number, describing conversations with Lexicon personnel and give the name and telephone number of the person directly responsible for maintaining the unit. Clearly label your package with your Return Authorization number.

Include both remotes. Do not include accessories such as manuals, cables, etc. with the unit unless these are specifically requested by Lexicon personnel.

2

Specifications

Specifications

Inputs: Audio: 4 stereo pairs
Minimum Input Level: 300 mVrms for maximum output
50 mVrms for Dolby level
Input Impedance: 100 kΩ in parallel with 100pf

Video: 3 composite, NTSC M standard
Input Sensitivity and Impedance: 1V p-p, 75Ω

Outputs: Audio: 8 outputs (Left, Right, Center, Subwoofer, 2 Side, 2 Rear)
Maximum Output Level: 6 Vrms
Output Impedance: 500 Ω

Video: 1 composite, NTSC M standard
Output Level and Impedance: 1V p-p, 75Ω

Frequency Response: Unprocessed channels: 10 Hz - 100 kHz, +1, -3dB, Ref. 1 kHz
Processed channels: 10 Hz - 18 kHz, +1, -3dB, Ref. 1 kHz

Subwoofer: 10 Hz-80 Hz, +1, -6dB, Ref. 31.5Hz, 24dB/octave rolloff

THD: All channels: Less than .025% @1 kHz, max level
Subwoofer: Less than .025% @10-100 Hz, max level

Signal to Noise Ratio: 90dB minimum, A-weighted, Ref. 1 kHz max level

Power Requirements: 120 VAC ±10% 50-60 Hz 35W
100/220/240 VAC versions available
3-pin IEC detachable power cord provided

Dimensions: 17.5"W x 14.5"D x 3.7"H (445 x 368 x 94mm)
Brackets supplied for rack mounting: conforms to 19" standard, 2U high
(3.5"H without feet)

Weight: 18 lbs. 4oz. (8.3kg)

Environment: Operating Temperature: 32° to 95°F (0° to 35°C)
Storage Temperature: -22° to 167°F (-30° to 75°)
Humidity: 95% maximum without condensation

Remote Controls: 2 hand-held, battery-powered remote control units provided with each CP-3; each uses 2 AA batteries (provided):
1 18-button "Standard" remote
1 36-button "Expanded" remote

Specifications subject to change without notice.

3

Performance Verification

Performance Verification

The information in this section can help you determine whether or not a unit is operating correctly. Always complete the performance verification before proceeding to the troubleshooting procedures.

Initial Inspection

Required Equipment:

Clean, antistatic, well lit work area

High Quality Music Source

Playback System:
Compact Disc player, stereo amplifier, 2 full-range stereo speakers, stereo headphones and the proper cables for hooking up the system.

Audio Patch Cables:
2 single-ended, shielded audio cables with RCA plugs on both ends for connecting the outputs of the compact disc player to the inputs of the CP-3.

2 single-ended, shielded audio cables with RCA plugs on one end and appropriate connectors on the other end for connection to the input of the stereo amplifier.

Low Distortion Oscillator :
Single-ended 600 ohm output, <.005% THD.

Cables:
Audio Input Y Cable: shielded audio Y cable with 2 RCA plugs on the Y end and an appropriate connector on other end for connection to the Low Distortion Oscillator output.

1. Check all front panel switches for smooth mechanical operation and verify that the display acknowledges its function.
2. Verify that all of the front panel LED's light.
3. Check all buttons on both the Expanded and the Standard infrared remote and verify that the display is responding to all commands. The Expanded remote will be used for all tests unless otherwise noted in the text.
4. Listen to the unit with an audio source to verify that the inputs and outputs are passing clean audio.

Setup

1. Connect the left and right outputs from the music source to the CP-3 left and right INPUT 1 jacks.
2. Connect the outputs from the oscillator to the CP-3 left and right INPUT 2 jacks.
3. Set the oscillator to output 220 Hz @ -10dBV (316 mv).
4. Connect the CP-3 left and right FRONT audio outputs to the amplifier left and right inputs.
5. Set the volume level on the amplifier to its lowest setting.
6. Power on the CP-3.
7. With the Expanded remote, select Preset 12 (Surround Full Range) and INPUT 1.
8. Increase the CP-3 system volume to maximum output (+12dB).

Listening

Input the music source to the CP-3. Slowly increase the volume level on the amplifier to a comfortable listening level and verify that the output is free from noise, distortion or any other audio irregularities.

MDAC Test

1. Input the oscillator to the CP-3 by selecting INPUT 2.
2. Lower the CP-3 system volume level and verify that the change in signal level is smooth (no zipper noise).
3. Increase the CP-3 system volume level to maximum output (+12dB).

Mute Test

1. Press the MAIN MUTE button and verify that the output signal disappears.
2. Press the MAIN MUTE button again and verify that the output signal returns.
3. Repeat the Listening, MDAC and Mute tests for the side, rear, center and sub woofer outputs and for the remaining inputs.

If any of the above tests fail, refer to the Troubleshooting section of this manual.

Audio Performance Verification

Performing these tests will insure that all audio signal paths in the CP-3 are functional and that the CP-3 meets its published specifications. When troubleshooting problems with the audio signal paths, these tests may be used in conjuction with the signal flow diagrams found in the Troubleshooting section of this manual to help locate the source of the problem.

Required Equipment

Clean, antistatic, well lit work area

Low Distortion Oscillator:
single-ended 600 ohm output, <.005% THD.

THD+N Distortion Analyzer

Level Meter:
with switchable 30kHz or audio bandpass filtering.

Audio Input Cable:
single-ended, shielded audio cable with RCA plug on one end and an appropriate connector on the other end for connection to the Low Distortion Oscillator output.

Audio Output Cable:
single-ended, shielded audio cable with RCA plug on one end and an appropriate connector on the other end for connection to the THD+N Distortion Analyzer.

#2 Phillips head screwdriver

#2 Posidriv screwdriver

Setup

1. Using the rear panel power switch, power off the CP-3.
2. Detach the trim panels or rack mounting brackets by removing three (3) Phillips screws from each side of the unit.
3. To remove the top cover, remove three (3) screws from each side, three (3) screws from the top, and one (1) screw from the rear of the unit. Please note that the smaller, 6-32 screws are Pozidriv, and should be removed with a Pozidriv screwdriver. A Phillips screwdriver may be used if a Pozidriv is not available.
4. Locate the digital board in the center compartment. Remove jumpers W1 and W2 which can be found between U24 and U34, the two 40-pin DIP ICs.
5. Using the rear panel power switch, power on the CP-3 and verify the following display sequence:

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   LEXICON 1991

   CP-3 Diagnostics

   If this message is not displayed, power off the unit with the rear panel power switch, check to make sure that the correct jumpers (W1 and W2) were removed from the digital board, and reapply power to the unit.
6. Press the front panel BANK button three times. The display should read:

   ROUTING TESTS

   If a different message is displayed, keep pressing BANK until this message is displayed.
7. Press the PROGRAM ▲ button and verify that the INPUT 1 LED lights.

Note: All level references will be stated in terms of dBV and equivalent RMS volts (Vrms). If the test equipment used to perform these procedures is referenced to dBu or dBm, add 2.2 dB to the stated dBV values to convert to dBu or dBm.

Input Test

This test verifies the functionality of the Audio Inputs and Tape Outputs by checking gain, frequency response, THD+N, and S/N Ratio.

Audio Connections

1. Attach the audio input cable between the Low Distortion Oscillator and the CP-3 Right channel Input 1 jack.
2. Attach the audio output cable between the CP-3 Right Tape Out jack and the input of the Distortion Analyzer.

Procedure

1. Apply a 1 kHz signal at +4 dBV (1.58 Vrms) to the input channel.
2. Set the scale on the Distortion Analyzer to measure +4 dBV (1.58 Vrms) signal level. Make sure any filters are off.
3. Verify that the output level from the CP-3 is +4 dBV (1.58 Vrms) +/-0.5 dB.
4. Use the output level from step 3 for the 0dB reference to check frequency response. Sweep the oscillator frequency from 10 Hz to 100 kHz. Verify that the signal level is within +1/-3dB of the reference level over the frequency band.
5. Set the oscillator frequency to 1 kHz. Adjust the scale on the Distortion Meter to measure 0.025% THD+N, and turn on the 30 kHz low pass or audio bandpass filter. Verify that THD is less than 0.025%.
6. Set the scale on the Distortion Meter to measure -80 dBV signal level. With the filter still on, either turn off the output from the oscillator or disconnect the oscillator from the CP-3 input. Verify that the noise floor is less than -80 dBV.
7. Repeat this test for the left channel by swapping the audio connections from the Right to the Left Input 1 jack and the Right to the Left Tape Out jack on the CP-3.
8. Repeat steps 1-7 for inputs 2, 3 and 4 by attaching the audio input cable from the oscillator to the appropriate R or L Input jack on the CP-3 and selecting the corresponding audio input with the front panel INPUT switches.

Direct Front Test

This test verifies the functionality of the Front Left and Right Direct (unprocessed) audio signal paths. The performance of the Input and Front L & R level control stages are checked through gain, frequency response, THD+N, and S/N Ratio tests.

Audio Connections

1. Attach the audio input cable between the Low Distortion Oscillator and the CP-3 Right channel Input 1 jack.
2. Attach the audio output cable between the CP-3 Right Front Output jack and the input of the Distortion Analyzer.
3. Verify that Input 1 is selected on the front panel.

Procedure

1. Select the Front Direct routing test by pressing the PROGRAM ▼ button on the front panel. The display should read:

   FDIR ENABLE
   ON

2. Apply a 1 kHz signal at +4 dBV (1.58 Vrms) to the input channel.
3. Set the scale on the Distortion Analyzer to measure +4 dBV (1.58 Vrms) signal level. Make sure any filters are off.
4. Verify that the output level from the CP-3 is +4 dBV (1.58 Vrms) +/-0.5 dB.
5. Use the output level from step 4 for the 0 dB reference to check frequency response. Sweep the oscillator frequency from 10 Hz to 100 kHz. Verify the signal level is within +1/-3dB of the reference level over the frequency band.
6. Set the oscillator frequency to 1 kHz. Adjust the scale on the Distortion Meter to measure 0.025% THD+N and turn on the 30 kHz low pass or audio bandpass filter. Verify that THD is less than 0.025%.
7. Set the scale on the Distortion Meter to measure -80 dBV signal level. With the filter still on, either turn off the output from the oscillator or disconnect the oscillator from the CP-3 input. Verify that the noise floor is less than -80 dBV (0.1 mVrms).
8. Repeat this test for the left channel by swapping the audio connections from the Right to the Left Input 1 jack and the Right to the Left Front Output jack on the CP-3.

Direct Front with High Pass Filter Test

This test verifies the functionality of the Front Left and Right Direct (unprocessed) audio signal paths. The performance of the Input and Front L & R level control stages, and 80 Hz high pass filters are checked through gain, frequency response, THD+N, and S/N Ratio tests.

Audio Connections

1. Attach the audio input cable between the Low Distortion Oscillator and the CP-3 Right channel Input 1 jack.
2. Attach the audio output cable between the CP-3 Right Front Output jack and the input of the Distortion Analyzer.
3. Verify that Input 1 is selected on the front panel.

Procedure

1. Select the Front Direct routing test by pressing the PROGRAM ▼ button on the front panel. The display should read:

   FDIR ENABLE

   ON

2. Turn the 80 Hz high pass filters on by pressing the EFFECTS MUTE button on the front panel. The display should read:

   HI-PASS ENABLE

   ON

3. Apply a 1 kHz signal at +4 dBV (1.58 Vrms) to the input channel.
4. Set the scale on the Distortion Analyzer to measure +4 dBV (1.58 Vrms) signal level. Make sure any filters are off.
5. Verify the output level from the CP-3 is +4 dBV (1.58 Vrms) +/-0.5 dB.
6. Use the output level from step 5 for the 0 dB reference to check frequency response. Sweep the oscillator frequency from 200 Hz to 100 kHz. Verify that the signal level is within +1/-3dB of the reference level over the frequency band. With the oscillator frequency set at 80 Hz, check that the signal level is between -2 and -4 dB of the referance level. A graph of the frequency response for the 80 Hz high pass filter may be found in the Theory of Operation section of this manual.
7. Set the oscillator frequency to 1 kHz. Adjust the scale on the Distortion Meter to measure 0.025% THD+N and turn on the 30 kHz low pass or audio bandpass filter. Verify that THD is less than 0.025%.
8. Set the scale on the Distortion Meter to measure -80 dBV signal level. With the filter still on, either turn off the output from the oscillator or disconnect the oscillator from the CP-3 input. Verify that the noise floor is less than -80 dBV (0.1 mVrms).
9. Repeat this test for the left channel by swapping the audio connections from the Right to the Left Input 1 jack and the Right to the Left Front Output jack on the CP-3.

Processed Output Test

This test verifies the functionality of the Front Left and Right Processed audio signal paths. Additional procedures check the Center, Side L & R, and Rear L & R Processed audio signal paths. The performance of the A/D and D/A conversion circuitry, as well as the Center, Side and Rear level control stages, are checked through gain, frequency response, THD+N, and S/N Ratio tests.

Audio Connections

1. Attach the audio input cable between the Low Distortion Oscillator and the CP-3 Right channel Input 1 jack.
2. Attach the audio output cable between the CP-3 Right Front Output jack and the input of the Distortion Analyzer.
3. Verify that Input 1 is selected on the front panel.

Setup

1. Make sure the 80 Hz high pass filters are off by pressing the EFFECTS MUTE button on the front panel until the display reads:

   HI-PASS ENABLE
   OFF

2. Select the Front Processed routing test by pressing the PROGRAM (up arrow) button on the front panel. The display should read:

   FPROC ENABLE
   ON

Procedure for Front L & R Outputs

1. Apply a 1 kHz signal at +4 dBV (1.58 Vrms) to the CP-3 right input.
2. Set the scale on the Distortion Analyzer to measure +4 dBV (1.58 Vrms) signal level.
3. Verify the output level from the CP-3 is +4 dBV (1.58 Vrms) +/-0.5 dB.
4. Adjust the scale on the Distortion Meter to measure 0.025% THD+N and turn on the 30 kHz low pass or audio bandpass filter. Verify that THD is less than 0.025%.
5. Set the oscillator's output level to -10 dBV (316 mVrms).
6. Set the scale on the Distortion Analyzer to measure -10 dBV (316 mVrms) signal level. Turn off the 30 kHz low pass or audio bandpass filter. Verify that the output level from the CP-3 is -10 dBV +/- 0.5 dB. Use this level as the 0 dB reference to check frequency response.
7. Sweep the oscillator frequency from 10 Hz to 16 kHz. Verify that the signal level is within +1/-4 dB of the reference level over the frequency band.
8. Set the scale on the Distortion Meter to measure -80 dBV signal level. With the filter on, either turn off the output from the oscillator or disconnect the oscillator from the CP-3 input. Verify that the noise floor is less than -80 dBV (0.1 mVrms).
9. Repeat this test for the left channel by swapping the audio connections from the Right to the Left Input 1 jack and the Right to the Left Front Output jack on the CP-3.

Procedure for Front Center Output

1. Apply a 1 kHz signal at +4 dBV (1.58 Vrms) to the left input of the CP-3.
2. Connect the audio cable from the Distortion Analyzer to the CP-3 Center Output jack.
3. Set the scale on the Distortion Analyzer to measure +4 dBV (1.58 Vrms) signal level.
4. Verify that the output level from the CP-3 is +4 dBV (1.58 Vrms) +/-0.5 dB.
5. Adjust the scale on the Distortion Meter to measure 0.025% THD+N and turn on the 30 kHz low pass or audio bandpass filter. Verify the THD is less than 0.025%.
6. Set the oscillator's output level to -10 dBV (316 mVrms).
7. Set the scale on the Distortion Analyzer to measure -10 dBV (316 mVrms) signal level. Turn off the 30 kHz low pass or audio bandpass filter. Verify that the output level from the CP-3 is -10 dBV +/- 0.5 dB. Use this level as the 0 dB reference to check frequency response.
8. Sweep the oscillator frequency from 10 Hz to 16 kHz. Verify the signal level is within +1/-4 dB of the reference level over the frequency band.
9. Set the scale on the Distortion Meter to measure -80 dBV signal level. With the filter on, either turn off the output from the oscillator or disconnect the oscillator from the CP-3 input. Verify that the noise floor is less than -80 dBV (0.1 mVrms).

Procedure for Side and Rear L & R Outputs

1. Select the Rear Processed output for the Side Outputs by pressing the VOLUME ▼ button on the front panel until the display reads:

   SIDE SOURCE IS
   REAR

2. Apply a 1 kHz signal at +4 dBV (1.58 Vrms) to the CP-3 right input .
3. Connect the audio cable from the Distortion Analyzer to the CP-3 Right Side Output jack.
4. Set the scale on the Distortion Analyzer to measure +4 dBV (1.58 Vrms) signal level.
5. Verify that the output level from the CP-3 is +4 dBV (1.58 Vrms) +/-0.5 dB.
6. Adjust the scale on the Distortion Meter to measure 0.025% THD+N and turn on the 30 kHz low pass or audio bandpass filter. Verify that the THD is less than 0.025%.
7. Set the oscillator's output level to -10 dBV (316 mVrms).
8. Set the scale on the Distortion Analyzer to measure -10 dBV (316 mVrms) signal level. Turn off the 30 kHz low pass or audio bandpass filter. Verify that the output level from the CP-3 is -10 dBV +/- 0.5 dB. Use this level as the 0 dB reference to check frequency response.
9. Sweep the oscillator frequency from 10 Hz to 16 kHz. Verify that the signal level is within +1/-4 dB of the reference level over the frequency band.
10. Set the scale on the Distortion Meter to measure -80 dBV signal level. With the filter on, either turn off the output from the oscillator or disconnect the oscillator from the CP-3 input. Verify that the noise floor is less than -80 dBV (0.1 mVrms).
11. Repeat this test for the left channel by swapping the audio connections from the Right to the Left Input 1 jack and the Right to the Left Side Output jack on the CP-3.
12. Repeat this test for the Left and Right Rear Outputs by swapping the appropriate audio connectons. Apply the signal to the CP-3 left input to test the Left Rear output and to the right input of the CP-3 to test the Right Rear output.
13. The Front Processed to Side Output signal paths may be tested by pressing the VOLUME ▼ on the front panel until the display reads:

    SIDE SOURCE IS
    FRONT

Repeat steps 2-11 of this procedure to complete this test.

Re-EQ and Surround EQ Test

This test verifies the functionality of the Front Left, Center and Right Re -EQ and Rear Left and Right Surround EQ circuits by checking gain, THD+N, and S/N Ratio. Frequency response is not checked as part of this performance verification due to the complexity of the filters' responses. For reference, frequency response information is given in the Theory of Operation section of this manual.

Audio Connections

1. Attach the audio input cable between the Low Distortion Oscillator and the CP-3 Right channel Input 1 jack.
2. Attach the audio output cable between the CP-3 Right Front Output jack and the input of the Distortion Analyzer.
3. Verify that Input 1 is selected on the front panel.

Setup

Select the Re-EQ/Surround EQ routing test by pressing the BANK button on the front panel. The display should read:

THX ENABLE
ON

Procedure for Re-EQ - Front L & R, Center Outputs

1. Apply a 1 kHz signal at +4 dBV (1.58 Vrms) to the CP-3 right input.
2. Set the scale on the Distortion Analyzer to measure +4 dBV (1.58 Vrms) signal level.
3. Verify that the output level from the CP-3 is +4 dBV (1.58 Vrms) +/-0.5 dB.
4. Adjust the scale on the Distortion Meter to measure 0.025% THD+N and turn on the 30 kHz low pass or audio bandpass filter. Verify the THD is less than 0.025%.
5. Set the scale on the Distortion Meter to measure -80 dBV signal level. With the filter on, either turn off the output from the oscillator or disconnect the oscillator from the CP-3 input. Verify that the noise floor is less than -80 dBV (0.1 mVrms).
6. Repeat this test for the left Re-EQ by swapping the audio connections from the Right to the Left Input 1 jack and the Right to the Left Front Output jack on the CP-3.
7. Repeat this test for the center Re-EQ by applying the signal to the Left Input 1 jack and measuring the signal from the Center Output jack on the CP-3.

Procedure for Surround EQ - Rear L & R Outputs

1. Apply a 1 kHz signal at +4 dBV (1.58 Vrms) to the CP-3 right input.
2. Connect the audio cable from the Distortion Analyzer to the CP-3 Right Rear Output jack.
3. Set the scale on the Distortion Analyzer to measure +4 dBV (1.58 Vrms) signal level.
4. Verify the output level from the CP-3 is +4 dBV (1.58 Vrms) +/-0.5 dB.
5. Adjust the scale on the Distortion Meter to measure 0.025% THD+N and turn on the 30 kHz low pass or audio bandpass filter. Verify that THD is less than 0.025%.
6. Set the scale on the Distortion Meter to measure -80 dBV signal level. With the filter on, either turn off the output from the oscillator or disconnect the oscillator from the CP-3 input. Verify that the noise floor is less than -80 dBV (0.1 mVrms).
7. Repeat this test for the left Surround EQ by swapping the audio connections from the Right to the Left Input 1 jack and the Right to the Left Rear Output jack on the CP-3.

Dolby Filter Test

This test verifies the functionality of the Rear Left and Right Dolby Filter circuits by checking gain, THD+N, and S/N Ratio. Frequency response is not checked as part of this performance verification due to the complexity of the filters' responses.

Audio Connections

1. Attach the audio input cable between the Low Distortion Oscillator and the CP-3 Right channel Input 1 jack.
2. Attach the audio output cable between the CP-3 Right Rear Output jack and the input of the Distortion Analyzer.
3. Verify that Input 1 is selected on the front panel.

Setup

1. Select the Re-EQ/Surround EQ routing test by pressing the BANK button on the front panel. The display should read:

   THX ENABLE
   ON

2. Activate the Dolby Filter circuitry by pressing the VOLUME ▲ button on the front panel. The display should read:

   DOLBY ENABLE
   ON

Procedure for Dolby Filter - Rear L & R Outputs

1. Apply a 1 kHz signal at +4 dBV (1.58 Vrms) to the CP-3 right input.
2. Connect the audio cable from the Distortion Analyzer to the CP-3 Right Rear Output jack.
3. Set the scale on the Distortion Analyzer to measure +4 dBV (1.58 Vrms) signal level.
4. Verify that the output level from the CP-3 is +4 dBV (1.58 Vrms) +/-0.5 dB.
5. Adjust the scale on the Distortion Meter to measure 0.025% THD+N and turn on the 30 kHz low pass or audio bandpass filter. Verify the THD is less than 0.025%.
6. Set the scale on the Distortion Meter to measure -80 dBV signal level. With the filter on, either turn off the output from the oscillator or disconnect the oscillator from the CP-3 input. Verify that the noise floor is less than -80 dBV (0.1 mVrms).
7. Repeat this test for the left Dolby Filter by swapping the audio connections from the Right to the Left Input 1 jack and the Right to the Left Rear Output jack on the CP-3.

Subwoofer Output Test

This test verifies the functionality of the Subwoofer audio signal path by checking gain, frequency response, THD+N, and S/N Ratio. For reference, a frequency response graph for the subwoofer output is given in the Theory of Operation section of this manual.

Audio Connections

1. Attach the audio input cable between the Low Distortion Oscillator and the CP-3 Right channel Input 1 jack.
2. Attach the audio output cable between the CP-3 Subwoofer Output jack and the input of the Distortion Analyzer.
3. Verify that Input 1 is selected on the front panel.

Procedure

1. Apply a 30 Hz signal at +4 dBV (1.58 Vrms) to the input channel.
2. Set the scale on the Distortion Analyzer to measure +10 dBV (3.16 Vrms) signal level.
3. Verify the output level from the CP-3 is +8 dBV (2.51 Vrms) +/-1.0 dB.
4. Use the output level from step 3 for the 0 dB reference to check frequency response. Sweep the oscillator frequency from 10 Hz to 80 Hz. Verify that the signal level is within +1/-7 dB of the reference level over the frequency band.
5. Set the oscillator frequency to 30 Hz. Adjust the scale on the Distortion Meter to measure 0.025% THD+N and turn on the 30 kHz low pass or audio bandpass filter. Verify that THD is less than 0.025%.
6. Set the scale on the Distortion Meter to measure -80 dBV signal level. With the filter still on, either turn off the output from the oscillator or disconnect the oscillator from the CP-3 input. Verify that the noise floor is less than -80 dBV.
7. Repeat this test for the left input by swapping the audio connections from the Right to the Left Input 1 jack on the CP-3.

Video Performance Verification

Required Equipment

Clean, antistatic, well lit work area

Video Source:
with Composite NTSC output.

Color TV Monitor:
with NTSC Composite inputs.

Video Input Cable:
single-ended, shielded video cable with RCA plug on one end and an appropriate connector on the other end for connection to the output of the Video Source.

Video Output Cable:
single-ended, shielded audio cable with RCA plug on one end and an appropriate connector on the other end for connection to the input of the Color TV Monitor.

Setup

1. Using the rear panel power switch, turn CP-3 power off.
2. Connect the output of the video source to CP-3 Video Input 1. Connect the CP-3 output to the input of the Monitor.

Procedure

1. Turn on both the video source and the TV Monitor. Verify that the picture quality is "good". (When the CP-3 is off the signal is fed directly through the unit, from Input 1 to the Output, without going through any internal circuitry.)
2. Power on the CP-3. Make sure INPUT 1 is selected. If no signal appears, or text appears on the screen, press SETUP to go into the Setup Menu and set "Display Time" to "Always On". See Owner's Manual for instructions.
3. Verify that the picture quality is the same as before. If repeated comparison is necessary, the CP-3 can be powered off and then on again.
4. Keeping CP-3 power on, check the On Screen Text quality. Verify that the text is synchronized and stable on the screen.
5. Select INPUT 2. Verify that the CP-3 on-screen display changes to blue screen in less than 5 seconds. Also verify that text is clear and stable.
6. Select INPUT 1. Verify that it takes less than 5 seconds for the CP-3 to change from blue screen to the video signal that is apparent at INPUT 1.
7. Move the cable that is connected to CP-3 INPUT 1 to INPUT 2, then select INPUT 2. Verify that the input video signal appears on the screen.
8. Move the cable that is connected to CP-3 INPUT 2 to INPUT 3, then select INPUT 3. Verify that the input video signal appears on the screen.

NOTE: The CP-3 video inputs are designed for NTSC "M" compositevideo signals. The video circuitry is capable of overlaying text on the incoming video signal; it is also capable of generating its own blue text background in the absence of an incoming video signal. Even though the video circuitry is designed for NTSC only, it can synchronize to incoming PAL and SECAM composite video signal and overlay text on the picture. In doing this, however, the text will lose sharpness, especially in SECAM.

4

Troubleshooting and Calibration

Troubleshooting

Power Supply

Equipment Required

Work Area:
clean, antistatic and well lit.

Variac:
Variable AC supply, 2 amp minimum.

Digital Multimeter (DMM):
3 1/2 digit, 0.25% accuracy or better.

Oscilloscope:
60MHz minimum bandwith w/X10 probe.

Initial Tests

1. Inspect the CP-3 for obvious signs of physical damage. Verify that all switches operate smoothly.
2. Remove the CP-3 top cover (16 screws) and bottom cover (7 screws) and verify that:

- There is a protective shield under the fuse and other areas of the power supply board.
- The value of the fuse (F1) is correct for the AC line voltage the CP-3 will be operating from.

Figure 4.1

Line	Fuse
100/120V	0.5 AMP/250V SLO-BLO
220/240V	0.25 AMP/250V T

CAUTION

REPLACE FUSE ONLY WITH SAME TYPE AND RATING.

- All socketed ICs are fully and correctly seated.
- All ribbon cables are installed correctly and secure.
- The chassis ground connection from each RCA connector block on the digital and analog boards is secure and far enough away from surrounding signal pins to avoid shorts.
- There are no burnt or obviously damaged components.

Power Supplies

1. Connect the CP-3 to a Variac or isolation transformer.
2. Power on the CP-3 with the rear panel power switch and slowly bring up the Variac to the required line voltage. The current should not exceed 0.4 AMPS for a 100/120V unit or 0.2 AMPS for a 220/240V unit. If the unit draws excessive current, turn it off and check the supply rails for shorts.

Figure 4.2

Nominal VAC	Operating VAC
100	90-110
120	105-130
220	200-240
240	220-260

3. Use a DMM to measure all the power supply rails by using the CP-3 chassis ground as the 0Vdc reference. Verify that all voltages are within the tolerance range shown below.

Power Supply Board

Figure 4.3

Supply Rail	Tolerance	Location
LCD+3.78	3.53-4.03	Right side of R1 (viewed from above)

Upper Analog Board

Supply Rail	Tolerance	Location
+15V	14.25-15.75	Large pad in the center of the PC board closest to the front of the unit.
-15V	14.25-15.75	Large pad in the center of the PC board closest to the rear of the unit.
+5VB	4.59-5.61	Cathode of CR204.

Figure 4.4

Lower Analog Board (bottom of P.C. board)

Supply Rail	Tolerance	Location
+5VA	4.59-5.61	U6 pin 16
-3.9VA	3.51-4.29	U6 pin 7
+15VCL	14.25-15.75	U25 pin 26
-15VCL	14.25-15.75	U25 pin 28
+5VD	4.75-5.25	FB1

Figure 4.5

Digital Board

Supply Rail	Tolerance	Location
+5V	4.75-5.25	U29 pin 16
+5V Video	4.75-5.25	U32 pin 22

Figure 4.6

Power Fail Test

1. Connect the + lead of the DVM to U24 pin 17.
2. Reduce the AC line voltage on the Variac to -15% of the rated line voltage. (See table below.) Verify the voltage reading is >4V (see table).
3. Reduce AC line voltage to -33% of the nominal voltage and verify the voltage reading is <1V

Nominal	-33%	-15%
100VAC	67VAC	85VAC
120VAC	80VAC	102VAC
220VAC	147VAC	187VAC
240VAC	161VAC	204VAC

Figure 4.7

3. Return the Variac to nominal AC line voltage.

Battery

Power off the CP-3 using the rear panel power switch. Measure the battery voltage at U33 pin 28 to ground and verify that it is >2.50 VDC.

Voltage Regulation Test

Power on the CP-3 using the rear panel power switch. Alternately set the Variac to both extremes of the AC line voltage operating range given in Table 4.2 and verify that the regulated supply rails remain within their tolerance range. Then, return the Variac to nominal AC line voltage.

Diagnostics

CP-3 Diagnostics are grouped for description as follows:

- Power Up Tests
- Burn In Tests
- Individual Tests
- Routing Test

Power Up Tests are run automatically every time the CP-3 is turned on via the rear panel POWER switch. These tests are run regardless of W1, W2 installation. Power Up diagnostics are also activated during normal operating mode power on. Refer to the diagnostic test sequence diagrams at the end of this chapter, as well as to individual test descriptions.

Burn InTests, which run automatically, quickly verify system functionality. Two types of Burn In tests are available: Pre-Burn In and Post-Burn In. The only difference between these is that the Pre-Burn In test completely clears the Master RAM, while the Post-Burn In test leaves the volatile memory intact. Each of the Burn-In tests can be run individually, and is described in the Individual Tests section.

Descriptions of the *Individual Tests* include those run automatically by the Burn In tests, as well as tests which require additional operator interaction.

The *Routing Test* section describes an audio I/O program that allows control over various aspects of CP-3 audio routing.

Diagrammatic instruction for acessing and running Diagnostics are presented at the end of this chapter.

Accessing Diagnostics

CP-3 Diagnostics are accessed by powering off the unit, then removing jumpers W1 and W2 on the Digital board. The CP-3 automatically runs Diagnostics when the unit is powered up without these jumpers.

W1 and W2 connect the two most significant bits (A14 and A15) of the System Processor (U24) to its ROM (U25). When the jumpers are removed these two ROM address lines are pulled high by R43 and R45, forcing the CPU to boot from address 0xC000h instead of from 0x0000h.

Operating Diagnostics

CP-3 Diagnostics are designed for control from either the front panel, or from the Expanded Remote. The small number of switches on the front panel requires some switches to have multiple functions, and others to perform toggle functions (press once to turn on, press again to turn off, etc.). Test groups are selected via the front panel BANK key, or via the PARAM key on the remote. Repeated presses of these switches will cycle through the main test groups.

Note: To use the Expanded Remote to run Diagnostics, press and hold any key on the remote, and aim it at the CP-3 during power-up.

From the main test menu, select a test group with the PROGRAM ▲ key on the CP-3 front panel or the PARAM s on the remote. Within each test group, selection is as follows:

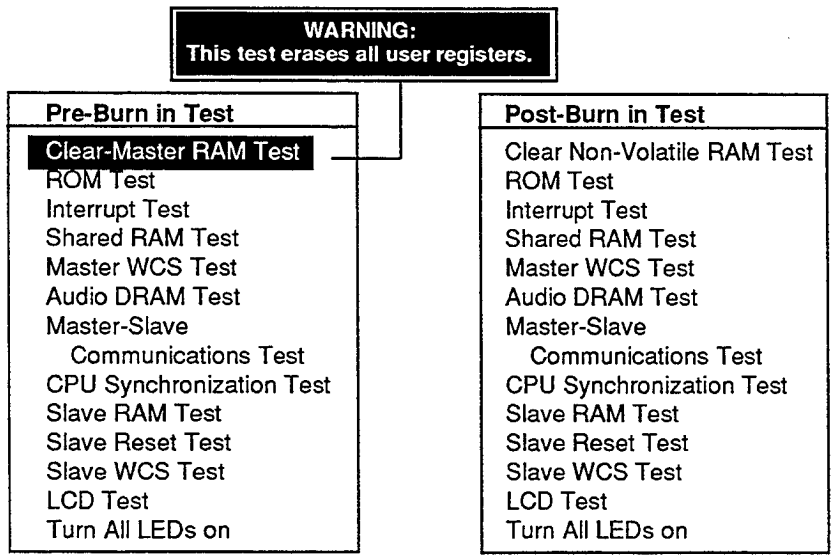
	Front Panel	or	Remote
To run the displayed test, press:	PROGRAM ▼		PARAM ▼
To step to the next selection press:	PROGRAM ▲		PARAM ▲

Any variation from this general set of controls, such as a requirement for additional keystrokes, is described in the individual test descriptions.

Burn In Tests

There are two types of Burn In tests: Pre-Burn In, and Post-Burn In. These are identical except that the Pre-Burn In Test clears the Master RAM, whereas the Post-Burn In Test clears only the Clear non-Volatile RAM.

The tests run automatically by the Burn In Tests are as follows:



Individual Test Descriptions

This section provides descriptions of each test run by the Burn In procedures, as well as the following five tests:

Non-Destructive Master RAM Test
Front Panel Switch Test
LCD Contrast Test
IR Remote Test
RAM Checksum

Clear Master RAM Test

This test will destroy any user presets, and should be avoided if possible, as setting up presets for this product can be somewhat time consuming. If the system has proven to be functional at one time, use the Non Destructive RAM Test.

This test checks the entire Master RAM, initializing memory as it goes. As the test moves the stack into the first two memory locations in the Slave shared RAM (the stack only consists of 2 bytes at this point), problems with Slave RAM (U35) or Master Processor access to it, will affect the outcome of the test.

The actual test consists of a series of write/reads to the RAM with address values as data, then 55h, AAh, FFh, and finally 00h (which gets left in the RAM at the conclusion of the test). Failure is reported by the message "TEST FAILED".

Clear Non-Volatile RAM Test

This is a test only of the non-volatile portions of the Master RAM. None of the user-stored programs are affected by this test. The test does, however, move the stack into the first two memory locations in the Slave shared RAM (the stack only consists of 2 bytes at this point). This means that problems with the Slave RAM (U35) or Master Processor access to it will affect the outcome of this test.

The actual test consists of a series of write/reads to the RAM with address values as data, then 55h, AAh, FFh, and finally 00h (which gets left in the RAM at the conclusion of the test). This test checks the RAM by completely filling a section of RAM, then reading it back in a second pass. Success indicates that the address lines are all working properly. Failure is reported by the message "TEST FAILED".

ROM Test

This test verifies ROM checksum. When system software is compiled, the checksum is calculated and stored in ROM (0FFFDh for Diagnostics; 0CFFDh for system software). The ROM Test adds up the value stored at each address, and compares the result with the stored value. A mismatch is indicated by the message "ROM TEST FAILED". The uppermost headroom LED is also lighted as an alternate indicator of test failure in the event that the display is not operational.

Note: Two versions of the ROM test exist: one run by the system, and one run by the Diagnostics. The system software test that runs on normal system power-up checks the system portion of ROM. The Diagnostics version checks only the Diagnostics portion of the ROM. If this test fails, do not run any other tests until this is repaired.

Interrupt Test

The Interrupt test checks the operation of the IR RECEIVER INTERRUPT TIMER (Digital board schematic, Sheet 2). The circuit divides the 36.0kHz WC/ signal (sample clock) down to 281.25Hz which gets signal conditioned down to a pulse which interrupts the Master Processor every 3.56ms. Because the WC/ line is only active when a program is running in the Lexichip, the test begins by loading and running a program. The test enables the interrupt (it is not normally enabled in Diagnostics), then immediately tests for an interrupt. It then waits about 8ms and checks again for an interrupt (which should have occurred twice by this time). The test then times the interrupt to verify that it is no less than 3.2ms and no more than 3.9ms (Ò10%).

Shared RAM Test

This is a test of the shared portion of the Slave Processor RAM from the perspective of the Master Processor. This test requires the Master to gain control of the Slave address and data buses by exerting a low on the MSREQ/ and SLVRAM/ lines. This should produce a low on the ACC/ line when the Slave relinquishes control. In this mode, the Master Processor accesses the shared RAM exactly as it would its own RAM. This is also a test of the interface between the Master and Slave Processor. This test is run with the slave Z80 reset at all times. The decoding is different and the timing is not critical. There will be no activity on the shared bus unless it is from the Master.

The actual test consists of a series of write/reads to the RAM with address values as data, then 55h, AAh, FFh, and finally 00h (which gets left in the RAM at the conclusion of the test). This test checks the RAM by completely filling a section of RAM, then reading it back in a second pass. Success indicates that the address lines are all working properly. Failure is reported by the message "TEST FAILED".

In the event of test failure, the interface chips between the Master and Slave are just as suspect as the Slave components. This interface consists of U26-29 and U36 with U16 assisting in the decoding process. Note that the buses are alternately controlled by the Master and Slave Processors. To verify that the Master address and data are reaching the Slave buses, remove the Slave Processor (U34) and the Slave decode (U16), and tie the ACC/ line low. Lift the RESET/ pin of the Master Processor (U24 pin 26) and apply a low frequency square wave (~20-100Hz) at TTL levels (0 to +5VDC) to the lifted pin. When the system is powered up the Master processor will be continuously reset at the rate of the oscillator. While it won't have time to do anything meaningful, it will have some activity on both its address and data buses which can be observed on a scope. Activity on all address and data lines of the Slave RAM (U35) indicates that the interface chips are at least capable of passing data between the buses. Bringing the ACC/ line high should disconnect the Master Processor from the Slave buses, and will appear as lack of activity on the Slave buses.

Master WCS Test

The Master WCS test is a RAM test of the Lexichip WCS memory, as executed by the Master Processor. As with the Shared RAM test, this tests the interface between the Master Processor and the Lexichip as well as the WCS. The primary difference between this and the Shared RAM Test is in the memory positions tested by the Master Processor. In terms of address lines, AD12 and AD13 are in opposite states for the Shared RAM Test. In addition, in this test, the LEX/ line goes low instead of the SLVRAM/ line. If LEX/ access works but Slave/ access does not, the problem is in RAM. If nothing works, the problem is likely to be the interface.

Audio DRAM Test

This is a test of the "AUDIO MEMORY" section shown on sheet 4 of the Digital board schematics. The actual mechanics of the test are executed by the Lexichip (U30) under the control of the Master Processor. The microcode which the Lexichip executes is actually generated while the test is run, and not stored in ROM.

The test itself is a fairly standard RAM test with 55555h, AAAAAh and FFFFFh hex each stored, then read back from memory followed by an address test. The address test basically loads a counting sequence of numbers into the DRAM then reads them back checking them as it goes. The test finishes by writing all 0s, then reading them back from the DRAM. In the event of failure, a message identifying data (55555, AAAAA etc.) or, for the address tests, "DRAM DATA ERROR" or "DRAM ADDR ERROR". The "DRAM ADDR ERROR" message indicates a floating bus. Due to time constraints, the slave is reset here.

Master-Slave Communication Test

This test verifies the ability of the two processors to send and receive messages to one another via the mailbox. The test consists of a set of sub-tests which do the following:

1. The Master resets the Slave and loads a program into a portion of the shared RAM, instructing the Slave to check the remaining shared RAM for complemented address data.
2. The Master clears the unused portion of shared RAM and releases the Slave from reset.
3. The Master waits while the Slave checks for address data. A "FAILED" message is expected from the Slave, as address data is not, in fact, written into the shared RAM.
4. The Master Processor then fills the unused portion of the shared RAM with complemented address data, waits for the Slave to run the program again, then checks for a "PASSED" message from the Slave.
5. The Master resets the Slave, and loads a new program into a portion of the shared RAM, instructing the Slave to fill the remaining shared RAM with un-complemented address data.
6. The Master then checks the shared RAM for un-complemented data, expecting not to find it.
7. The Master releases the Slave from reset, waits a short time, then checks for the uncomplemented data in the unused portion of the shared memory.

The purpose of this test is to run both processors simultaneously to verify that Master Processor can effectively control the Slave Processor. This test can effectively be considered an extension of the Slave RAM Test.

CPU Synchronization Test

This tests checks the synchronization of the Master and Slave Processors to the SWAIT/ signal generated by the Lexichip based on the WC/ (sample MWAIT/ clock). The test is performed by setting up a variable in the shared RAM, having the Slave increment it, then having the Master decrement it, once each sample period. With the Slave incrementing the variable and the Master decrementing it, the variable should remain at 0. The value is checked by the Master after each increment/decrement with "FAILED" reported if the variable is not equal to 0. If the test passes for 65k sample periods, "TEST PASSED" is reported.

This test loads and runs a program on the Lexichip. It is, therefore, also a test of some of the Lexichip's basic timing operations, as well as a test of the ability of the two processors to respond to WAIT signals. Both the SWAIT/ and the MWAIT/ lines should show activity while this test is run.

Slave RAM Test

This is a test of the Slave Processor RAM (U35) from the perspective of the Slave Processor under the control of the Master Processor. There is no need to run this test if communication between the buses does not work.

The Master Processor loads the test code into the Slave RAM then gives it a command to run the program. The test is divided into two blocks, allowing one portion of RAM to run while the other is tested. The first test is loaded and run from the bottom of the Slave memory (address 0000 hex); the second starts at address 0800 hex.

While "PASSED" may indicate that the Slave can access its RAM, and that the RAM itself is OK, almost any problem with the Slave Processor (U34) will cause a failure. Therefore, this can be considered as a general Slave Processor test. If the Shared RAM Test passes, then the RAM itself is probably OK, and the problem is with the Slave Processor (U34), the Dual Bus Interface (U26-29) or the Slave Decoder (U16).

The test itself is a fairly standard RAM test with 55h, AAh and FFh hex each stored, then read back from memory, followed by an address test. The address test basically loads a counting sequence of numbers into Slave RAM, then reads them back, checking them as it goes. The test concludes with all 0s written and read back from the RAM. Test results are displayed by the messages "PASSED" or "FAILED".

Slave Reset Test
This test checks the Master Processor's ability to reset the Slave Processor. To perform this test the Master Processor resets the Slave by setting the SRST/ line (from U37 pin 12) low and loads a program into the Slave RAM. The program instructs the Slave to write a message into the mailbox. With the Slave Processor still held in reset, the Master clears the mailbox, waits for a short period of time, then checks the mailbox for messages. If there is no message, the Master assumes all is well and releases the reset on the Slave. Again, the Master waits then checks to see that the Slave has, in fact, written a message into the mailbox. The test is repeated once to verify results.

This test is very important because most (all while its program is loaded) operations involving the Slave Processor require that it be reset while its program is loaded. When this test is run, two pulses should be detected on the Slave Processor reset (pin 26). If a pulse is detected, but the test still fails, the problem is probably with Master or Slave Processor access to the shared RAM. Run the Shared RAM Test, then the Slave RAM Test, and follow the troubleshooting procedures indicated.

Slave WCS Test
This test is similar to the Slave RAM Test except that it is run on the WCS memory in the Lexichip. Because the Lexichip is mapped into the memory space of the Slave Processor, the Slave views it as raw memory. The test program is loaded into the Slave RAM at address 0000 hex and is controlled and monitored by the Master Processor.

The test itself is a fairly standard RAM test with 55h, AAh and FFh hex each stored, then read back from memory, followed by an address test. The address test loads a counting sequence of numbers into the WCS, then reads them back, checking them as it goes. The test concludes with all 0s written and read back from the RAM. Test results are displayed by the messages "PASSED" or "FAILED".

LCD Test
Because the liquid crystal display (LCD) module contains a processor with memory space, the LCD Display Test is more than just a checkout of the display pixels and drivers. The test checks the LCD processor's ability to respond to commands as well as its ability to track the current display message.

The test initially turns the display off. The test then clears LCD memory by writing 0x20 (blank space code) into each memory location. The test then reads the memory to verify that the values are still 0x20. This process is repeated with the address number written into each memory location (1 = 1, 2 = 2, 3 = 3, etc.). These values are then read back and checked. When these tests have passed, the test loads a block character (FFFF hex) into each LCD memory location, and turns on the display.

NOTE: On Individual Test or power-up failure only:
Failure will halt testing until the operator presses PROGRAM ▼ on the CP-3 front panel or PARAM ▼ on the remote. This returns you to the Diagnostics menu with the message "TEST PASSED".

The Master Processor can only write to the LCD processor, if it verifies that the LCD isn't busy with some other task. If the LCD is busy, and the Master processor has to wait for more than 4ms, the LCD processor is assumed to be faulty, and the message "LCD DISPLAY FAIL" is displayed. The bottom four LEDs for both channels are also lit, as an alternate display in the event the LCD is not operational.

LED Test

The LED test is a simple program that sequentially lights each front panel LED. On completion, all LEDs are simultaneously lit. Because of the limitations of the matrixing that is used to light the LEDs, the intensity of the LEDs is not uniform when all LEDs are on. The intensity of each can only be judged when it is individually lit in the test, or during normal operation. The LEDs should light for about 1/2 second in the following order:

EFFECTS MUTE
MAIN MUTE
INPUT 4 (right)
INPUT 3
INPUT 2
INPUT 1 (left)
Right Headrooms (low to high)
Right Overload
Left Headrooms (low to high)
Left Overload

Non-Destructive Master RAM Test

This test checks each memory location in Master RAM (U33) without destroying its contents. The test retains memory values by testing each location individually with the value FFh then 00h. For each location, content is saved, then restored after testing.

While this test should be effective for testing the RAM itself, its ability to test the address and data bus to the Lexichip are somewhat limited, and it is possible for the processor to be writing to and reading from the same memory location through the entire test. The results of this test, therefore, should only be considered valid after the Non-Volatile RAM Test has passed.

When a failure occurs on power-up, the two yellow headroom LEDs will light and the message "RAM TEST FAILED" will be displayed.

Front Panel Switch Test

The Front Panel Switch test displays the most recently pressed key on the CP-3 front panel. The test doesn't report a pass or fail condition, so it is up to the operator to press each key and determine if the message is correct. If the front panel keys don't respond as expected, use the following circuit description to find the problem:

The front panel keys are read using a scanning technique that allows 12 switches to be read using only an 8-bit gate (U2) and two bits of a 6-bit latch (U3). The latch is clocked at pin 9 every 178µs (5.6kHz), three 500ns pulses 35us apart. The first pulse clocks SWC1 high, the second clocks SWC2 high (and SWC1 low), and the third pulse clocks the current LED data (and SWC2 low). When a key is pressed, SWC1 or SWC2 is connected to the input of U2. U2 is gated with two 500ns pulses every 178µs (5.6kHz). The first pulse occurs during the high portion of the SWC1 pulse; the second pulse ocurs during SWC2. The Master Processor determines which switch was pressed using these pulses.

To exit the test, press and hold the PROGRAM ▲ key on the CP-3 Front Panel or the PARAM ▲ key on the remote.

LCD Contrast Test

The LCD Contrast test is a utility program that allows the operator to set the contrast of the LCD display from Diagnostics. When run, the operator presses VOLUME ▲ to increase the contrast and VOLUME ▼ to decrease it. To exit the test, press and hold the PROGRAM ▲ key on the CP-3 Front Panel or the PARAM ▲ key on the remote.

The actual contrast is controlled by adjusting the DC voltage feeding pin 3 (CONADJ) of the LCD CONTROL LINK cable. The DC voltage is controlled with a simple D/A converter set up using a latch (U37) with some resistors and diodes. The outputs of the latch feed a resistive ladder through a signal diode with decreasing resistor value as the weight of the bit increases (lsb to msb with msb having the highest weight). When VOLUME ▲ is pressed, the outputs of U37 toggle as follows to alter the CONADJ voltage:

	MDB 0123	Hex	Voltage DC (typical)
full down	0000	00	0.27
	0001	01	0.35
	0010	02	0.43
	0011	03	0.50
	0100	04	0.58
	0101	05	0.64
	0110	06	0.71
	0111	07	0.77
	1000	08	0.77
	1001	09	0.83
	1010	0A	0.89
	1011	0B	0.95
	1100	0C	1.01
	1101	0D	1.06
	1110	0E	1.11
full up	1111	0F	1.16

Figure 4.8

A 500ns low pulse should be present on the CONTRAST/ line each time the binary value to U37 changes. While pressing and holding the VOLUME ▲ or VOLUME ▼ keys, this amounts to 16 pulses before the maximum value is reached. The presence of this pulse can be checked with Pulse Detector (LEX #770-90025) or with a scope set for NORM (manual) trigger level set at 2.5VDC.

IR Remote Test

The IR Remote test is a utility program that allows the CP-3 to identify and display the key being pressed on the infrared remote. The test will display "IR RESPONSE" on the LCD display if the IR decoder (U1 on the Front Panel IR board) detects infrared data. If a CP-3 code is detected, the actual key name will be displayed. This is important to confirm that the CP-3 is getting data.

When the IR Test is being run, the IRD/ signal to U31 on the Digital board is a 560ns pulse at a frequency of 8.4kHz (119us) or 5.6kHz (177us) in most of the other diagnostic tests. Serial data should be visible on a scope on the IRDATA line when a key on a remote is pressed and a 461kHz clock should be present on the IRCLK line. Each of the outputs from the IR DECODER chip (U23) should toggle if one of the remote keys is pressed. (Different keys will toggle different lines.) Note that the IRRST line must be low in order for the decoder chip to work. For the IR remote to work with the diagnostics the operator must press a key on the remote while the unit under test is powering up. This will toggle the IRRST line low. Running IR Remote Test automatically activates the remote circuitly during the test.

To exit the test, press and hold the PROGRAM ▲ key on the CP-3 front panel or the PARAM ▲ key on the remote. IRRST will be pulled high if it was not initialized on power up.

RAM Checksum Test

This test checks the ability of the Master RAM to retain data when the system is power-cycled. When the test is run the Master processor adds up the values of the data stored in all of the Master RAM locations and compares the result with the value calculated the last time the test was run. Note, therefore, if the test has never been run, these numbers will not match and this test will initially produce a "TEST FAILED" message.

Note that any changes in the RAM made by other Diagnostics tests will cause this test to fail. When the system first powers up under Diagnostics, pressing the front panel PROGRAM ▼ key or PARAM ▼ on the remote when "CP-3 Diagnostics" is displayed, will run this test immediately. This assures that the contents of the memory is not disturbed before the test is run.

Routing Test

The Routing test is actually an audio utility program that allows the operator to toggle all of the critical control signals related to the analog circuitry and to pass audio through the unit. When the Routing tests are loaded, an audio I/O program is loaded into the Lexichip that passes digital audio data from the A/D converter to the D/A converter. In order to provide a fair testing platform, the Lexichip does NO processing of the audio data as it passes through the system. This assumes that the digital circuitry is working properly (an assumption that shouldn't be made if you are troubleshooting audio problems).

Routing Tests are activated by pressing PROGRAM ▲ on the front panel or PARAM ▲ on the remote. To exit, press and hold the front panel PROGRAM ▼ or remote PARAM ▼ key. The analog control lines can be toggled by pressing various front panel or remote keys as shown in the following table:

Function	Front Panel	IR Remote	Control Line(s)	Location
Hi-Pass enable	EFFECTS MUTE	EFFECTS MUTE	HPEN/	U3.6
Mute Outputs	MAIN MUTE	MAIN MUTE	MUTE/	U3.5
Dolby Filter En	VOLUME ▲	VOLUME ▲	DOLBYEN/	U3.9
Side Out source	VOLUME ▼	VOLUME ▼	SIDESEL	U7.11
THX Filter En	BANK	N/A	THXEN	U7.7
Front Process En	PROGRAM ▲	PARAM ▲	FPROCEN	U3.2
Front Direct En	PROGRAM ▼	PARAM ▼	FDIREN	U7.14
Input Select	INPUT 1	INPUT 1	INSEL0	U3.19
Input Select	INPUT 2	INPUT 2	INSEL1	U3.16
Input Select	INPUT 3	INPUT 3	INSEL2	U3.15
Input Select	INPUT 4	INPUT 4	INSEL3	U3.12

Figure 4.9

It should be noted that the THX filter enable, Front Processed output enable, and the Front Direct output enable, are all mutually exclusive — when one is selected, the others are de-selected.

Once in the Routing Tests, pressing SETUP on the remote will reset all of the routing parameters, as if the program were just loaded.

MDACS

The Routing test also has controls which affect the MDACs which set the system input and output analog signal levels. These allow you to check the operation of the MDACs, and the system's ability to control them. Only the five most significant bits of the control bus can be checked, covering a control range of 30dB.

Each gain control node consists of two MDACs: one acting as input element, and one acting as the feedback element in an op amp circuit. One MDAC, therefore, controls positive gain and the other controls negative gain. The operator can send a value to any of the MDACs in the system.

Select an MDAC with the BALANCE ▲ and BALANCE ▼ keys on the remote. Press one of the Program keys (1-6) to send a value to the selected MDAC. The MDAC elements are shown to the left, in the order accessed by the BALANCE keys.

Display	MDAC Element
A	Input A (left and right)
B	Input B (left and right)
C	Center A Output
D	Center B Output
E	Subwoofer A Output
F	Subwoofer B Output
G	Front Left A
H	Front Left B
I	Front Right A
J	Front Right B
K	Side Left A
L	Side Left B
M	Side Right A
N	Side Right B
O	Rear Left A
P	Rear Left B
Q	Rear Right A
R	Rear Right B

Figure 4.10

When the BALANCE switches are pressed, a letter appears in the lower left corner of the display, identifying an MDAC element. Note that both left and right input MDACs are always accessed together, while all of the output MDACs can be discretely selected. The BALANCE ▲ key steps down the list; the BALANCE ▼ key steps up the list.

The following table shows the values that can be set to the MDAC, the remote key press required to send it, the resulting gain change, and the acceptable limits:

Binary Remote Key	Gain	Hex Data		Data	Limits
1 NORMAL	unity	ff	1111	1111	——
2 WIDE 6dB	7f	0111	1111	+0.3dB	
3 BINAURAL	12dB	3f	0011	1111	+0.6dB
4 SMALL	18dB	1f	0001	1111	+0.9dB
5 MEDIUM	24dB	0f	0000	1111	+2.0dB
6 LARGE	30dB	07	0000	0111	+3.0dB

Figure 4.11

The MDACs are typically tested by keeping one MDAC element fixed, sending the values shown above to the other element, then checking the resulting gain. The test is started by setting both of the MDACs to unity gain (both elements at ff), and taking a reference of the output level. The MDAC under test is then sent each value shown above, and the resulting gain is checked against the limit. Always return the value to ff before you step to the next MDAC.

Troubleshooting the MDACs is fairly straightforward. After entering the Routing Test, press the BALANCE ▲ and/or BALANCE ▼ key on the remote until the letter associated with the MDAC you want to test appears in the lower left corner of the CP-3 display. Feed the unit +7dBu for A tests or -23dBu for B tests and take a reference of the appropriate output's signal level. Press the key on the remote to produce the desired gain and verify that the output level changes by the amount indicated in the table (minus for A elements, plus for B elements).

When an MDAC is not functioning properly, the component itself should be replaced. If replacing the MDAC doesn't clear up the problem, the device is probably not getting the proper strobes or data. A primary suspect for these problems is the ribbon cable. Before proceeding to additional troubleshooting, verify that this cable is properly seated on both ends. If the cable is OK, monitor each of the outputs of U2 on the digital board while pressing the AMBIENCE 6 LARGE (07) key on the remote. Each time the key is pressed, there should be activity on bits 0-4. There should also be activity on the WR pin of the selected MDAC. Also check the outputs of U2.

Video

The Routing Test puts the video overlay chip (U32) into I/O mode, passing the video it receives back to its output. In all other Diagnostic tests, the video overlay chip is generating a character set display.

The overlay chip gets the data for these characters in a single pass when the diagnostics initialize, making the circuit somewhat tricky to troubleshoot. One way to get some activity out of the parallel to serial chip U38 and the GAL U40 is to repeatedly press the SETUP key on the remote. This re-initializes the Routing Test, which sends a command to the overlay chip to go into the bypass (I/O) mode. When this happens, there should be activity on the VCS/, SCLK and VCLK lines.

NOTE: The IR Remote Receiver is activated by holding down any key on the remote while powering on the unit.

The operation of the GAL can be checked by lifting pin 2 (of U40) and connecting it to ground. In this configuration the SCLK and VCLK lines should have a 50% duty cycle square present at 570kHz. Note that these clocks will be at opposite phase from one another. The ZCLK/ feeding the clock input to the GAL should be at 4.55MHz and the VCS/ line should be at the same state as the VIDEO/ line.

Troubleshooting

The following diagnostic flow charts provide a quick reference guide through CP-3 Diagnostics.

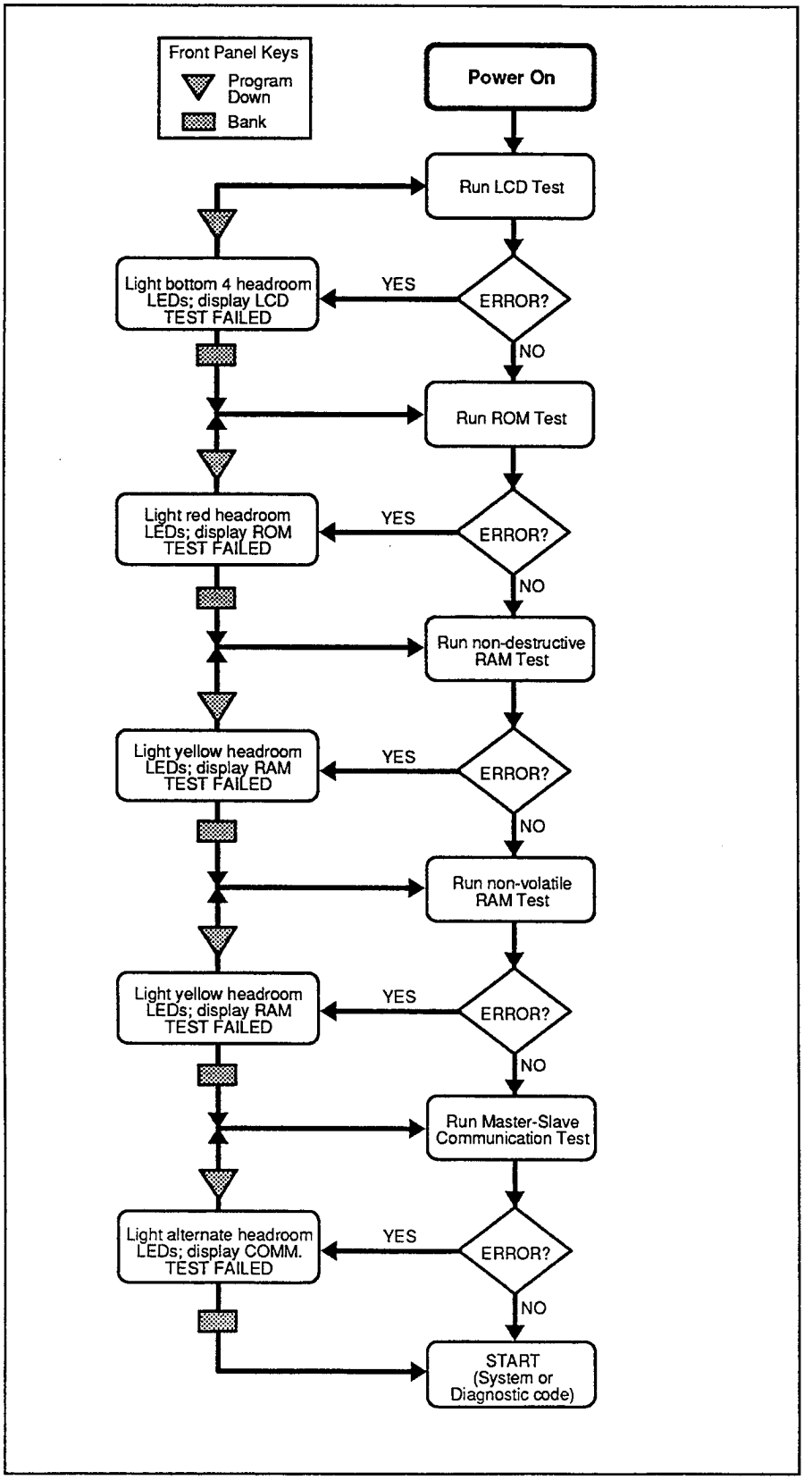


Figure 4.12
CP-3 Power Up Tests

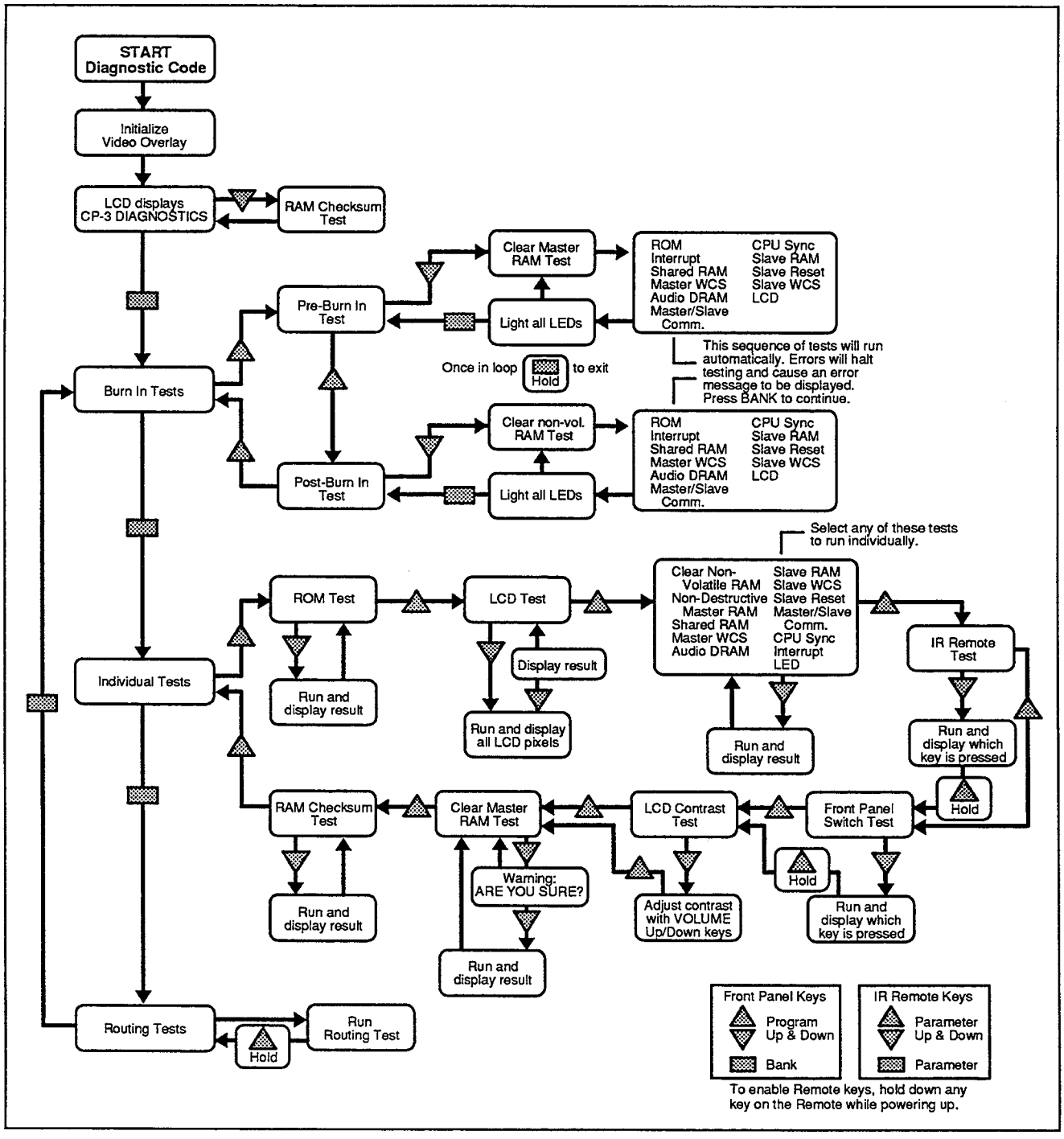


Figure 4.13
CP-3 Diagnostics

Preserving User Presets

Because the development of user presets for this product is often difficult, and there is no way to back them up, it is desirable to preserve them if possible. One method of preserving user presets is to set up a 28 pin DIP clip with a 3V battery connected from pin 28 (+) to pin 14 (-) and a 10kΩ pull up resistor connected from pin 20 to pin 28. The DIP clip is clipped onto the Master RAM (U33) in the unit under test with the power to the system off. If the IC is removed from the CP-3 Digital board with the DIP clip attached, the unit will retain its contents. A backup RAM is then installed in the unit. The RAM/DIP clip should be stored in non-conductive foam to prevent it from powering down. Reinstalling the RAM after troubleshooting, with the system powered off, should restore the user presets.

Initialization Problems

The causes for this type of problem with the CP-3 can be somewhat far reaching. The following provides some tricks and techniques for getting the system up. The first thing to check is power fail, reset, and the Lexichip for "dead" system problems.

While the Master Processor is capable of operating without the Slave processor, there are things that the Slave can do that will take the whole system down. The MWAIT/ line which is output from the Slave Decoder (U16 pin 19), if held low, will keep the Master Processor waiting forever. If you observe this on a scope, lift pin 19 of U16 and tie U24 pin 24 to +5V. This will allow the Master Processor to get on with business, but will also interfere with communication between the Master and Slave. There is, however, sufficient activity to perform some tests. The lifted pin of U16 should be high with very quick strobes low whenever the Master attempts to run a Slave test. This can be picked up with a scope in the NORM mode with the trigger level set for about 2.5VDC. The TRIGGER lamp should briefly light.

Slave Problems

As the Slave Processor has no ROM, all software it receives arrives from the Master Processor via the shared RAM. It is vital, therefore, for the Master to be able to access the shared RAM. A problem with this could have all the appearances of a Slave problem. As the Lexichip/Slave is capable of hanging up the Master by pulling down the MWAIT/ line, this line should be checked and disabled as outlined in the previous section to get things running again.

Once the Master can access the shared RAM, attention can be directed to the Slave Processor itself. As the Processor, the RAM, and the GAL are all socketed, they are candidates for replacement. If replacement chips aren't readily available, parts in the Master and Slave can be swapped (except for the GALs). If the operation of the system changes, there is a strong possibility that the last part swapped is defective, or that the socket is defective or poorly soldered. If replacing the main components in the Slave doesn't cure the problem, by process of elimination, the DUAL BUS INTERFACE and MASTER BUFFER become prime suspects. These parts are soldered in, so they cannot be easily swapped out. Fortunately, the operation of the chips in these circuits is fairly straightforward. The DUAL BUS INTERFACE is simply a bank of AC157s which are quad 2-input data selectors. When the ACC/ line (SEL pin) is low, the A inputs from the Master Processor are routed to the Y outputs. When ACC/ is high, the B inputs from the Slave Processor are routed to the Y outputs. The trick is to force the ACC/ line high, get some activity on the Slave address lines and check to see if they make it to the outputs of the 157s and ultimately to the RAM. Actually the real trick is to keep the Master Processor address lines quiet while you are performing this test, to determine if what you are seeing at the outputs of the 157s is in fact the Slave address information.

One method of quieting the Master Processor is to remove it. If the Slave Processor is also removed and the ACC/ line is pulled high (with U16 pin 18 lifted), the ZCLK signal at pin 6 of the U34 socket can be jumped to each of the address lines. If the associated address line on the other side of the 157s is checked, the clock signal should be detected.

CP-3 Memory Map

The following tables are the memory maps for the Master and Slave processors. They are included here as a troubleshooting tool to help match diagnostic failures to specific pieces of hardware. The piece of hardware is identified along with the memory space it occupies notated in both hex and in binary. The binary version was included to help match memory space to actual address lines. Please note that the first line indicates the starting address and the second line indicates the ending address with all of the binary values between implied. Shared memory is available to both processors.

Master Processor:

			Binary (address lines)					
			15	12	8	4	0	
Hardware	**IC #**	**Hex**					**Size (bytes)**	**Notes**
ROM	U25	0000	0000	0000	0000	0000	52k	
		CFFF	1100	1111	1111	1111		
MDACs	see	D000	1101	0000	0000	0000	20	
	Route sect	D013	1101	0000	0001	0011	(1 each)	
ROUT Reg1	U3	D01B	1101	0000	0001	1011	1	
ROUT Reg2	U7	D01F	1101	0000	0001	1111	0.5	
Lexichip	U30	D400	1101	0100	0000	0000	1k	Shared
		D7FF	1101	0111	1111	1111		
Slave RAM	U35	E000	1110	0000	0000	0000	4k	Shared
		EFFF	1110	1111	1111	1111		
Master RAM	U33	F000	1111	0000	0000	0000	4k	
		FFFF	1111	1111	1111	1111		

Slave Processor:

			Binary (address lines)					
			15	12	8	4	0	
Hardware	**IC #**	**Hex**					**Size (bytes)**	**Notes**
Slave RAM	U35	0000	0000	0000	0000	0000	4k	Shared
		0FFF	0000	1111	1111	1111		
		1000	0001	0000	0000	0000	4k	
		1FFF	0001	1111	1111	1111		
Lexichip	U30	2000	1101	0100	0000	0000	1k	Shared
		23FF	1101	0111	1111	1111		

Figure 4.14

Audio Performance Troubleshooting

When troubleshooting any kind of equipment, intermittent problems are among the most difficult to trace. The first step when troubleshooting any problem is to collect as much information as possible. The following table outlines some basic questions which should be answered before attempting to troubleshoot an analog problem on the CP-3. (Additional troubleshooting techniques can be found in the Diagnostics section earlier in this chapter.)

Does the problem occur:
1. on only one output?
2. at only certain signal frequencies?
3. at only certain signal levels?
4. in only certain programs?
5. with input only?
6. without input only?

In general, it is best to run all of the audio proof of performance tests to further isolate the problem. This can be vital when troubleshooting subtle problems. While some system failures may cause a variety of tests to fail, troubleshooting based on one type of symptom may be much easier than another. For example, a bad capacitor may produce a high level of distortion and a frequency response problem. The frequency response problem would be easier to trace because the signal level can be monitored with an ordinary scope probe.

Bad Input Channel(s)

Probably the most useful piece of information to gather is whether the problem is on only one or on both channels. If the problem is occurring on only one output, the following assumptions can be made with some level of confidence:

The power supplies are OK.
The system timing (clocks) is O.K.
The digital circuitry up to the filter is O.K.

These types of problems can be fairly easy to troubleshoot because the working channel can be used as a reference. With the same signal applied to both inputs compare the signal on both channels at various points along the analog signal path. Depending on the nature of the problem this can help localize the problem fairly quickly. The signal flow diagrams at the end of this chapter, along with the tests described under Audio Performance Verification, can help isolate the faulty circuitry.

If the problem is occurring on both channels, it is unlikely that two corresponding components failed in the same way at the same time. Therefore, the problem can probably be traced to a component which is common to both channels or to a system type of problem such as a power supply or timing problem. If there is no output, refer to the following section for more troubleshooting information.

No Output

With no output signal, determination of whether one or both channels are bad can reduce the number of suspicious circuits dramatically.

When the system has no output from only one channel, the problem can usually be easily traced by feeding a sine wave into both inputs and

comparing the left and right signals at various points in the circuit. Any problems related to one channel only will probably not occur in this circuitry.

The first thing to check is the +15V, -15V and +5VA power supplies on the Analog boards. Verify that they are within the specified voltage ratings given in the Power Supply description. If they are OK, check the OUTMUTE voltage at the collector of Q5 on the Lower Analog board for a reading of -15V. If the voltage isn't present, one of the 8 FETs (Q200-Q207) may be defective and could drag down the OUTMUTE signal causing no output from any channel. If OUTMUTE is OK, feed a sinewave into both inputs and check for signal at the output of the A-D converter chips (U25 pin 23 and U12 pin 23). If there is signal present, check the signal to the output of the deglitch circuits at U24 pin 6 (left) and U10 pin 6 (right). If no signal is present, check for HOLD and HOLD/ at U28 and U11 pins 1 & 9 (HOLD), 8 & 16 (HOLD/).

No +15V Supplies

If the +15V supplies are down, there is a problem on one of the analog boards. Check the +15V supplies for shorts. If there are no shorts, remove the cable at J207 on the Upper Analog board and power up the CP-3. If the supplies return, one of the MDACs may be faulty. Power down the CP-3, reinstall the cable at J207, power up the CP-3 and carefully check the MDACs (U201, 203, 210, 211, 212, 215, 221, 225) for heat. A hot MDAC is usually bad and will pull down the +15V supplies.

User Registers don't sound the same as when they were stored

This can be caused by a number of things. To help localize the problem, several preliminary tests should be performed. Verification of the system's ability to store and generate a modified program can usually be done by creating a program variation, storing it, power cycling the unit several times and checking the register. If the register has noticeably changed, the problem is probably in the Master Processor static RAM (U33) or the battery circuit. If the register seems unchanged, the fault may be in the Digital Signal Processor (DSP) or the audio signal path itself.

Video Performance Troubleshooting

The Video portion of the CP-3 comprises the rear portion of the Digital board. Initial troubleshooting is similar to the procedure described in the audio section. First, collect as much information as possible. Verify that all the power supplies are within specification, then proceed to narrow down the possible faults. Before attempting to troubleshoot a video problem with the CP-3, you should be able to answer these questions.

Does the problem occur:
1. on only one input?
2. on only certain programs?
3. with input only?
4. without input only?

If possible, perform the video calibration and run the diagnostic tests to determine if the rest of the Digital board is functioning. This can be vital when troubleshooting subtle problems. While some system failures may cause a variety of tests to fail, troubleshooting based on one type of symptom may be

much easier than another. Potential failure modes in the video section can be classified into the following four categories:

1. No video output.
2. No video output with only one particular input.
3. No on-screen programming.
4. Poor video quality.

No Video Output

The majority of the functionality of the video circuit is handled by the Sync Separator (U1) and the Character Overlay (U32) ICs. In cases where no video is being output, first check all the power supplies. If the supplies are within specifications, check the video signal path. Input a video signal into one of the inputs on the rear of the CP-3 and select the corresponding front panel video input. Verify that the video signal appears at U1 pin 21. If no video signal appears here, trace back to the video input selected through the video pre-amp section, Q3 and Q4, to the relay section and then to the video input jack. To verify that the relay section is being properly selected, check U14, R15, and R20. Use the table below to verify relay selection.

Video Input Selected	U14 pin 11	West (left) Side R15	South Side R20
Channel 1	high	low	high
Channel 2	low	low	low
Channel 3	low	high	low
Channel 4	high	low	high

Figure 4.15

If the video signal is present at U1 pin 21, verify that HSYNC/and VSYNC/ are present at U1 pins 9 and 14. These signals should be high with low-going pulses. HSYNC/ should have a low-going pulse every 63.6us and the pulse should stay low for about 6us. VSYNC/ should pulse low every 16.9ms. If the correct video information is reaching U1 and the free running adjust can be properly calibrated (as per the Calibration section), U1 is probably faulty.

Verify that the character overlay IC (U32) is putting out a video signal. If it is, trace the video output signal through the output buffer (Q7), to the output relay (RY2). If there is no video output at U1 pin 12, check pins 7 and 8 for a clocksignal. If a clock signal is present, check pins 17, 18 and 19 for the correct control signals. Pin 17 (VDATA) should have a group of low-going pulses about every 7.14ms. The group of low-going pulses actually consists of two sets of low going pulses spaced about 63.6µs apart. Pin 17 (VCS/) should have a low-going pulse about every 7.14ms. Pin 18 (VCLK) should be the inverse of pin 17. If all the correct clock and control signals are present, the chip itself (U32) is likely to be faulty.

Bad Input Channel(s)

The most useful piece of information to gather is whether the problem is on a single input or on multiple inputs. If the problem is occurring on only one input, you can assume that the power supplies are OK.
The most likely source of the problem is that the relay, or the associated circuitry which selects the input is defective. Refer to the relay control circuitry information in the preceding section.

No On-Screen Programming

U32, the IC that controls on-screen programming, may be faulty. Refer to No Video Output and check for the correct clock and control signals on U32.

Poor Quality Video

This problem is difficult as it involves verifying the correct signal amplitudes, frequencies, ringing on signals, noise on signals etc. throughout the entire video path. If possible, compare the signal amplitude and overall quality against those of a functioning CP-3. If this is not possible, follow the video path as outlined above in No Video Output and look for changes in video signal quality. Also look for clean edges on all the control and clock signals. A capacitor could be lossy, one of the BJT's could have an incorrect bias voltage, or one of the relays could have a high contact resistance or be making poor contact. If all of the signals look acceptable, U1 or U32 is probably at fault.

Converter Calibration

Calibration

Converter calibration allows the DC offset being sensed by the converter to be nulled to a minimum. Some operating modes are very sensitive to DC offset, thereby allowing the converters to be calibrated. There is no test performed on this calibration and bad calibration will only reveal itself in a potentially bad signal-to-noise and generally bad sonic performance.

Required Equipment

Clean, antistatic, well lit work area

Oscilloscope:
60 MHz minimum with a X10 probe

Low Distortion Oscillator:
single-ended 600 ohm output, <.005% THD

Audio Input
Y Cable: shielded audio Y cable with RCA plugs on the Y end and an appropriate connector on the other end for connection to the Low Distortion Oscillator output

Small slotted screwdriver

Setup

1. Power off the CP-3 from the rear panel power switch.
2. Remove the CP-3 top cover (16 screws).
3. Power on the CP-3 from the rear panel and select Program 2 (Panorama WIDE).
4. Select INPUT 1 on the CP-3 front panel.

Audio Connections

Attach an audio input Y cable between the Low Distortion Oscillator and both CP-3 INPUT 1 jacks.

Procedure

1. Apply a 1kHz signal at -47.25dBV to both channels of INPUT 1.
2. Adjust R120 (left channel) and R60 (right channel) on the lower analog board for the fewest lit headroom LEDs.

Video Calibration

Required Equipment

Clean, antistatic, well lit work area

Frequency Counter:
7-digit resolution with 10 MHz measurement capability

Oscilloscope:
60 MHz minimum with X10 probe.

Setup

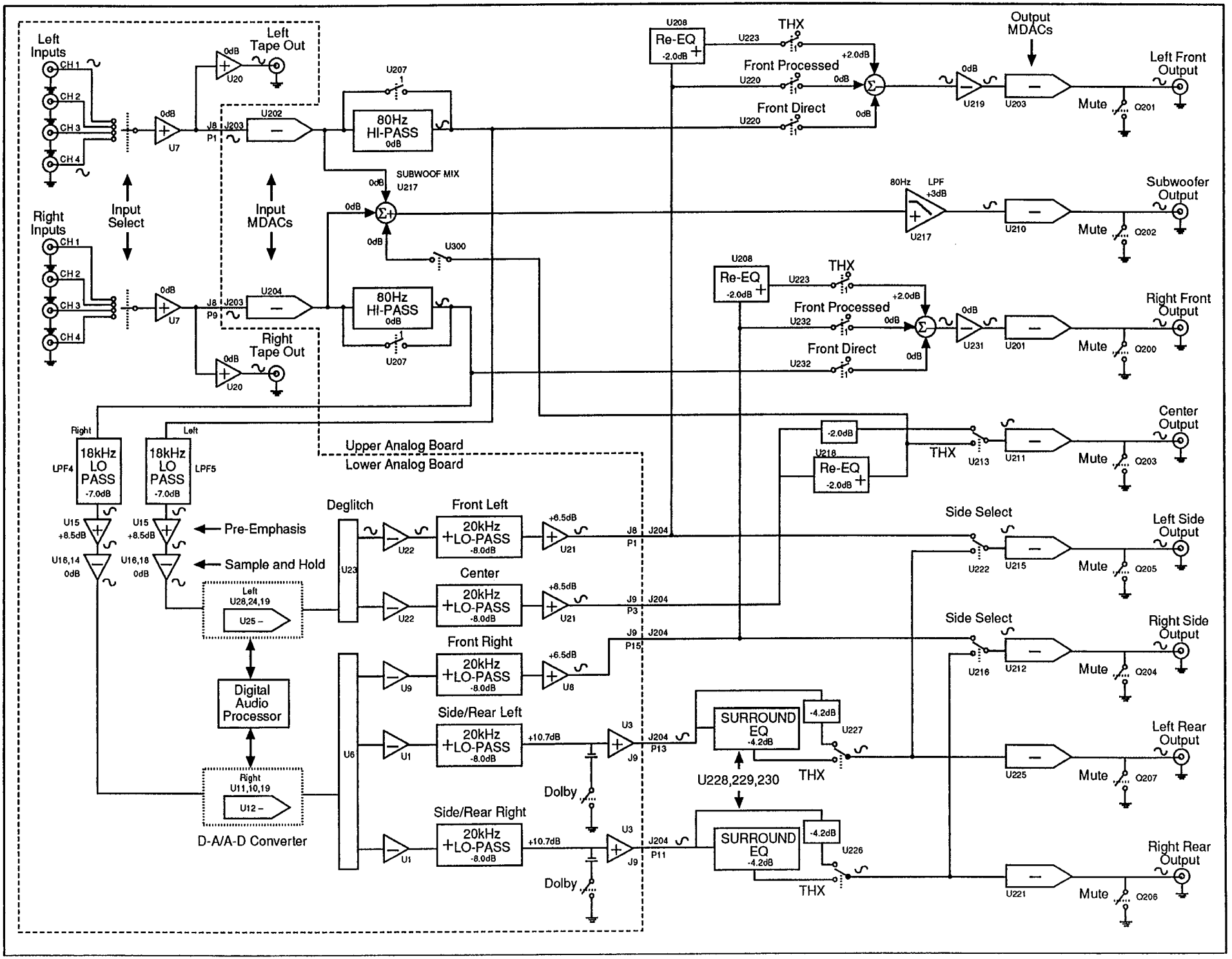
1. Power off the CP-3 from the rear panel power switch.
2. Remove the CP-3 top cover (16 screws).

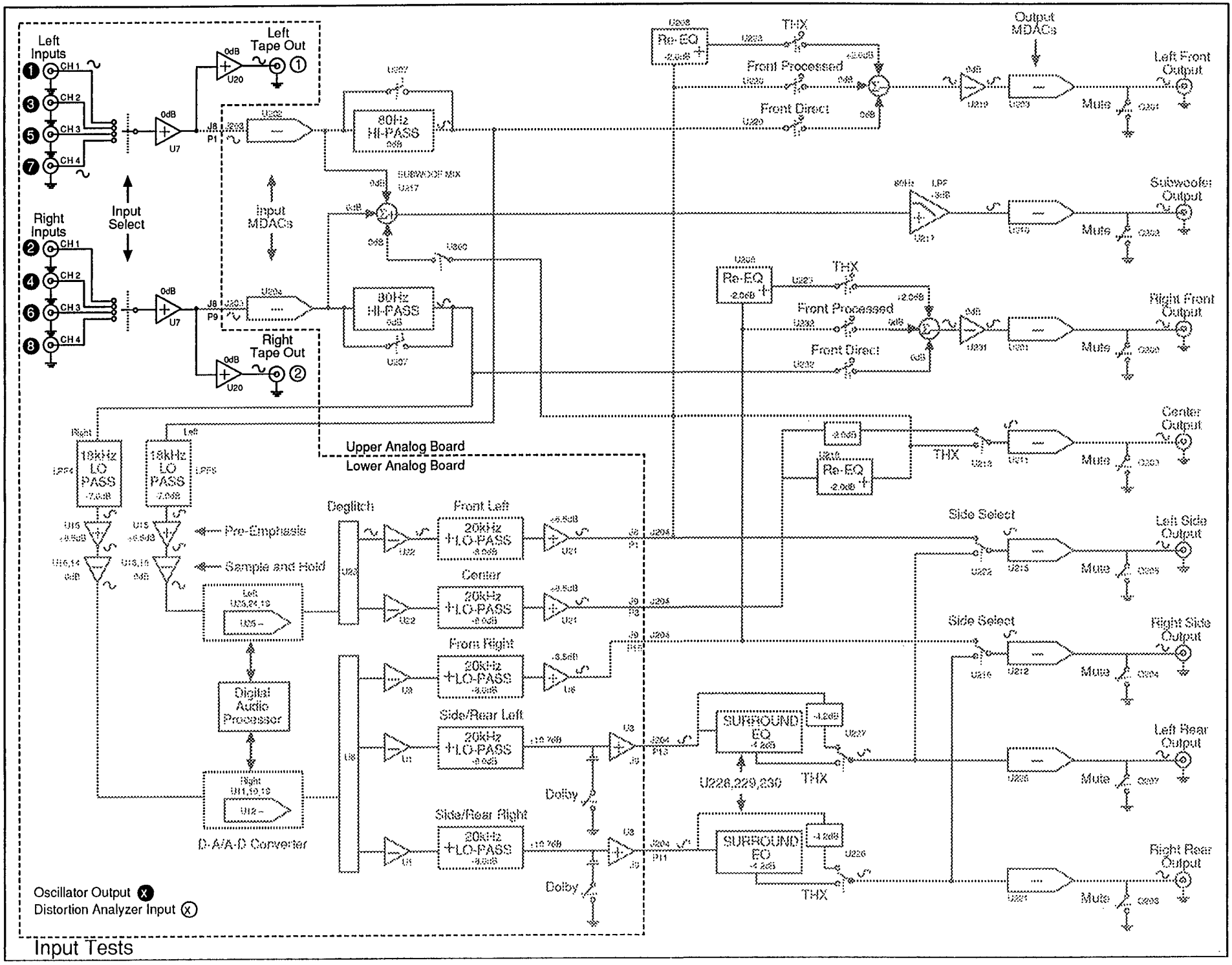
Video HSYNC Free Running Frequency Adjustment

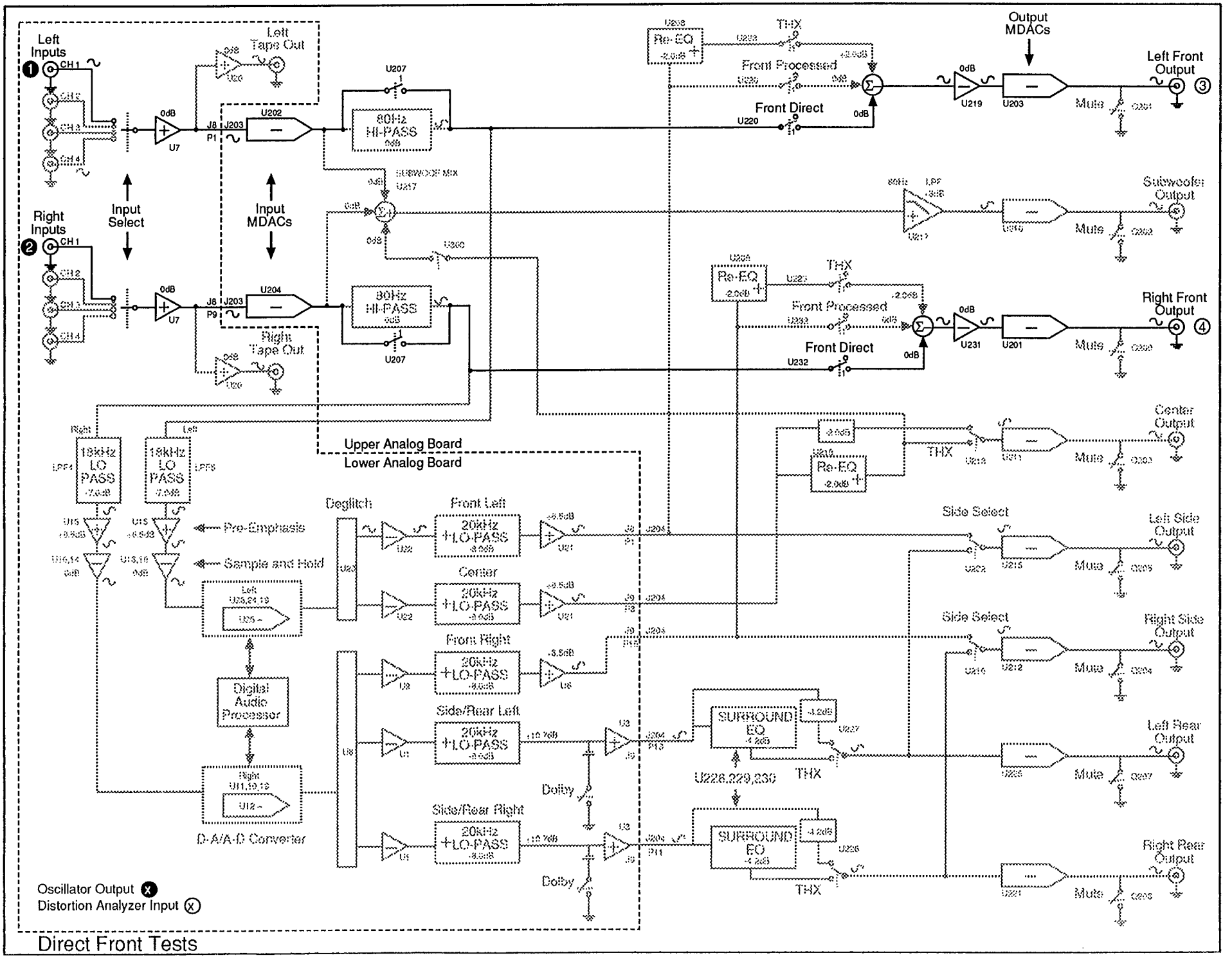
Procedure

1. Install a jumper at W3 on the Digital board.
2. Power on the CP-3 from the rear panel power switch.
3. Connect the X1 probe from the frequency counter to TP1 on the Digital board.
4. For 100V-120V units, adjust R16 for 15.73kHz ±.01kHz (15720-15740Hz).

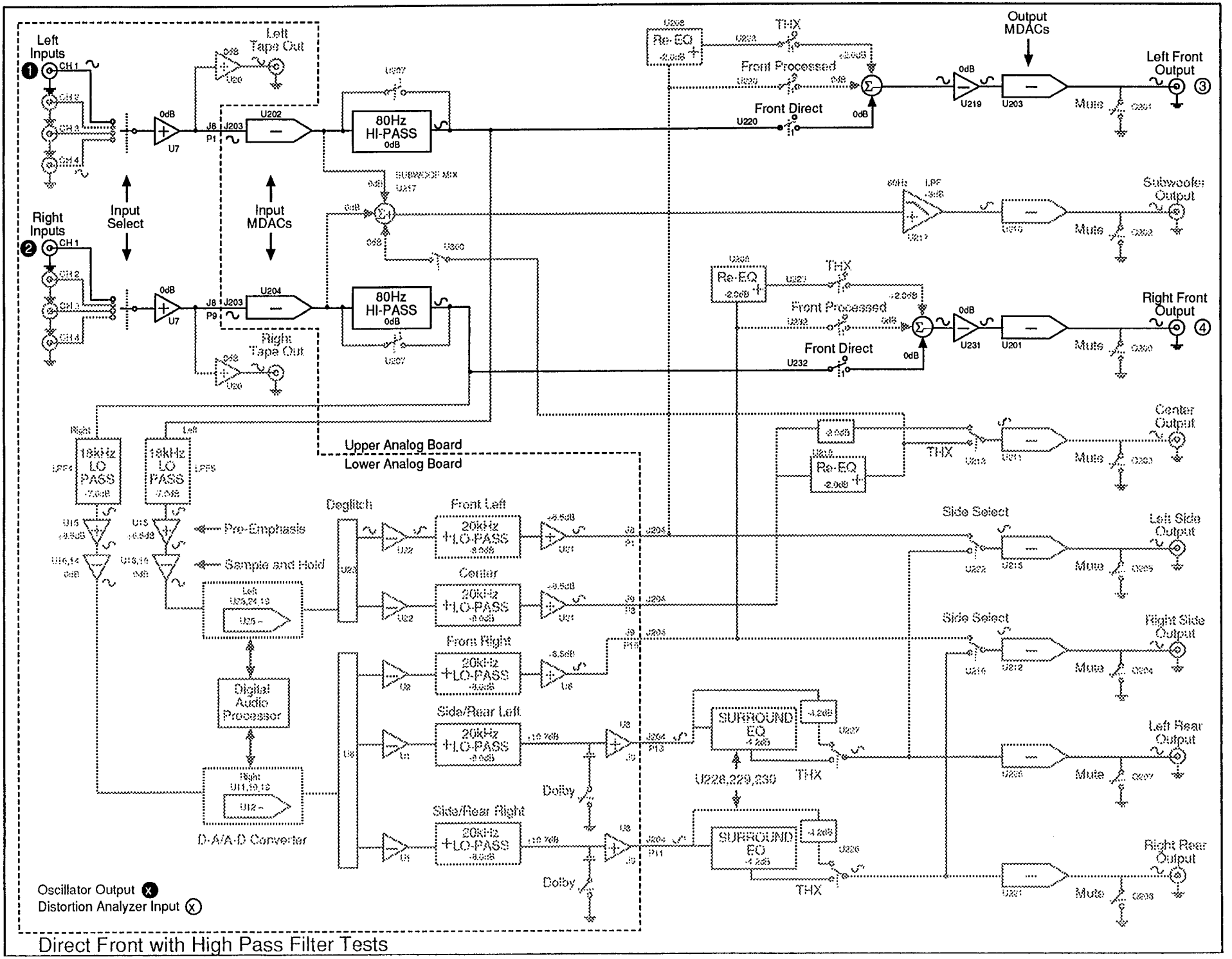
   For 220V-240V units, adjust R16 for 15.62kHz ±.01kHz (15610-15630Hz).
5. Power off the CP-3 from the rear panel power switch.
6. Remove jumper at W3.


Left Inputs
CH 1
CH 2
CH 3
CH 4
Left Tape Out
0dB
U20
U7
J8
P1
J203
U202
80Hz HI-PASS 0dB
U207
SUBWOOF MIX
U217
U300
Input Select
Input MDACs
Right Inputs
Right Tape Out
J204
U204
Upper Analog Board
Lower Analog Board
Right
Left
18kHz LO PASS -7.0dB
LPF4
LPF5
U15 +8.5dB
U16,14 0dB
U16,18 0dB
Pre-Emphasis
Sample and Hold
Left U28,24,19
U25 –
Digital Audio Processor
Right U11,10,19
U12 –
D-A/A-D Converter
Deglitch
U23
Front Left
Center
Front Right
Side/Rear Left
Side/Rear Right
20kHz +LO-PASS -8.0dB
+6.5dB
+10.7dB
U22
U21
U9
U8
U1
U3
U6
Dolby
U208
Re-EQ -2.0dB
THX
U223
U220
U232
Front Processed
Front Direct
+2.0dB
Output MDACs
U219
U203
Left Front Output
Mute
Q201
80Hz LPF +3dB
U217
U210
Subwoofer Output
Q202
U231
U201
Right Front Output
Q200
-2.0dB
U218
U213
U211
Center Output
Q203
Side Select
U222
U215
Left Side Output
Q205
U216
U212
Right Side Output
Q204
SURROUND EQ -4.2dB
-4.2dB
U227
U228,229,230
U225
Left Rear Output
Q207
U226
U221
Right Rear Output
Q206

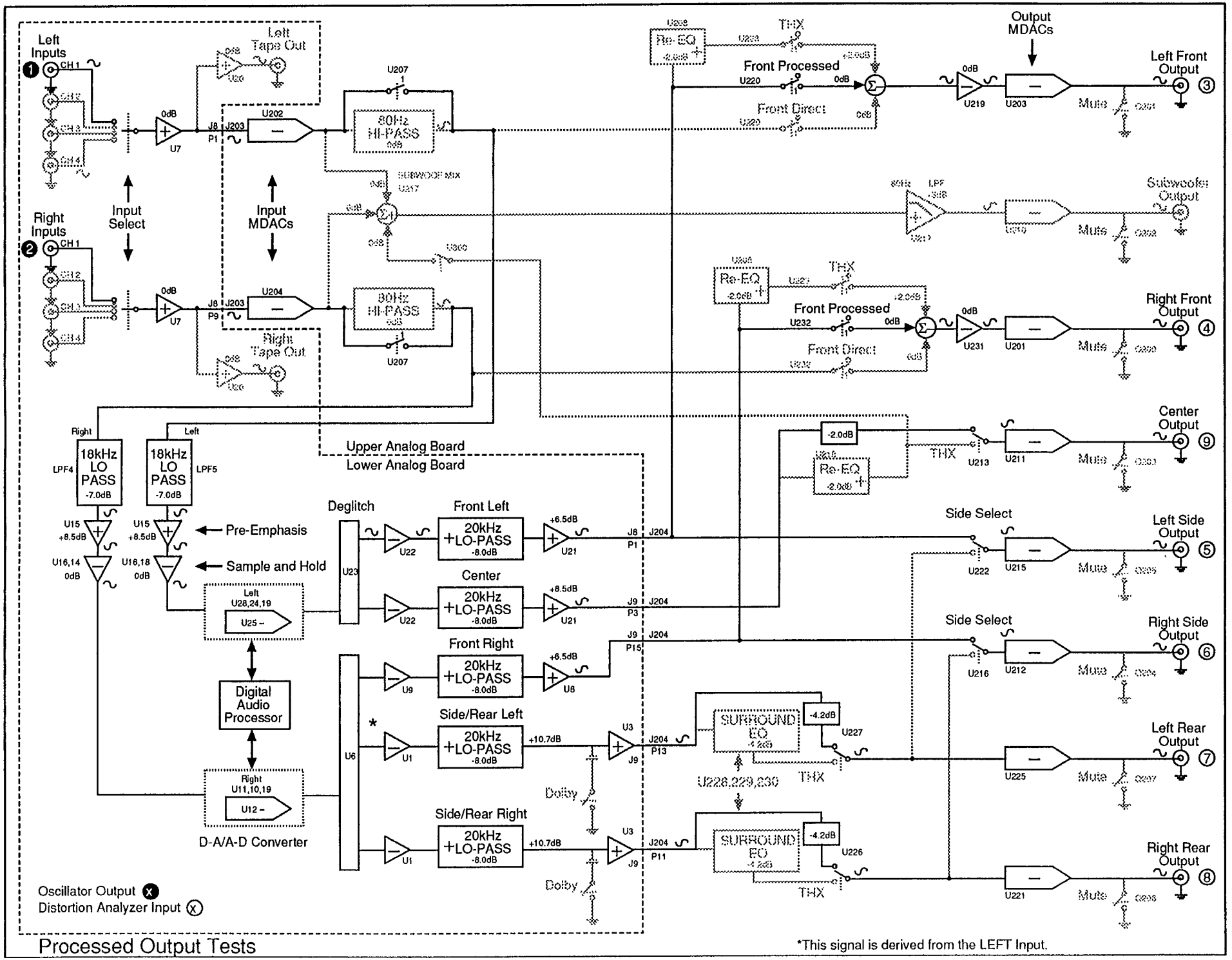

Left Inputs
Right Inputs
Input Select
Input MDACs
Left Tape Out
Right Tape Out
Upper Analog Board
Lower Analog Board
Pre-Emphasis
Sample and Hold
Digital Audio Processor
D-A/A-D Converter
Deglitch
Front Left
Center
From Right
Side/Rear Left
Side/Rear Right
Dolby
Re-EQ
THX
Front Processed
Front Direct
Output MDACs
Left Front Output
Subwoofer Output
Right Front Output
Center Output
Side Select
Left Side Output
Right Side Output
Left Rear Output
Right Rear Output
SURROUND EQ
Mute
Oscillator Output
Distortion Analyzer Input
Input Tests

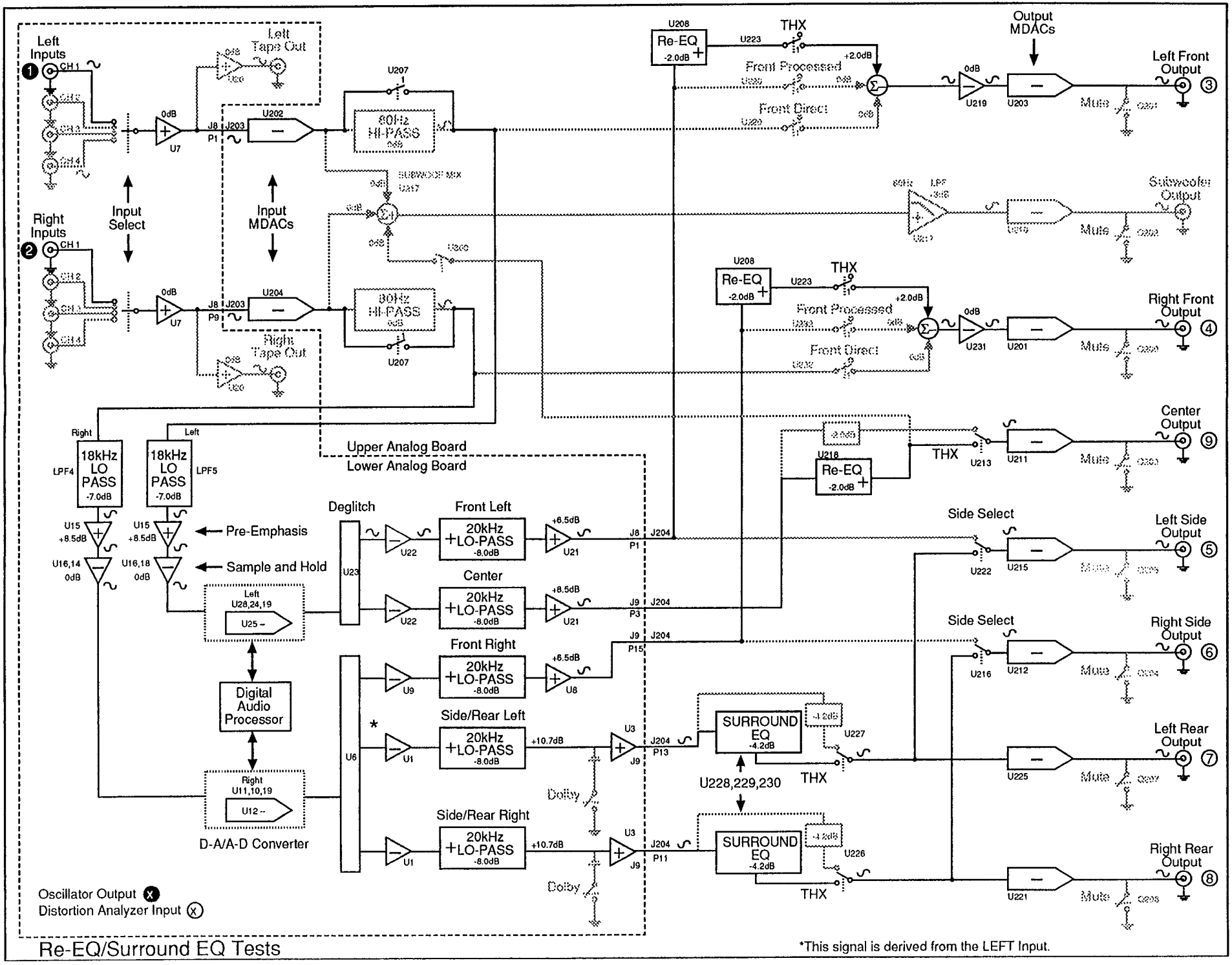


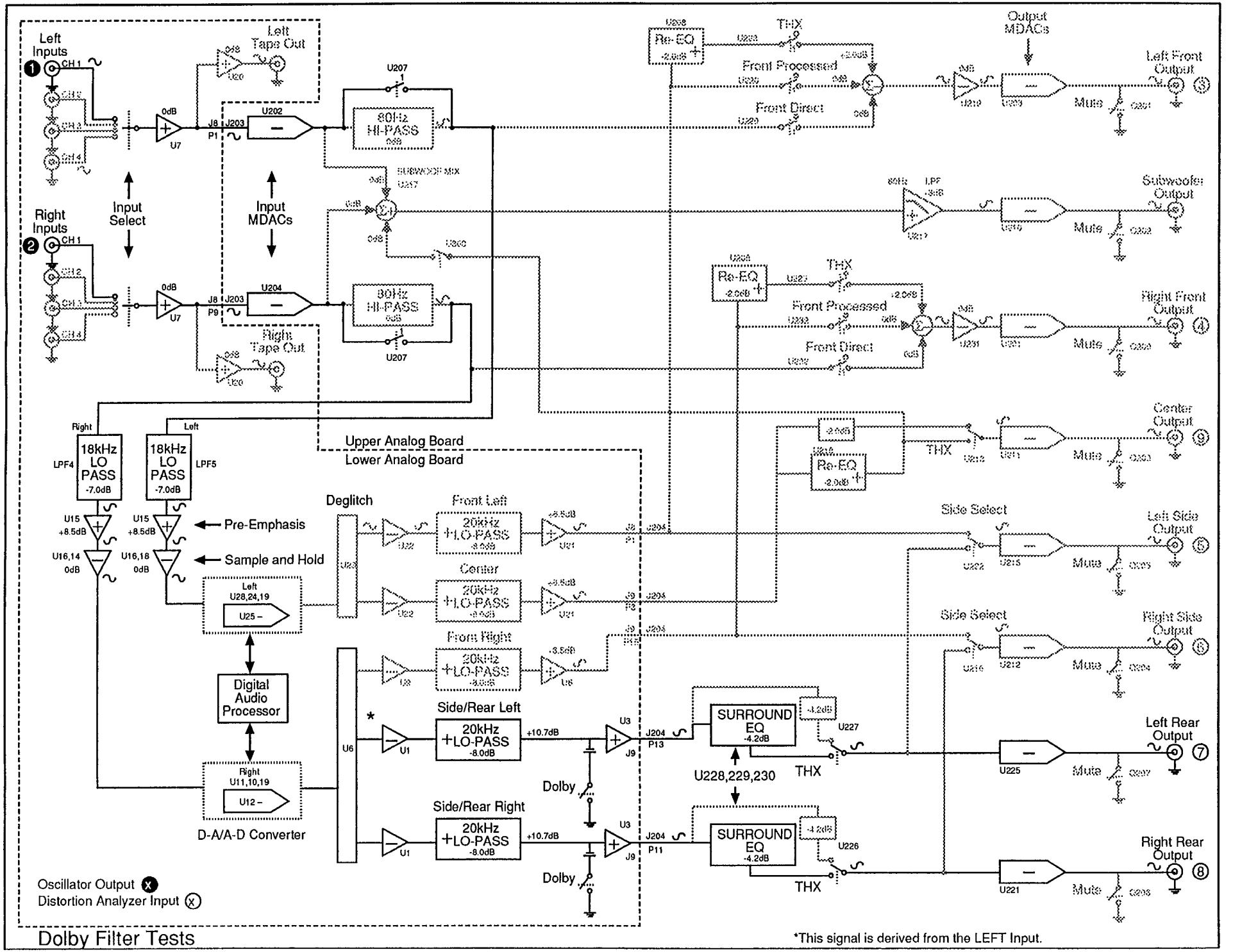
Direct Front Tests

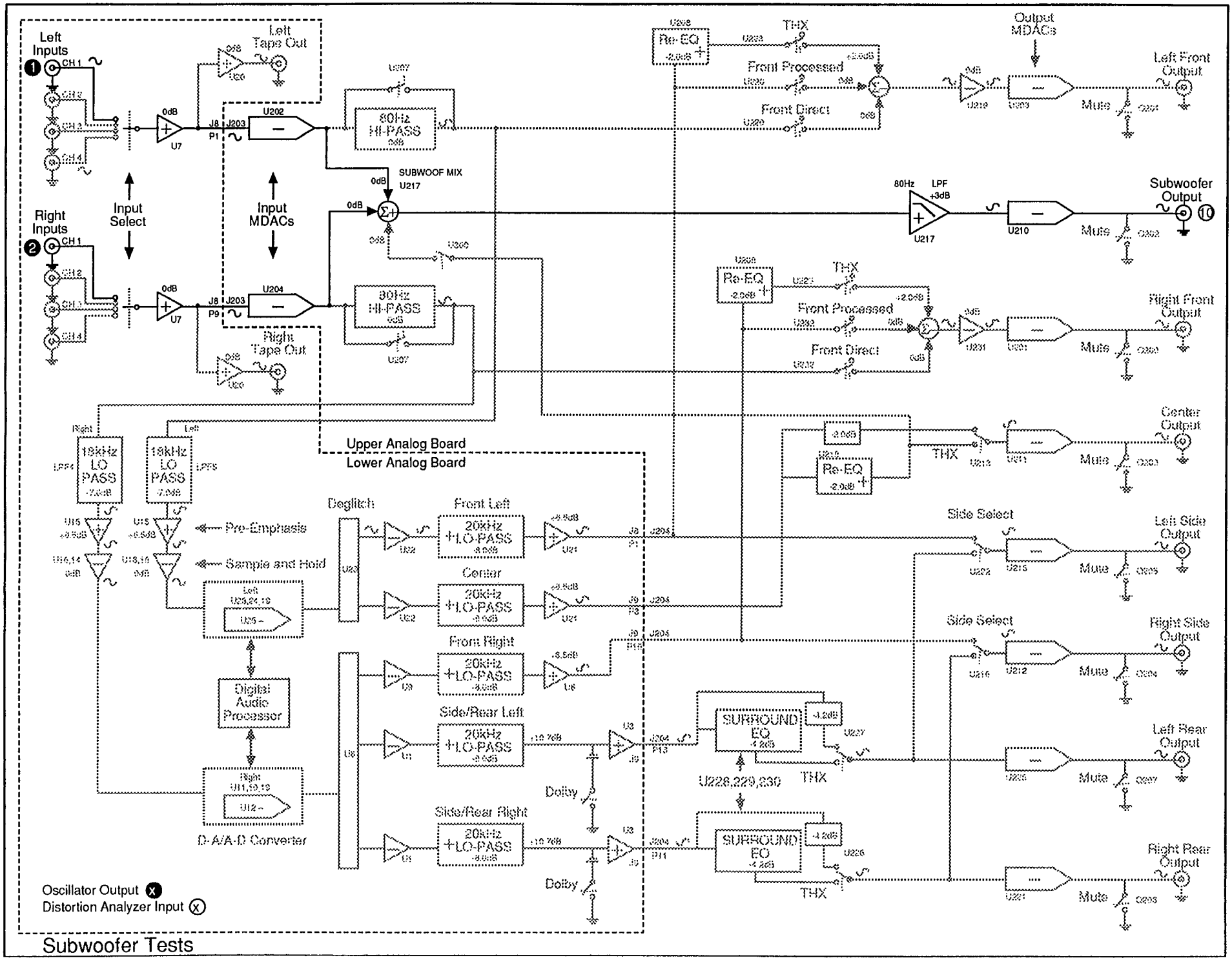


Direct Front with High Pass Filter Tests


Left Inputs
Right Inputs
Input Select
Input MDACs
Left Tape Out
Right Tape Out
Upper Analog Board
Lower Analog Board
Output MDACs
Left Front Output
Right Front Output
Center Output
Subwoofer Output
Left Side Output
Right Side Output
Left Rear Output
Right Rear Output
Front Processed
Front Direct
THX
Re-EQ
Mute
Side Select
Deglitch
Front Left
Center
Front Right
Side/Rear Left
Side/Rear Right
Pre-Emphasis
Sample and Hold
Digital Audio Processor
D-A/A-D Converter
18kHz LO PASS -7.0dB
20kHz +LO-PASS -8.0dB
80Hz HI-PASS
SURROUND EQ
Dolby
Oscillator Output
Distortion Analyzer Input
Processed Output Tests
*This signal is derived from the LEFT Input.


Left Inputs
Right Inputs
Input Select
Input MDACs
Left Tape Out
Right Tape Out
Upper Analog Board
Lower Analog Board
Deglitch
Front Left
Center
Front Right
Side/Rear Left
Side/Rear Right
Pre-Emphasis
Sample and Hold
Digital Audio Processor
D-A/A-D Converter
Re-EQ
THX
Front Processed
Front Direct
Output MDACs
Left Front Output
Right Front Output
Subwoofer Output
Center Output
Side Select
Left Side Output
Right Side Output
Left Rear Output
Right Rear Output
SURROUND EQ
U228,229,230
Oscillator Output
Distortion Analyzer Input
*This signal is derived from the LEFT Input.
Re-EQ/Surround EQ Tests


Left Inputs
Right Inputs
Input Select
Input MDACs
Left Tape Out
Right Tape Out
Upper Analog Board
Lower Analog Board
Pre-Emphasis
Sample and Hold
Digital Audio Processor
D-A/A-D Converter
Deglitch
Front Left
Center
From Right
Side/Rear Left
Side/Rear Right
Dolby
Re-EQ
THX
Front Processed
Front Direct
Output MDACs
Left Front Output
Right Front Output
Subwoofer Output
Center Output
Side Select
Left Side Output
Right Side Output
Left Rear Output
Right Rear Output
SURROUND EQ
Mute
Oscillator Output
Distortion Analyzer Input
Dolby Filter Tests
*This signal is derived from the LEFT Input.


Left Inputs
Right Inputs
Input Select
Input MDACs
Left Tape Out
Right Tape Out
80Hz HI-PASS
SUBWOOF MIX
U217
Output MDACs
Left Front Output
Right Front Output
Center Output
Subwoofer Output
Left Side Output
Right Side Output
Left Rear Output
Right Rear Output
Front Processed
Front Direct
THX
Re-EQ
Mute
80Hz LPF +3dB
Upper Analog Board
Lower Analog Board
18kHz LO PASS
Deglitch
Front Left
Center
Front Right
Side/Rear Left
Side/Rear Right
20kHz +LO-PASS
Pre-Emphasis
Sample and Hold
Digital Audio Processor
D-A/A-D Converter
Dolby
Side Select
SURROUND EQ
U226,229,230
Oscillator Output
Distortion Analyzer Input
Subwoofer Tests

5

Theory of Operation

Analog Circuit Description

Overview

The CP-3 provides simultaneous switching capability for four stereo audio inputs and three composite video inputs. A single composite video output features an on screen display. The associated video overlay circuitry resides on the digital PC board and is described in the digital theory of operation.

Eight audio outputs include left front, right front, center, subwoofer, two sides and two rears. Five outputs are created internally by time sharing two 16-bit digital-to-analog converters (DACs) with Lexicon's own digital signal processor (DSP). Different combinations of the DSP outputs, stereo inputs and various filters are selected for the actual audio outputs. Particular combinations are chosen by the master microprocessor according to the operating mode of the CP-3. Front left and right outputs can be derived either directly from the stereo input or from two separate DSP outputs. The center and rear outputs are created by the other three DSP outputs. Side outputs may come from the front or rear DSP outputs. The output for the subwoofer is a sum of the stereo inputs passing through a 80 Hz low pass filter.

Two PC boards are located in the left hand section (with the CP-3 facing you). This section contains the upper and lower analog PC boards. Note that the signal path alternates between both boards. Referring to the CP-3 block diagram, in the Troubleshooting section of this manual, as well to as the lower and upper analog schematics may be helpful in understanding the analog theory of operation.

Input Select (Lower Bd.,sheet 1)

Four sets of stereo inputs are provided by the CP-3. Two sets of quad RCA jacks are located on the lower analog board next to the rear panel (J2,J6). 100 ohm resistors (R11,20,39,43,55,62,75,76) and 100 pF capacitors (C7,19,24,31,42,53,55,58) are located near each jack which act as a filter for unwanted high frequencies. 1N4148 diodes (CR1-3,5,7-10,13-16,18-21) are back-biased to the analog voltage rails to protect the input circuitry from static charges. In addition, 100K resistors (R8,21,24,40,61,72,73,79) to ground help to avert DC voltages from building up on the inputs or outputs of the analog switches.

Four double-pole single-throw SSM2402 analog switches are incorporated to select the audio input (U2,5,13,17). The SSM2402 has been developed by PMI specifically for audio circuitry. The switches turn on and off gradually which enables them to switch silently. Each switch selects the associated left and right signals of a given stereo input. The switches are controlled by INSEL<0:3>, which comes from the digital board through the upper analog board (J208 to J203), to connector J8 on the lower board. A high logic signal (+5V) on INSEL 0 selects stereo input 1, INSEL 1 selects input 2, INSEL 2 selects input 3 and INSEL 3 selects input 4. In certain cases, such as CALIBRATE mode, all inputs are deselected; that is, INSEL 0-3 are all low.

NOTE: When the CP-3 is powered down, the analog switches will short the signal path to ground, thereby causing the outputs of any equipment hooked to the CP-3's inputs to be loaded by 100 ohms. Normally, this should not cause any problems, as all audio/video equipment used with the CP-3 will be powered down as well. However, if equipment is connected in parallel with the CP-3's inputs, its audio signal may be substantially attenuated while the CP-3 is turned off.

The left and right outputs from the analog switches are connected together, respectively. Each signal feeds one side of a dual op amp (U7). This op amp is configured as a unity gain voltage follower and serves as an input buffer. A FET op amp has been selected to provide high input impedance. The outputs of the input buffers feed the tape out circuitry and go on to connector J203 on the upper board via AC coupling caps (C29,46) and connector J8. These signals are labeled LIN and RIN.

Tape Outputs (Lower Bd.,sheet 1)

A stereo tape output is provided for taping any input source before it is processed by the CP-3. A dual op amp (U20) serves as a unity gain voltage follower for both left and right channels. DC blocking capacitors (C67,71) are incorporated as well as RFI filters (C83,93). A dual RCA jack (J16), located on the lower board near the rear panel, is provided for tape out connections. Note the tape out signals will be the same level as the selected input signals and are not affected by the CP-3's input gain setting.

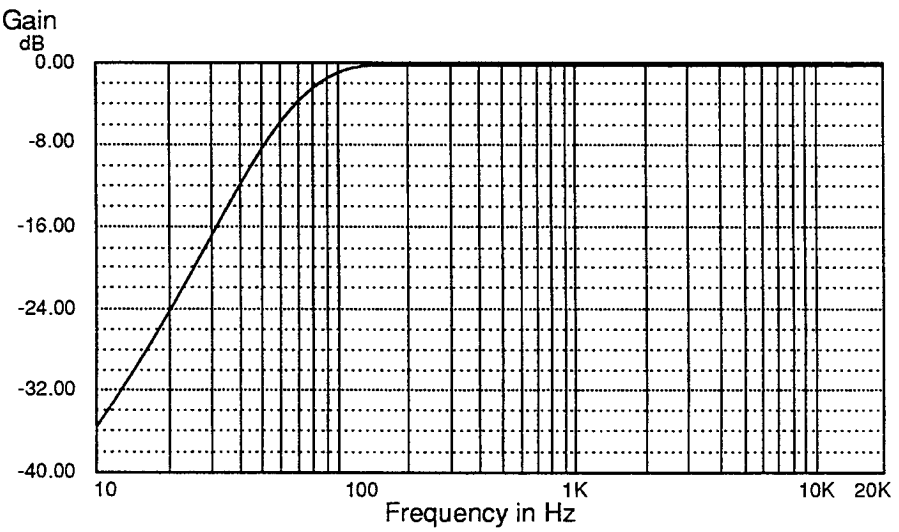
Input MDACs (Upper Bd.,sheet 1)

Two dual MDACs (U202,204) adjust the input level from +12 dB to -18 dB. The MDACs are used with a dual op amp (U205) in an inverting amplifier configuration, with one side of the MDAC's resistor ladder acting as the input resistor and the other as the feedback resistor. In this configuration, it is possible to have between ±48 dB of gain, as well as muting capability. Caps (C207,223) are placed in the feedback loop for compensation.

Left and right signals (LIN, RIN) with their respective grounds enter the upper board at J203, then go into pin 4 of the MDACs. The outputs of the input level adjust stage feed the subwoofer and the 80 Hz high pass filters.

80 Hz High Pass Filters (Upper Bd.,sheet 1)

High pass filters are provided for the left and right signals to roll off low frequencies for speaker systems that may not be able to handle them or that incorporate a subwoofer. Two-pole filters are used with a -3 dB point at 80 Hz and a rolloff of 12 dB/octave. The filters exhibit unity gain at frequencies above 200 Hz. Circuitry includes a dual op amp (U206) with associated components. Poles are determined by a capacitor and resistor combination (Left: C210 & R206, C211 & R204; Right: C233 & R224, C236 & R234). Errors in the filter response will most likely be due to capacitor tolerance; an error window of ±1 dB is necessary for this design.



L/R Input High Pass Filter Frequency Response

An analog switch (U207) bypasses the filter by shorting the output of the input level adjust stage to the non-inverting input of op amp U206. U206 now acts as a unity gain voltage follower. The switch bypasses both left and right signals at once and is enabled (in bypass mode) when HPEN/ is high (+5V).

The outputs of U206 go to other analog switches (U220,232) on the upper board and the anti-aliasing filters on the lower board through connector J203. These signals are labeled LINHP and RINHP.

18 kHz Low Pass Filters (Lower Bd.,sheet 2)

Two 9-pole passive filters are used for removing frequencies above 18 kHz from the left and right signals before the A to D conversion to prevent aliasing. The filters are located towards the middle of the lower board and are enclosed in the larger green packages (LPF4,5). Three resistors are used in conjuction with the filters to produce the desired frequency response (Left: R74,78,82; Right: R59,63,67). The filters have an approximate 7dB loss in the passband.

The signals LINHP and RINHP with their respective grounds come from the upper board to connector J8 on the lower board. LINHP then passes through R78 to LPF5; RINHP passes through R63 to LPF4. The outputs of the filters then go into the non-inverting inputs of dual op amp U15.

Pre-emphasis (Lower Bd.,sheet 2)

Dual op amp U15, along with its associated components, boosts the high frequencies before the A to D conversion. This helps account for the aperture loss due to the conversion process, and also provides pre-emphasis. The time constants for this filter are determined by C63, R81 & R83 for the left channel, and C49, R65 & R66 for the right channel. The gain in this stage is approximately +8.5 dB at frequencies below 2 kHz.

Analog to Digital Conversion (Lower Bd.,sheets 2-5)

The pre-emphasis stages are followed by unity gain track/hold circuits. Each circuit consists of an op amp, two resistors, a capacitor and an analog switch (Left: U18,R84,R85,C59,U16; Right: U14,R68,R69,C54,U16). The analog switches are controlled by the HOLD/ signal. When this signal is high, each circuit "tracks" the input signal level by charging or discharging the capacitor. When HOLD/ is low, the charge on the capacitor "holds" the signal level constant while the analog to digital conversion takes place.

One of two sampling rates is selected according to the CP-3's mode of operation. Ambience, Reverb and Mono Logic modes require 128 program steps which results in a sampling rate of 36.000 kHz. Panorama and all other Surround modes use 112 program steps at a sampling rate of 41.143 kHz. The audio in/out program used in the diagnostic mode also runs at the 41.143 kHz sampling rate. For information about the signals associated with the conversion process, refer to the timing diagrams located at the beginning of the schematics section of this manual.

Signals HOLD and HOLD/ control the analog switches (Left: U28; Right: U11) that set up the DACs for either A to D or D to A conversion. These signals come from the digital board through connector J7 on the lower board. During the A to D cycle, the track/hold outputs are connected to the feedback resistor internal to each DAC and the associated op amps (Left: U24; Right: U10) are set up for 0 volts out.

A to D conversion is performed by the Lexichip (U30 on the digital board), two comparators (Left: U19; Right: U4) and two 16-bit DACs (Left: U25; Right: U12). The left and right DACs' data bus are signified by LDAC<0:15> and RDAC<0:15> and come from the digital board via connectors J4, J7 and J17 on the lower board. LDATA and RDATA are the comparators outputs which leave the lower board at J7. Successive approximation registers (SAR) within the Lexichip are used to write to the DACs during the A to D conversion. The comparator looks at the resultant summation of the input and DAC generated currents. The Lexichip uses this information to reduce this current to zero by setting the DAC value through the SAR that complements the input signal current. This is performed by successively setting each of the 16 bits, starting with the most significant (MSB), while examining the comparator output to see if each bit set results in over- or under-compensating for the incoming signal. If over-compensated, the bit is reset and the next significant bit is tried. If under-compensated, the bit remains on and the next significant bit is set. The maximum signal level for the A to D converter is ±3 volts peak.

Note that only one side of the dual comparators are used to improve performance. Additionally, 2SC3381 dual NPN transistors (Left: Q7; Right: Q3) improve performance by acting as current-to-voltage converters for the comparators' inputs. Trimpots (Left: R120; Right: R60) have been included in

this circuitry to be able to adjust any offsets due to the combination of errors in the DACs, op amps, comparators and transistors used for the conversion process. The procedure for adjusting offsets is included in the Performance Verification and Calibration section of this manual.

Digital to Analog Conversion (Lower Bd.,sheets 3-5)

The DACs (Left: U25; Right: U12) are time-shared for both A to D and D to A conversion cycles. For the D to A cycle, the track/hold outputs are disconnected from the DACs by the analog switches (Left: U28; Right: U11). These switches also connect the op amps' (Left: U24; Right: U10) output to the DACs' feedback resistor as well as its inverting input to the DACs' current output. The op amps then act as current-to-voltage converters for the digital code loaded to each DAC. The maximum output level for the D to A conversion is ±3 volts peak, equivalent to the A to D conversion.

Five separate outputs are generated by the Lexichip, two via the left channel DAC and three via the right channel DAC. The LFrt and RFrt outputs are typically used for the main Left and Right outputs from the CP-3. The left channel DAC also produces CTR, the Center Output. The surround outputs, LSur and RSur, come from the right channel DAC.

The different outputs are created by loading different digital codes from the Lexichip into the DACs at different times. The signals DEG0/, DEG1/, DEG2/ and DEG3/ control the separate deglitch circuits. These signals originate at the digital board and come to the lower board via connector J7. The deglitch circuitry is located on the lower analog board. All are unity gain. Left channel circuitry consists of analog switch U23, dual op amp U22, R110, R115, R119, R124, C79 and C99. Right channel circuitry includes analog switch U6, dual op amps U1 and U9, R41, R42, R10, R17, R35, R36, C33, C9 and C14.

Upon the completion of the A to D conversion, digital codes are written to each DAC by the Lexichip. After allowing 1.3 µS settling time for the DAC and op amp, DEG0/ goes low. This puts the left and right primary deglitch circuits into acquire mode by connecting the output of the current-to-voltage op amp to their respective inputs. These circuits charge their feedback capacitors to the proper level. After 2.4 µS (4.1 µS for 36 kHz sampling rate), DEG0/ goes high and the deglitch circuits hold this level for the rest of the D to A conversion as well as the A to D cycle. At this time, another set of digital codes are written to each DAC for the left and right secondary outputs. 1.3 µS is allowed for the DAC and op amp to settle before DEG1/ and DEG2/ go low. DEG1/ places the left secondary deglitch circuit in acquire mode. After 3.7 µS (5.4 µS for 36 kHz sampling rate), DEG1/ goes high and the signal level is held until DEG1/ goes low in the next D to A cycle. DEG2/ puts the right secondary deglitch circuit in acquire mode for 1.3 S (2.1 µS for 36 kHz sampling rate). At this point, DEG2/ goes low and this signal level is held until DEG2/ goes high in the next D to A cycle. Upon DEG2/ going low, the Lexichip loads a new digital code to the right DAC only. After 1.1 µS settling time, DEG3/ goes low and the right tertiary deglitch circuitry acquires the corresponding signal level. 1.3 µS (2.1 µS for 36 kHz sampling rate) later, DEG2/ goes high and the right tertiary signal level is held until the next D to A cycle.

All five deglitched outputs are followed by equivalent de-emphasis and reconstruction filters. AC coupling capacitors (C74,105,32,1,20) remove any DC components from the signal before it is filtered. De-emphasis filters consist of two resistors and a capacitor (LFrt: R107,R108,C77; Ctr: R117,R118,C104; RFrt: R47,R48,C39; LSur: R7,R16,C6; RSur: R27,R28,C18). The time constant for the de-emphasis filter is different from the pre-emphasis to allow compensation for the high frequency aperture loss caused by the conversion process.

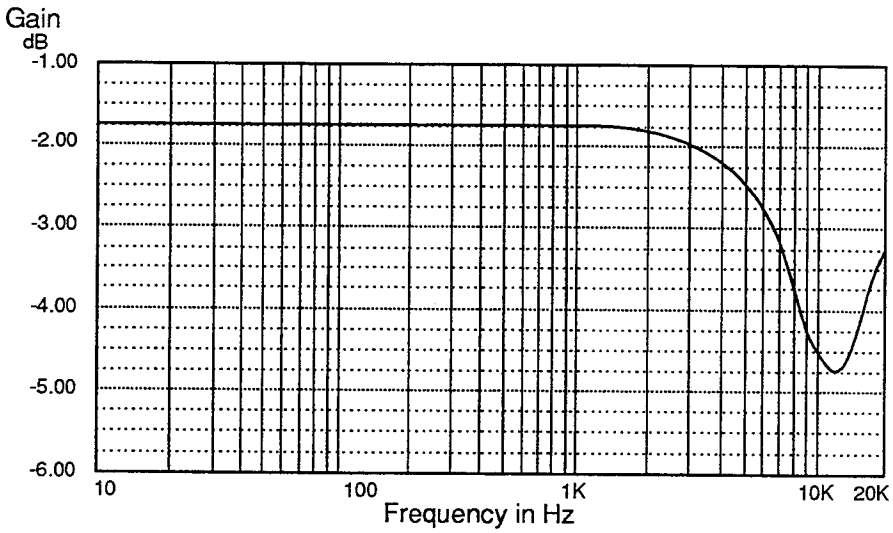
Each de-emphasis filter is followed by a 7-pole passive 20 kHz low pass filter. These filters can be found on the lower board in the smaller green packages. Their function is to smooth out the sample frequency components of the deglitched signals. Two resistors provide the proper input and output termination impedances for the filters. A third resistor is necessary for providing a path between different filter sections. The filter components for the different outputs are LFrt: LPF6,R106,R104,R97; Ctr: LPF7,R116,R123,R125; RFrt: LPF3,R46,R45,R54; LSur: LPF1,R9,R6,R1; RSur: LPF2,R26,R33,R34. The low pass filters attenuate a 1 kHz signal by 8 dB.

Our discussion will now concentrate on each set of outputs separately to avoid confusion and allow for more detailed information.

Left and Right Outputs (Lower Bd,sheets 3,4; Upper Bd,sheets 2,3)

After the 20 kHz low pass filters, the left and right outputs follow identical but separate paths. A non-inverting stage with a gain of 6.5 dB compensates for the loss in the filters (Left: U21,R102,R103,C78; Right: U8,R57,R58,C44). The outputs of these stages (LFrt, RFrt) leave the lower board at J9 and enter the upper board at J204. Here the signals enter analog switches (Left: U220; Right: U232) and the re-equalizer filters.

The re-equalizer filters were designed for the CP-3 to meet the requirements for Home THX Cinema. Their purpose is to roll-off high frequencies to compensate for the flat response associated with home speakers. Movies are usually mixed for theatres which use speakers that substantially attenuate high frequencies. Dual op amp U208 with its associated components acts as the re-equalizer for the left and right channels. The filter consists of two sections: an RC section that gives 3 dB attenuation at 15 kHz (Left: R268,C266; Right: R292,C285), and a bandpass filter (Left: R211,R212,C206,C215; Right: R228,R229,C234,C241). These sections together produce a dip of 3 dB at approximately 8 kHz which flattens out to about 5 dB of attenuation above 10 kHz. In addition, resistor dividers (Left: R213,R214; Right: R230,R231) maintain a gain of -2 dB at 1 kHz. The left and right re-eq outputs drive an analog switch (U223). The response of the re-equalizer is shown in the following figure. An error window of ±0.25 dB is associated with this particular design.



L/C/R Re-equalizer Frequency Response

Three SSM2402 analog switches (U220,223,232) are used to choose the signals that will be routed to the left and right outputs. The choices are the direct input signals (LINHP, RINHP), the left and right primary processed outputs (LFrt, RFrt), and the re-equalized primary processed outputs. Two dual op amps (Left: U219; Right: U231) are configured as summing amps for the three signals from the switches, thereby allowing any combination of the signals to be chosen. The switches are closed by a +5 volt control signal and opened with 0 volts. The control signals (FDIREN, FPROCEN, REQEN) from the digital board arrive at J208 on the upper board. FDIREN controls the LINHP and RINHP signals, FPROCEN controls the LFrt and RFrt signals, and REQEN controls the re-equalized signals. Note that there is no case in any of the CP-3s operating modes where FPROCEN and REQEN are simultaneously enabled.

The summing amps use different input resistor values to help correct gain imbalances between the direct, processed and re-equalized signals. The direct signals are boosted by 0.4 dB (R266,290). The processed signals pass at unity gain (R265,289). The re-equalized signals are boosted 2.9 dB (R267, R291) to account for the loss through the filters.

The other side of dual op amps U219 and U231 correct the phase inversion from the summing amps and pass the LFOUT and RFOUT signals at unity gain. These signals are then fed through AC coupling caps (C216,205) to the output level adjust MDACs and the RCA jacks (J200) labeled "LEFT" and "RIGHT" on the rear panel.

Center Output (Lower Bd.,sheet 3; Upper Bd.,sheets 2,3)

After passing through its 20 kHz LPF, the Center output (Ctr) is boosted by 8.5 dB through one side of U21. Ctr then passes from J9 on the lower board to J204 on the upper board where it goes to the center channel re-equalizer circuitry as well as a voltage follower.

One side of dual op amp U218 is part of the re-equalizer circuitry required for Home THX Cinema. [A more detailed explanation of the re-equalizer is contained in the left and right outputs description. Its response is shown in the preceding figure.] Here R241, R242, C249 and C251 create a bandpass filter, R236 and C238 create a 15 kHz low pass filter, and R243 and R244 act as a voltage divider. This divider attenuates the signal by approximately 2 dB. The output of this divider goes to the non-inverting inputs of U218. The other side of this op amp is set up as a unity gain voltage follower. Its output and the re-equalizer output go to a single-pole double-throw analog switch (U213). This switch is controlled by REQEN, a control signal from the digital board that appears on the upper board via J208. When REQEN is high the re-equalized signal is passed through the switch, otherwise the Ctr signal is chosen. The output of the switch (CTROUT) goes through an AC coupling capacitor (C243), on to the output level adjust MDAC, and to the RCA jack labeled "CENTER" on the rear panel.

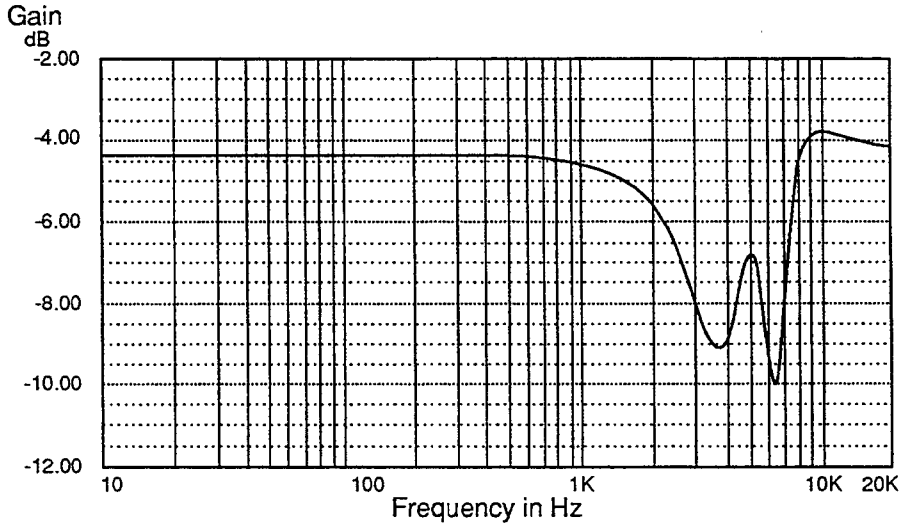
Side and Rear Outputs (Lower Bd,sheets 4,5; Upper Bd,sheets 2,4)

The Left and Right Surround channels are typically used for both side and rear outputs from the CP-3. After passing through respective 20 kHz low pass filters, they enter opposite non-inverting inputs of a dual op amp (U3). This op amp provides 10.7 dB of gain. In addition, a capacitor in series with a FET switch to ground (LSur: C2,Q1; RSur: C26,Q4) acts as a pole for the Dolby B filter. This pole is created by the total resistance of the low pass filter and its source resistor when the capacitor is shorted to ground through the FET. The signal DOLBYEN/ signifies that the Dolby B filter is activated when low. Originating on the digital board, this signal passes through J208 to J204 on the upper board, to J9 on the lower board. DOLBYEN/ goes to a level shifter circuit (Q2,R12-R15,C8) through R12. Normally, DOLBYEN/ is high, which turns off Q2 and puts -15V at its collector and the signal, DOLBYEN, which turns off the FETs. When Dolby is active, DOLBYEN/ is low, which turns on Q2, putting DOLBYEN at about +1.5 volts which turns on the FETs. Because the Dolby B Noise Reduction filter is dynamic, with its characteristics changing with signal level, the majority of the filter is created by DSP.

The outputs of U3 (LSur, RSur) pass from J9 on the lower board to J204 on the upper board. Here RSEC and RTER go to the surround equalizers as well as separate voltage dividers (LSur: R297, R298; RSur: R275, R276). The dividers attenuate the signals by about 4 dB to complement the attenuation of the surround equalizer filters.

The surround channels have different requirements per the Home THX Cinema standard. The chief reason for the surround equalizer is to compensate for human hearing which is different for sources coming from the front of the listener than those from the sides. A secondary reason is to compensate for the flatness of home speakers, similar to the reasoning behind the re-equalizers. The surround equalizer acts on frequencies above 1 kHz. It includes a -5 dB dip at 3.8 kHz, a -2.5 dB peak at 5.5 kHz, and another -5 dB dip at 6.3 kHz. The surround equalizers include three dual op amps

(U228,229,230) with their associated circuitry. Three bandpass filters are constructed for each channel of equalization, which include voltage dividers to determine the proper amount of gain/attenuation. The first stage (U230) contains a notch filter centered at 6.3 kHz (LSur: R284,R285,C283,C290; RSur: R311,R312,C303,C307) and a divider with 0.6 dB attenuation (LSur: R286,R287; RSur: R313,R314). The second stage (U229) includes a filter with a peak at 5.5 kHz (LSur: R281-R283,C282,C284; RSur: R308-R310,C302,C306). The third stage (U228) provides a filter with a dip at 3.8 kHz (LSur: R277,R278,C281,C289; RSur: R304,R305,C301,C305) as well as a divider with an attenuation of 3.6 dB (LSur: R279,R280; RSur: R306,R307). All three stages add together to create the required response for the surround equalizers, which is shown in the figure below. This particular filter design has an error band of ±1dB.



Surround Equalizer Frequency Response

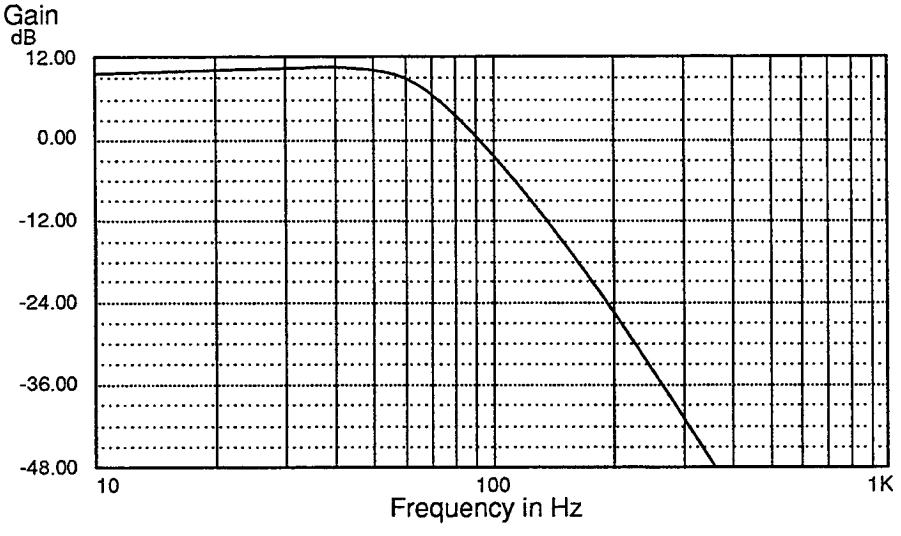
The outputs of the surround EQs (LSurEQ, RSurEQ) go to separate single-pole double-throw analog switches (U226,227). U227 selects either LSur or LSurEQ for the left rear and/or side outputs. U226 selects either RSur or RSurEQ for the rear and/or side outputs. The signal THXEN, which comes from the digital board via J208, is used to control the analog switches. When THXEN is low, LSur/RSur are selected; when THXEN is high LSurEQ/RSurEQ are selected.

The outputs of the switches go to the output level adjust MDACs and mute circuitry for the rear channels via AC coupling caps (C276,291). The signals exit the rear of the unit at the RCA jacks (J205) labeled "REAR". These signals also feed another pair of single-pole double-throw analog switches (U216,222). These switches select either the front processed (LFrt, RFrt) or rear outputs for the sides. SIDESEL is the control signal for these switches and comes from the digital board via connector J208. When SIDESEL is high, LFrt and RFrt are used for the side outputs; with SIDESEL low, the side outputs will be the same as the rear outputs. The outputs of the side select switches go via AC coupling caps (C255,265) to the output level adjust MDACs and mute circuitry for the side outputs. The side outputs appear at the rear of the unit at RCA jacks (J205) labeled "SIDE".

Subwoofer Output (Upper Bd.,sheets 1,3)

All subwoofer circuitry is located on the upper board. The left and right signals are summed together after the input level adjust MDACs through R259 (LINB) and R262 (RINB). Dual op amp (U217) is used for summing the signals and creating the necessary low pass filter. In addition to left and right, the re-equalized center signal may also be used for the subwoofer. An analog switch (U300) controls the summing node for CTREQ at R260. CTREQ is used to pass the CP-3's internal noise to the subwoofer during calibration only. The analog switch is enabled when all inputs are deselected, or logic level low, which occurs only during calibration. INSEL0 through INSEL4 are ORed together (U301) to provide this control.

The subwoofer filter is designed per Home THX Cinema specifications to be 6 dB down at 80 Hz with a 24 dB/octave rolloff. C246, C248, C269 and C270 along with the associated resistors provide the filter characteristics. The design allows for a error window of ±2 dB. The output of U217 (SUBOUT) passes through an AC coupling cap (C230) to the output level adjust MDAC and mute circuitry for the subwoofer. The signal goes to an RCA connector (J200) on the rear panel labeled "SUBWOOFER".



Subwoofer Output Frequency Response

Output MDACs (Upper Bd.,sheets 3,4)

Dual MDACs (U201,203,210,211,212,215,221,225) are used with dual op amps (U200,209,214,224) to provide adjustment of the output levels from +15 dB to -48 dB. All components are located towards the rear of the upper analog board. Each dual MDAC is used with one side of a dual op amp in an inverting amplifier configuration, with one side of the MDAC's resistor ladder acting as the input resistor and the other as the feedback resistor. In this configuration, it is possible to have between ±48 dB of gain, as well as muting capability. 18 pF caps (C203,218,231,244,257,268,278,294) are placed in the feedback loop for compensation.

Both input and output level adjust MDACs share an 8-bit data bus. Their CS and WR pins are used for addressing the appropriate channel, while A/B selects the respective side of each dual MDAC. For more information concerning the addressing of the MDACs, see the Digital Circuit Description.

Output Mute Circuitry (Lower Bd,sheet 5; Upper Bd,sheets 3,4)

The muting and protection circuitry is virtually identical for all outputs. A 390 ohm resistor in series with the output of the op amp is followed by a FET (Q200-207) to ground. Turning this FET on shorts the output signal to ground, thereby muting the output. The gate of the FET is AC coupled to its drain to enhance performance for large positive and negative signals. A pair of diodes back-biased to the voltage rails protect the CP-3 from high voltages due to improper termination of its outputs. In addition a series capacitor with a resistor to ground prevent any DC bias from appearing at the CP-3's outputs. A 100 ohm series resistor limits the current for the protection diodes, and also acts as an RFI filter with a 100 pF cap to ground.

The muting FETs are controlled by the signal OUTMUTE which appears on the opposite side of a 470k resistor in series with the gate. This signal comes from the lower board via connectors J8 and J203. The output mute drive circuitry can be found at the right front corner of the lower board.

Upon power up, the gates of the FETs are at 0 volts which means they are on and the outputs are muted. The emitter of Q5 rises with +15 volt supply through CR23. Meanwhile, C120 is being charged through current-limiting resistor R113, and C61 is being charged slowly through R94 and R95. Q5 turns on when the +15 volt supply is approximately 1.5 volts above ground. The collector voltage (OUTMUTE) follows the emitter voltage so a positive voltage is applied to the FETs, which keeps them turned on and the outputs muted. Eventually, C61 becomes fully charged, which turns Q5 off. At this point, OUTMUTE goes to -15 volts and turns off the FETs, unmuting the outputs. R112 and C84 inhibit high frequency transients that may turn off the FETs while powering up.

When powering down, C61 discharges quickly through CR25 to the falling +15 volt supply. This turns Q5 on when the supply has dropped about two volts. Q5's emitter remains positive due to the back-biasing of CR29. Its collector (OUTMUTE) goes positive which turns the FETs on and mutes the outputs. OUTMUTE remains positive while C86 discharges through R113, which keeps the FETs on until the CP-3 is fully powered down.

The muting circuitry may also be controlled by the microprocessor through MUTE/, which comes from the digital board via connector J7. Assuming the unit is already powered up, a high level (+5V) MUTE/ will turn Q8 on and Q6 off. As C61 becomes charged, Q5 turns off. OUTMUTE is pulled to -15 volts very quickly through R112 which turns off the FETs and unmutes the outputs. When MUTE/ goes low (0V), Q8 turns off and Q6 turns on. C61 discharges rapidly through CR26 and Q6, turning Q5 on. OUTMUTE goes positive which turns on the FETs and mutes the outputs.

Analog Power Supply (Lower Bd,sheets 2,5; Upper Bd,sheet 5)

Regulation for the analog power supplies is provided on the lower analog board for better performance and noise immunity. The unregulated ±15 volt supplies come from the power supply board and enter the lower board at connector J19. C95 and C101 provide a path for unwanted high frequencies to return to the power supply before entering the analog world. 7815 and 7915 type voltage regulators in TO-220 packages provide the necessary regulation and protection for the analog supplies. They are heat sinked to the chassis by a separate piece of aluminum. Capacitors C87, C88, C94 and C96 provide local filtering while CR29 through CR32 protect the voltage regulators from high voltage spikes and from becoming reverse-biased. A cable brings the regulated ±15 volt supplies to the upper analog board.

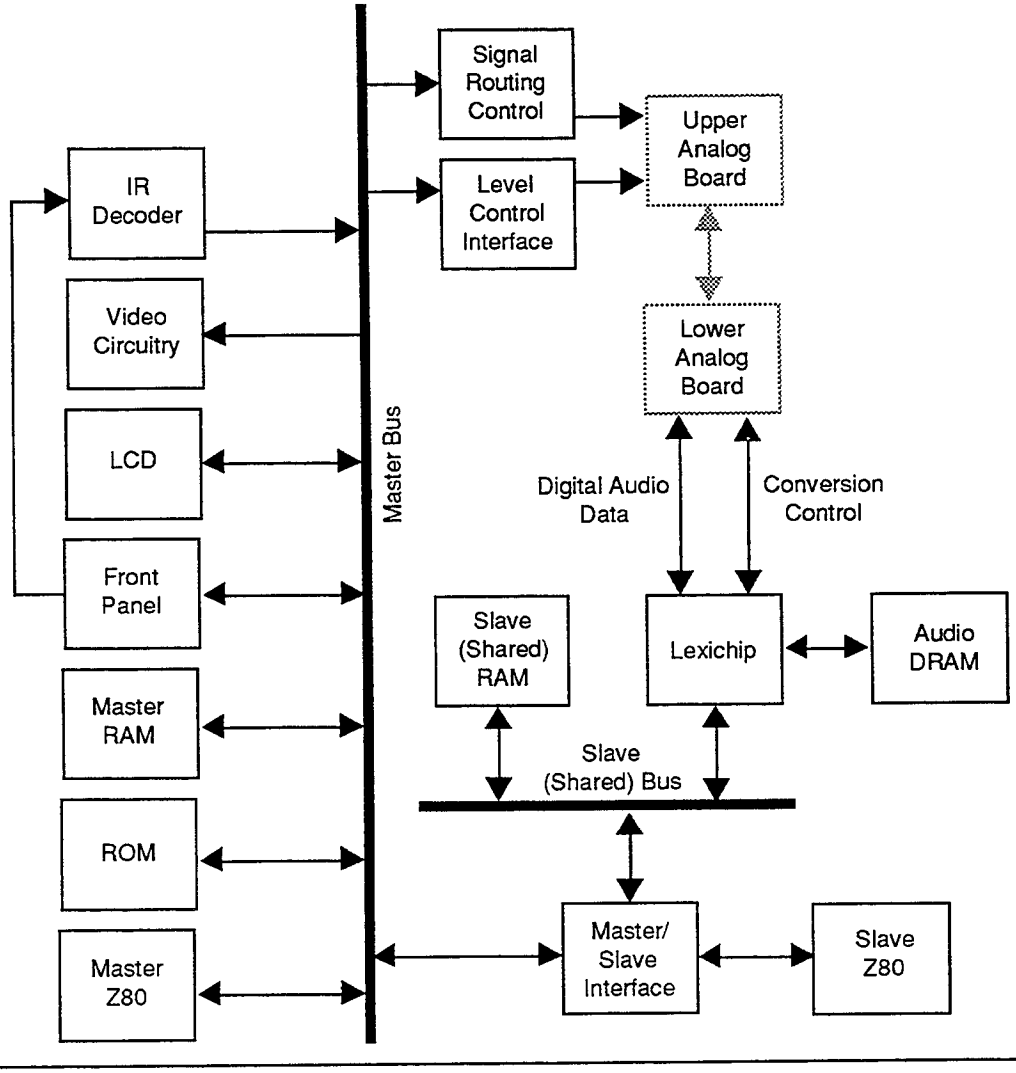
The ±15 volt supplies are additionally filtered by 47 µH chokes for the conversion circuitry (±15VCL, ±15VCR). Separate filters are used for the left and right channels. Some of the analog switches require separate voltage rails. +5VA is created by a 1N751 zener diode (CR33) with R126 and C106. It is used by the 74HC4053 and DG444 analog switches. In addition, -3.9VA is created by a 1N748 zener diode (CR17) and R71, C50 and C52. -3.9 volts is used by the 74HC4053s. On the upper analog board, +5VB is created by a 1N751 zener diode (CR204), R217 and C221. +5VB is used for the DG419 analog switches.

Digital Circuit Description

Overview

The CP-3 Digital board contains both digital and video circuitry. Both, therefore, will be discussed in this section. The CP-3 utilizes two Z80 microprocessors (Master and Slave) and the Lexichip Digital Signal Processor (DSP) to perform multiple digital audio effects. These effects are controlled via the front panel user interface or the Standard/Expanded remote controls. Each Z80 processor has it own support circuitry, data and address busses. Although each processor is capable of running independently, the Slave is dependent on the Master Z80 to load programs into the Slave RAM. The Master also has control over the Slave's RESET/ signal. In addition to accessing Slave (or Shared) RAM, the Master Z80 can access the Lexichip Writable Control Store (WCS) through the Master/Slave interface. The Slave processor can access only the Slave RAM and the Lexichip. A block diagram of the CP-3 digital circuitry is shown below.

CP-3 Digital Circuitry Block Diagram



During normal operation, sampled audio is converted into digital data by successive approximation A/D converters. Digital effects processing is performed by the Lexichip under the control of both Master and Slave Z80 processors. The Lexichip controls not only the effects processing, but also the Analog-to-Digital and Digital-to-Analog conversions. The Master Z80, which handles all operator I/O and housekeeping functions, is able to pass DSP control information to the other two processors. The Slave Z80 is dedicated to the task of controlling the Lexichip and is, therefore, used to perform any DSP control functions which require precise timing.

The CP-3 Digital board has four layers, with +5V and GND on the internal two layers. On-Screen Display (OSD) video circuitry is also located on the Digital board (adjacent to the rear panel). To prevent the introduction of noise to the video signal from the digital circuitry, power to the video circuitry is fed directly from a Power Supply board via ferrite beads to the video circuitry.

Unless otherwise noted, all schematic references in this section refer to SCHEM DIGITAL BD,CP-3 sheets 1-7, 060-08135, included in the last section of this manual. Sheet number and location of areas of interest within the schematic are referenced parenthetically where appropriate.

Master Z80

The Master Z80 (U24, 1/D7) handles basic system control and user I/O operation. It can write program code and data directly to the Slave Program RAM (U35, 3/D4) and to the Lexichip WCS (U30, 4/B7) via the Slave (shared) Z80 bus and the Master / Slave interface. The Master Z80 controls:

- User data input from the front panel or from either of the two remote controls
- LCD, Video Overlay and LED operations
- Volume control
- Audio- and video signal paths
- Audio muting hardware
- Maintenance of non-volatile, user-controlled registers
- Loading and manipulation of Slave processor program code and data
- Control of Slave processor reset
- Processing data and instructions to and from the Lexichip

Master Z80 Addressing

The Master Z80 can access up to 64K of memory. It can also access other peripherals in I/O mode. The Master Z80 addressing organization is shown in the following tables; decoding will be discussed in later sections.

Address (hex)	Size	Signal	Description	Slave/Master Sharing
0000 - CFFF	52K	ROM/	ROM select	No
D000 - D3FF	1K	MDAC/	MDACs + Audio routing select	No
D400 - D7FF	1K	LEX/	Master access to Lexichip	Yes
D800 - DFFF	2K	N/A	Not used	N/A
E000 - EFFF	4K	SLVRAM/	Master access to Slave RAM	Yes
F000 - FFFF	4K	RAM/	Master RAM	No

Master Z80 memory addressing

Address (hex)	Signal	Description
00	ROWSEL	Front panel LED Row Select write port
01	COLSEL	Front panel LED Column Select write port
02	KEYSTAT/	Front panel switch read port
03	CONTRAST/	LCD Contrast control write port
04	VIDEO/	Video overlay data & control write port
05	MSYNC/	Master/Slave Synchronization write port
07	IRD/	Infrared remote read port
06	LCDEN/	Write to LCD instruction register
16	LCDEN/	Read LCD instruction register
0E	LCDEN/	Write to LCD character register
1E	LCDEN/	Read LCD character register

Master Z80 I/O addressing

System Reset

The reset circuitry insures proper operation of the CP-3 during power up and down by holding the reset signals low while the power rails are stabilizing. There are three different reset signals generated on the Digital board: LRST/ , ZRST/ and SRST/.

LRST/ and ZRST/ are generated by the SYSTEM RESET circuitry (1/A7), of which there are currently two versions. On Digital boards marked rev 3 (or lower), reset is triggered by the regulated +5 V. On boards higher then rev 3, reset is triggered by the Power Fail (PFAIL/) signal generated by the Power Supply board .

LRST/ (Lexichip reset) is generated by two inverting Schmitt Triggers (U39, 74HC14), R69 and C65 (1/A6-8). During power up C65 starts charging through R69. LRST/ will be kept low until C65 reaches the triggering level of 74HC14 (U39). Where PFAIL/ triggers reset, C65 is discharged rapidly through CR16 at power down to ensure that the reset signal is asserted before the +5 V rails go out of regulation.

ZRST/ (Z80 reset) is the main reset signal. This signal initializes the majority of the system. ZRST/ resets the Master Z80 and clears the output ports. To prevent the system from booting during Lexichip initialization, ZRST/ is delayed by R65 and C57 during power up until LRST/. Where PFAIL/ triggers reset, CR17 ensures rapid discharging of C57 during power down , assuring rapid ZRST/ assertion .

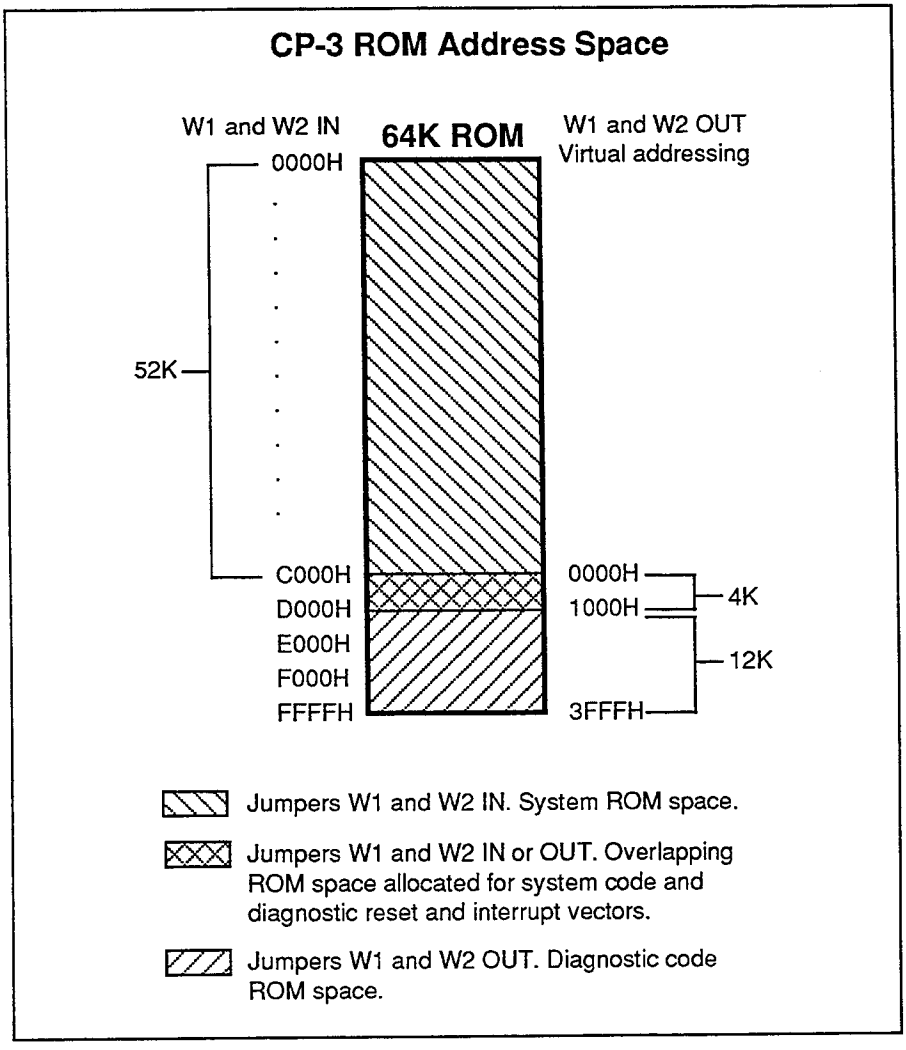
SRST/ (Slave Reset) is generated at the LCD Contrast port (U37, 2/C4) and controlled by the Master Z80. U37, which is a D Flip-Flop with Clear (74HC174), is cleared during power up by ZRST/. This means the Slave Z80 will be in a reset state until the Master Z80 removes the SRST/ signal. The port is I/O mapped at address 03H. MDB5 controls the SRST/ signal. (See Front Panel Liquid Crystal Display (LCD).

ROM

The ROM (U25 1/D6) is a 64K EPROM (27C512) connected to the Master Z80 bus and allocated the address space 0000H -CFFFH. The ROM cannot be accessed by the Slave Z80. Decoding for the ROM/ signal is done by U13 (1/B7) — a GAL16V8.

The CP-3 System code is located at ROM address 0000 - CFFFH, with the exception of the space between C000 and C08FH which is allocated to diagnostic RESET-, INT- and NMI- vectors.(See Diagnostics.)

The Diagnostic code is located at D000 - FFFFH. Because this space is allocated to other parts of the system, two jumpers, W1 and W2, (1/D6) have been added. Removing these two jumpers disconnects the ROM's two most significant address bits (A14 and A15) from the Master Z80 address bus. When the jumpers are removed, these two bits are pulled high through R43 and R45, allowing the Master Z80 to access the remaining physical ROM address space (C000 to FFFFH) as address 0000 - 3FFFH. It is important to note that C000 - CFFFH is overlapped. As this area is dedicated to the System code, the virtual address space for the Diagnostic code is 1000 - 3FFFH. Other addressing is unaffected as the jumpers affect only the ROM.



This figure shows how the physical ROM space is split between the Diagnostic and System code. Shared space is used by the System code, except C000 - C08FH which is reserved for Diagnostic code Reset- and Interrupt- vectors.

Master RAM

The Master RAM is an 8K low power 6264 CMOS RAM (U33, 1/D4), used for system variables and stack pointers. To allow more ROM space, only 4K of the 8K are accessible by the Master Z80. The Master RAM Address space (F000 - FFFFH) can only be accessed by the Master Z80. Battery backup circuitry provides protection of non-volatile data in the Master RAM when the CP-3 is powered down. Decoding for the RAM/ signal is done by U13 — a GAL16V8.

Memory Battery Backup

The battery backup circuitry (1/D2-4), transistor Q10, diodes CR8, CR9, CR12 and battery BAT1, provide protection of the non-volatile memory (U33, Master RAM). When the regulated 5V supply drops below a certain level Q10 turns off to allow battery BAT1 to provide backup power to the Master RAM. Zener diode CR8 (3.9V 1N748) sets the limit at which Q10 turns off. Schottky diodes CR9 and CR12 prevent current from flowing the wrong way. R83 provides extra protection for the battery in the event of CR12 malfunction.

Master RAM Protect

The Memory protect circuitry (1/A5-A4) is designed to protect the data in the Master RAM (U33), during power up or down cycles by pulling down the CE2 pin on U33 to disable the chip. This circuitry is controlled by two signals, ZRST/ (1/A6) and PFAIL/ (Schem 060-08142 Power Supply 1/A3). ZRST/ is the power on/off reset signal and PFAIL/ is generated on the Power Supply board when power failure is detected. The protect circuitry consists primarily of transistors Q9, Q11, Q12 , a few resistors and one capacitor (C63). It functions somewhat like a two-input AND gate.

During power up, ZRST/ stays low until the +5V rails stabilize. While ZRST/ is low, Q9 is off. This turns Q11 off, causing the output, PROT/, to go low. This means that PROT/ stays active low as long as ZRST/ is active low. Normally, PFAIL/ goes high very early during power up, turning on Q12. When the Power Fail circuitry detects power failure PFAIL/ goes low, turning off Q12 and causing PROT/ to go low as C63 discharges through Q11 and R67.

The PROT/ signal(1/A2) also goes to the video section (6/D8, 5/D8), where it determines whether the incoming video signal goes to the video circuitry or is hard wired straight to the video output. (See On-Screen Video Display for more information.)

IR Remote Control Circuitry

The InfraRed (IR) decoder circuitry (2/C5-7) receives a serial bit stream from the front panel IR detector. The actual decoding is done by U23 (2/C7) — a Sharp LU59002 which converts the serial bit stream to parallel data. The decoder is connected to the Master Z80 data bus through the IR Buffer (U31, 2/C6) — a 74HC541 Octal Tri State Buffer.

IR Decoder Interface

The decoding for the IRD/ select signal is done by U15 (1/B7) — a 74HC138 3-to-8 Line Decoder. The IORQ/ and M1/ signals, in association with MADR<1:3>, determine the decoding. IRD/ will go active low when the Master Z80 performs an I/O request to address 07H. In that case, the IR Buffer (U31, 2/C6) opens to allow the Master Z80 access to the parallel data from the IR decoder. The following table shows the functionality of the data bits in the IR remote read port.

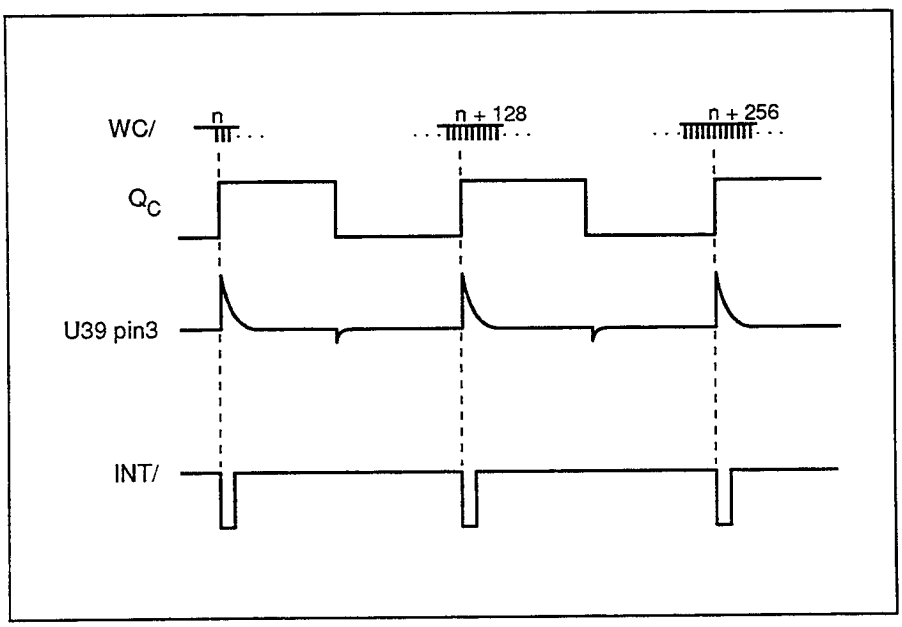
Data bit	Signal	Function	Active state
MDB<0:5>	PD<0:5>	Encoded IR remote buttons	Button dependent
MDB6	PD6+PD7/	IR CP-3 code detect	0
MDB7	VIDDET	Video input detect	1

IR Remote Control port data bits

IR Receiver Interrupt Timer

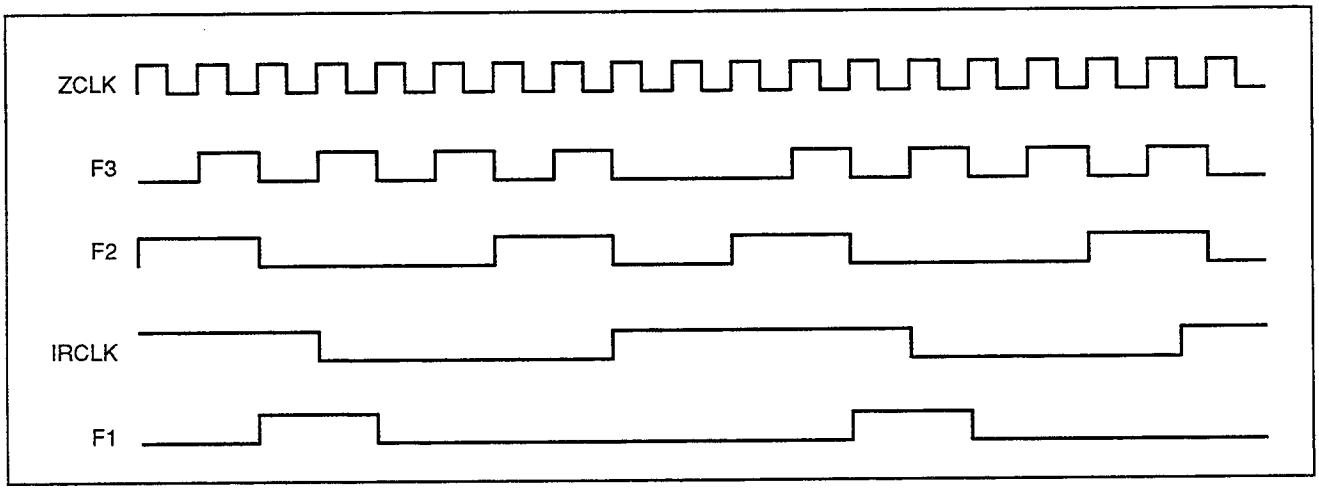
The IR Receiver Interrupt Timer circuitry (2/D6-D4) generates the interrupt pulses (INT/, 2/D3) for the Master Z80. The INT/ signal is connected to the Master Z80 Interrupt.

This circuitry is driven by the Lexichip Word Clock signal (WC/, 4/A2). WC/ is a pulse signal which appears at the same frequency as the sampling rate for the audio signal. The frequency of the WC/ signal will, therefore, vary depending on which program the CP-3 is running. All of the Ambience and Reverb programs and the Surround program: Mono Logic run at a 36 KHz sample rate. The Panorama programs and the remaining Surround programs run at a 41.143 kHz sampling rate. WC/ is run through U41 (2/D6), which is a 74HC393 dual 4-bit binary counter. There, the frequency is divided by 128, resulting in an INT/ signal frequency of 281.25 Hz (3.56 ms), or 321.43 Hz (3.11 ms) ,depending on which program is running. After the frequency division the signal has 50% duty cycle. The signal is then sent through pulse shaping circuitry (C66, R70, R80, CR15 and U39; 2/D4) which shortens the INT/ pulse width.



Signals associated with the IR Receiver Interrupt Timer

IR Decoder Clock The clock signal, IRCLK (3/B5) for the IR decoder chip (U23), is generated by U16 (3/B5) — a 16V8 GAL. This is done by using the ZCLK signal and dividing it by 10, which results in IRCLK frequency of 461 KHz.



IR Decoder The CP-3 Infrared remote control system uses the Pulse Position Modulation (PPM) system for 15-bit serial signals.

The IR decoder (U23) receives coded 15-bit data from the IR receiver. The 15-bit data can be considered as having 5 sections: system address, data code, data expansion bits, mask bit and data judging bit.

IR Receiver The IR detecting unit in the CP-3 is a SHARP GP1U521X with band pass filter for 38 kHz located on the Front Panel pc board . This detector senses modulated signals from the IR remote controls and converts them into a serial bit stream.

IR Remote Controls The CP-3 utilizes two remote controls: the Expanded remote for setting up and adjusting the system, and the Standard remote for simple daily operation.

Although these remotes differ in appearance (see Owner's Manual) they are built with identical circuitry and they both send the same code, with the exception of the codes for ON/OFF. The CP-3 system software differentiates the two remotes by sensing which remote is used to turn the CP-3 on.

MDAC Interface

The MDAC (Multiplying Digital Analog Converter) interface (1/B4) consists of an Octal Tri-State Buffer (U2, 74HC541), a 3-8 Line Decoder (U12, 74HC138), two OR gates (U14, 74HC32) and an inverter. This interface enables the Master Z80 to write data to the MDACs located on the upper analog board. By writing different values to the MDACs the Master Z80 is able to control the level of the incoming and outgoing processed audio signals.

MDAC Decoding

The MDAC/ enable signal is generated by U13 (1/B7) — a 16V8 GAL. It activates the MDAC Gain Buffer (U2, 1/B3), thereby giving the Master Z80 access to the MDAC data bus. The MDAC/ signal, in conjunction with MWR/ and MADR<0:4>, determine which MDAC is written to.

The A/BSEL signal is generated by the MDAC/ signal and MADR0 by ORing them together with an OR gate (U14, 1/C3). It selects which MDAC, A or B, within each MDAC chip (AD7628) is written to. A/BSEL active low selects the A MDAC. The LEFT/ and RIGHT/ (sometimes called LEFT) signals are generated by ORing (U14), the MDAC/ and MADR1 signals. The RIGHT/ signal is the LEFT/ signal inverted by U4 (1/C3). These signals generally select the left or right audio channels. The left and right input MDACs are selected together (their CS/ signal is permanently tied low). The center and subwoofer channels are selected by LEFT/ and RIGHT/, respectively. The NWR/, CTRWR/, FWR/, SWR/, and RWR/ signals are generated by U12 (1/B3), which is a 3-8 Line Decoder.

MADR<0:4> A4 A3 A2 A1 A0	ADDRESS	DESCRIPTION
0 0 0 1 0	D002H	Left and Right inputs A MDACs
0 0 0 1 1	D003H	Left and Right inputs B MDACs
0 0 1 0 0	D004H	Center A MDAC
0 0 1 0 1	D005H	Center B MDAC
0 0 1 1 0	D006H	Subwoofer A MDAC
0 0 1 1 1	D007H	Subwoofer B MDAC
0 1 0 0 0	D008H	Left Front A MDAC
0 1 0 0 1	D009H	Left Front B MDAC
0 1 0 1 0	D00AH	Right Front A MDAC
0 1 0 1 1	D00BH	Right Front B MDAC
0 1 1 0 0	D00CH	Left Side A MDAC
0 1 1 0 1	D00DH	Left Side B MDAC
0 1 1 1 0	D00EH	Right Side A MDAC
0 1 1 1 1	D00FH	Right Side B MDAC
1 0 0 0 0	D010H	Left Rear A MDAC
1 0 0 0 1	D011H	Left Rear B MDAC
1 0 0 1 0	D012H	Right Rear A MDAC
1 0 0 1 1	D013H	Right Rear B MDAC
1 1 0 1 1	D01BH	Routing Register 1
1 1 1 1 1	D01FH	Routing Register 2

MDAC and Routing Register addresses.

The MDAC Data Bus

The MDAC data bus is buffered by U2 (1/B3) ,which is an Octal Tri-State Buffer (74HC541) activated by the MDAC/ signal. Both the MDAC data bus and control bus (called GAIN on the schematics) have series 120Ω resistors on the Digital board (RP7 and RP8, 7/D3) and pull-up resistors on the upper Analog board. The control bus has 4.7K pull-up resistors (RP2, schem. 060-08127) except INWR/. INWR/ and the data bus have 10k pull-up resistors (RP1, schem. 060-08127).

Audio Routing Control

The routing control signals steer the audio signal through the desired path in the analog circuitry. (See Analog Circuit Description.) The routing select signals, ROUT1 and ROUT2, are generated by U12 (1/B4). These signals trigger a Quad D Flip-Flop (U7, 2/B7, 74HC175) and an Octal D Flip-Flop (U3, 2/A7, 74HC273), which latch the selected routing.

Routing Signals

Routing control is implemented through two registers, ROUT1 and ROUT2 (Rout Control Latch). The ROUT1 register (U3) controls:

- Audio and video input selection (INSEL<0:3>).
- Enabling/Disabling of the Dolby filter for the rear channels (DOLBYEN/).
- Enabling/Disabling of the input high-pass filter (HPEN/).
- Enabling/Disabling of the output mute circuitry (MUTE/).
- Enabling/Disabling of the front processed audio signal to the main front channel outputs (FPROCEN).

Data bit MDB<0:7>	Signal name	Source location	Function	Active state
0	INSEL0	2/A6	Input #1 select	1
1	INSEL1	2/A6	Input #2 select	1
2	INSEL2	2/A6	Input #3 select	1
3	INSEL3	2/A6	Input #4 select	1
4	DOLBYEN/	2/A6	Enable dolby lo-pass filter	0
5	HPEN/	2/A6	Enable input hi-pass filter	0
6	MUTE/	2/A6	Mutes all outputs. (-40 dB)	0
7	FPROCEN	2/A6	Enable processed, non-THX filtered outputs to front outputs	1

ROUT1 register bit functionality and active states.

The ROUT2 register is implemented with a Quad D - Flip-Flop (U7) and a "NOR" gate (U5 + U4, 2/A5-6). This "NOR" gate is used to generate REQEN, which routes the audio signal through the front Re-EQ filters. The REQEN signal is a combination of the THXEN/ signal (ROUT2 register) and the FPROCEN signal (ROUT1 register). FDIREN enables/disables the direct audio signal path from the inputs to the front outputs. SIDESEL selects whether the audio signal going to the side outputs originates from the front processed signal path or from the rear signal path (after the SURROUND-EQ filters). THXEN selects whether or not the front processed audio signal (see REQEN description above) goes through the front Re-EQ filters. THXEN also enables/disables the rear channel SURROUND-EQ filters.

IRRST is a reset signal for the IR decoder chip.

Signal name	Source location	Data bit MDB<0:3>	Active state	Function
IRRST	2/B7	0	1 (inv. output)	Reset IR Remote decoder.
THXEN	2/B6	1	1	Enable Surround EQ filters.
THXEN/	2/B6	1	0 (inv. output)	Used to generate REQEN
SIDESEL	2/B6	2	1 = front 0 = rear (inv. output)	Side source, front or rear processed
FDIREN	2/B6	3	1 (inv. output)	Enable dry signal to front.
REQEN	2/A6	1 NOR (7 ROUT1 reg)	1 (THXEN/ = 0 FPROCEN = 0)	Enable front EQ filters.

ROUT2 register data bits and their active state

Slave Z80 Circuitry

The CP-3's two Z80 CPUs can perform independently, or their operation can be synchronized. One Z80 has been designated as the Master (U24, 1/D7) and has full control over the Slave Z80 (U34, 3/D5) via the Slave Reset circuitry and the Master Slave Interface. The Slave Z80 is dedicated to controlling Lexichip operation and must rely on the Master Z80 to load programs to its static 8K Slave RAM (U35, 6264, 3/D3). The Slave Z80 data bus (SDB<0:7>) has direct access to the Slave RAM and the Lexichip WCS. The Slave address bus goes through the Dual Bus Interface, which consists of four Quad 2-Input Multiplexers (U26 - U29, 74AC157, 3/A4-7). These multiplexers are normally switched in such a way that the Slave address bus is always connected to the Slave RAM and the Lexichip. When the Master requires access to the Slave RAM, the multiplexers change state to connect the Master Z80 address bus to the Shared Bus. As access is available only when the Slave Z80 is going through a refresh cycle, no data bus switching is necessary. The Slave Z80 data lines are Tri-Stated during the refresh period.

The DWR/, DRD/ and DADR<0:13> signals are shared by the Master Z80 and the Slave Z80, depending on which has access to the Slave RAM or the Lexichip. The SWAIT/ signal is generated by the Lexichip and is used to synchronize the Slave Z80 to the audio processing cycle within the Lexichip.

Slave Z80 Decoding

As the Slave Z80 can access only the Slave RAM and the Lexichip, the decoding is very simple. Basically, SADR13 low selects Slave RAM; SADR13 high selects the Lexichip. SMREQ/ must also be low and, to prevent conflict between the Master Z80 and the Slave Z80, ACC/ signal must also be high. Slave decoding is performed by the same GAL16V8 (U13, 1/B7) as Master decoding.

Address (hex)	Size	Signal	Description	Slave/Master Sharing
0000 - 1FFF	8K	SLVRAM/	Slave RAM select	Yes 0000-0FFFH
2000 - 23FF	1K	LEX/	Slave Lexichip select	Yes

Slave Z80 addressing

Master Z80 Access to Slave Z80 Circuitry

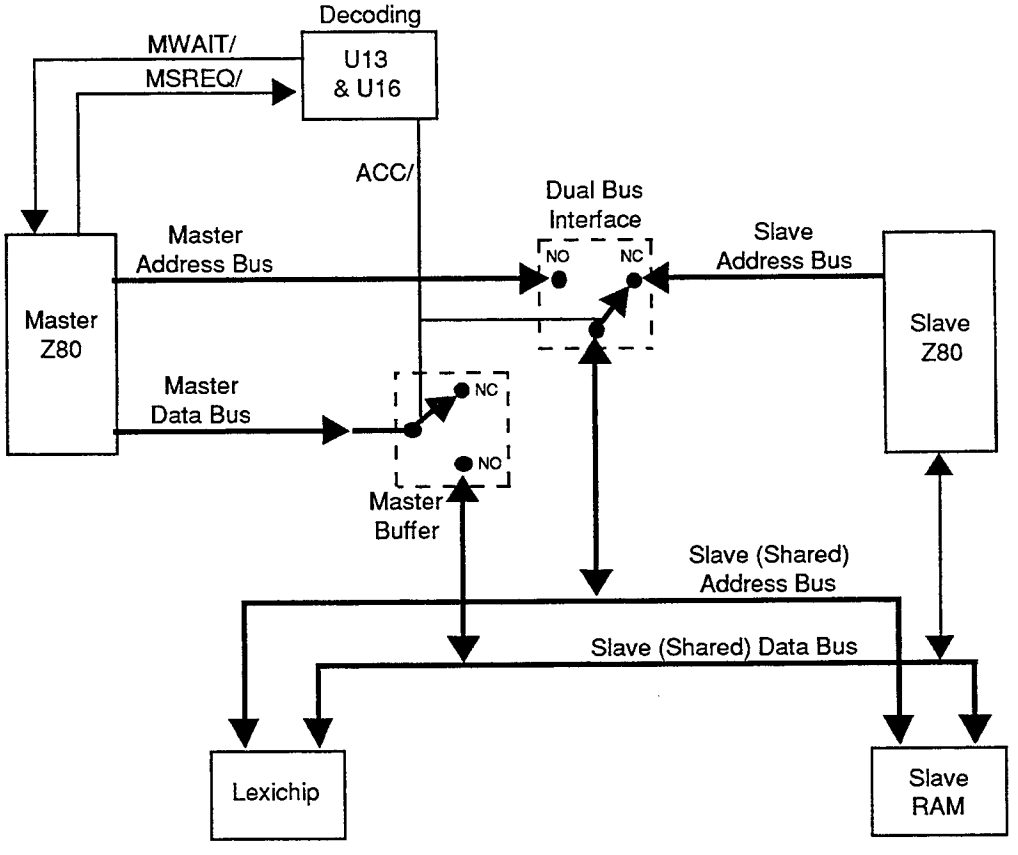
In order to access Slave RAM and the Lexichip (U30) WCS, the Master Z80 loads program code from the ROM to the Slave RAM and the Lexichip. The Master Z80 can access Slave circuitry only when:

1. Slave Z80 is in Reset,
2. Slave Z80 is in the last two clock periods of an instruction fetch operation. (Refresh period)

The Master Z80 accesses the Slave Z80 via the Dual Bus Interface and the Master Buffer (U26-U29, U36) and two PLDs (U13 and U16, GAL16V8, 1/B7 and 3/B5). The Slave Z80 has always full access to Slave RAM and the Lexichip (U30) and does not go in to a wait state while the Master Z80 is accessing the Slave RAM or the Lexichip. (The Slave Z80 will only go into a wait state if the Lexichip is told to activate SWAIT/ to synchronize the Slave Z80 and the Lexichip.) As the Slave RAM used by the Slave Z80 does not

require refreshing, the Master Z80 utilizes the Slave Z80's refresh period (two clock cycles during every instruction fetch) to access Slave memory. If the Slave Z80 is in Reset mode, the Master gains immediate access to the Slave bus. Synchronization of timing and handling of access signaling for the Slave bus is performed by PLDs U13 and U16.

CP-3 Master/Slave Interface



MSREQ/	Master Z80 requests Slave bus access.
MWAIT/	Decoding circuitry returns a wait signal to the Master Z80 until Slave bus is available. No wait signal is necessary if the Slave Z80 is in Reset.
ACC/	Decoding circuitry asserts the Access signal, removes the wait signal and the Master Z80 gains access to the Slave bus.

Access Decoding

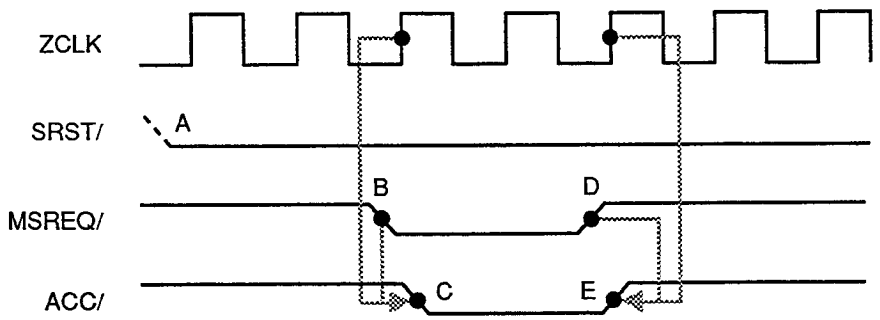
SLVRAM/ and LEX/ are generated by the Master Slave decoder (U13). These signals are activated for either processor to access Slave RAM or the Lexichip. When access to the shared Slave bus is required by the Master Z80, the Master Decoder (U13) pulls MSREQ/ low. Then the Slave Decoder (U16) asserts ACC/ to give the Master Z80 access. Assertion of ACC/ by the slave decoder is as follows:

If SRST/ is asserted (Slave Z80 in Reset mode), ACC/ is activated immediately.

If the Slave Z80 is running, ACC/ will not be asserted until the Slave Z80 reaches its refresh cycle.

When ACC/ cannot be activated, the Slave decoder will assert MWAIT/ and X number of W-states will be added to the Master Z80 Memory Read or Write cycles. When the Slave Z80 refresh period is over, MWAIT/ is released and ACC/ is asserted.

Slave Reset Access

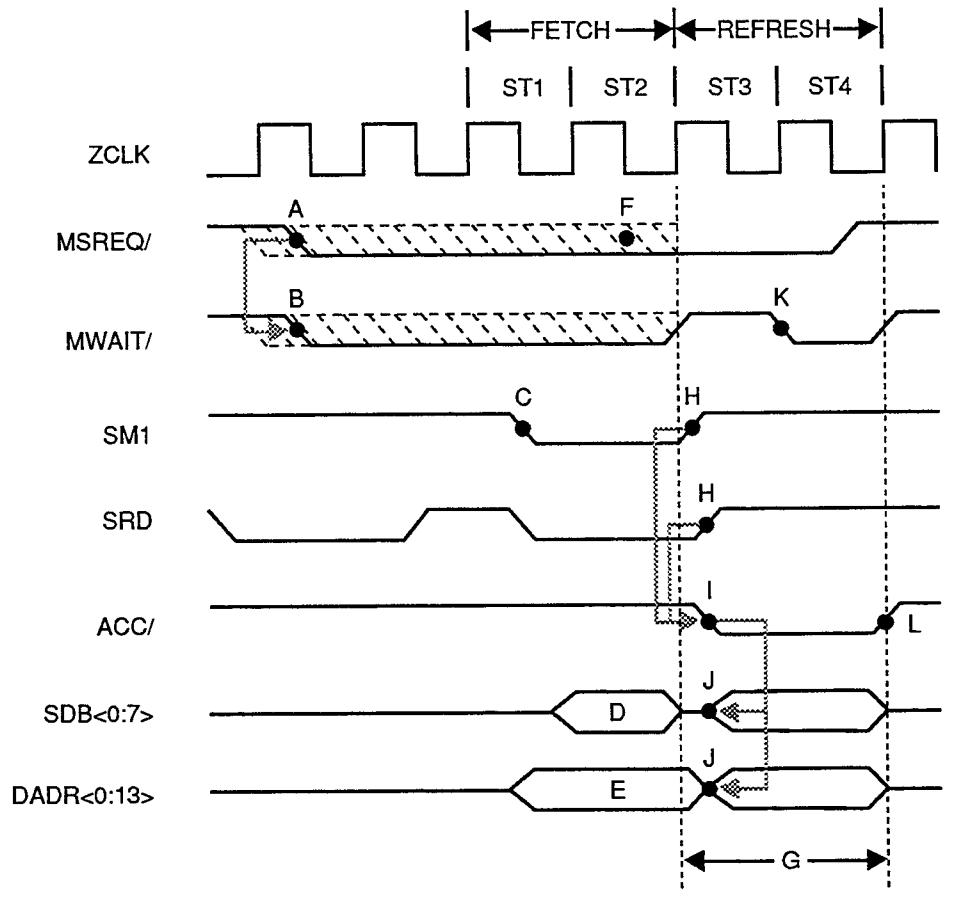


A Slave Z80 reset signal is active (low). B Master Z80 requests access to Slave Bus by asserting MSREQ/	C On rising edge of ZCLK, ACC/ is asserted, allowing Master Z80 access to Slave Bus. D After read/write operation is performed, MSREQ/ is de-activated.	E On rising edge of ZCLK, ACC/ is de-activated and bus is returned to Slave Z80.

When ACC/ is asserted:

- Multiplexers U26 - U29 switch state and the Master Z80 address bus is connected to the shared (slave) address bus.
- Master Buffer U36 is turned on (remember Slave Z80 data bus is Tri-Stated during the refresh period) and Master Z80 data bus is connected to the Slave Z80 data bus. MRD/ signal controls the direction of data flow through the buffer.

Slave Refresh Access



A The Master Z80 requests Slave access by asserting MSREQ/

B MWAIT/ is asserted to keep the Master Z80 in a wait state until the Refresh window occurs

C SM1/ indicates Slave Z80 Instruction Fetch period

D Slave reads instruction code from the Slave Data Bus

E Slave Z80 places the contents of the program counter on the Slave (Shared) Address Bus

F If MSREQ/ is asserted during the second T state of Instruction Fetch period (SM1/), the Master Z80 is in sync with the Slave Z80 Refresh period, and no wait states will occur

G The Refresh access window ocurs for the last two T states during a Slave Z80 Instruction Fetch cycle.

H SM1/ and SRD/ switch to high and activate the ACC/ signal

I The ACC/ signal is asserted, and the Master Z80 gains access to the Slave (Shared) Bus (J)

J During this Refresh period, the Slave Z80 data lines are placed in a high impedance state. The Master Z80 is then allowed access to the data bus for a read or write operation.

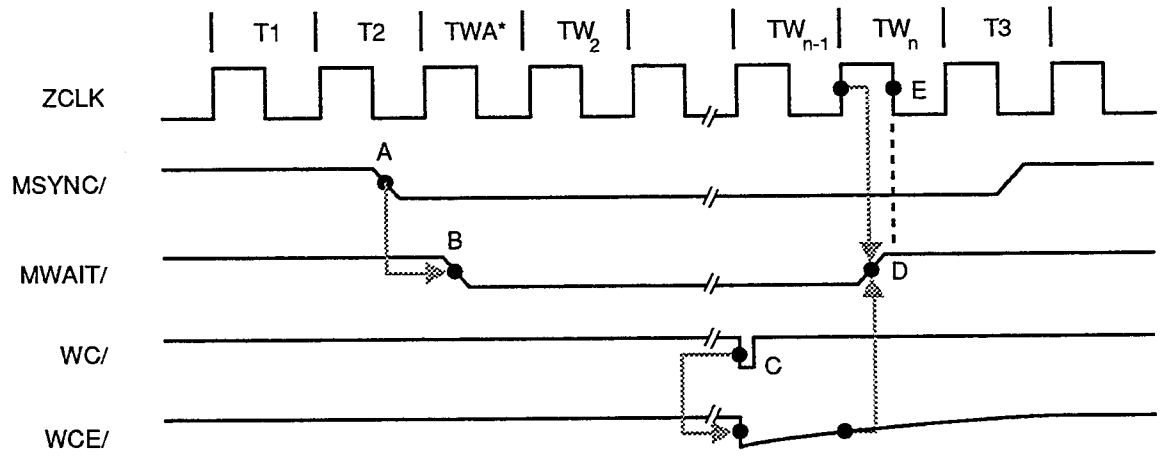
K MWAIT/ goes low for the 4th T state of the Slave Instruction Fetch period. If the Master Z80 has already gained access to the Slave bus at this point, this MWAIT/ will be ignored. If MSREQ is activated just after D, this wait signal will be acknowledged, and the Master Processor will insert waits until the next Refresh period.

L At the end of the Slave Refresh Access, ACC/ is returned to a logical high, which removes Master Z80 from the Slave Bus.

Master and Slave Z80 Synchronizing

The CP-3's audio signal processing algorithms require the Slave and Master Z80s to synchronize with the Lexichip. The Slave Z80 is synchronized to the Lexichip by instructing the Lexichip to pull SWAIT/ low. SWAIT/ stays low until the Word Clock (WC/, 4/A7) signal goes low. (WC/ is a clock reference signal generated by the Lexichip to indicate the beginning of a A/D conversion cycle.) Synchronization of the Master Z80 to the Lexichip is done by the Master itself writing any data to the MSYNC/ port (I/O address 05). When this is done, the Slave decoder (U16) asserts MWAIT/ and X number of wait states are added to the Master Z80 cycle, until the Lexichip generates WC/. Because the duration of the WC/ pulse is too short for the slave decoder, it is extended to become WCE/ by CR2, R30 and C34 (3/B6 - C7).

MSYNC Signaling



A MSYNC/ is asserted during a Master Z80 I/O write operation. B As a result of MSYNC/ input, Slave Decoder asserts MWAIT/ until WCE/ is asserted.	C WC/ is asserted and is extended to produce WCE D On rising edge of ZCLK, Slave Decoder, seeing WCE/ active, removes MWAIT/ signal.	E On rising edge of ZCLK, Master Z80 sees MWAIT/ removed and finishes the instruction. * One wait state is assserted automatically by Z80 during I/O operations. Additional wait states ocur if MWAIT/ is asserted.

Lexichip Digital Signal Processor

The Lexichip (U30, 4/A6-C7) performs most of the digital effects processing calculations for the CP-3. It receives instructions from its internal program RAM, referred to as the Writable Control Store (WCS). Address, data and control lines for the WCS are shared by the Slave and Master Z80s. This allows both Slave and Master Z80 processors to load audio effects programs into the Lexichip, monitor status of audio data, and synchronously change program parameter values in the audio programs. Both Master and Slave Z80 processors treat the 768 bytes of WCS as static RAM.

Lexichip Clock Signals

An internal crystal oscillator driver circuit drives a 18.432 MHz crystal mounted across pins 75 and 76 on the Lexichip. Internal Lexichip circuitry divides this clock frequency down by four to provide the 4.608 MHz ZCLK which is used by the Z80 processors.

WC/ is used as a clock reference by the CP-3. It operates at 36 kHz or 41.143 kHz frequency depending on which program the CP-3 is running. It is utilized by the IR Receiver Interrupt Timer circuitry, as well as by the Slave decoding circuitry, to synchronize the Master processor to DSP operations.

The Lexichip generates numerous clock signals for controlling the A/D and D/A conversion. A list of these signals can be found at the end of this chapter.

Two additional DEG/ signals have been created outside of the Lexichip by using two D Flip-Flops (U6, 74HC74, 4/C4) one inverter (U4, 74HC04, 4/C5) and two OR gates (U5, 74HC32, 4/C3). Schem. Timing Diagram (060-08839 and 060-08840) at the end of this manual, show the deglitch timing.

DRAM Audio Memory

The Lexichip has 64K of 20-bit DRAM for its use when running the DSP algorithms. Five 64K x 4-bit dynamic RAM ICs (U18 - U22, 4464, 4/D3-D8) are provided for specific Lexichip usage. DRAM read, write and refresh functions are performed by dedicated set of address and control lines and a 20-bit data bus provided by the Lexichip.

Conversion Latches

Internal control logic circuitry enables the Lexichip to command complete control over external DAC functionality with minimal external circuitry. Four external 8-bit latches (U8 - U11, 4/A3 - B5) are used to latch 16-bit data out to the DAC via the DRAM data bus. Two latches are used per "left" and "right" side. CCLK0 and CCLK1 are used to clock data into these latches.

On-Screen Video Display

The CP-3 is equipped with On-Screen Display (OSD) capability in addition to the front panel display. With the video signal routed through the CP-3, the user can display full menu options on a TV screen at any time. Not only does this make it easier for the user to interact with the system, but it allows the video source to be changed when the audio source is changed.

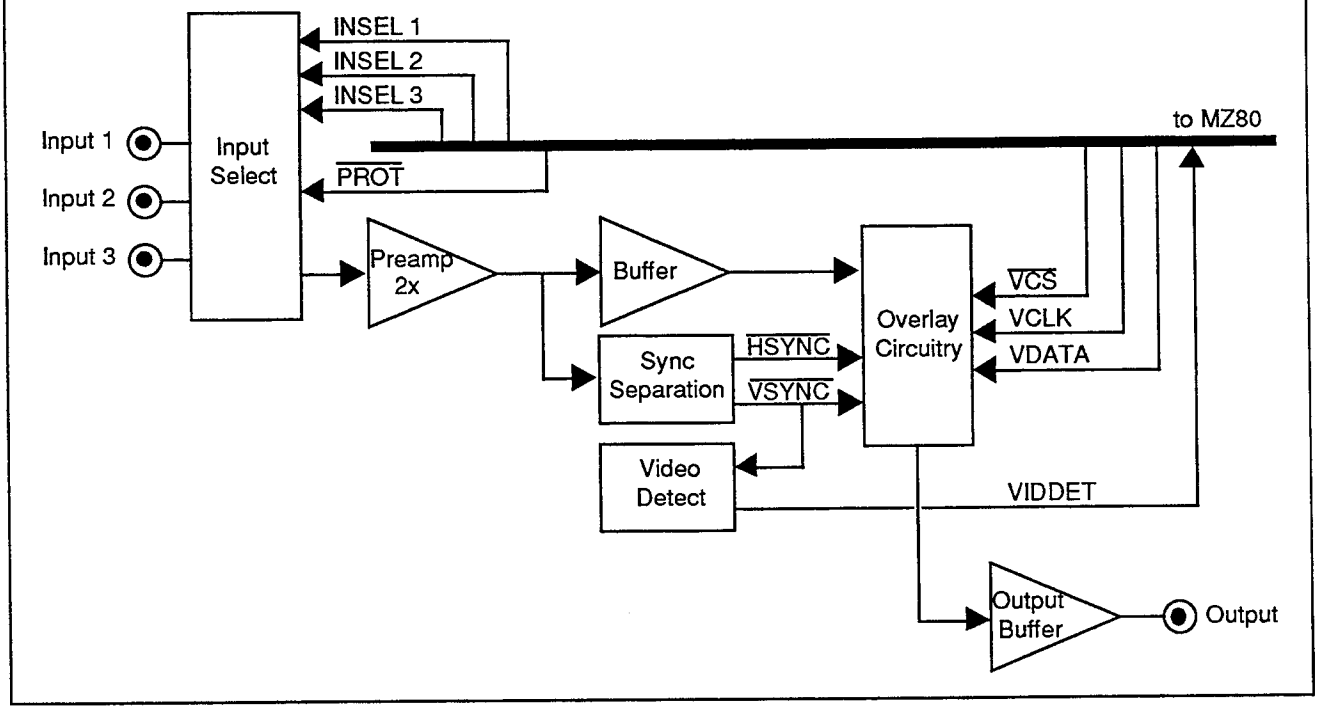
> Note: The CP-3 video circuitry is designed for NTSC "M" composite video signals (used in USA, Canada and Japan). The video circuitry is capable of superimposing text onto the incoming video signal; it is also capable of generating its own blue background in the absence of an incoming video signal. Even though the video circuitry is designed for NTSC signals, it can synchronize to incoming PAL (used in Europe) and SECAM (used in France and former USSR) composite video signals and overlay text on the picture. In doing this, however, the text will lose sharpness, especially in SECAM. The quality of the PAL/SECAM video signal should not be affected any more than the quality of an NTSC signal. Therefore, a user should feel confident in using the CP-3 video circuitry for switching between different PAL/SECAM type sources. The video circuitry can not generate its own PAL/SECAM blue background signal in the absence of incoming video signal.

The OSD video circuitry is located on the digital board closest to the rear panel. Its power supply is routed separately from the Power Supply board to minimize the introduction of noise from the digital circuitry. To further decrease the noise generated by the digital circuitry, the +5 V rails and GND are filtered by FB4 (6/A3), FB5 (6/B8) C33 and C32 (6/B8). Mixing is performed primarily by two video chips: NJM2217 (U1, 6/A7,) which separate the synchronization signals from the incoming video signal and by MB88324A-K1 (U32, 6/A4), which superimposes text onto the incoming video signal. The Master Z80 is responsible for controlling the text overlay chip (U32).

There are currently two versions of the video circuitry. The version that is used on Digital boards up to Revision 3, is on sheet 5 on the schematics. The version used on boards with a higher Rev than 3, is located on sheet 6. The differences between versions are mainly in resistor and capacitor values except for the clamping circuitry (5/C3-4), which has been replaced on the newer version by a built-in clamper (U1 pin 21). The circuitry description below refers primarily to sheet 6. The circuitry consists of seven major blocks:

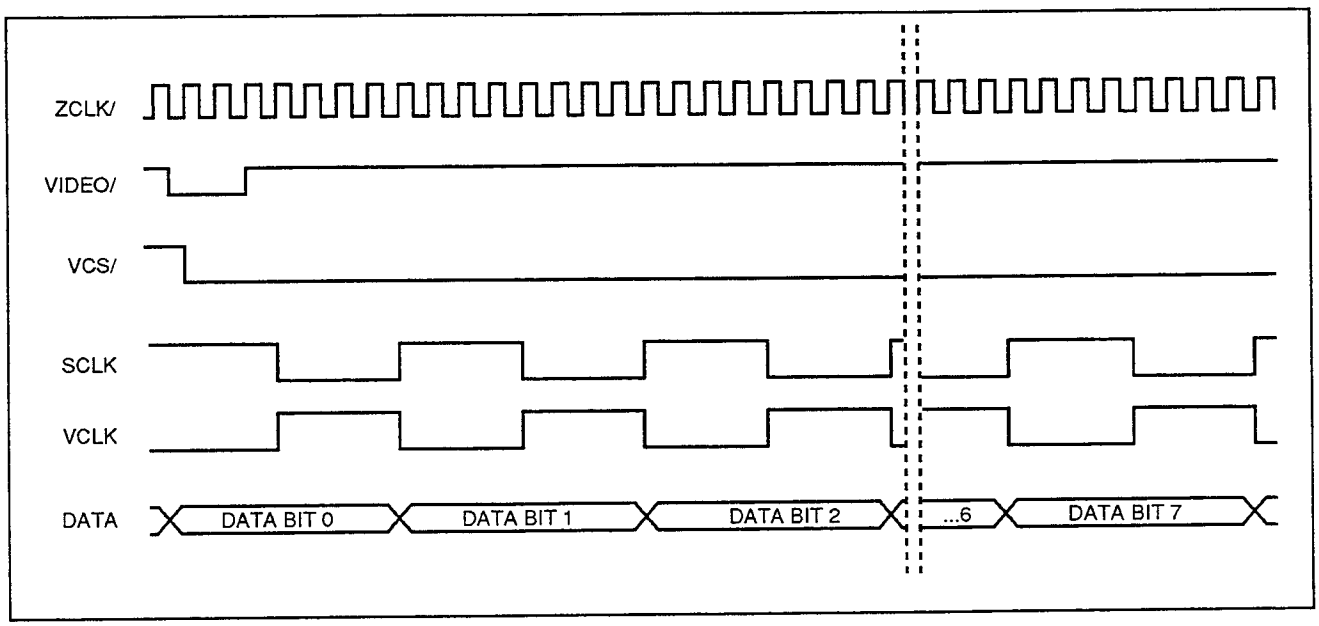
Input Switching
Gain stage (Pre amplifier)
Buffer
Character overlay circuitry
Horizontal and Vertical sync. separator
Video detect circuitry
Output buffer

CP-3 Video Circuitry Block Diagram



Video Overlay Interface

The interface between the Master Z80 and the Video Overlay circuitry consists mainly of U40 (2/A5, GAL16V8) and U38 (2/B5, 74HC165, 8-bit parallel-to-serial Shift Register). U40 generates the clock and select signals necessary to control the parallel-to-serial conversion and data transfer to the overlay chip (U32).



Input Switching

Input composite video signals can be accepted from three different devices via three switchable input jacks. These inputs are numbered 1-3 and are configured in such a way that they change with the audio inputs. There are four audio inputs versus three video inputs. Audio inputs 1-3 relate to the corresponding video inputs. If audio input 4 is selected, video input 1 is selected by default. If the CP-3 is turned off via the rear panel power switch, the input switches will automatically bypass the CP-3 video circuitry and connect video input 1 to the output. In this case, there is no 75Ω termination within the CP-3. PROT/ (1/A5) ensures proper behavior of the relays during power on and off. Q2, Q5, Q8 act as drivers for the relays.

During Output Level Adjustment (when the CP-3 is generating its internal noise signal), all inputs are deselected. In this state, the CP-3 will not pass any video and will automatically generate its own blue background.

Pre Amplifier

After the video signal has gone through the input switches, it enters the pre-amplifying stage (Q3, Q4, 6/C4-D5) which amplifies the signal 6 dB. From there, the signal takes two different paths. One leads to the synchronizing pulse separation circuitry (U1, NJM2217, 6/A6-B8). The video input (pin 21) of U1 has an integral clamping circuitry. This is used to clamp the tip of the video signal to a fixed DC level to ensure that the level of the video signal and the level of the superimposed character signal will always match, regardless of the Average Picture Level (APL)*. The other signal path leads to a buffer (Q13) before entering the Character Overlay circuitry. In versions of the video circuitry used on Rev 3 and lower Digital boards, a special circuit (Q6, 5/C4) is used to clamp the signal.

*APL is the average signal level during active scanning time, excluding blanking and synchronizing signals, integrated over a frame period. (EIA/TIA-250-C)

Synchronizing Signal Separation

The synchronizing signal separation circuitry (U1, NJM2217, 6/A6-B8) is responsible for generating synchronizing signals for the character overlay circuitry (U32, 6/A3-B5). This circuit "removes" all video information from the video signal, leaving only the HSYNC/ (Horizontal sync) and VSYNC/ (Vertical sync) pulses. The character superimposing circuitry uses these pulses to synchronize generated text to the incoming video signal. The NTSC HSYNC/ pulse frequency is 15.734 kHz; the VSYNC/ frequency is 59.94 Hz.

U1 has an integral Automatic Frequency Control (AFC) circuit which it uses to lock onto the incoming video signal. This circuitry requires tuning by adjustment of the free-running frequency with R16. (See Video Calibration.)

Character Overlay Circuitry

The main component in the Character Overlay Circuitry is U32 (6/A4, MB88324A-K1). This chip superimposes text information (previously loaded into its RAM by the Master Z80) onto the incoming video signal (Mode 1). When no video signal is present, the chip is capable of generating its own blue background, synchronizing signals and superimposing text onto the background (Mode 2). This blue background signal is an artificial blue screen which is only generated in the absence of incoming video signal. A "character background" appears when a video signal is present (Mode 1) to enhance character contrast and readability.

The overlay chip requires communication with the Master Z80, and an oscillator to generate the subcarrier frequency when it is operating in Mode 2 (generating its own blue background). Y2 (6/A5), which is a 7.15909 MHz crystal, oscillates at double the subcarrier frequency. C53 provides adjustment for the subcarrier frequency. L3, with C55 and C60 (6/A5) provide another oscillator for U32, used to generate character pixels. The frequency of this oscillator is 7 - 8 MHz. The variation in frequency influences character position on the TV screen.

Note: If a probe is attached to any of the oscillators leads, the added capacitance will change the frequency. U32 is supplied by U1 with synchronizing pulses. These pulses, HSYNC/ and VSYNC/, are essential for the overlay chip. If they are absent or unstable the chip will be unable to display stable text on the TV screen (Mode 1).

Pins 13, 15, 16 (U32) and attached resistors control the luminance level of the characters, the character background and the DC offset of the self generated blue background. To ensure that U32 boots up correctly during power on, it has been provided with its own reset circuitry (6/B3-4).

After the signal has gone through the overlay chip, it goes to the output buffer (6/C2-D4) which drives the 75Ω load.

Video Detect Circuitry

The Video Detect Circuitry (6/B4-C6) determines whether or not there is a video signal present by using the VSYNC/ pulse to charge C5 through Q1 and other passive components. If the pulse is there, C5 is charged and VIDDET is "1". If the pulse is absent, C5 is discharged through R7 and R6 and VIDDET changes to "0".

Front Panel Liquid Crystal Display (LCD)

The CP-3 LCD is an Intelligent display with built-in display controller, ASCII character generator, custom character generator and an integral command register for the most common display functions. As it can take as long as 1.64ms to execute some display commands, the display also has a "busy "signal to alert the microprocessor that it is unable to receive the next instruction.

LCD Interface

The LCD display is I/O mapped and the decoding interface is very simple. U15 (1/B7) which is a 74HC138 (1-of-8 Decoder), generates a select/latch signal (active on falling edge). Timing requirements do not allow the Master Z80 Read/ Write signal to be used. Therefore, MADR4 is used as a LCD Read/ Write signal, and MADR3 is used to select the LCD Command register or Character register.

The Contrast Adjust circuitry (2/C3-5) is a simplified DAC. It consists mainly of U37 (74HC174), resistors and diodes.

Signal name	Source location	Data bit MDB<0:6>	Active state	Function
CONADJ	2/C3	0 - 3	N/A	Analog contrast signal for the LCD, created by MDB<0:3>.
N/A	2/C4	0	1	CONADJ Least Significant Byte.
N/A	2/C4	1	1	
N/A	2/C4	2	1	
N/A	2/C4	3	1	CONADJ Most Significant Byte.
N/A	N/A	4	X	Not used.
SRST/	2/C4	5	0	Slave Z80 Reset Signal
BKLTEN/	2/C4	6	0	LCD Backlight enable signal.

LCD Contrast Port bits

The LCD Backlight power source is located on the Power Supply board. See Power Supply Circuit Description.

Front Panel Circuitry

The CP-3 Front Panel board is located in the CP-3 front panel. It is included here because all of its signals and the +5V and GND originate from the Digital board. Unless otherwise noted, all references to schematics in this section refer to SCHEM, FRONT PANEL BD., CP3 ; 060-08149. The Front Panel Board circuitry involves all LED indicators and Switches and the IR Detector.

Front Panel Interface

The Front Panel Interface is I/O Mapped for the Master Z80. For address mapping see the table in the section on Master Z80 Addressing. U15 (1-of-8 Decoder, 1/B7, on the Digital board) generates the select signals: COLSEL, ROWSEL and KEYSTAT/. Both the LEDs and the switches are arranged in two matrixes. These matrixes are driven by three registers, two of which are write only, one of which is read only. The LED matrix is controlled by two Hex D Flip-Flops, U3 (1/D7) and U4 (1/B7). U3 drives the column signals, both for the 4 LED columns and 2 switch columns. U4 drives the 6 LED rows. The switch rows are read through the Keystat register U2 (A/3) — an Octal 3-State Noninverting Line Receiver (74HC541).

Power Supply Circuit Description

Overview

The CP-3 has an internal supply which produces the required DC supplies from various line voltages. It may be strapped for line voltages of 100, 120, 220 and 240 VAC at either 50 or 60 Hz. All DC voltages are produced by linear supplies. A bipolar 15 volt supply is required by the analog electronics and is regulated locally on the lower analog board. The digital and video electronics each require +5 volts. One regulator, located on the power supply board, is used for both supplies. Separate wires are used for bringing +5 volts with its ground to the digital and video sections of the digital board. A second voltage regulator present on the power supply board is used for the liquid crystal display's LED backlighting. Additional circuitry provides a power fail indication for the CP-3's microprocessors. The power supply board is located behind the transformer on the right hand side of the CP-3 with the unit facing you.

Transformer Primary

A detachable IEC-standard line cord mates with the power connector at the rear panel of the CP-3. This connector contains a passive filter for preventing undesireable RFI emissions from entering or leaving the unit. A Grn/Yel wire connects the power connector's ground pin to the CP-3 chassis. Brown and Blue wires with quick disconnects provide the bond between the power connector and the power supply board. The hot (Brown) side of the line goes through a fuse (F1) to the power switch located on the front panel. The cold side of the power switch is terminated according to the line voltage(100/220 or 120/240 VAC).

The power transformer has two 120 volt primary windings. One winding has a separate tap for 100 volts. The windings are placed in parallel for 100 or 120 VAC; in series for 220 or 240 VAC. The transformer does not have to be rewired for different line voltages. Instead, three jumpers (W1,2,3) are used for changing the configuration of its windings. The following table may be handy for reconfiguring the CP-3 for different voltages:

Primary Component	100 VAC	120 VAC	220 VAC	240 VAC
Power switch retn (Brn)	100/220V	120/240V	100/220V	120/240V
W1 Jumper (Blue)	NO	NO	YES	YES
W2 Jumper (Blue)	YES	YES	NO	NO
W3 Jumper (Brown)	YES	YES	NO	NO
Fuse	0.5 Amp T, 20mm	0.5 Amp Slo-Blo, 3AG	0.25 Amp T, 20mm	0.25 Amp T, 20mm

CAUTION
THE CP-3 COMPLIES WITH
UL, CSA AND TUV SAFETY REGULATIONS.
MODIFICATIONS TO THE POWER SUPPLY ARE NOT RECOMMENDED.

Transformer Secondary

The power transformer contains two secondary windings, each with a center tap. One winding, indicated by Red and Yellow wires, is used for the bipolar supplies required by the analog world. The ±15 volt supplies are created by placing diodes CR1-4 in a center-tap configuration. The positive supply develops across C2; the negative across C1. C3 and C4 filter unwanted high frequencies. Each supply, along with its respective ground return, is passed to the lower analog board for local regulation.

The other secondary winding is marked by Green and Violet wires. This winding is used for meeting the digital, video and LCD backlighting supply requirements. Two diodes, CR9 & 10, are used in a full-wave center-tap configuration to develop +5VRAW across C8. C11 and C12 provide high frequency filtering. +5VRAW is passed to two LM317 voltage regulators as well as the power fail circuitry.

Voltage Regulator U1 is used for the front panel display's LED backlighting. C5 provides local filtering of +5VRAW while CR5 protects the regulator from becoming reverse-biased. U1 is configured as a current regulator. R1 sets the output current to about 240 mA by using the built-in biasing of the LM317 regulator. In addition, this regulator may be shut down by turning on Q1, a transistor at U1's adjust pin. R2 limits the current through Q1. The control signal BKLTEN/ determines whether the LCD backlighting is on or off, and comes from the digital board via connector J16. When BKLTEN/ is low, Q1 is off and the display's backlighting is turned on. With BKLTEN/ is high, Q1 is on and the display turns off.

The 5 volt supplies for the digital and video electronics share a common voltage regulator, U2. Diodes CR6 and CR7 protect the voltage regulator from becoming reverse-biased and from negative spikes. C6 and C7 locally filter +5VRAW, while C10 filters the output from U2. R4 and R5 bias the voltage regulator for a nominal +4.98 VDC output. C9 protects the adjust pin on the requlator from high frequency spikes. The +5 volt output (+5VD) with its ground go through separate twisted pair cables to the digital board.

+5VRAW is also used to determine if a power fail condition is present. A zener diode (CR8) drops the +5VRAW voltage by 6.2 volts. R8 and R9 serve as a divider to drop the voltage as well as its ripple further, closer to the Vbe voltage for the transistor. This causes Q3 to turn off when the line voltage drops below 90 VAC (when the CP-3 is configured for 120 VAC). When Q3 turns off, Q2 turns on, causing the PFAIL/ signal to go from +5 to 0 volts. PFAIL/ goes to the digital board via J16, where it is monitored by the CP-3's microprocessors. When the microprocessors see PFAIL/ go low, they perform routines to prepare the CP-3 for power shut down.

For further information concerning tolerances for the various supplies, please see the Troubleshooting section of this manual. Note that calibration is not required for the power supply.

Signal Descriptions

Analog Signals

Signal	Description
AGND	Analog Ground
CTR	Center Processed Output
CTREQ	Center Re-EQ output signal
CTROUT	Center Output MDAC signal
LDACOUT	Left D to A Output
LFOUT	Left Front Output MDAC signal
LFRT	Left Front Processed Output
LIN	Left Input signal to Input MDAC (from lower board)
LINB	Left Input signal from Input MDAC to Subwoofer filter
LINGND	Left Input signal ground
LINHP	Left Input High Pass Filter signal (from upper board)
LSAMP	Left Sample and Hold Output signal
LSUR	Left Surround Processed Output
LSUREQ	Left Surround EQ Output
RDACOUT	Right D to A Output
RFOUT	Right Front Output MDAC signal
RFRT	Right Front Processed Output
RIN	Right Input signal to Input MDAC (from lower board)
RINB	Right Input signal from Input MDAC to Subwoofer filter
RINGND	Right Input signal ground
RINHP	Right Input High Pass Filter signal (from upper board)
RSAMP	Right Sample and Hold Output signal
RSUR	Right Surround Processed Output
RSUREQ	Right Surround EQ Output
SUBOUT	Subwoofer filter Output signal

MDAC Signals

Signal	Description
A/BSEL	Select A (input) or B (feedback) side of MDAC for writing 8-bit data
CTRWR/	Center and Subwoofer Output MDACs Write signal
FWR/	Front Left and Right Output MDACs Write signal
GAIN	MDAC control bus
INWR/	Left and Right Input MDACs Write signal
LEFT	Right Output MDACs Chip Select
LEFT/	Left Output MDACs Chip Select
MDAC<0:7>	MDAC Data bus
RWR/	Rear Left and Right Output MDACs Write signal
SWR/	Side Left and Right Output MDACs Write signal

Analog Routing Control Signals

Signal	Description
DOLBYEN	Dolby Filter Enable (high=+1.6V; low= -15V)
DOLBYEN/	Dolby Filter Enable (from Digital board)
FDIREN	Front Left and Right Direct Output Enable
FPROCEN	Front Left and Right Processed Output Enable
HPEN/	Input High Pass Filter Enable
INSEL<0:3>	Input Select
MUTE/	Output Mute Control signal (from Digital board)
OUTMUTE	Output Mute Control signal (low= -15V)
REQEN	Front Left and Right Center Re-EQ Enable
SIDESEL	Side Source Select (high=front; low=rear)
THXEN	THX Surround EQ Enable

A to D-D to A Conversion

Signal	Description
CNT	Conversion Control bus
DEG0/	Deglitch 0 (for Front Left and Right D to A Output Hold)
DEG1/	Deglitch 1 (for Center D to A Output Hold)
DEG2/	Deglitch 2 (for Left Surround D to A Output Hold)
DEG3/	Deglitch 3 (for Right Surround D to A Output Hold)
HOLD	Hold Control signal (active high for A to D Conversion)
HOLD/	Hold Control signal (active low for A to D Conversion)
LDAC<0:15>	Left Audio DAC Data bus
LDATA	Left Audio A to D Comparator Output
RDAC<0:15>	Right Audio DAC data bus
RDATA	Right Audio A to D Comparator Output

Digital Signals

Signal	Description
ACC/	Master access to Shared Bus
DADR<0:13>	Shared address bus
DRD/	Shared read signal for the Slave RAM and the Lexichip
DWR/	Shared write signal for the Slave RAM and the Lexichip
INT/	Master Interrupt.
IORQ/	Master Input/Output Request.
IRDATA	15 bit serial stream of IR remote control data.
IRRST	Reset signal for IR decoder, active high.
IRCLK	Clock signal for the IR decoder (461 kHz).
IRD/	Decoded select signal for the IR decoder. I/O mapped address 07H.
LEX/	Decoded Lexichip select signal
M1/	Master Machine cycle one.
MADR<0:15>	Master Z80 Address bus.
MDAC/	Decoded MDAC select signal
MDB<0:7>	Master Z80 Data bus.
MMREQ/	Master Memory Request.
MRD/	Master Read.
MSREQ/	Master/Slave request
MSYNC/	Input, Master/Slave synchronizing signal
MUTE/	Mute all outputs
MWAIT/	Master wait signal
MWR/	Master Write.
PFAIL/	Master NMI/ (Non-Maskable Interrupt). Power Fail detect signal (low=shut down)
PROT/	Power down/up protect signal for the Master RAM
RAM/	Decoded RAM select signal
ROM/	Decoded ROM select signal
SADR<0:13>	Slave Z80 address bus
SDB<0:7>	Slave Z80 data bus
SLVRAM/	Decoded Slave RAM signal
SLVWR/	Slave Z80 write signal
SMREQ/	Slave Reset signal
SM1/	Slave Machine cycle one
SRD/	Slave Z80 read signal
SWAIT/	Slave Wait signal
VIDDET	Video detect signal.
WCE/	Extended Word Clock signal from the Lexichip
ZCLK	System clock 4.608 MHz.(18.432MHz/4)
ZRST/	System Reset. Non controllable, works at power on

Digital Routing Control Signals

Signal	Description
DOLBYEN/	Enable dolby low-pass filter
FDIREN	Enable dry signal to front.
FPROCEN	Enable processed, non-THX filtered outputs to front outputs
HPEN/	Enable input high-pass filter
INSEL0	Input #1 select
INSEL1	Input #2 select
INSEL2	Input #3 select
INSEL3	Input #4 select
REQEN	Enable front THX filters.
ROUT1	Select signal for the routing 1 register.
ROUT2	Select signal for the routing 2 register.
SIDESEL	Side source, front or rear processed.
SRST/	Input, Slave Reset signal
THXEN	Enable THX filters
THXEN/	Used to generate REQEN

Conversion Signals

Signal	Description
CCLK0	Conversion clock signal. Used to latch data into the "left side" DAC latches.
CCLK1	Conversion clock signal. Used to latch data into the "right" DAC latches.
DEG0/	Deglitch signal. DEG0/ directs the DA conversion to the front channels.
DEG1/	Deglitch signal. DEG1/ directs the DA conversion to the center channel.
DEG2/	Deglitch signal. DEG2/ directs the DA conversion to the left rear channel.
DEG3/	Deglitch signal. DEG3/ directs the DA conversion to the right rear channel.
HLD/	Hold signal. Used to set up the DACs for either A to D or D to A conversion.
HOLD	Same as HLD/ but inverted.
HOLD/	Same as HLD/.
PCLK0	Programmable clock. Used with DEG1/ to generate DEG2/ and DEG3/.
SWAIT/	Slave wait signal. Synchronizes the Slave Z80 to Lexichip DSP algorithms.
WC/	Word Clock signal. Indicates the beginning of a conversion cycle.

Video Circuitry Signals

Signal	Description
HSYNC/	Horizontal synchronizing signal. (15.734 kHz, NTSC)
SCLK	Shift Clock for parallel to serial shift register.
VCLK	Shift clock for serial data transfer to the video overlay chip.
VCS/	Chip select signal for video overlay chip.
VDATA	Serial data for overlay chip.
VIDDET	Video detect signal. Active "1" if video signal is present at the inputs.
VIDEO/	1I/O decoded select signal for the On-Screen Display port. Address
VSYNC/	Vertical synchronizing signal. (59.94 Hz, NTSC)

LCD Signals

Signal	Description
CONADJ	Contrast adjust signal
CONTRAST/	Select signal for the contrast port
LCDEN/	Non inverted LCDEN
LCDEN	Data Latch signal for the LCD
BKLTEN/	Enable signal for LCD backlight Active "0" for LCD backlight on.
ILED	Power for LCD Backlight

Front Panel Signals

Signal	Description
ROWSEL	Front Panel LED Row Select signal
COLSEL	Front Panel LED Column Select signal
KEYSTAT/	Front Panel Key Status select signal
IRDATA	Serial Data stream from IR detector
LEDC1	Front Panel LED Column 1
LEDC2	Front Panel LED Column 2
LEDC3	Front Panel LED Column 3
LEDC4	Front Panel LED Column 4
SWI1	Front Panel Switch Column 1
SWI2	Front Panel Switch Column 2
LEDR1	Front Panel LED Row 2
LEDR2	Front Panel LED Row 3
LEDR3	Front Panel LED Row 4
LEDR4	Front Panel LED Row 5
LEDR5	Front Panel LED Row 6
LEDR6	Front Panel LED Row 7

6

Parts List

Parts List

DIGITAL BOARD — Rev. 4

PART NO.	DESCRIPTION	QTY	REFERENCE
RESISTORS			
201-00432	RES,TRM,ST,PC,5K,SA,CER	1	R16
202-00505	RES,CF,5%,1/4W,10 OHM	1	R7
202-00508	RES,CF,5%,1/4W,33 OHM	3	R27,28,40
202-00509	RES,CF,5%,1/4W,47 OHM	1	R22
202-00510	RES,CF,5%,1/4W,51 OHM	1	R21
202-00511	RES,CF,5%,1/4W,68 OHM	1	R41
202-00512	RES,CF,5%,1/4W,75 OHM	1	R18
202-00514	RES,CF,5%,1/4W,100 OHM	5	R4,8,46,62,80
202-00515	RES,CF,5%,1/4W,150 OHM	1	R25
202-00521	RES,CF,5%,1/4W,330 OHM	2	R68,74
202-00524	RES,CF,5%,1/4W,470 OHM	2	R9,52
202-00529	RES,CF,5%,1/4W,1K OHM	10	R14,15,20,29,49,57,59,61,67,83
202-00530	RES,CF,5%,1/4W,1.2K OHM	1	R50
202-00531	RES,CF,5%,1/4W,1.5K OHM	1	R79
202-00534	RES,CF,5%,1/4W,2.2K OHM	4	R1,2,11,64
202-00538	RES,CF,5%,1/4W,3.3K OHM	3	R43,45,48
202-00540	RES,CF,5%,1/4W,3.9K OHM	1	R60
202-00543	RES,CF,5%,1/4W,5.1K OHM	2	R77,78
202-00545	RES,CF,5%,1/4W,6.8K OHM	1	R17
202-00547	RES,CF,5%,1/4W,8.2K OHM	1	R55
202-00549	RES,CF,5%,1/4W,10K OHM	7	R24,30,63,65,66,69,70
202-00551	RES,CF,5%,1/4W,12K OHM	1	R13
202-00554	RES,CF,5%,1/4W,16K OHM	1	R53
202-00555	RES,CF,5%,1/4W,20K OHM	2	R3,76
202-00558	RES,CF,5%,1/4W,27K OHM	1	R12
202-00563	RES,CF,5%,1/4W,47K OHM	1	R6
202-00570	RES,CF,5%,1/4W,100K OHM	5	R5,71-73,75
202-00580	RES,CF,5%,1/4W,1M OHM	1	R10
202-08077	RES,CF,5%,1/4W,43 OHM	2	R44,51
203-00456	RES,MF,1%,1/8W,1.00K OHM	1	R56
203-00460	RES,MF,1%,1/8W,2.15K OHM	1	R58
205-01485	RES,NET,DIP,2%,33X8	1	RP5
205-02900	RES,NET,DIP,2%,120X8	6	RP1-4,7,8
205-07157	RES,NET,SIP,2%,BUS EL,4.7KX9	1	RP6
CAPACITORS			
240-00608	CAP,ELEC,2.2uF,50V,RAD	4	C18,50,57,58
240-00613	CAP,ELEC,22uF,25V,RAD	1	C65
240-00614	CAP,ELEC,47uF,16V,RAD	3	C5,29,73
240-00617	CAP,ELEC,470uF,16V,RAD	1	C19
240-01262	CAP,ELEC,330uF,25V,RAD	4	C4,33,59,77
240-06611	CAP,ELEC,1000uF,25V,RAD	1	C74
244-00660	CAP,MYL,.01uF,100V,10%,RAD	1	C13
244-00662	CAP,MYL,.1uF,5%,RAD	2	C20,31
244-04960	CAP,MYL,1uF,5%,RAD	1	C62
245-03609	CAP,CER,.1uF,50V,Z5U,AX	49	C2,3,6,7,10,11,14-16,21-25,27,28, C30,32,35-39,42-45,47,49,51,54,56, C61,63,64,67,70,72,75,76,78-86
245-03868	CAP,CER,33pF,100V,COG,10%,AX	2	C26,52
245-03869	CAP,CER,100pF,100V,COG,10%,AX	1	C34
245-03871	CAP,CER,1000pF,100V,X7R,10%,AX	2	C1,66
245-07544	CAP,CER,18pF,100V,COG,10%,AX	2	C55,60

PART NO.	DESCRIPTION	QTY	REFERENCE
245-08171	CAP,CER,680pF,50V,5%,NPO	2	C9,12
246-09419	CAP,TRIM,2.8-10pF,VAR	1	C53
INDUCTORS			
270-06320	INDUCTOR,22uH,SHIELDED	1	L3
270-06671	FERRITE CHOKE,2.5 TURN	6	FB1-6
270-07725	INDUCTOR,47UH,SHIELDED	2	L1,2
DIODES			
300-01029	DIODE,1N914 AND 4148	11	CR1,3-7,11,13-16
300-01032	DIODE,1N5404	1	CR10
300-02401	DIODE,BAR 35,SCHOTTKY,LOW VF	4	CR2,9,12,17
300-07132	DIODE,ZENER,3.9V,1N748	1	CR8
TRANSISTORS			
310-01007	TRANSISTOR,2N3904	8	Q2,3,5,7-9,12,13
310-01008	TRANSISTOR,2N3906	4	Q1,4,10,11
INTEGRATED CIRCUITS			
330-03482	IC,DIGITAL,74HC04	1	U4
330-03581	IC,DIGITAL,74HC138	2	U12,15
330-03585	IC,DIGITAL,74HC14	1	U39
330-03611	IC,DIGITAL,74HC273	1	U3
330-03638	IC,DIGITAL,74HC393	1	U41
330-04509	IC,DIGITAL,74HC74	1	U6
330-06204	IC,DIGITAL,LEXICHIP 1	1	U30
330-06879	IC,DIGITAL,74HCT574	4	U8-11
330-07068	IC,DIGITAL,74HC165	1	U38
330-07260	IC,DIGITAL,74HC32	2	U5,14
330-07537	IC,DIGITAL,74AC08	1	U17
330-07713	IC,DIGITAL,74HC174	1	U37
330-07714	IC,DIGITAL,74AC245	1	U36
330-07715	IC,DIGITAL,74HC541	2	U2,31
330-08169	IC,DIGITAL,74HC175	1	U7
330-08170	IC,DIGITAL,74AC157	4	U26-29
345-06160	IC,INTER,LU59002,IR RCVR	1	U23
345-08335	IC,INTER,NJM2217D,VID SYNC SEP	1	U1
345-08336	IC,INTER,MB88324AP-K1,VID OVLY	1	U32
350-07490	IC,DRAM,64KX4,100NS	5	U18-22
350-08567	IC,GAL,16V8,CP-3,VIDEO,V1.00	1	U40
350-08568	IC,GAL,16V8,CP-3,MSTR,V2.00	1	U13
350-08569	IC,GAL,16V8,CP-3,SLAVE,V1.00	1	U16
350-08570	IC,SRAM,6264,8KX8,100NS,LPS	2	U33,35
350-08696	IC,ROM,27C512,CP-3,V3.40	1	U25
365-04834	IC,uPROC,Z80B,CMOS,6MHZ	2	U24,34
CRYSTALS			
390-03339	CRYSTAL,18.432 MHz	1	Y1
390-08168	CRYSTAL,7.15909 MHz,PAR	1	Y2
FANS/MOTORS/RELAYS			
410-08340	RELAY,2P2T,LOW LEVEL,MINI,5V	3	RY1-3
BATTERIES			
460-04285	BAT,LITH,3V@160mAh,VERT COIN	1	BAT1

PART NO.	DESCRIPTION	QTY	REFERENCE
DIGITAL BOARD — Rev 4 Continued			
CONNECTORS			
490-02356	CONN,JUMPER,.1X025,2FCG	2	W1,2
510-00826	CONN,POST,156X045,HDR,4MCG,LOK	1	J9
510-03961	CONN,POST,100X025,HDR,2MCG	3	W1-3
510-06168	CONN,POST,079,HDR,15MC	7	J1-5,7,8
510-06568	CONN,POST,079,HDR,6MC	1	J10
510-08344	CONN,RCA,PCRA,1FCGX4,YEL	1	J6
SOCKETS			
520-00946	IC SCKT,40 PIN,PC,LO-PRO	2	U24,34
520-01361	IC SCKT,20 PIN,PC,LO-PRO	3	U13,16,40
520-01458	IC SCKT,28 PIN,PC,LO-PRO	3	U25,33,35
520-02177	IC SCKT,18 PIN,PC,LO-PRO	5	U18-22
520-06184	IC SCKT,PLCC,84 PIN	1	U30
620-06897	LUG,PCB/#2 INT STAR	1	TP3
710-08129	PC BD,DIGITAL,CP-3	1	
720-02751	TAPE,FOAM,DBL-STK,1/8THX3/4W	1	.5" Y1
740-02469	LABEL,SN,PCB,.9X.25	1	

DIGITAL BOARD — Rev 3

PART NO.	DESCRIPTION	QTY	REFERENCE
RESISTORS			
201-00432	RES,TRM,ST,PC,5K,SA,CER	1	R16
202-00505	RES,CF,5%,1/4W,10 OHM	1	R7
202-00508	RES,CF,5%,1/4W,33 OHM	3	R27,28,40
202-00511	RES,CF,5%,1/4W,68 OHM	1	R41
202-00512	RES,CF,5%,1/4W,75 OHM	2	R18,44
202-00514	RES,CF,5%,1/4W,100 OHM	6	R4,8,22,46,51,62
202-00521	RES,CF,5%,1/4W,330 OHM	2	R25,68
202-00524	RES,CF,5%,1/4W,470 OHM	1	R9
202-00529	RES,CF,5%,1/4W,1K OHM	12	R14,15,20,29,49,52,56,57,59,61,67,74
202-00533	RES,CF,5%,1/4W,2K OHM	2	R32,38
202-00534	RES,CF,5%,1/4W,2.2K OHM	5	R1,2,11,58,64
202-00538	RES,CF,5%,1/4W,3.3K OHM	3	R43,45,48
202-00540	RES,CF,5%,1/4W,3.9K OHM	1	R60
202-00543	RES,CF,5%,1/4W,5.1K OHM	3	R19,77,78
202-00547	RES,CF,5%,1/4W,8.2K OHM	1	R55
202-00549	RES,CF,5%,1/4W,10K OHM	9	R17,24,30,54,63,65,66,69,70
202-00551	RES,CF,5%,1/4W,12K OHM	1	R13
202-00554	RES,CF,5%,1/4W,16K OHM	1	R53
202-00555	RES,CF,5%,1/4W,20K OHM	3	R3,50,76
202-00558	RES,CF,5%,1/4W,27K OHM	1	R12
202-00563	RES,CF,5%,1/4W,47K OHM	1	R6
202-00570	RES,CF,5%,1/4W,100K OHM	5	R5,71-73,75
202-00580	RES,CF,5%,1/4W,1M OHM	1	R10
202-01225	RES,CF,5%,1/4W,6.2K OHM	1	R37
202-08190	RES,CF,5%,1/4W,110 OHM	1	R21
205-01485	RES,NET,DIP,2%,33X8	5	RP1-5
205-02900	RES,NET,DIP,2%,120X8	2	RP7,8
205-07157	RES,NET,SIP,2%,BUS EL,4.7KX9	1	RP6
CAPACITORS			
240-00608	CAP,ELEC,2.2uF,50V,RAD	5	C17,18,50,57,58
240-00613	CAP,ELEC,22uF,25V,RAD	1	C65
240-00614	CAP,ELEC,47uF,16V,RAD	3	C5,19,29

PART NO.	DESCRIPTION	QTY	REFERENCE
240-01262	CAP,ELEC,330uF,25V,RAD	3	C4,33,59
244-00660	CAP,MYL,.01uF,100V,10%,RAD	1	C13
244-00662	CAP,MYL,.1uF,5%,RAD	3	C8,20,31
244-04960	CAP,MYL,1uF,5%,RAD	1	C62
245-03609	CAP,CER,.1uF,50V,Z5U,AX	37	C2,3,6,7,10,11,14-16,21-25,27,28,30,32, C35-39,42-45,47,49,51,54,56,61, C63,64,67,70
245-03868	CAP,CER,33pF,100V,COG,10%,AX	1	C52
245-03869	CAP,CER,100pF,100V,COG,10%,AX	1	C34
245-03871	CAP,CER,1000pF,100V,X7R,10%,AX	2	C1,66
245-07544	CAP,CER,18pF,100V,COG,10%,AX	3	C26,55,60
245-08171	CAP,CER,680pF,50V,5%,NPO	2	C9,12
245-08470	CAP,CER,15pF,100V,COG,5%,AX	2	C53,71
INDUCTORS			
270-06320	INDUCTOR,22uH,SHIELDED	1	L3
270-06671	FERRITE CHOKE,2.5 TURN	5	FB1-5
DIODES			
300-01029	DIODE,1N914 AND 4148	11	CR1,3-7,11,13-16
300-01032	DIODE,1N5404	1	CR10
300-02401	DIODE,BAR 35,SCHOTTKY,LOW VF	3	CR2,9,12
300-07132	DIODE,ZENER,3.9V,1N748	1	CR8
TRANSISTORS			
310-01007	TRANSISTOR,2N3904	9	Q2,3,5-9,12,13
310-01008	TRANSISTOR,2N3906	4	Q1,4,10,11
INTEGRATED CIRCUITS			
330-03482	IC,DIGITAL,74HC04	1	U4
330-03581	IC,DIGITAL,74HC138	2	U12,15
330-03585	IC,DIGITAL,74HC14	1	U39
330-03611	IC,DIGITAL,74HC273	1	U3
330-03638	IC,DIGITAL,74HC393	1	U41
330-04509	IC,DIGITAL,74HC74	1	U6
330-06204	IC,DIGITAL,LEXICHIP 1	1	U30
330-07068	IC,DIGITAL,74HC165	1	U38
330-07260	IC,DIGITAL,74HC32	2	U5,14
330-07536	IC,DIGITAL,74HC574	4	U8-11
330-07537	IC,DIGITAL,74AC08	1	U17
330-07713	IC,DIGITAL,74HC174	1	U37
330-07714	IC,DIGITAL,74AC245	1	U36
330-07715	IC,DIGITAL,74HC541	2	U2,31
330-08169	IC,DIGITAL,74HC175	1	U7
330-08170	IC,DIGITAL,74AC157	4	U26-29
345-06160	IC,INTER,LU59002,IR RCVR	1	U23
345-08335	IC,INTER,NJM2217D,VID SYNC SEP	1	U1
345-08336	IC,INTER,MB88324AP-K1,VID OVLY	1	U32
350-07490	IC,DRAM,64KX4,100NS	5	U18-22
350-08567	IC,GAL,16V8,CP-3,VIDEO,V1.00	1	U40
350-08568	IC,GAL,16V8,CP-3,MSTR,V2.00	1	U13
350-08569	IC,GAL,16V8,CP-3,SLAVE,V1.00	1	U16
350-08570	IC,SRAM,6264,8KX8,100NS,LPS	2	U33,35
350-08696	IC,ROM,27C512,CP-3,V3.30	1	U25
365-04834	IC,uPROC,Z80B,CMOS,6MHZ	2	U24,34
CRYSTALS			
390-03339	CRYSTAL,18.432 MHz	1	Y1
390-08168	CRYSTAL,7.15909 MHz,PAR	1	Y2

PART NO.	DESCRIPTION	QTY	REFERENCE
DIGITAL BOARD — Rev 3 Continued			
FANS/MOTORS/RELAYS			
410-08340	RELAY,2P2T,LOW LEVEL,MINI,5V	3	RY1-3
BATTERIES			
460-04285	BAT,LITH,3V@160mAh,VERT COIN	1	BAT1
CONNECTORS			
490-02356	CONN,JUMPER,.1X025,2FCG	2	W1,2
510-00826	CONN,POST,156X045,HDR,4MCG,LOK	1	J9
510-03961	CONN,POST,100X025,HDR,2MCG	3	W1-3
510-06168	CONN,POST,079,HDR,15MC	7	J1-5,7,8
510-06568	CONN,POST,079,HDR,6MC	1	J10
510-08344	CONN,RCA,PCRA,1FCGX4,YEL	1	J6
520-00946	IC SCKT,40 PIN,PC,LO-PRO	2	U24,34
520-01361	IC SCKT,20 PIN,PC,LO-PRO	3	U13,16,40
520-01458	IC SCKT,28 PIN,PC,LO-PRO	3	U25,33,35
520-02177	IC SCKT,18 PIN,PC,LO-PRO	5	U18-22
520-06184	IC SCKT,PLCC,84 PIN	1	U30
620-06897	LUG,PCB/#2 INT STAR	1	TP3
710-08129	PC BD,DIGITAL,CP-3	1	
720-02751	TAPE,FOAM,DBL-STK,1/8THX3/4W	1	Y1

LOWER ANALOG BOARD

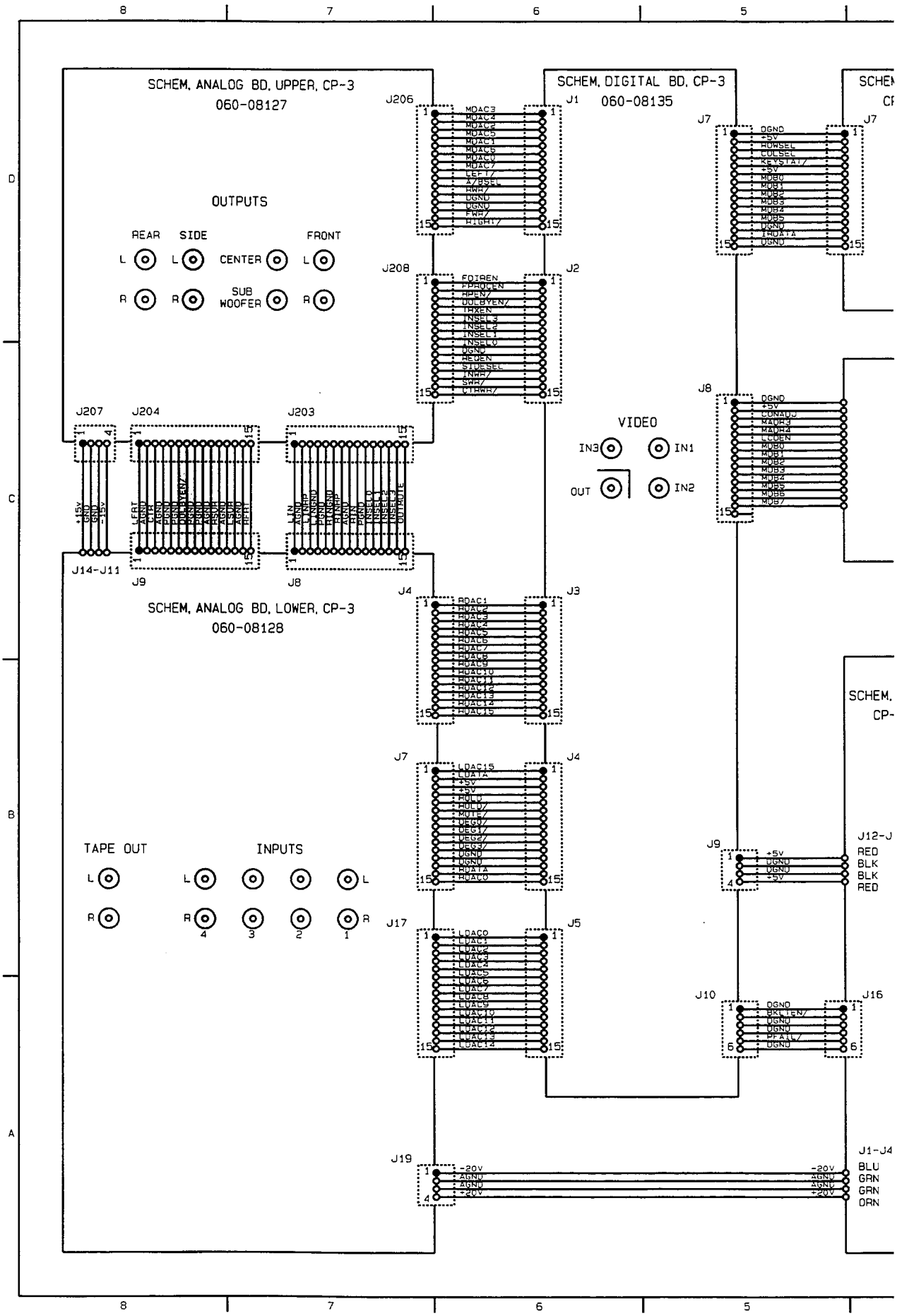
PART NO.	DESCRIPTION	QTY	REFERENCE
RESISTORS			
201-06098	RES,TRM,ST,PC,100K OHM,SA,CER	2	R60,120
202-00514	RES,CF,5%,1/4W,100 OHM	10	R11,20,39,43,55,62,75,76,100,105
202-00523	RES,CF,5%,1/4W,390 OHM	1	R113
202-00525	RES,CF,5%,1/4W,510 OHM	6	R18,23,71,77,88,126
202-00529	RES,CF,5%,1/4W,1K OHM	6	R38,44,56,70,86,111
202-00533	RES,CF,5%,1/4W,2K OHM	3	R14,52,53
202-00549	RES,CF,5%,1/4W,10K OHM	11	R12,13,15,29,89,91,93,98,99,101,112
202-00555	RES,CF,5%,1/4W,20K OHM	2	R90,92
202-00570	RES,CF,5%,1/4W,100K OHM	11	R8,21,24,40,49,50,61,72,73,79,95
202-00579	RES,CF,5%,1/4W,470K OHM	6	R2,3,19,30,51,114
202-01160	RES,CF,5%,1/4W,43K OHM	3	R37,94,109
203-00457	RES,MF,1%,1/8W,1.50K OHM	11	R1,22,25,34,54,66,83,87,96,97,125
203-00459	RES,MF,1%,1/8W,2.00K OHM	4	R68,69,84,85
203-00478	RES,MF,1%,1/8W,13.7K OHM	2	R4,31
203-01136	RES,MF,1%,1/8W,5.76K OHM	2	R65,81
203-01143	RES,MF,1%,1/8W,2.49K OHM	10	R10,17,35,36,41,42,110,115,119,124
203-01249	RES,MF,1%,1/8W,5.23K OHM	2	R58,103
203-01489	RES,MF,1%,1/8W,499 OHM	5	R16,27,47,107,117
203-02611	RES,MF,1%,1/8W,5.62K OHM	12	R5,6,32,33,45,57,67,82,102,104,122,123
203-02702	RES,MF,1%,1/8W,8.66K OHM	2	R64,80
203-03348	RES,MF,1%,1/8W,9.09K OHM	1	R121
203-03974	RES,MF,1%,1/8W,3.92K OHM	2	R63,78
203-06885	RES,MF,1%,1/8W,4.53K OHM	5	R9,26,46,106,116
203-07557	RES,MF,1%,1/8W,806 OHM	5	R7,28,48,108,118
203-08191	RES,MF,1%,1/8W,2.21K OHM	2	R59,74
CAPACITORS			
240-00608	CAP,ELEC,2.2uF,50V,RAD	1	C61
240-00613	CAP,ELEC,22uF,25V,RAD	11	C10,13,15,16,27,50,60,64,72,73,80
240-01262	CAP,ELEC,330uF,25V,RAD	4	C86-88,106

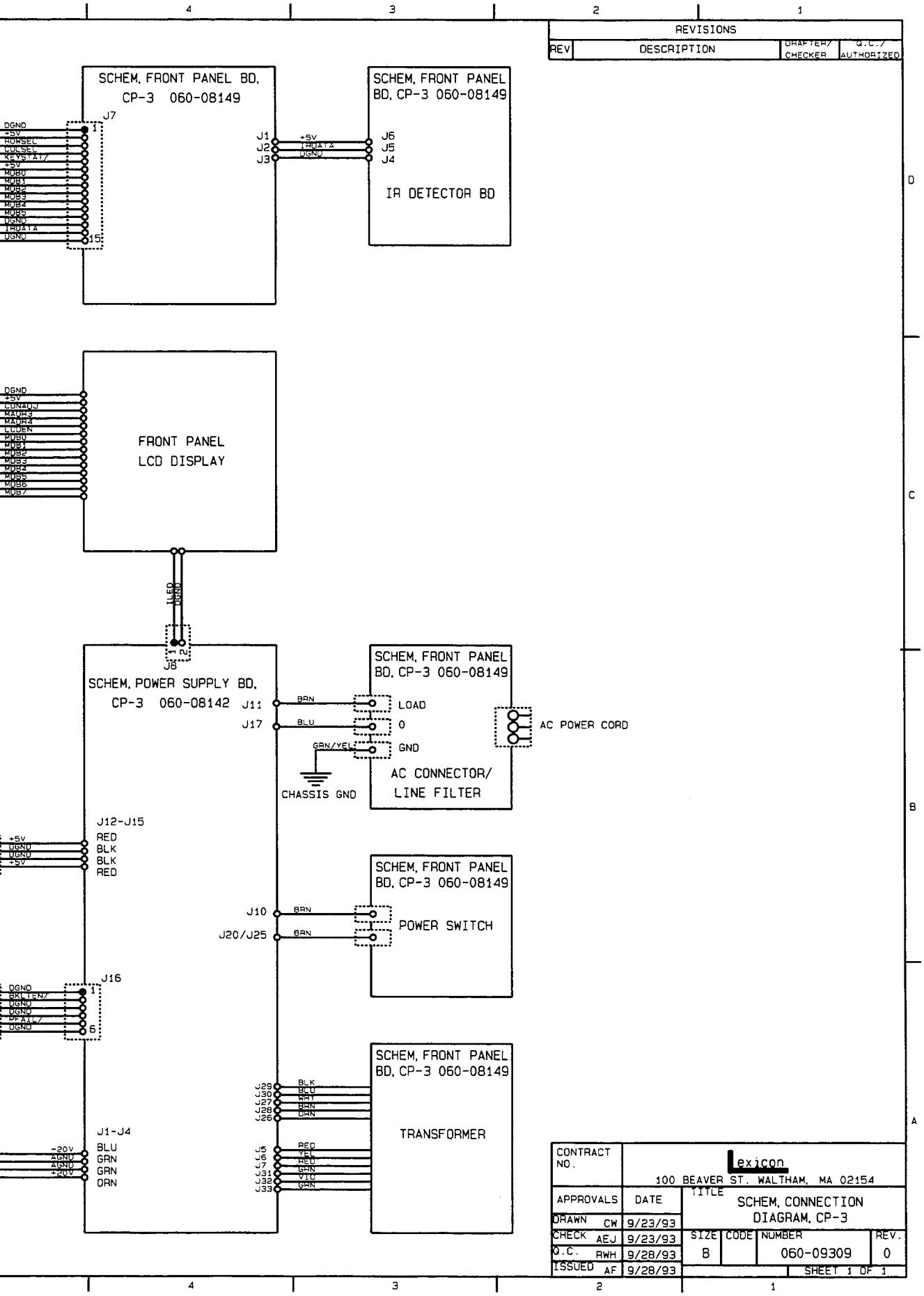
PART NO.	DESCRIPTION	QTY	REFERENCE
240-04277	CAP,ELEC,330uF,50V,RAD	2	C94,96
240-06096	CAP,ELEC,10uF,25V,RAD,NON-POL	5	C1,20,32,,74,105
240-07335	CAP,ELEC,47uF,25V,RAD,NON-POL	4	C29,46,67,71
244-01166	CAP,PP,240pF,2.5%	5	C9,14,33,79,99
244-02486	CAP,PP,510pF,160V,2.5%,AX	2	C54,59
244-06176	CAP,MYL,.047uF,5%,RAD	5	C6,18,39,77,104
244-06883	CAP,MYL,.01uF,5%,RAD	4	C23,49,63,76
244-06884	CAP,MYL,3300pF,5%,RAD	2	C2,26
245-03609	CAP,CER,.1uF,50V,Z5U,AX	38	C3,4,8,11,12,17,21,28,34,35,37,38,40,41, C43,45,47,48,52,56,57,65,66,69,70,82,84, C89-91,95,97,98,100,101,103,406,407
245-03867	CAP,CER,10pF,100V,COG,10%,AX	6	C22,36,75,92,C68,81
245-03868	CAP,CER,33pF,100V,COG,10%,AX	9	C5,25,30,44,51,62,78,85,102
245-03869	CAP,CER,100pF,100V,COG,10%,AX	10	C7,19,24,31,42,53,55,58, C83,93
INDUCTORS			
270-00779	FERRITE,BEAD	2	FB1,2
270-07725	INDUCTOR,47UH,SHIELDED	4	L1-4
DIODES			
300-01029	DIODE,1N914 AND 4148	27	CR1-16,18-28
300-01030	DIODE,1N4004 AND 4005	4	CR29-32
300-01154	DIODE,ZENER,5.1V,1N751	1	CR33
300-07132	DIODE,ZENER,3.9V,1N748	1	CR17
TRANSISTORS			
310-01007	TRANSISTOR,2N3904	2	Q6,8
310-01008	TRANSISTOR,2N3906	2	Q2,5
310-06612	TRANSISTOR,J108	2	Q1,4
310-08178	TRANSISTOR,2SC3381,DUAL NPN,LN	2	Q3,7
INTEGRATED CIRCUITS			
340-01183	IC,LINEAR,LF 356	2	U14,18
340-01566	IC,LINEAR,LF353,DUAL OP AMP	4	U1,7,9,22
340-07565	IC,LINEAR,MC33077	5	U3,8,15,20,21
340-08179	IC,LINEAR,LM319,DUAL HS COMP	2	U4,19
340-08189	IC,LINEAR,AD744	2	U10,24
346-06896	IC,SS SWITCH,74HC4053	3	U6,16,23
346-08337	IC,SS SWITCH,SSM2402P	4	U2,5,13,17
346-08339	IC,SS SWITCH,DG444DJ	2	U11,28
355-06038	DAC,PCM54HP	2	U12,25
380-08193	MOD,LPF,LC,7P,20kHz	5	LPF1-3,6,7
380-08194	MOD,LPF,LC,9P,18kHz	2	LPF4,5
CONNECTORS			
510-00826	CONN,POST,156X045,HDR,4MCG,LOK	1	J19
510-06168	CONN,POST,079,HDR,15MC	5	J4,7-9,17
510-06185	CONN,RCA,PCRA,1FCGX4,WHT/RED	2	J2,6
510-07785	CONN,RCA,PCRA,1FCGX2,VERT	1	J16
SOCKETS			
520-01458	IC SCKT,28 PIN,PC,LO-PRO	2	U12,25
HARDWARE			
620-06897	LUG,PCB/#2 INT STAR	3	J2,6,16
WIRES/CABLES			
670-01974	WIRE,JMP,22AWG,0.1",NON-INSUL	6	J1,3,5,10,15,18
680-08176	CABLE ASSY,4C,18G,6",SS/HSG	1	LO ANLG - J11-14 TO UP

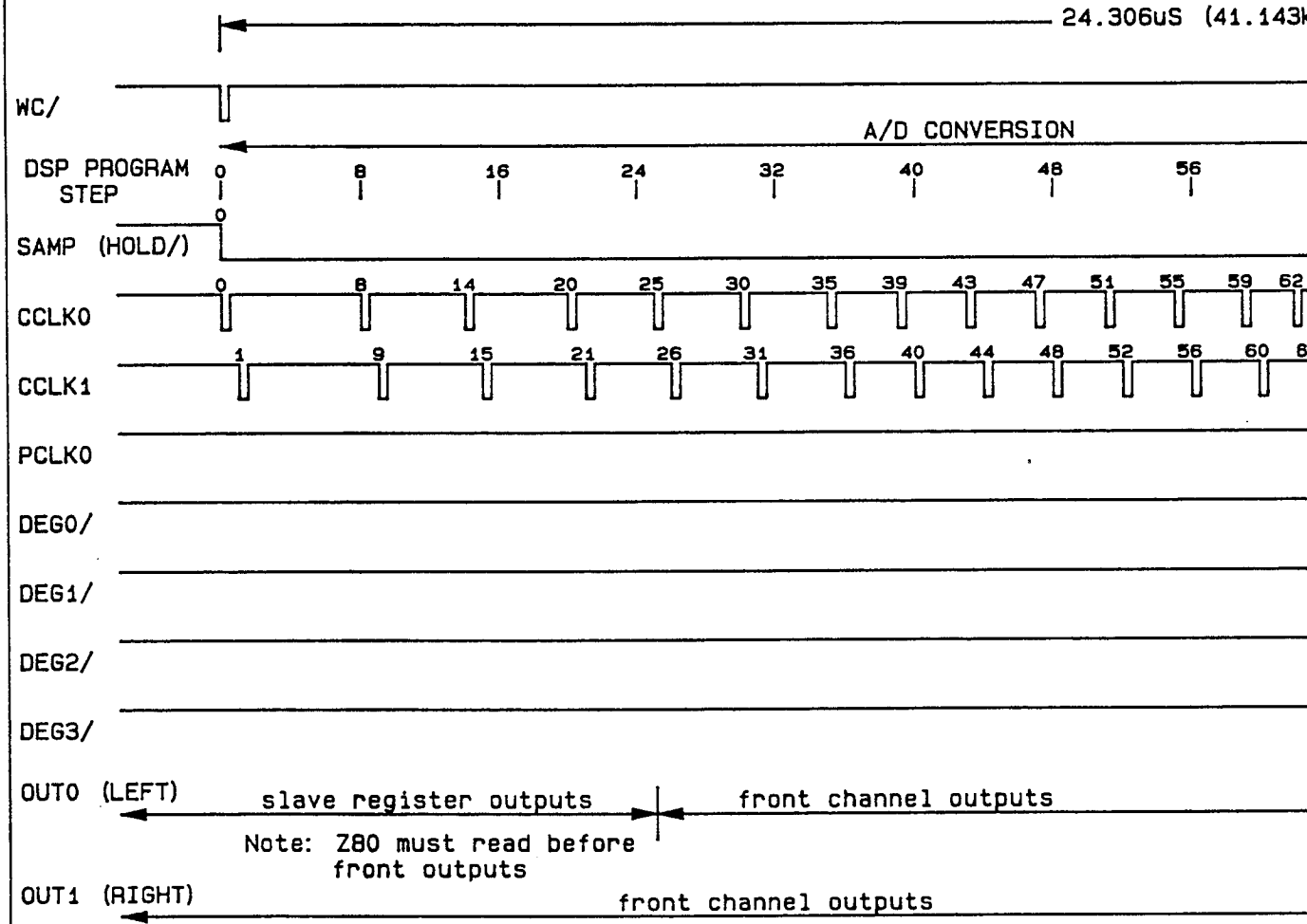
7

Schematics and Assembly Drawings

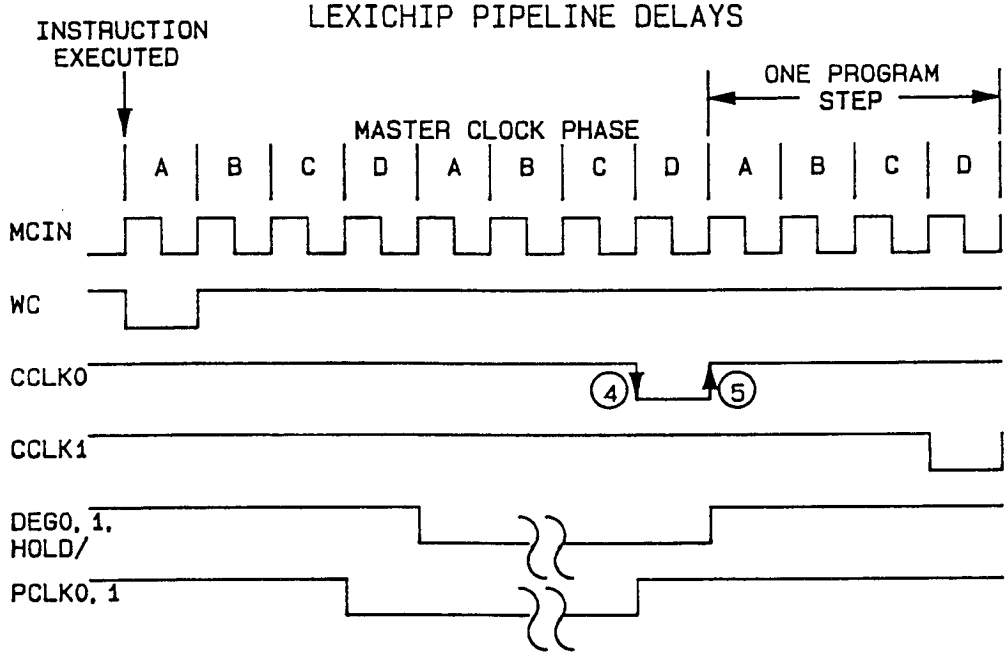
Connection Diagram
Timing Diagram (112)
Timing Diagram (128)
Step
Analog Board - Upper
Analog Board - Lower
Digital Board
Front Panel Board
Power Supply Board
Assy - Chassis
Assy - FP Mechanical


SCHEM, ANALOG BD, UPPER, CP-3
060-08127
OUTPUTS
REAR
SIDE
FRONT
CENTER
SUB WOOFER
J206
J208
J207
J204
J203
J14-J11
J9
J8
SCHEM, ANALOG BD, LOWER, CP-3
060-08128
TAPE OUT
INPUTS
VIDEO
IN3
IN1
OUT
IN2
SCHEM, DIGITAL BD, CP-3
060-08135
J1
J2
J3
J4
J5
J7
J8
J9
J10
J16
J17
J19
J12-J
J1-J4
SCHEM,
CP-


REVISIONS
REV
DESCRIPTION
DRAFTER/ CHECKER
Q.C./ AUTHORIZED
SCHEM, FRONT PANEL BD, CP-3 060-08149
J7
DGND
+5V
HDWSEL
CDLSEL
KEYSTAT/
+5V
MDB0
MDB1
MDB2
MDB3
MDB4
MDB5
DGND
TRDATA
DGND
1
15
J1
J2
J3
+5V
TRDATA
DGND
SCHEM, FRONT PANEL BD, CP-3 060-08149
J6
J5
J4
IR DETECTOR BD
FRONT PANEL LCD DISPLAY
DGND
+5V
CONADJ
MADR3
MADR4
LCDEN
MDB0
MDB1
MDB2
MDB3
MDB4
MDB5
MDB6
MDB7
VLED
DGND
J1
J2
SCHEM, POWER SUPPLY BD, CP-3 060-08142
J11
J17
BRN
BLU
GRN/YEL
CHASSIS GND
SCHEM, FRONT PANEL BD, CP-3 060-08149
LOAD
0
GND
AC CONNECTOR/ LINE FILTER
AC POWER CORD
J12-J15
+5V
DGND
DGND
+5V
RED
BLK
BLK
RED
SCHEM, FRONT PANEL BD, CP-3 060-08149
J10
J20/J25
BRN
BRN
POWER SWITCH
J16
DGND
BRITEN/
DGND
DGND
PFAIL/
DGND
1
6
SCHEM, FRONT PANEL BD, CP-3 060-08149
J29
J30
J27
J28
J26
BLK
BLU
WHT
BRN
ORN
TRANSFORMER
J1-J4
-20V
AGND
AGND
+20V
BLU
GRN
GRN
ORN
J5
J6
J7
J31
J32
J33
RED
YEL
RED
GRN
VIO
GRN
CONTRACT NO.
Lexicon
100 BEAVER ST. WALTHAM, MA 02154
APPROVALS
DATE
TITLE
SCHEM, CONNECTION DIAGRAM, CP-3
DRAWN CW 9/23/93
CHECK AEJ 9/23/93
Q.C. RWH 9/28/93
ISSUED AF 9/28/93
SIZE B
CODE
NUMBER 060-09309
REV. 0
SHEET 1 OF 1
4
3
2
1
D
C
B
A

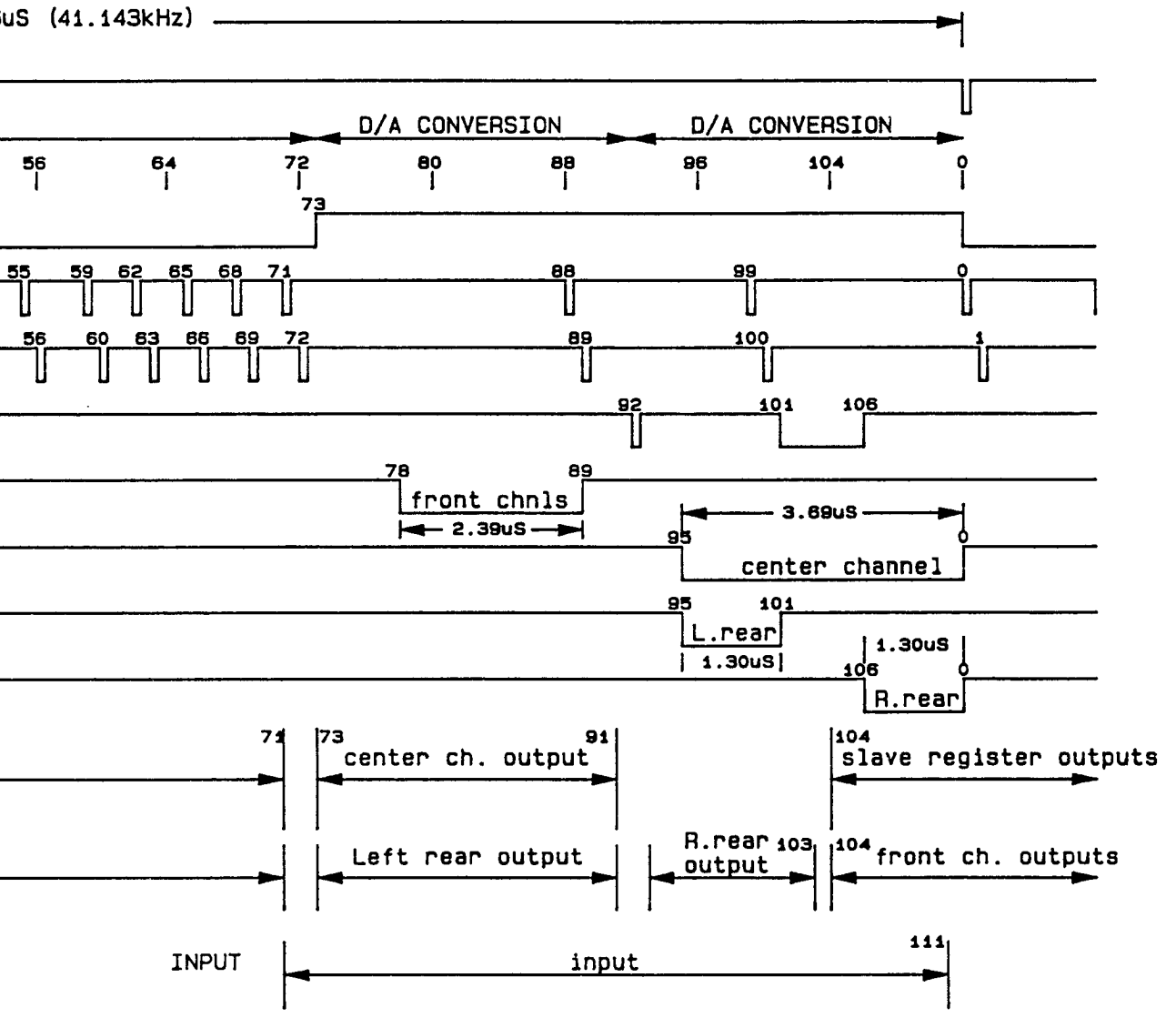


LEXICHIP PIPELINE DELAYS



1. PROPAGATION DE
2. EACH DSP PROGR TO FOUR MASTER
3. PROGRAM STEP N ACTUALLY APPEA FOR RELATIONSH
4. FALLING EDGE O INPUT TO THE S
5. RISING EDGE OF THE CONVERSION

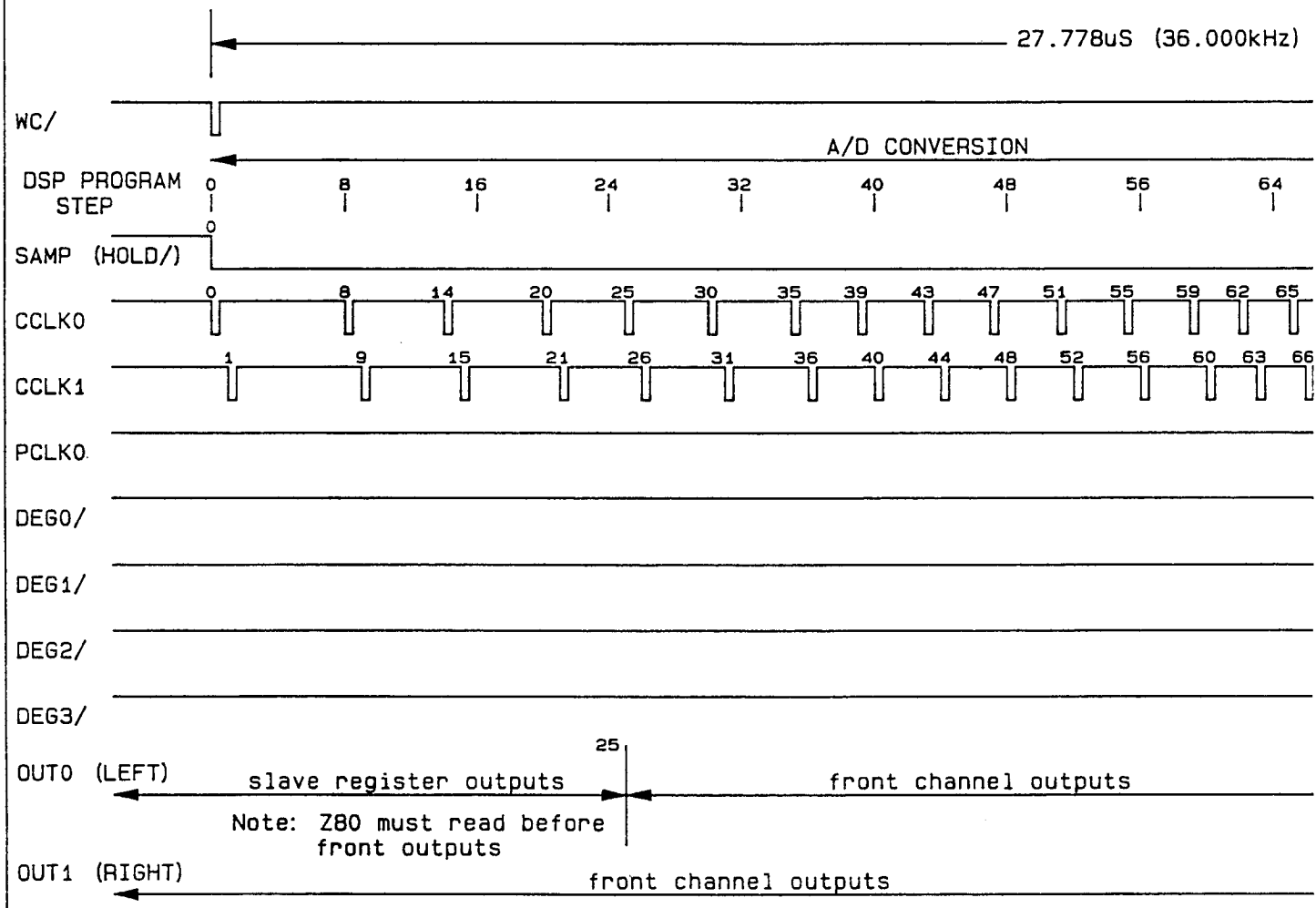
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	RS 4/9/90	
1	RELEASE FOR PRODUCTION	RS 5/14/91 AF 5-17-91	CW 5/21/91 AF 5/21/91



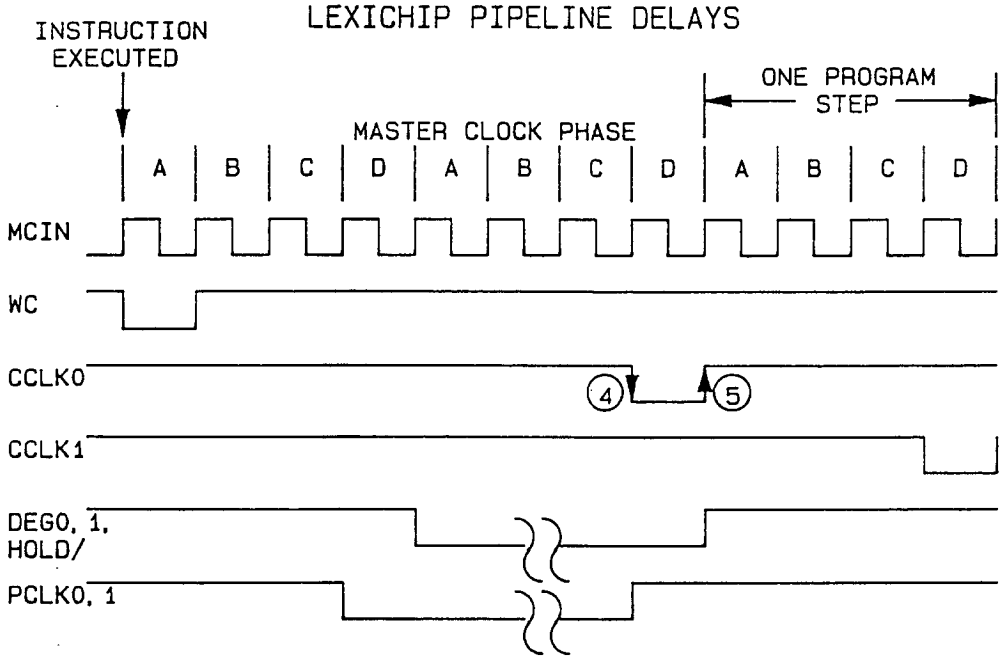
NOTES

PAGATION DELAYS ARE IGNORED.
H DSP PROGRAM STEP IS 217nS LONG, EQUAL FOUR MASTER CLOCK CYCLES.
GRAM STEP NUMBERS SHOWN ARE WHEN SIGNALS UALLY APPEAR. REFER TO PIPELINE DELAYS RELATIONSHIP TO EXECUTION STEP NUMBER.
LING EDGE OF CCLK LATCHES COMPARATOR DATA UT TO THE SAR IN LEXICHIP.
ING EDGE OF CCLK CLOCKS DATA OUTPUT VIA CONVERSION LATCHES TO THE DACS.

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154					
APPROVALS	DATE	TITLE SCHEM, TIMING DIAGRAM, 112 STEP, CP-3				
DRAWN RS	5-14-91					
CHECKED AF	5-17-91	SIZE	CODE	NUMBER	REV.	
ISSUED CW	5-21-91	B		060-08839	1	
Q.C. AF	5-21-91	SHEET 1 OF 1				

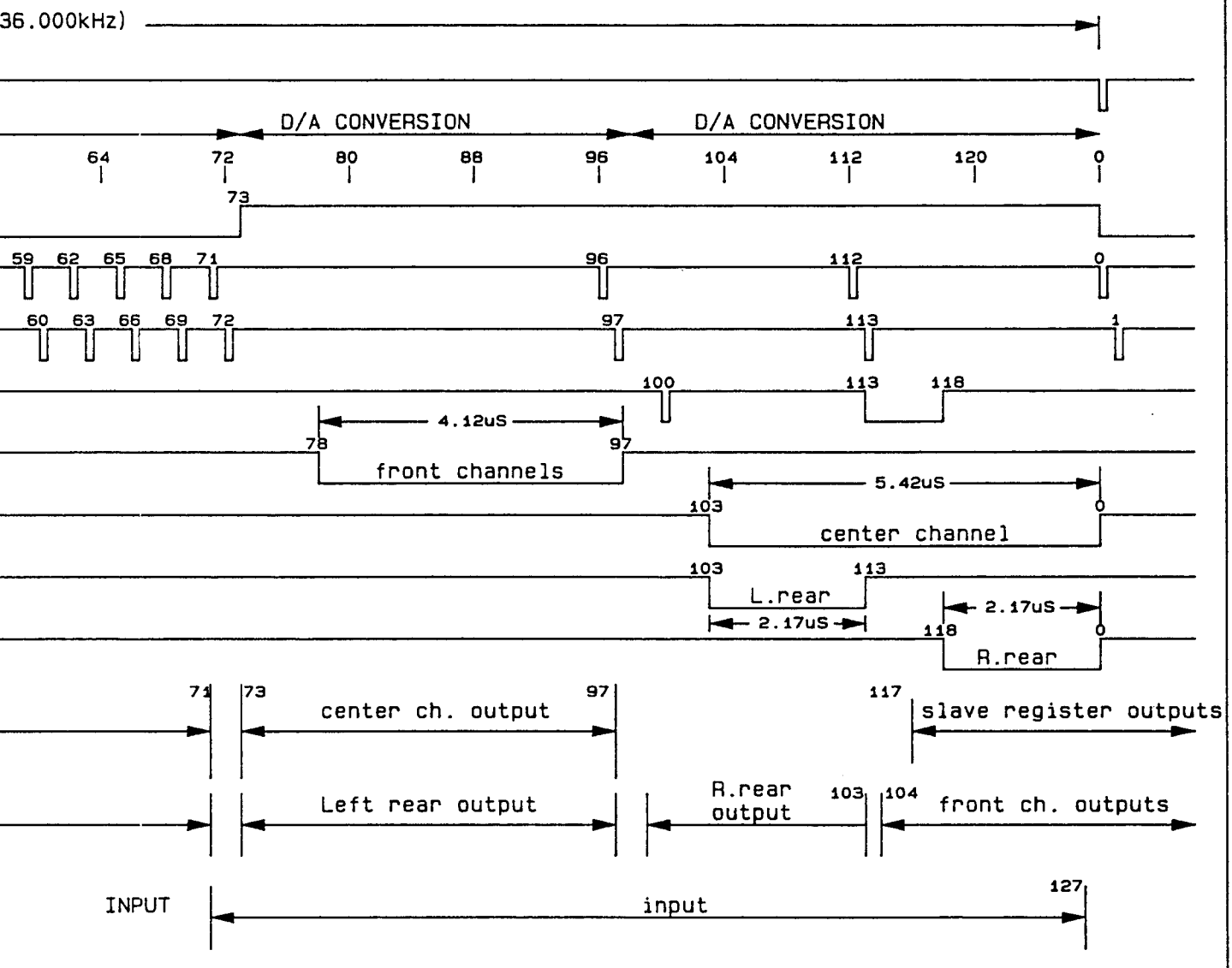


LEXICHIP PIPELINE DELAYS



1. PROPAGATION DELAYS
2. EACH DSP PROGRAM S TO FOUR MASTER CLO
3. PROGRAM STEP NUMBE ACTUALLY APPEAR. FOR RELATIONSHIP T
4. FALLING EDGE OF CC INPUT TO THE SAR I
5. RISING EDGE OF CCL THE CONVERSION LAT

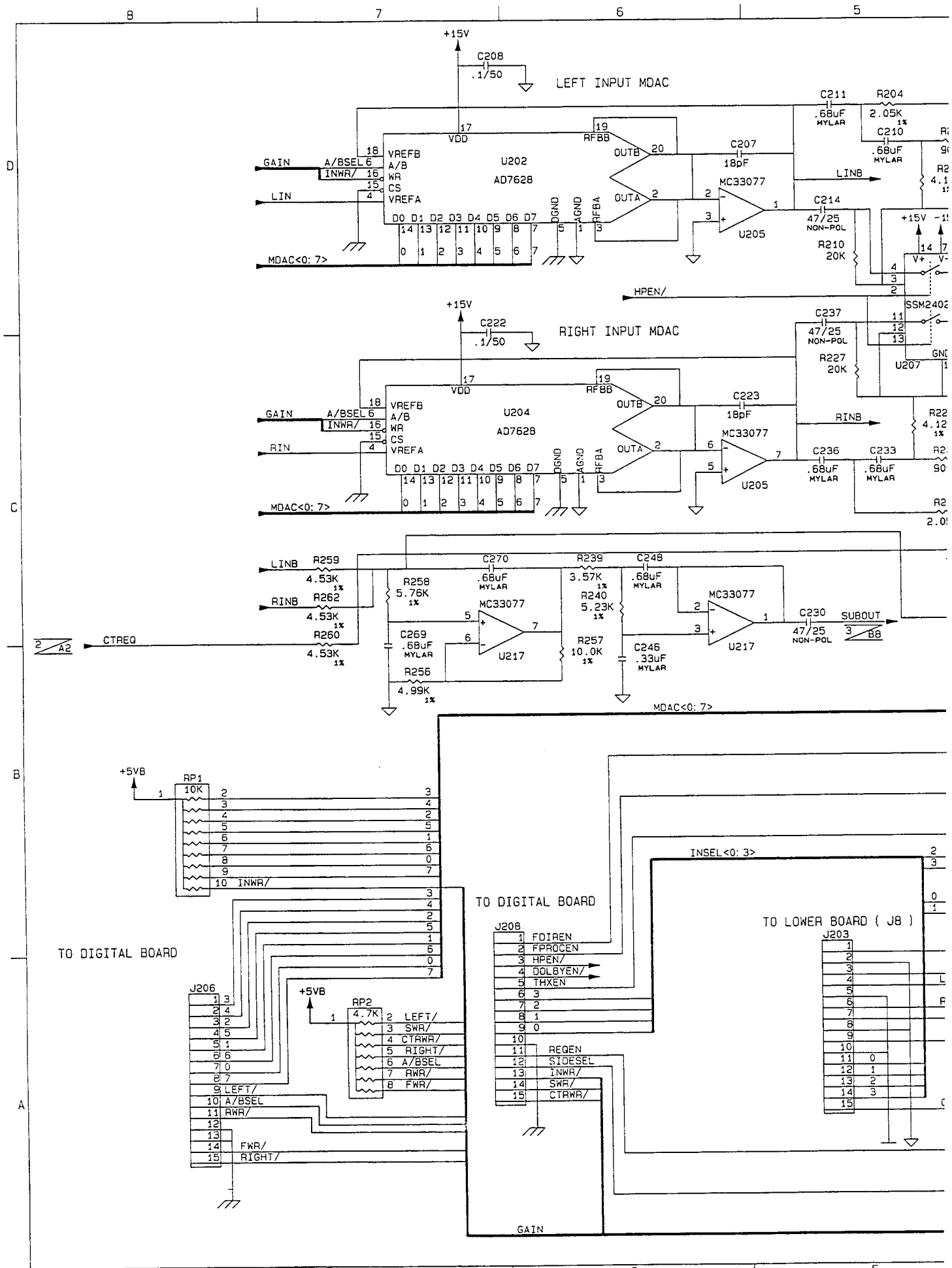
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	RS 4/9/90	
1	RELEASE FOR PRODUCTION	RW 5/16/91 A 5/17/91	CW 5/21/91 A 5/21/91

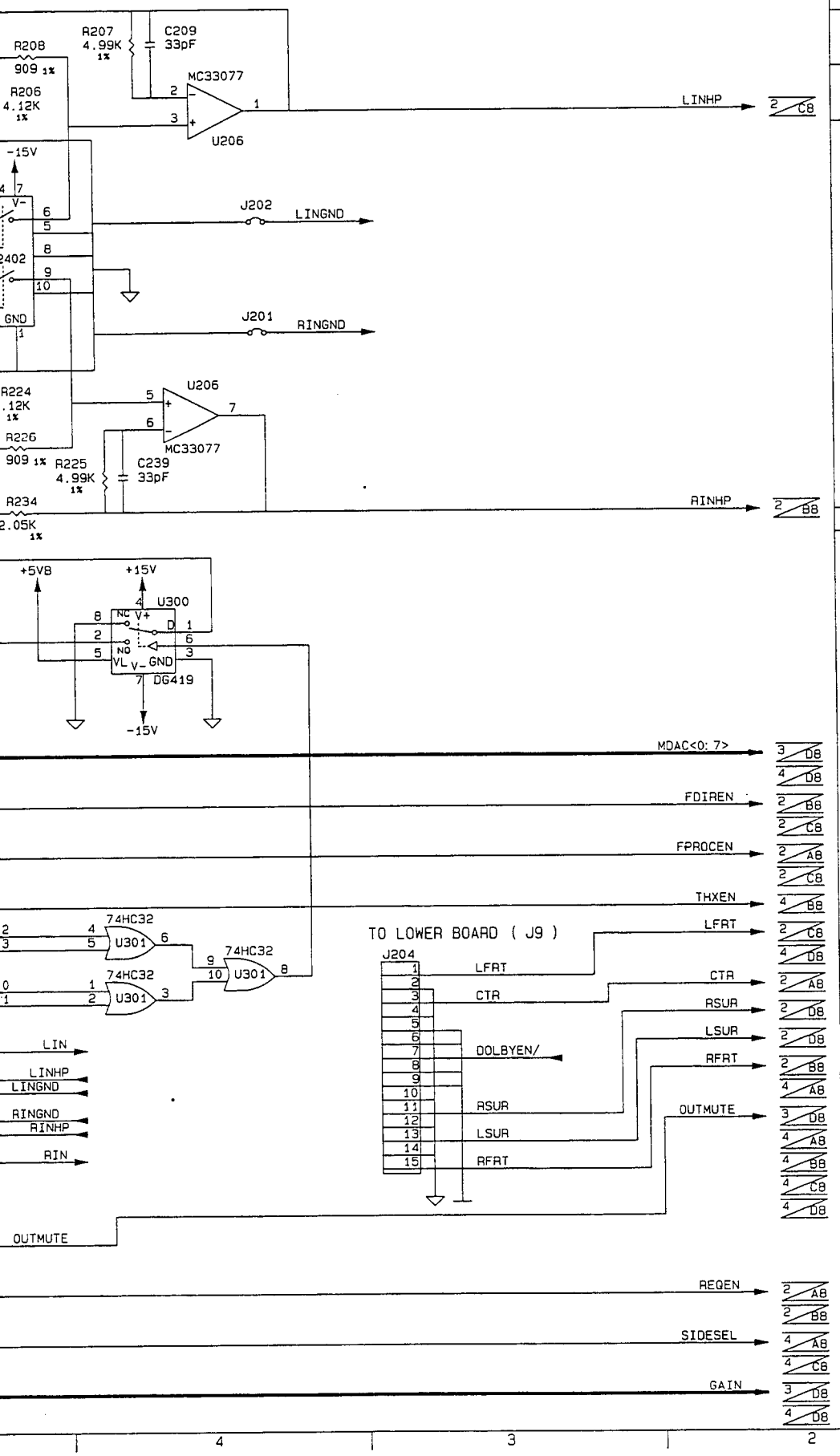


NOTES

TION DELAYS ARE IGNORED.
P PROGRAM STEP IS 217nS LONG, EQUAL MASTER CLOCK CYCLES.
STEP NUMBERS SHOWN ARE WHEN SIGNALS Y APPEAR. REFER TO PIPELINE DELAYS ATIONSHIP TO EXECUTION STEP NUMBER.
EDGE OF CCLK LATCHES COMPARATOR DATA O THE SAR IN LEXICHIP.
EDGE OF CCLK CLOCKS DATA OUTPUT VIA VERSION LATCHES TO THE DACS.

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154					
APPROVALS	DATE	TITLE SCHEM, TIMING DIAGRAM, 128 STEPS, CP-3				
DRAWN K	5/16/91					
CHECKED A	5/17/91	SIZE	CODE	NUMBER	REV.	
ISSUED CW	5/21/91	B		060-08840	1	
Q.C. A	5/21/91	SHEET 1 OF 1				


LEFT INPUT MDAC
RIGHT INPUT MDAC
U202
AD7628
U204
AD7628
MC33077
U205
U207
U217
SSM2402
GAIN
LIN
RIN
LINB
RINB
CTREQ
HPEN/
MDAC<0: 7>
SUBOUT
TO DIGITAL BOARD
TO LOWER BOARD (J8)
INSEL<0: 3>
GAIN
FDIREN
FPROCEN
HPEN/
DOLBYEN/
THXEN
REQEN
SIDESEL
INWR/
SWR/
CTRWR/
LEFT/
SWR/
CTRWR/
RIGHT/
A/BSEL
RWR/
FWR/
INWR
+15V
+5VB



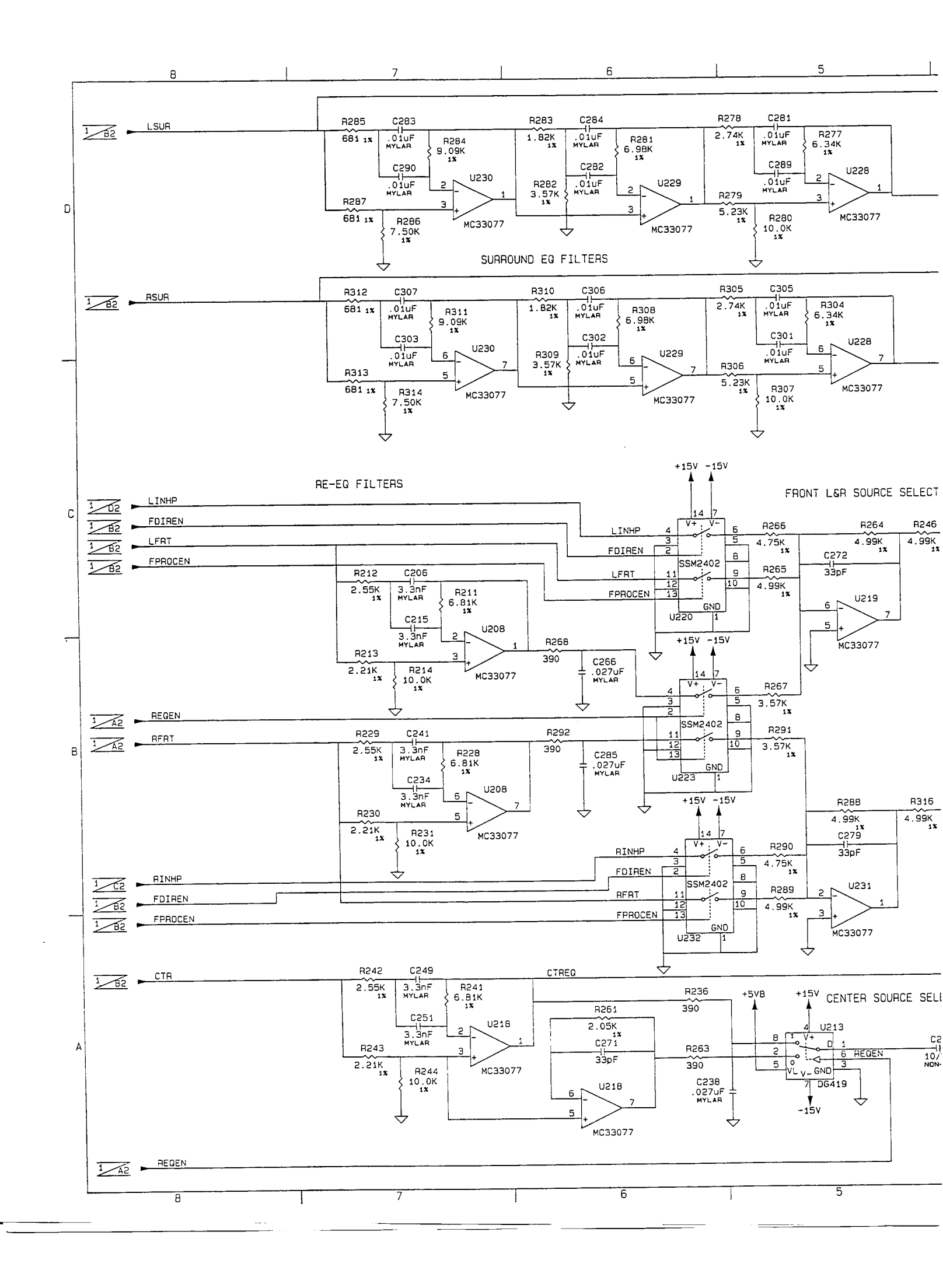
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	RS 03/07/90	
1	REVISED	RS 07/17/90	
2	RELEASED FOR PRODUCTION	RW 02/07/91	RWH 02/07/91
		AF 02/07/91	AF 02/07/91
3	REVISED PER DCR 920511-01	6/11/92	CW 6/19/92
		6/11/92	6/25/92

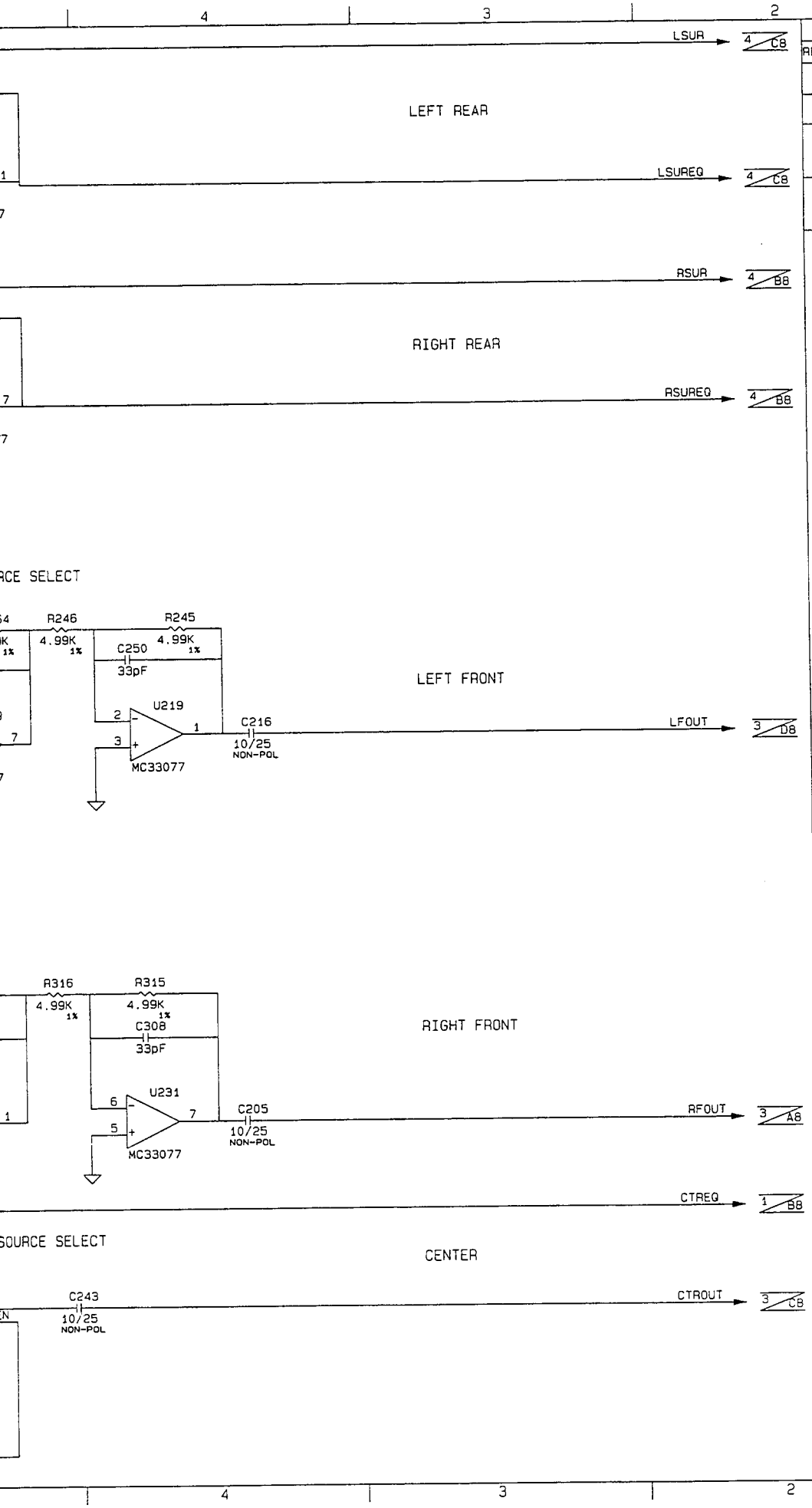
NOTES

1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE uF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
5. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION
7. REFERENCE DESIGNATORS. LAST USED: C308, CR216, J208, Q207, R316, U232. (C400-405, 408, 409 ARE ALSO USED.) (U300,301 ALSO USED.)

DOCUMENT CONTROL BLOCK: #060-08127	
SHEET NUMBER	REVISION
1 OF 5	3
2 OF 5	3
3 OF 5	3
4 OF 5	3
5 OF 5	3

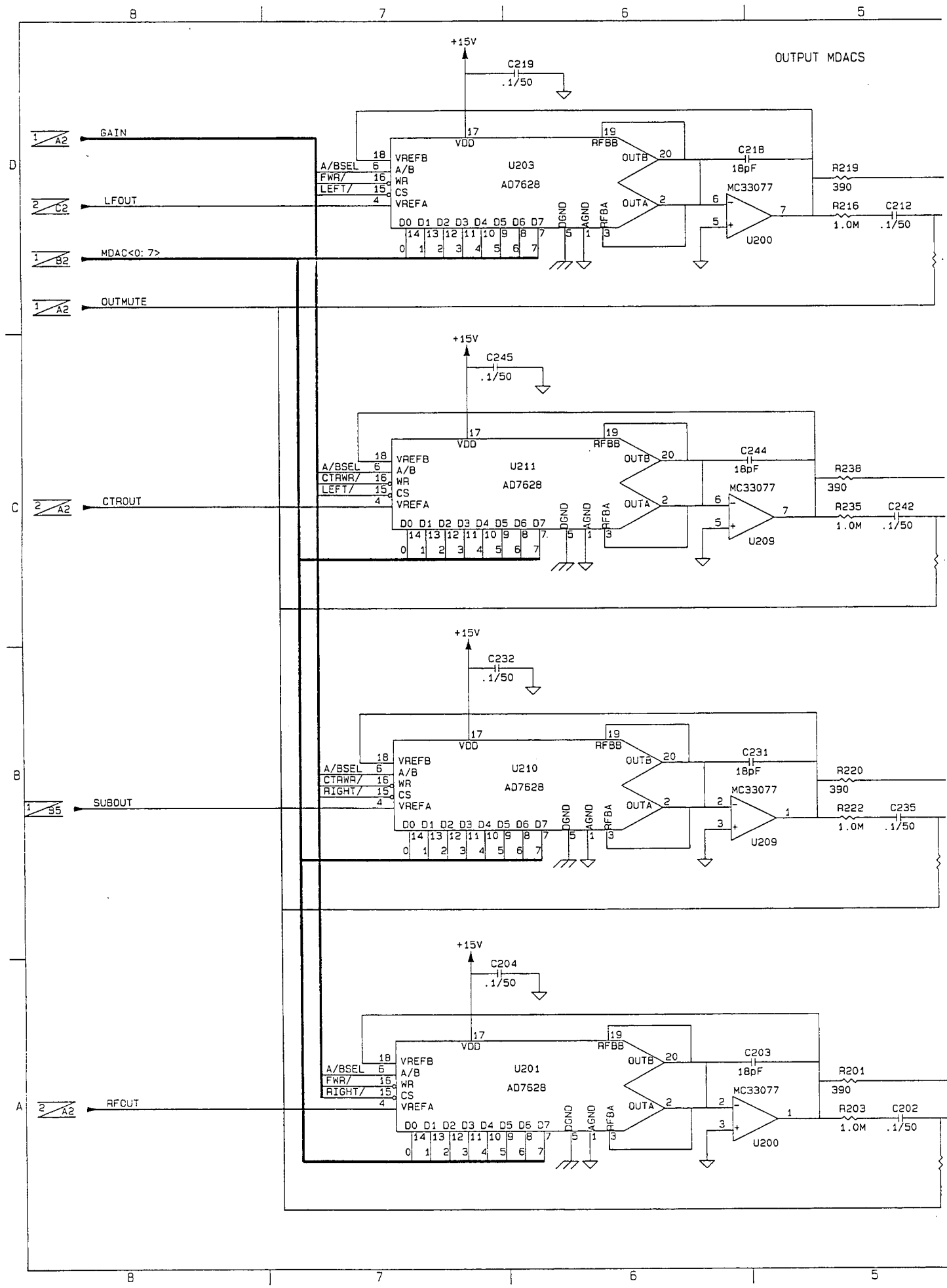
CONTRACT NO.		lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE SCHEM, ANALOG BD, UPPER, CP-3	
DRAWN RW	02/07/91		
CHECKED AF	02/07/91	SIZE D	CODE
Q.C. RWH	02/07/91	NUMBER 060-08127	REV. 3
ISSUED AF	02/07/91	SHEET 1 OF 5	

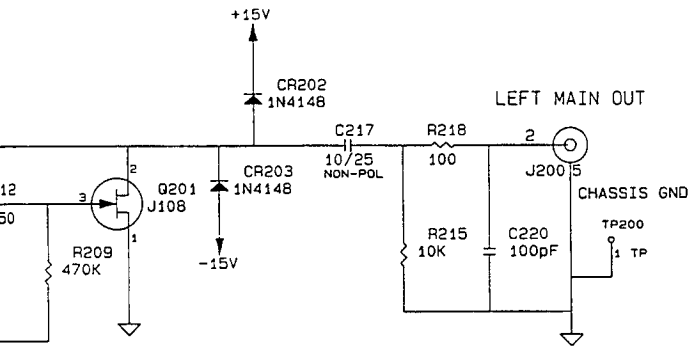

SURROUND EQ FILTERS
RE-EQ FILTERS
FRONT L&R SOURCE SELECT
CENTER SOURCE SELE
LSUR
RSUR
LINHP
FDIREN
LFRT
FPROCEN
REQEN
RFRT
RINHP
CTR
CTREQ
+15V -15V
+5VB
SSM2402
GND
MC33077
DG419
NON-

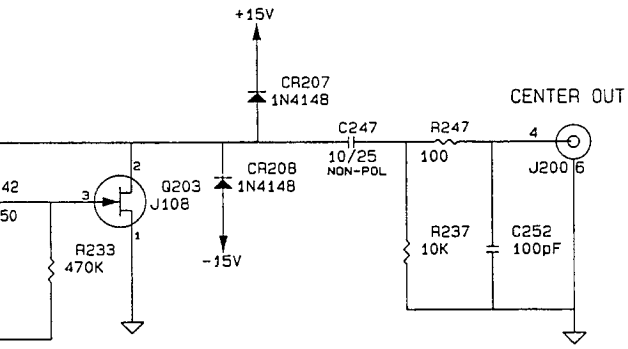


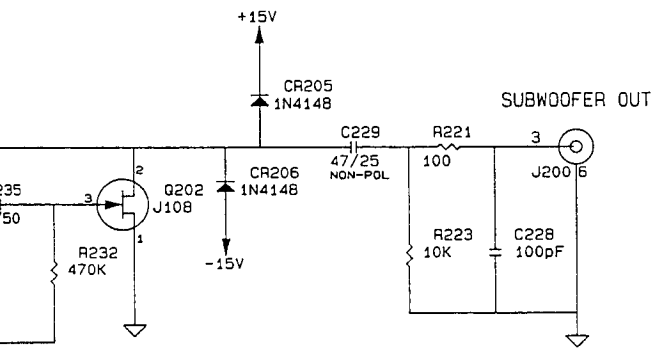
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	C.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	RS 03/07/90	
1	REVISED	RS 07/17/90	
2	RELEASED FOR PRODUCTION	RW 02/07/91	RWH 02/07/91
		AF 02/07/91	AF 02/07/91
3	REVISED PER DCR 920511-01	6/11/92	6/25/92
		AF 6/11/92	AF 6/25/92

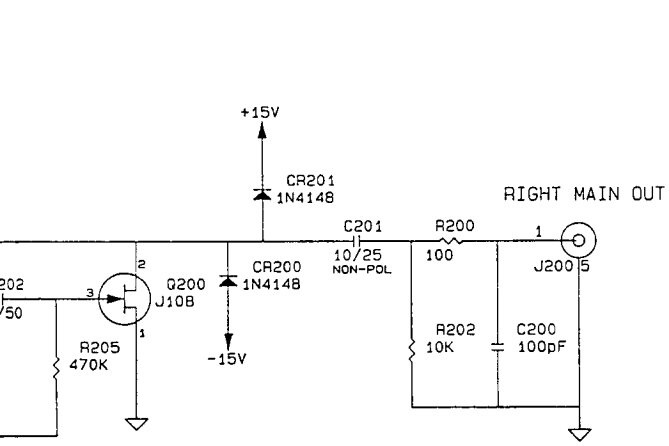
CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA. 02154				
APPROVALS	DATE	TITLE SCHEM, ANALOG BD, UPPER, CP-3			
DRAWN RW	02/07/91				
CHECKED AF	02/07/91	SIZE	CODE	NUMBER	REV.
Q.C. RWH	02/07/91	D		060-08127	3
ISSUED AF	02/07/91	SHEET 2 OF 5			


OUTPUT MDACS
+15V
C219
.1/50
GAIN
LFOUT
MDAC<0: 7>
OUTMUTE
VDD
RFBB
VREFB
A/B
WR
CS
VREFA
A/BSEL
FWR/
LEFT/
U203
AD7628
D0 D1 D2 D3 D4 D5 D6 D7
DGND
AGND
RFBA
OUTB
OUTA
C218
18pF
MC33077
U200
R219
390
R216
1.0M
C212
.1/50
+15V
C245
.1/50
CTROUT
CTRWR/
LEFT/
U211
AD7628
C244
18pF
MC33077
U209
R238
390
R235
1.0M
C242
.1/50
+15V
C232
.1/50
SUBOUT
A/BSEL
CTRWR/
RIGHT/
U210
AD7628
C231
18pF
MC33077
U209
R220
390
R222
1.0M
C235
.1/50
+15V
C204
.1/50
RFOUT
A/BSEL
FWR/
RIGHT/
U201
AD7628
C203
18pF
MC33077
U200
R201
390
R203
1.0M
C202
.1/50



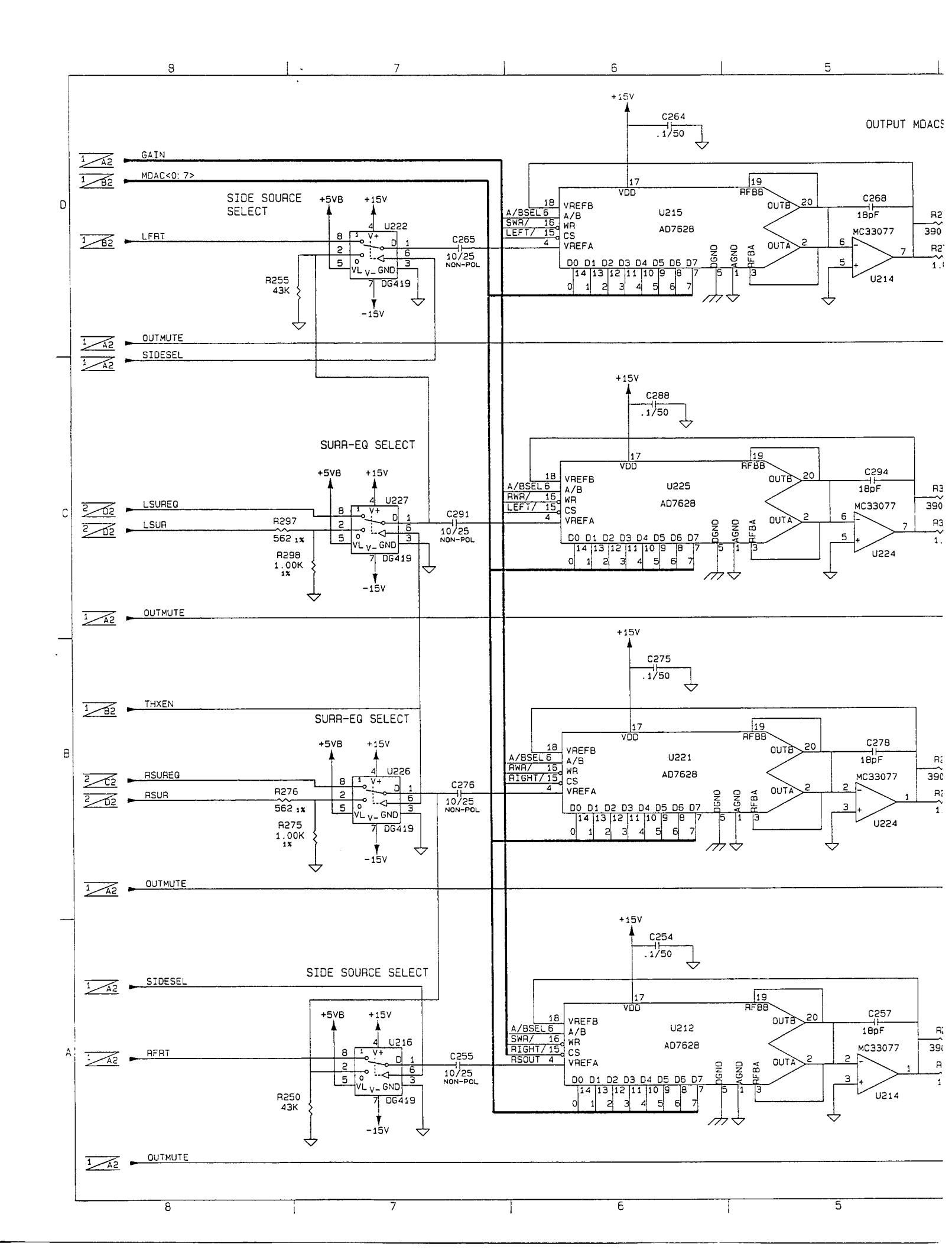




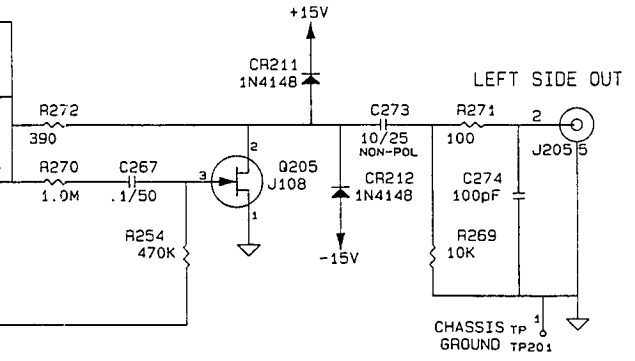


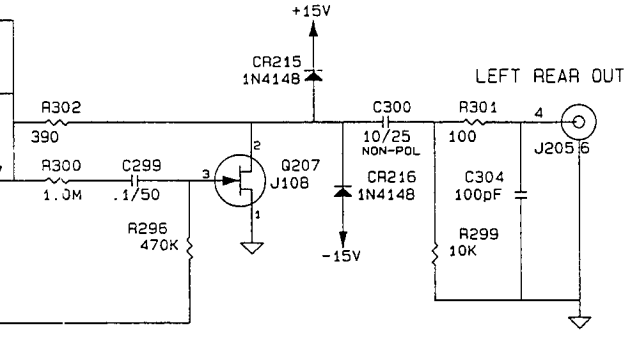
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	RS 03/07/90	
1	REVISED	RS 07/17/90	
2	RELEASED FOR PRODUCTION	RW 02/07/91	RWH 02/07/91
		AF 02/07/91	AF 02/07/91
3	REVISED PER DCR 920511-01	6/11/92	6/11/92
		AF 6/11/92	AF 6/11/92

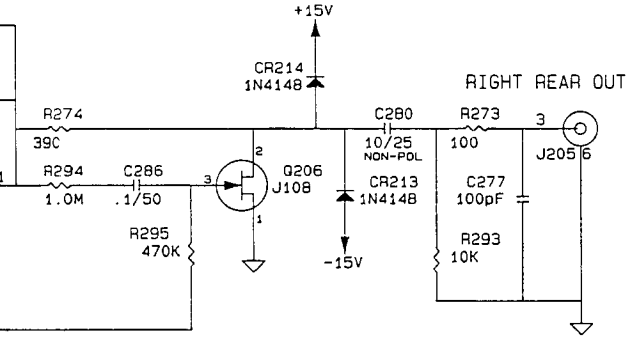
CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA. 02154		
APPROVALS	DATE	TITLE SCHEM, ANALOG BD, UPPER, CP-3	
DRAWN RW	02/07/91		
CHECKED AF	02/07/91	SIZE D	CODE
Q.C. RWH	02/07/91	NUMBER 060-08127	REV. 3
ISSUED AF	02/07/91	SHEET 3 OF 5	

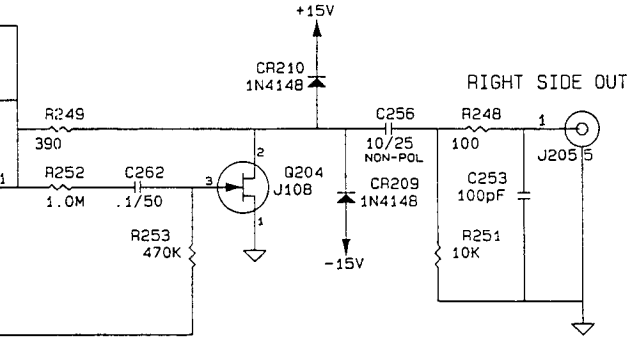

OUTPUT MDACS
GAIN
MDAC<0: 7>
SIDE SOURCE SELECT
+5VB
+15V
U222
LFRT
C265
10/25
NON-POL
R255
43K
-15V
DG419
OUTMUTE
SIDESEL
C264
.1/50
U215
AD7628
VREFB
A/B
WR
CS
VREFA
A/BSEL
SWA/
LEFT/
VDD
RFBB
OUTB
OUTA
RFBA
DGND
AGND
D0 D1 D2 D3 D4 D5 D6 D7
C268
18pF
MC33077
U214
SURR-EQ SELECT
LSUREQ
LSUR
U227
R297
562 1%
R298
1.00K
1%
C291
C288
U225
RWA/
C294
U224
THXEN
RSUREQ
RSUR
U226
R276
R275
C276
C275
U221
RIGHT/
C278
SIDE SOURCE SELECT
RFRT
U216
R250
C255
C254
U212
RSOUT
C257

MDACS



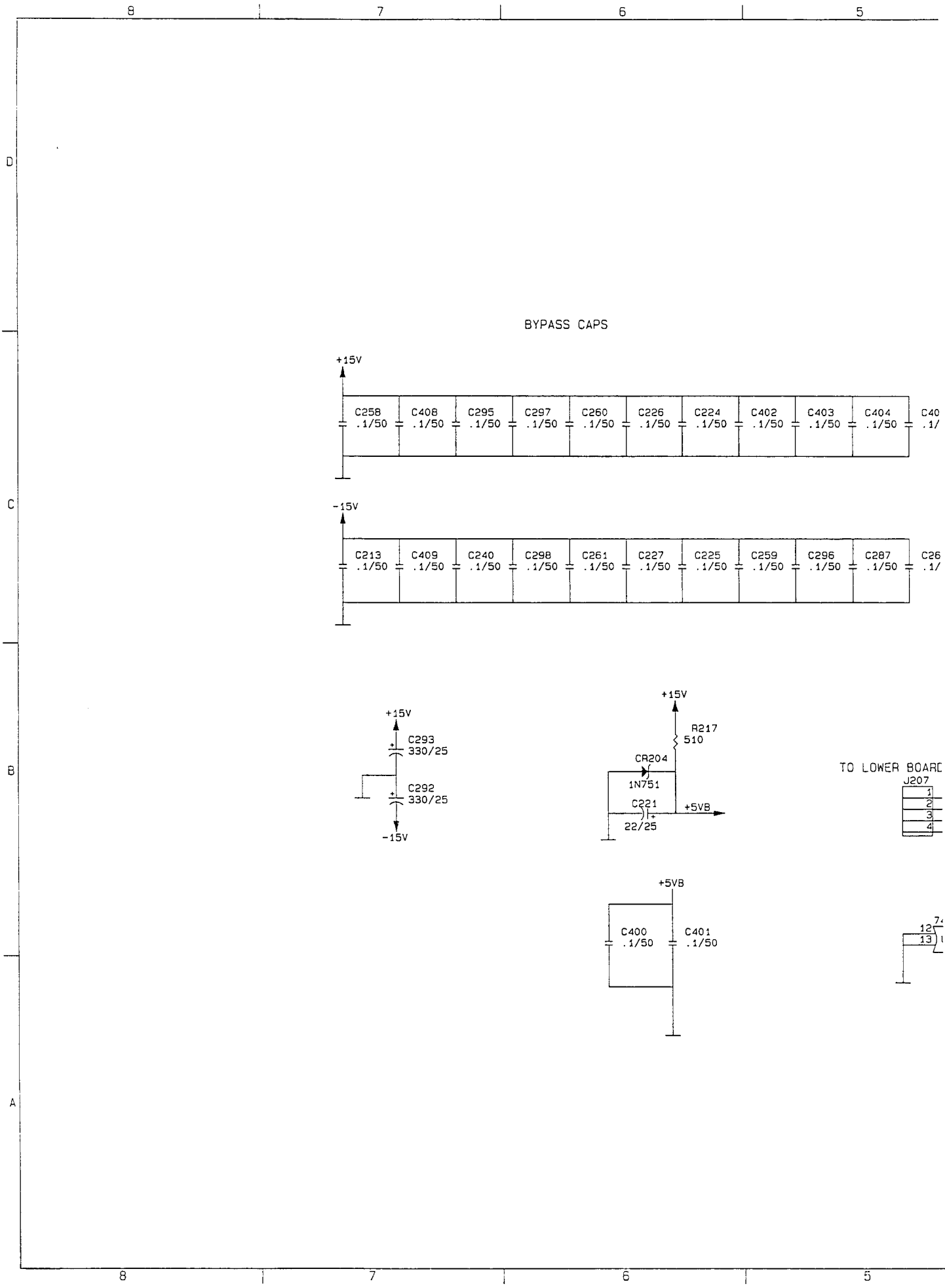






REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	RS 03/07/90	
1	REVISED	RS 07/17/90	
2	RELEASED FOR PRODUCTION	RW 02/07/91	RWH 02/07/91
		AF 02/07/91	AF 02/07/91
3	REVISED PER DCR 920511-01	6/10/92	6/12/92
		6/11/92	6/12/92

CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA. 02154				
APPROVALS	DATE	TITLE SCHEM, ANALOG BD, UPPER, CP-3			
DRAWN RW	02/07/91				
CHECKED AF	02/07/91	SIZE	CODE	NUMBER	REV.
Q.C. RWH	02/07/91	D		060-08127	3
ISSUED AF	02/07/91	SHEET 4 OF 5			

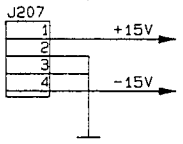

8
7
6
5
D
C
B
A
BYPASS CAPS
+15V
C258 .1/50
C408 .1/50
C295 .1/50
C297 .1/50
C260 .1/50
C226 .1/50
C224 .1/50
C402 .1/50
C403 .1/50
C404 .1/50
C40 .1/
-15V
C213 .1/50
C409 .1/50
C240 .1/50
C298 .1/50
C261 .1/50
C227 .1/50
C225 .1/50
C259 .1/50
C296 .1/50
C287 .1/50
C26 .1/
+15V
C293 330/25
C292 330/25
-15V
+15V
R217 510
CR204
1N751
C221 22/25
+5VB
TO LOWER BOARD
J207
1
2
3
4
+5VB
C400 .1/50
C401 .1/50
12
13

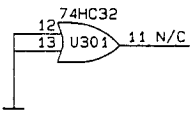
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	RS 03/07/90	
1	REVISED	RS 07/17/90	
2	RELEASED FOR PRODUCTION	RW 02/07/91	RWH 02/07/91
		AF 02/07/91	AF 02/07/91
3	REVISED PER DCR 920511-01	RW 6/10/91	6/19/92
		AF 6/11/92	AF 6/25/92

C405
.1/50

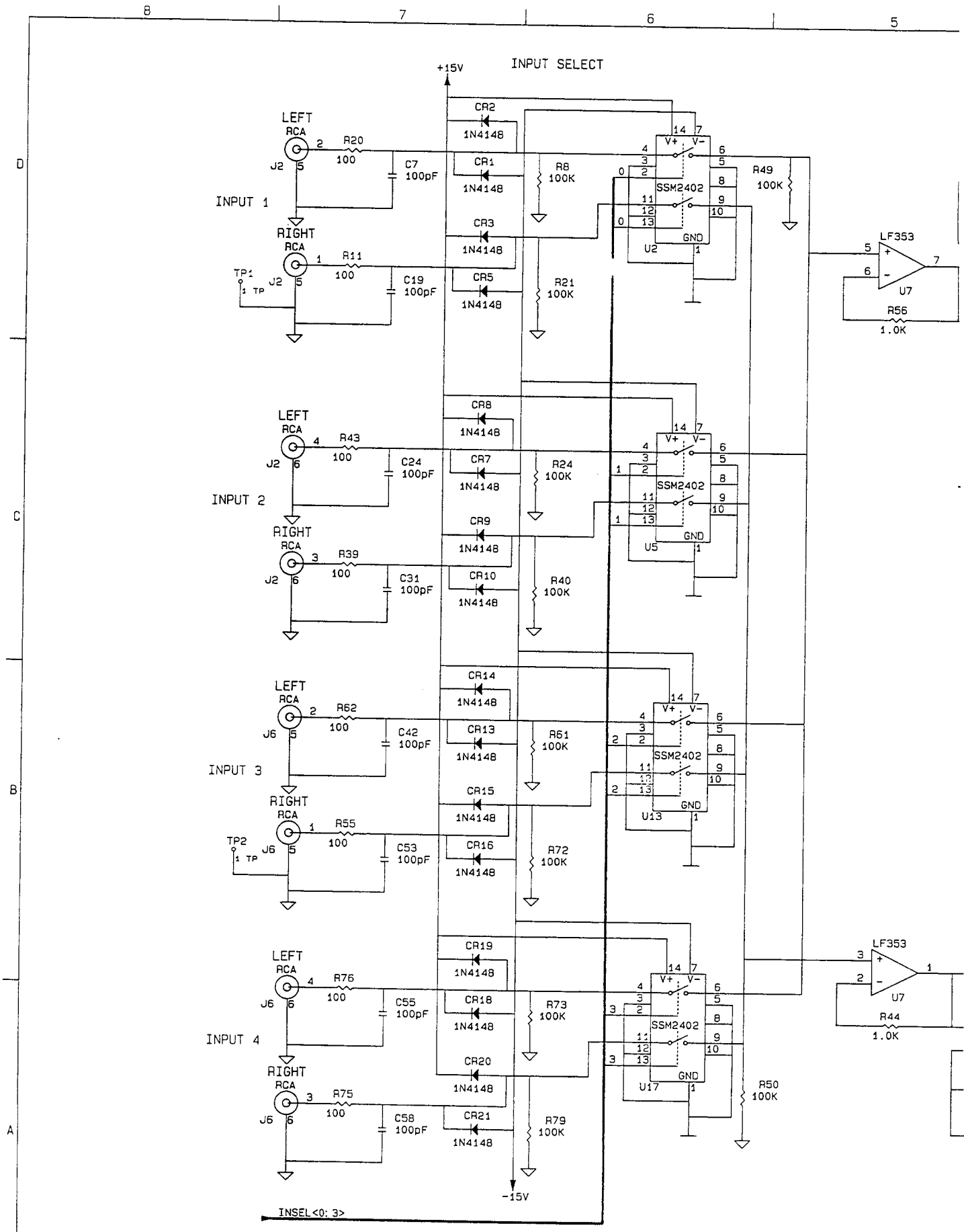
C263
.1/50

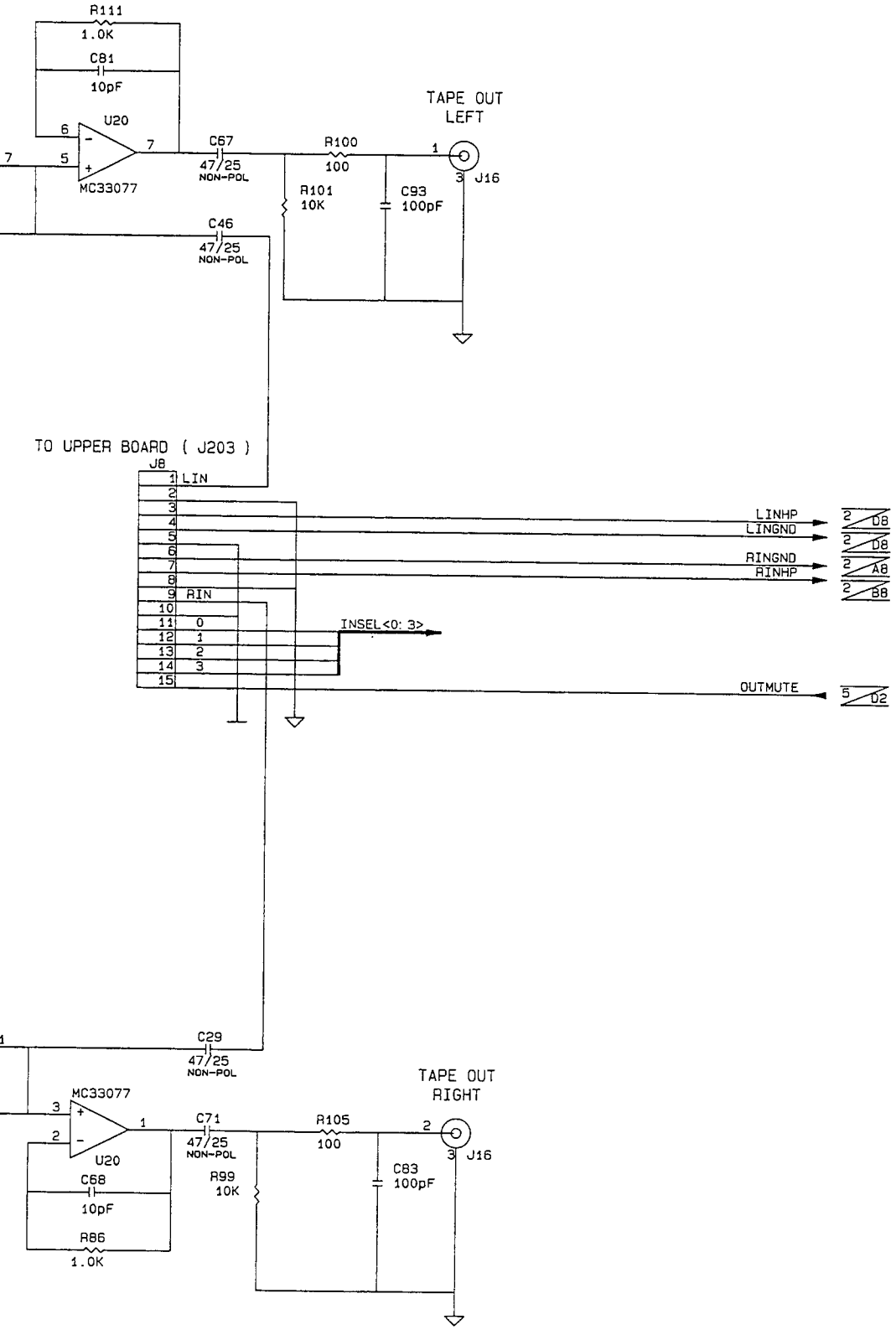
R BOARD (J11-14)





CONTRACT NO.		lexicon 100 BEAVER ST. WALTHAM, MA. 02154				
APPROVALS	DATE	TITLE SCHEM, ANALOG BD, UPPER, CP-3				
DRAWN RW	02/07/91					
CHECKED AF	02/07/91	SIZE	CODE	NUMBER		REV.
Q.C. RWH	02/07/91	D		060-08127		3
ISSUED AF	02/07/91				SHEET 5 OF 5	


INPUT SELECT
+15V
INPUT 1
INPUT 2
INPUT 3
INPUT 4
LEFT
RIGHT
RCA
J2
J6
TP1
TP2
R20
R11
R43
R39
R62
R55
R76
R75
100
C7
C19
C24
C31
C42
C53
C55
C58
100pF
CR1
CR2
CR3
CR5
CR7
CR8
CR9
CR10
CR13
CR14
CR15
CR16
CR18
CR19
CR20
CR21
1N4148
R8
R21
R24
R40
R61
R72
R73
R79
100K
SSM2402
V+
V-
GND
U2
U5
U13
U17
R49
R50
LF353
U7
R56
R44
1.0K
-15V
INSEL<0:3>
A
B
C
D
8
7
6
5



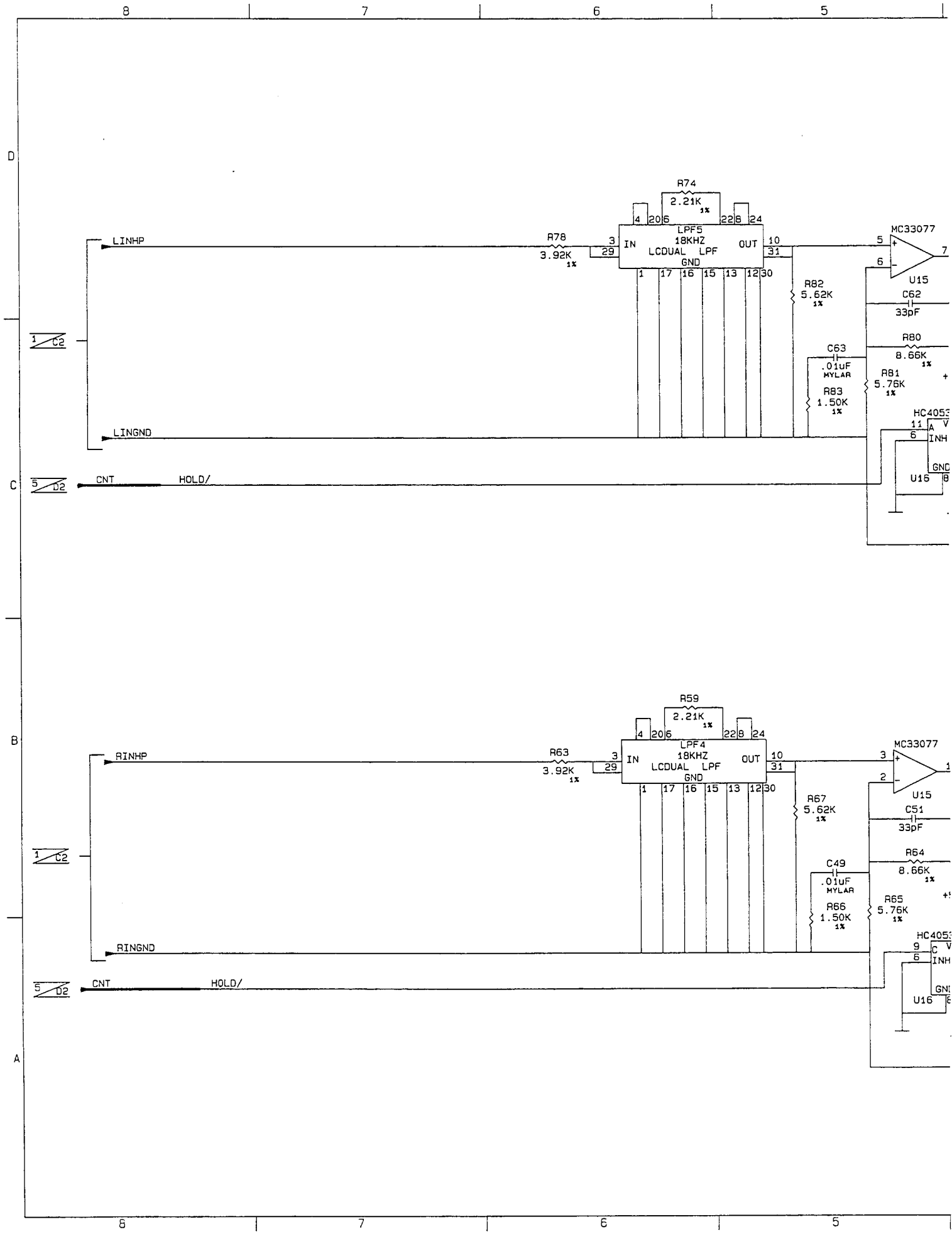
REVISIONS				
SCH	PCB	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0		RELEASE FOR PROTOTYPE	RS 03/07/90	
1		REVISED	RS	
2		RELEASED FOR PRODUCTION	AW 02/07/91	RWH 02/07/91
			AF 02/07/91	AF 02/07/91
3	3	REVISED SHEET 2 PER ECO # 911115-00	JV 03/02/92	RWH 03/04/92
			AF 03/02/92	AF 03/04/92
4	3	REVISED PER DCR 920511-01	6/11/92	6/19/92
			6/11/92	6/25/92

NOTES

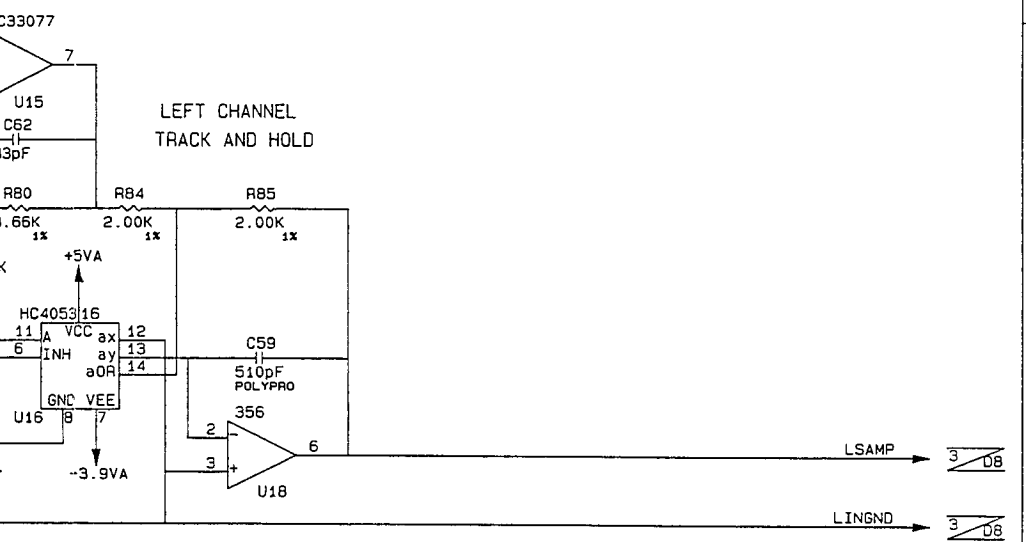
1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE uF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
5. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION
7. REFERENCE DESIGNATORS, LAST USED: C106, CR33, J19, Q8, R126, U28. (C406 AND 407 ARE ALSO USED.)

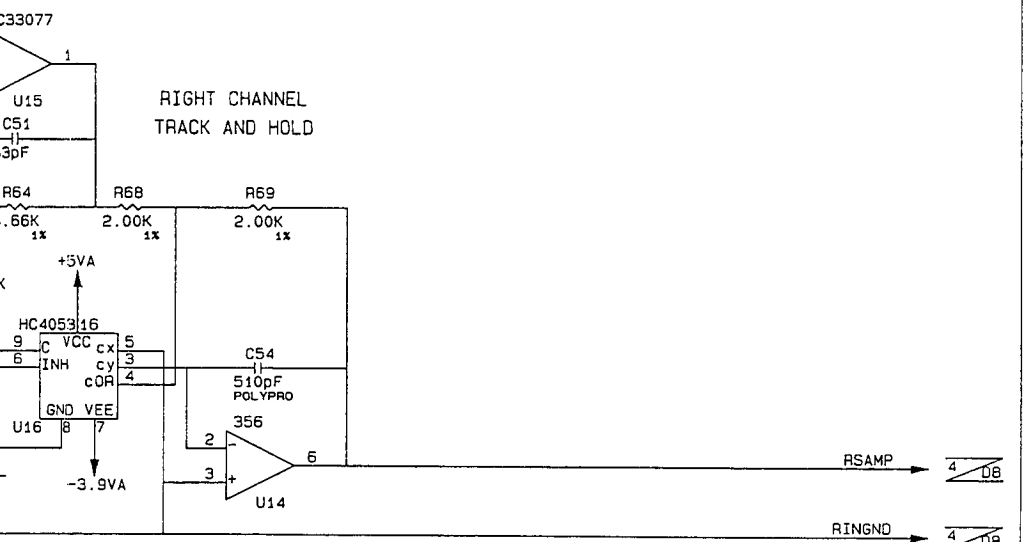
DOCUMENT CONTROL BLOCK: #060-08128	
SHEET NUMBER	REVISION
1 OF 5	4
2 OF 5	4
3 OF 5	3
4 OF 5	3
5 OF 5	3

CONTRACT NO.		lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEM, ANALOG BD, LOWER, CP-3	
DRAWN RW	02/07/91		
CHECKED AF	02/07/91	SIZE: D	CODE:
Q.C. RWH	02/07/91	NUMBER: 060-08128	REV.: 4
ISSUED AF	02/07/91	SHEET 1 OF 5	

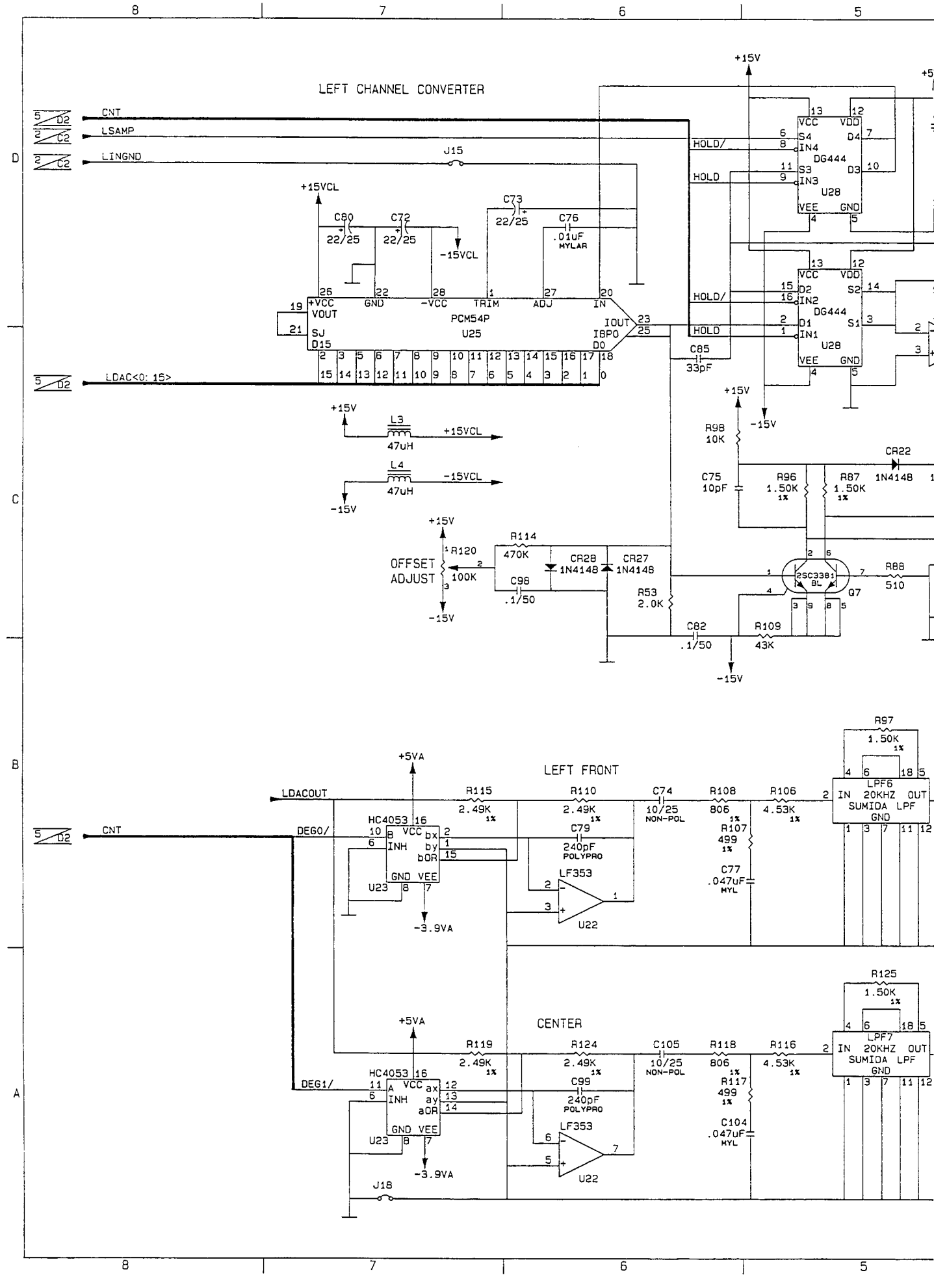

8
7
6
5
D
C
B
A
LINHP
LINGND
1 C2
5 D2
CNT
HOLD/
R78
3.92K 1%
R74
2.21K 1%
LPF5
18KHZ
LCDUAL LPF
IN
OUT
GND
R82
5.62K 1%
C62
33pF
MC33077
U15
R80
8.66K 1%
C63
.01uF MYLAR
R81
5.76K 1%
R83
1.50K 1%
HC4053
U16
INH
GND
RINHP
RINGND
R63
3.92K 1%
R59
2.21K 1%
LPF4
18KHZ
LCDUAL LPF
R67
5.62K 1%
C51
33pF
R64
8.66K 1%
C49
.01uF MYLAR
R65
5.76K 1%
R66
1.50K 1%

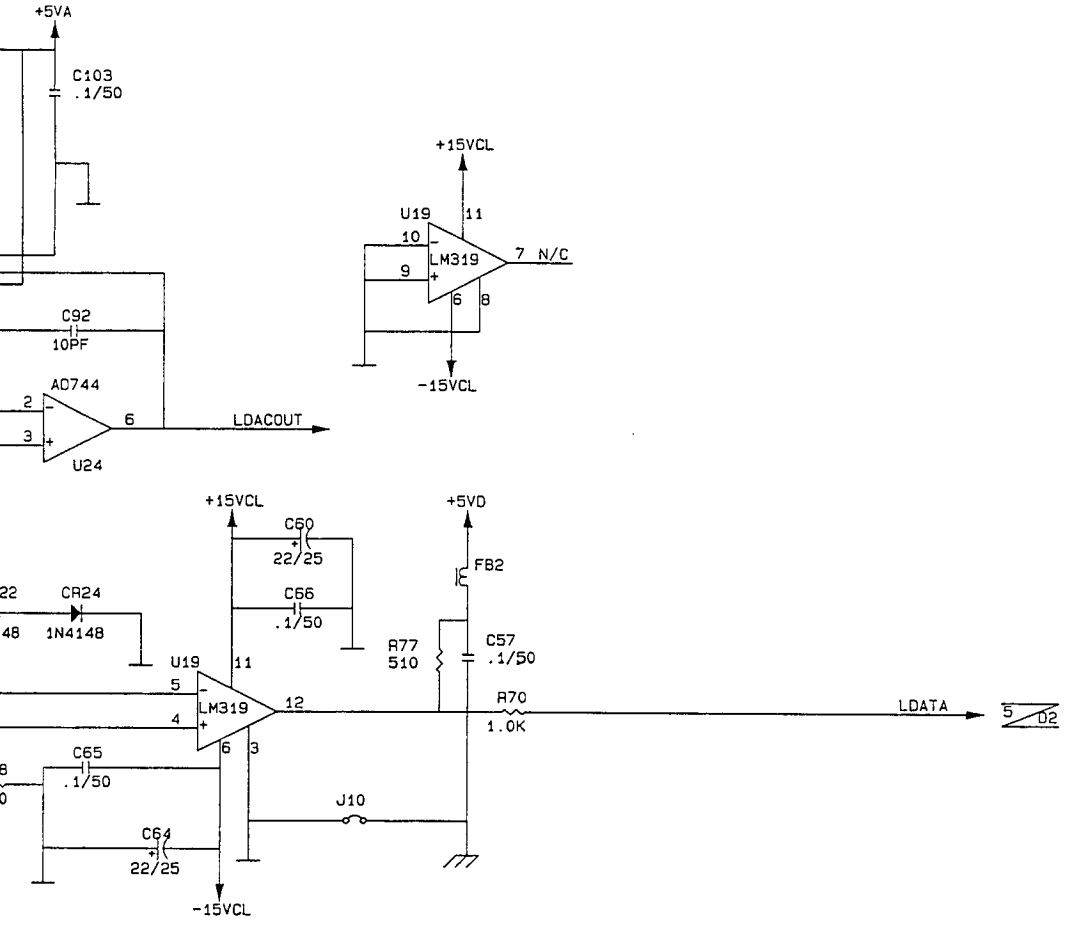
REVISIONS			
SCH	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	RS 03/07/90	
1	REVISED	RS 07/16/90	
2	RELEASED FOR PRODUCTION	RW 02/07/91	RWH 02/07/91
		AF 02/07/91	AF 02/07/91
3	CHANGED LPF4 & 5 INPUT PIN FROM 2 TO 3 PER ECO 911115-00	JV 03/02/92	RWH 03/04/92
		AF 03/02/92	AF 03/04/92
4	REVISED PER DCR 920511-01		

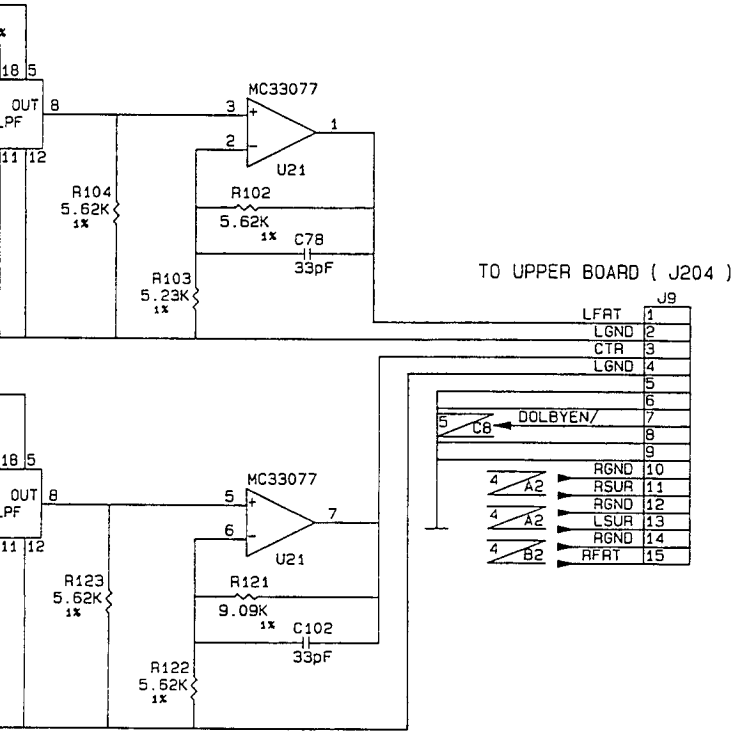




CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEM, ANALOG BD, LOWER, CP-3
DRAWN RW	02/07/91	
CHECKED AF	02/07/91	SIZE: D; CODE: ; NUMBER: 060-08128; REV.: 4
Q.C. RWH	02/07/91	
ISSUED AF	02/07/91	SHEET 2 OF 5

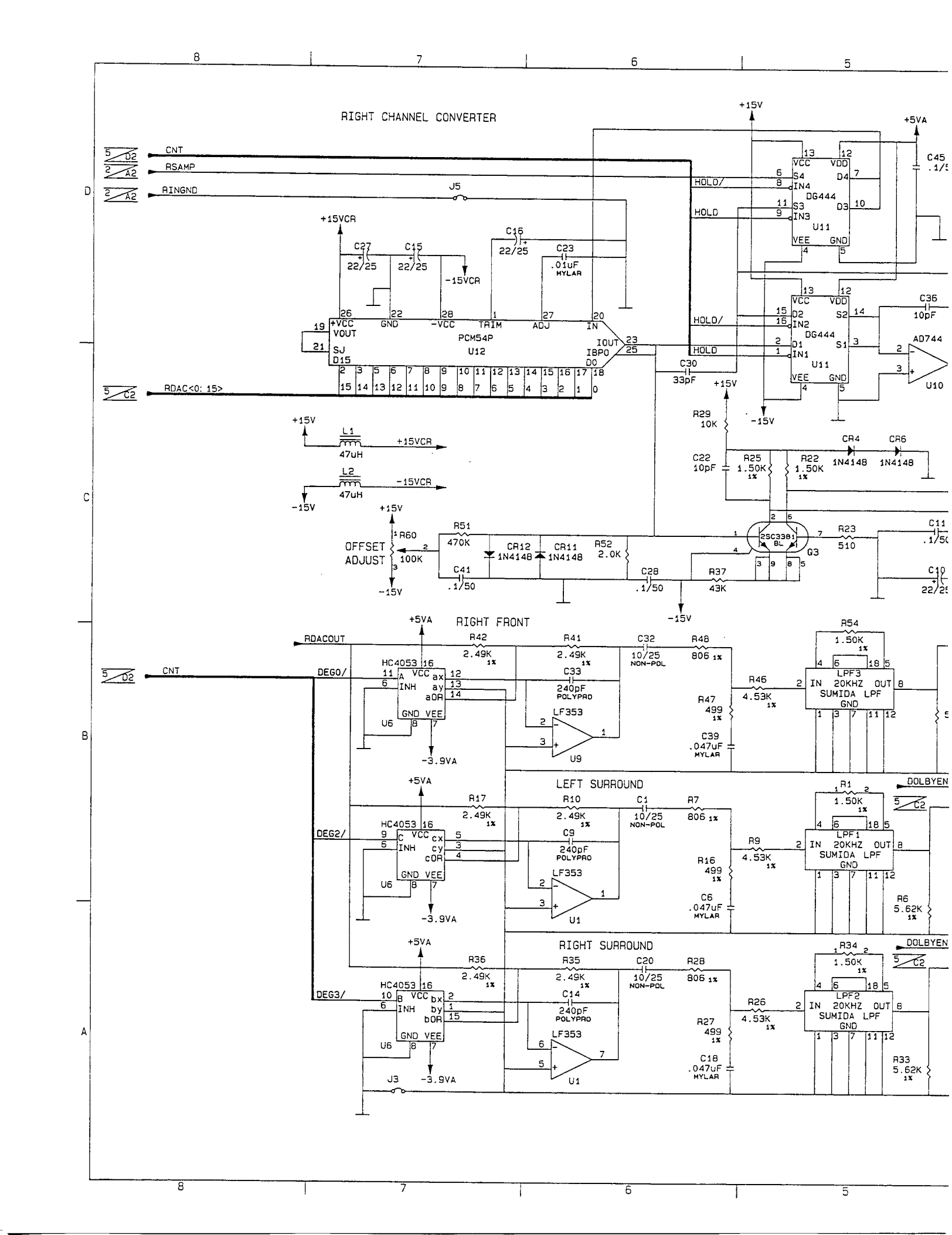

LEFT CHANNEL CONVERTER
CNT
LSAMP
LINGND
LDAC<0: 15>
J15
+15VCL
-15VCL
C80
22/25
C72
22/25
C73
22/25
C76
.01uF
MYLAR
PCM54P
U25
+VCC
VOUT
SJ
D15
GND
-VCC
TRIM
ADJ
IN
IOUT
IBPO
DO
C85
33pF
HOLD/
HOLD
DG444
U28
VCC
VDD
VEE
GND
S4
IN4
D4
S3
IN3
D3
D2
IN2
S2
D1
IN1
S1
+15V
-15V
L3
47uH
L4
47uH
R98
10K
CR22
1N4148
C75
10pF
R96
1.50K
1%
R87
1.50K
1%
OFFSET
ADJUST
R120
100K
R114
470K
CR28
1N4148
CR27
1N4148
C98
.1/50
R53
2.0K
2SC3381
BL
Q7
R88
510
C82
.1/50
R109
43K
+5VA
LEFT FRONT
LDACOUT
DEG0/
HC4053
INH
VCC
GND
VEE
bx
by
bOR
U23
-3.9VA
R115
2.49K
1%
R110
2.49K
1%
C74
10/25
NON-POL
C79
240pF
POLYPRO
LF353
U22
R108
806
1%
R107
499
1%
C77
.047uF
MYL
R106
4.53K
1%
R97
1.50K
1%
LPF6
IN 20KHZ OUT
SUMIDA LPF
GND
CENTER
DEG1/
ax
ay
aOR
R119
2.49K
1%
R124
2.49K
1%
C105
10/25
NON-POL
C99
240pF
POLYPRO
R118
806
1%
R117
499
1%
C104
.047uF
MYL
R116
4.53K
1%
R125
1.50K
1%
LPF7
IN 20KHZ OUT
SUMIDA LPF
GND
J18

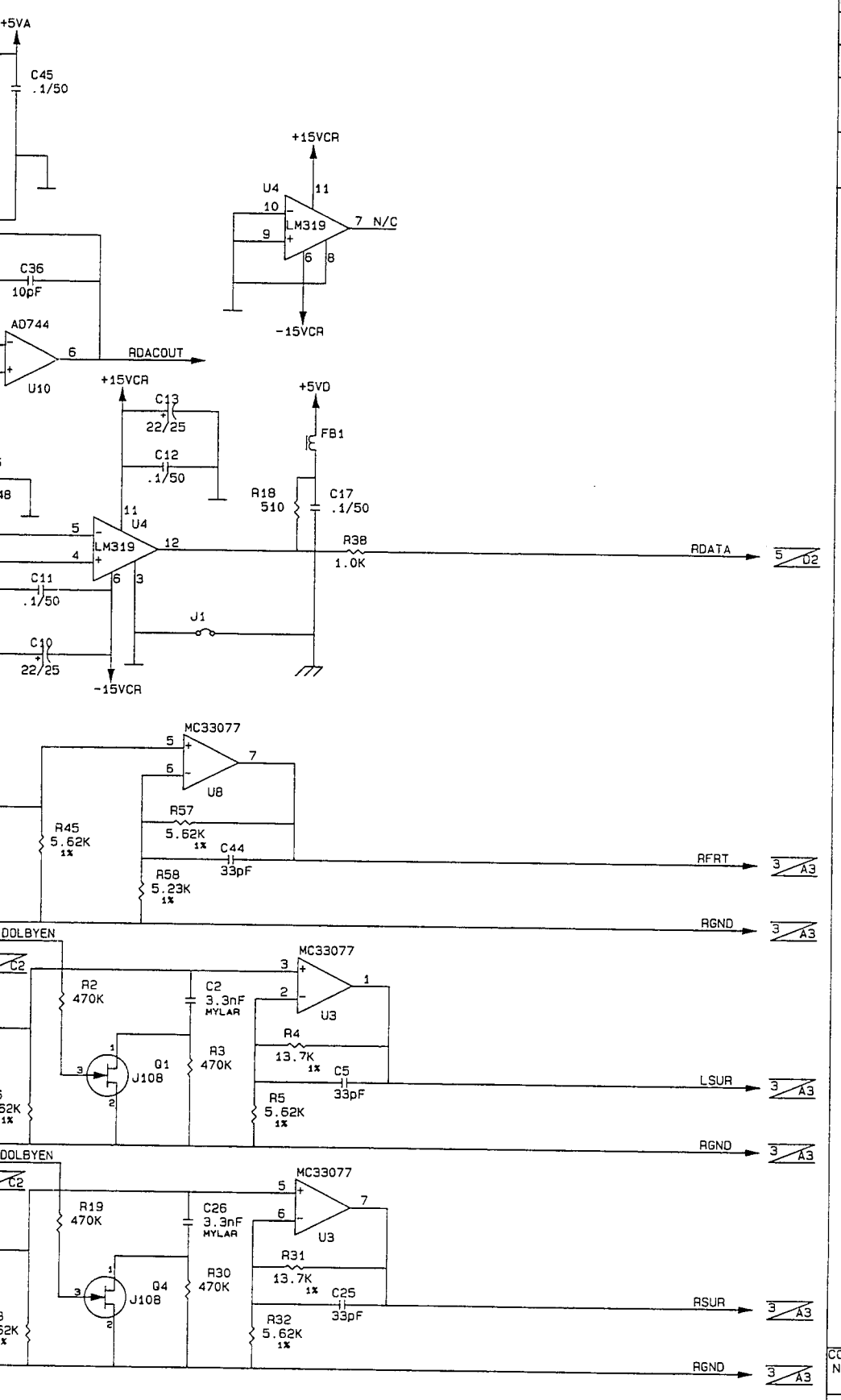




REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	G.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	RS 03/07/90	
1	REVISED	RS 07/16/90	
2	RELEASED FOR PRODUCTION	RW 02/07/91	RWH 02/07/91
		AF 02/07/91	AF 02/07/91
3	REVISED PER DCR 920511-01	RW 6/1/91	[illegible]
		AF 6/11/92	6/25/92

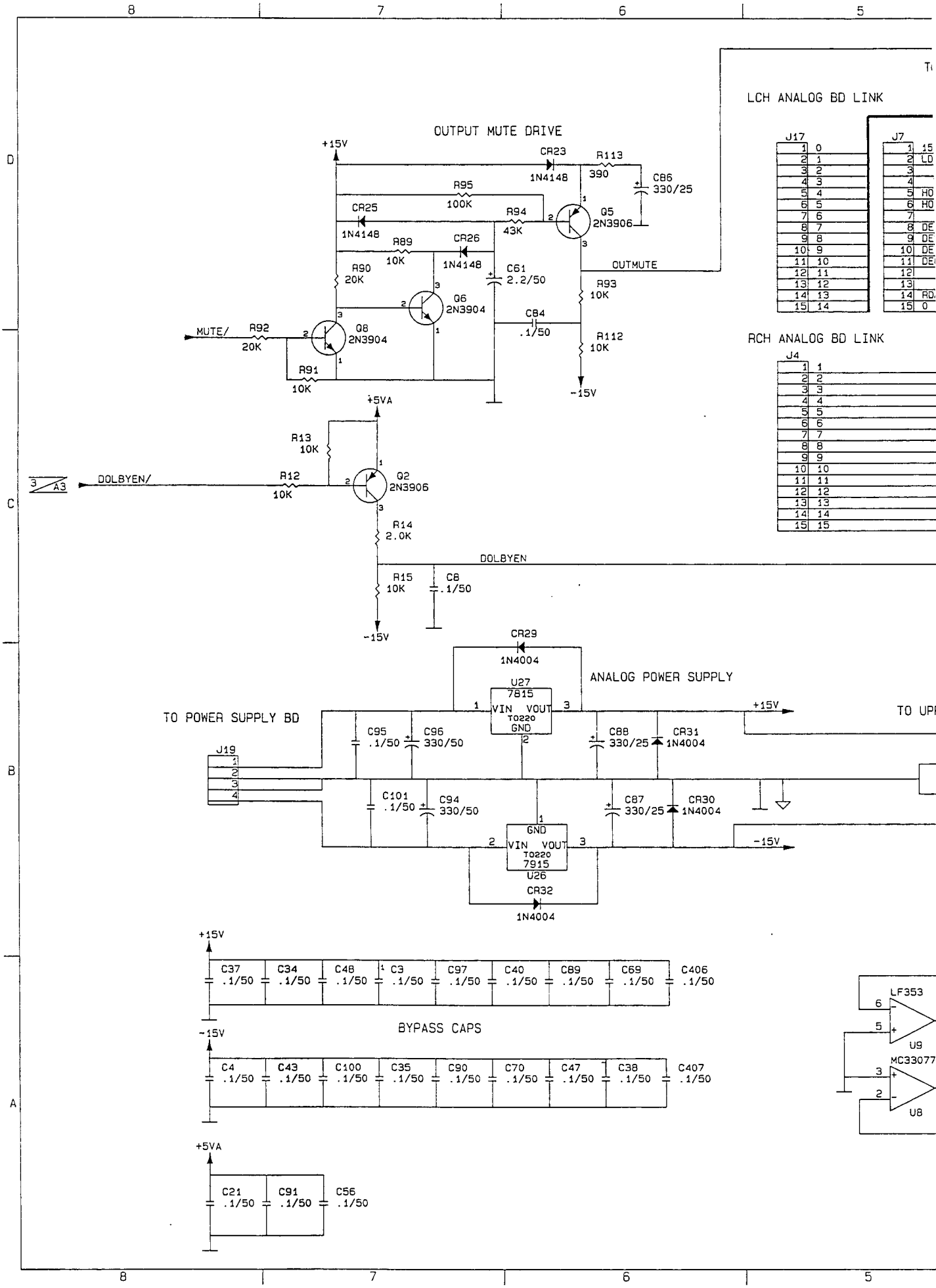
CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA. 02154				
APPROVALS	DATE	TITLE SCHEM, ANALOG BD, LOWER, CP-3			
DRAWN RW	02/07/91				
CHECKED AF	02/07/91	SIZE D	CODE	NUMBER 060-08128	REV. 3
G.C. RWH	02/07/91				
ISSUED AF	02/07/91	SHEET 3 OF 5			

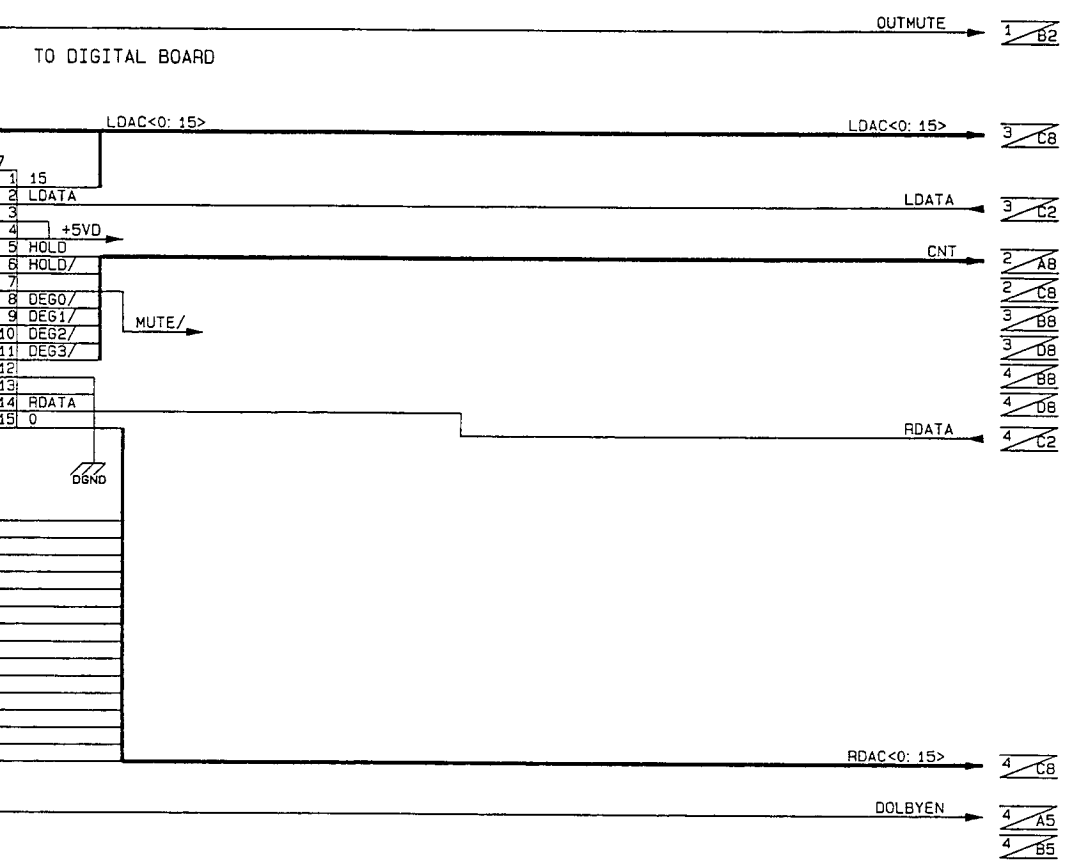

RIGHT CHANNEL CONVERTER
CNT
RSAMP
RINGND
J5
+15VCR
-15VCR
C27 22/25
C15 22/25
C16 22/25
C23 .01uF MYLAR
PCM54P U12
+VCC VOUT SJ D15
GND -VCC TRIM ADJ IN
IOUT IBPO DO
RDAC<0: 15>
+15V
-15V
+5VA
HOLD/
HOLD
DG444 U11
VCC VDD VEE GND
S4 S3 S2 S1
D4 D3 D2 D1
IN4 IN3 IN2 IN1
C45 .1/5
C36 10pF
AD744 U10
C30 33pF
R29 10K
C22 10pF
R25 1.50K 1%
R22 1.50K 1%
CR4 1N4148
CR6 1N4148
L1 47uH
L2 47uH
OFFSET ADJUST
R60 100K
R51 470K
CR12 1N4148
CR11 1N4148
R52 2.0K
C41 .1/50
C28 .1/50
R37 43K
2SC3381 BL Q3
R23 510
C11 .1/50
C10 22/25
RIGHT FRONT
RDACOUT
CNT
DEG0/
HC4053 U6
VCC INH GND VEE
ax ay aOR
bx by bOR
cx cy cOR
R42 2.49K 1%
R41 2.49K 1%
C32 10/25 NON-POL
R48 806 1%
C33 240pF POLYPRO
LF353 U9
R47 499 1%
C39 .047uF MYLAR
R46 4.53K 1%
R54 1.50K 1%
LPF3 SUMIDA LPF
IN 20KHZ OUT
GND
-3.9VA
LEFT SURROUND
DEG2/
R17 2.49K 1%
R10 2.49K 1%
C1 10/25 NON-POL
R7 806 1%
C9 240pF POLYPRO
LF353 U1
R16 499 1%
C6 .047uF MYLAR
R9 4.53K 1%
R1 1.50K 1%
LPF1 SUMIDA LPF
R6 5.62K 1%
DOLBYEN
RIGHT SURROUND
DEG3/
R36 2.49K 1%
R35 2.49K 1%
C20 10/25 NON-POL
R28 806 1%
C14 240pF POLYPRO
LF353 U1
R27 499 1%
C18 .047uF MYLAR
R26 4.53K 1%
R34 1.50K 1%
LPF2 SUMIDA LPF
R33 5.62K 1%
J3



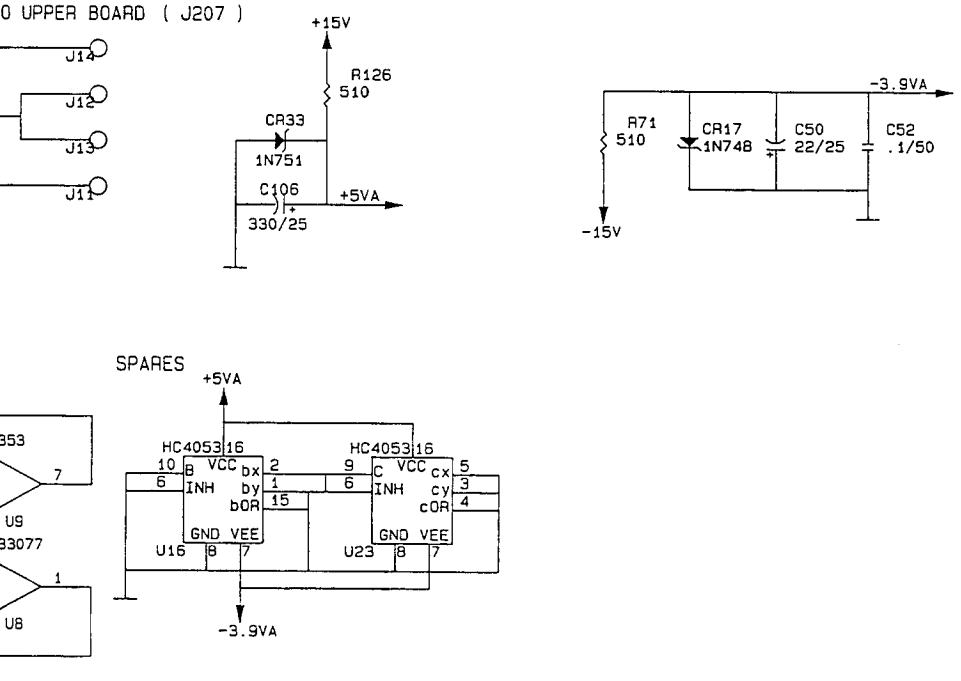
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	RS 03/07/90	
1	REVISED	RS 07/17/90	
2	RELEASED FOR PRODUCTION	RW 02/07/91	RWH 02/07/91
		AF 02/07/91	AF 02/07/91
3	REVISED PER DCR 920511-01	6/10/92	
		6/11/92	

CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA. 02154		
APPROVALS	DATE	TITLE: SCHEM, ANALOG BD, LOWER, CP-3	
DRAWN RW	02/07/91		
CHECKED AF	02/07/91	SIZE: D	CODE:
Q.C. RWH	02/07/91	NUMBER: 060-08128	REV.: 3
ISSUED AF	02/07/91	SHEET 4 OF 5	

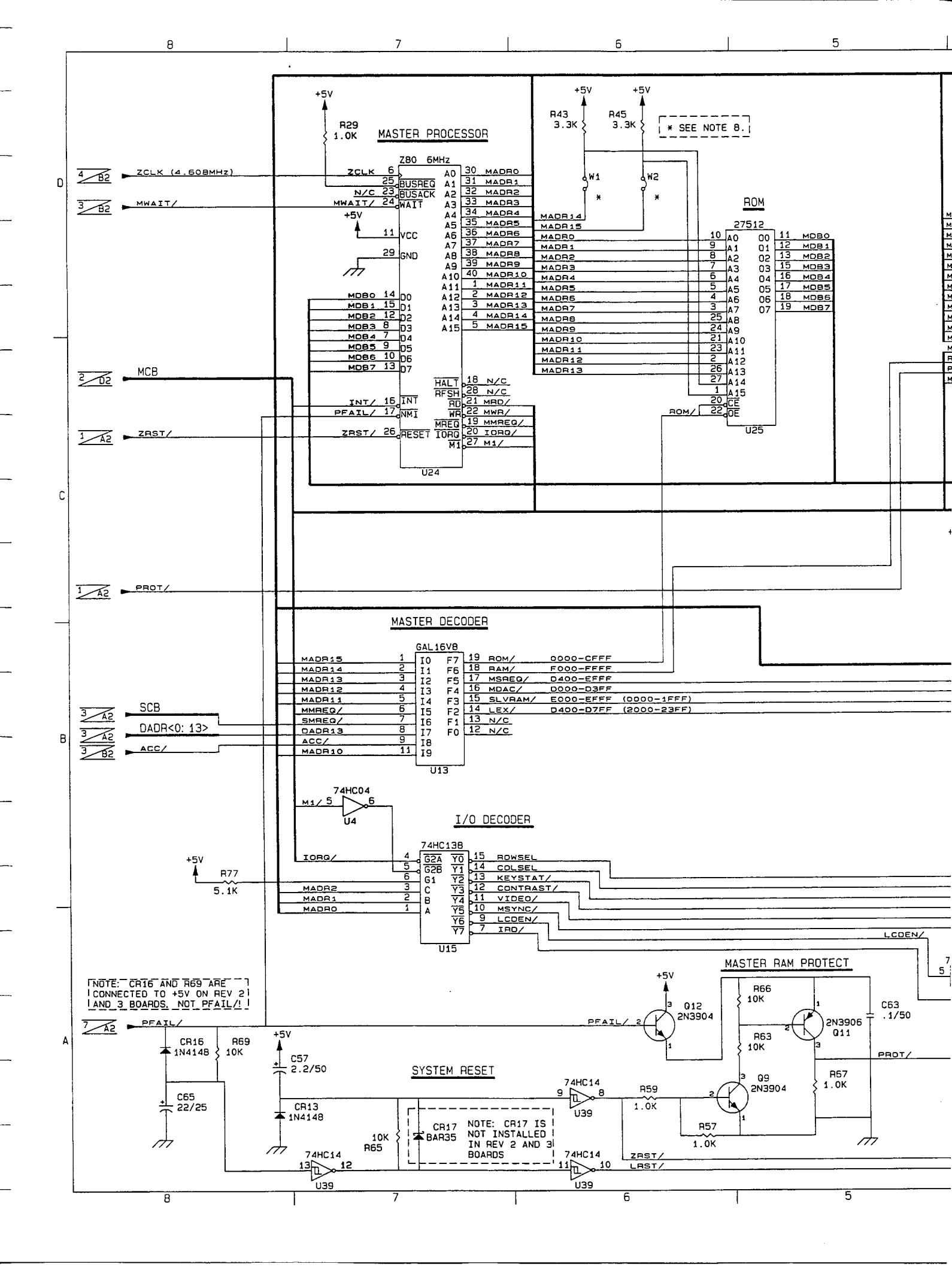

OUTPUT MUTE DRIVE
+15V
CR23
1N4148
R113
390
C86
330/25
R95
100K
CR25
1N4148
R94
43K
Q5
2N3906
R89
10K
CR26
1N4148
R90
20K
C61
2.2/50
OUTMUTE
Q6
2N3904
R93
10K
C84
.1/50
MUTE/
R92
20K
Q8
2N3904
R112
10K
R91
10K
-15V
+5VA
R13
10K
3
A3
DOLBYEN/
R12
10K
Q2
2N3906
R14
2.0K
DOLBYEN
R15
10K
C8
.1/50
-15V
LCH ANALOG BD LINK
J17
J7
RCH ANALOG BD LINK
J4
CR29
1N4004
U27
7815
VIN VOUT
TO220
GND
ANALOG POWER SUPPLY
TO POWER SUPPLY BD
+15V
TO UP
J19
C95
.1/50
C96
330/50
C88
330/25
CR31
1N4004
C101
.1/50
C94
330/50
C87
330/25
CR30
1N4004
GND
VIN VOUT
TO220
7915
U26
-15V
CR32
1N4004
+15V
C37
.1/50
C34
.1/50
C48
.1/50
C3
.1/50
C97
.1/50
C40
.1/50
C89
.1/50
C69
.1/50
C406
.1/50
BYPASS CAPS
-15V
C4
.1/50
C43
.1/50
C100
.1/50
C35
.1/50
C90
.1/50
C70
.1/50
C47
.1/50
C38
.1/50
C407
.1/50
+5VA
C21
.1/50
C91
.1/50
C56
.1/50
LF353
U9
MC33077
U8

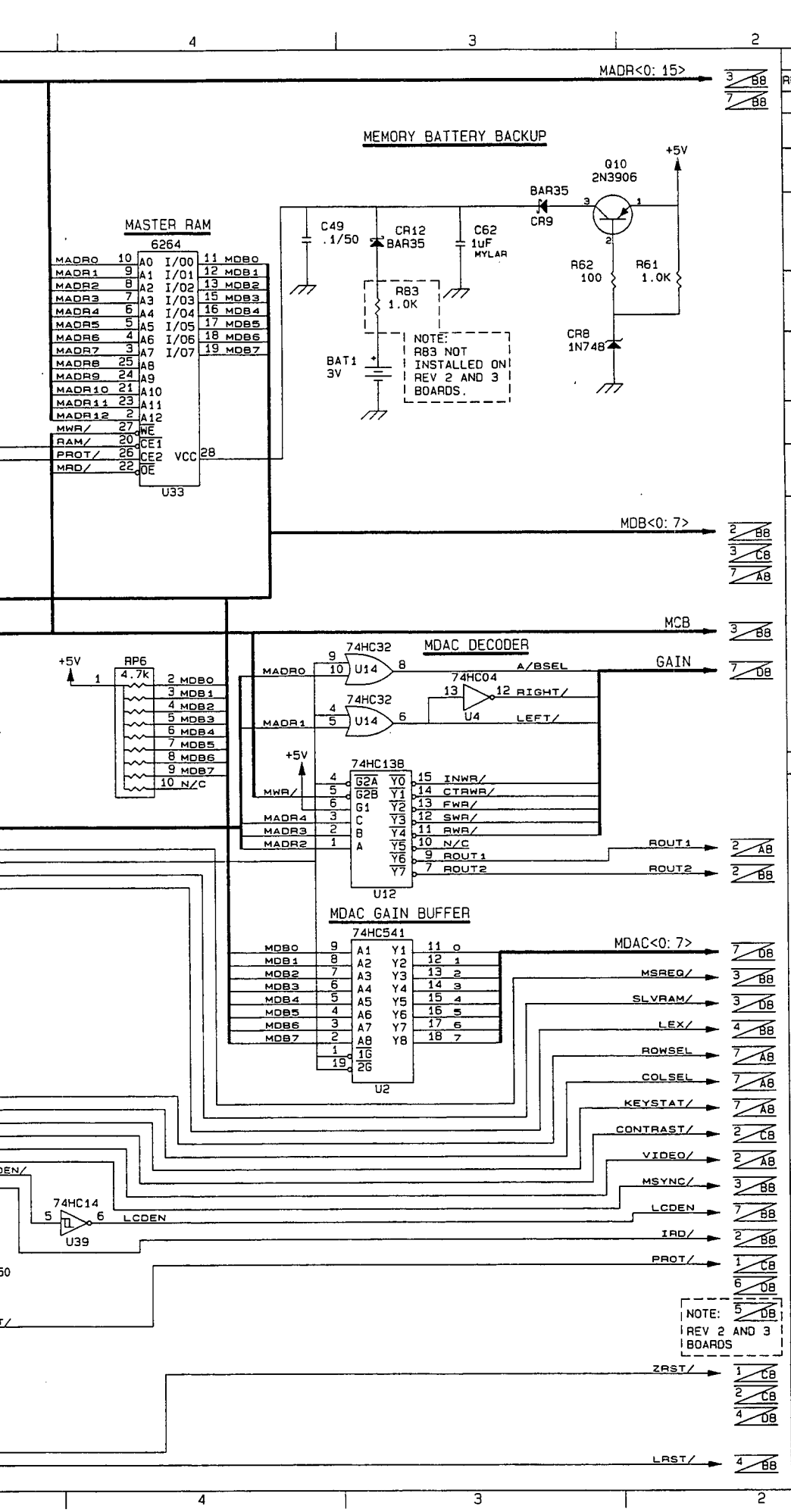


REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	RS 03/07/90	
1	REVISED	RS 07/17/90	
2	RELEASED FOR PRODUCTION	RW 02/07/91	RWH 02/07/91
		AF 02/07/91	AF 02/07/91
3	REVISED PER DCR 920511-01	6/04/92	6/5/92
		6/11/92	6/5/92



CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA. 02154				
APPROVALS	DATE	TITLE SCHEM, ANALOG BD, LOWER, CP-3			
DRAWN RW	02/07/91				
CHECKED AF	02/07/91	SIZE D	CODE	NUMBER 060-08128	REV. 3
G.C. RWH	02/07/91				
ISSUED AF	02/07/91	SHEET 5 OF 5			


MASTER PROCESSOR
Z80 6MHz
R29 1.0K
+5V
ZCLK (4.608MHz)
MWAIT/
MCB
ZRST/
PROT/
SCB
DADR<0:13>
ACC/
MDB0
MDB1
MDB2
MDB3
MDB4
MDB5
MDB6
MDB7
INT/
PFAIL/
U24
R43 3.3K
R45 3.3K
* SEE NOTE 8.
W1
W2
ROM
27512
ROM/
U25
MASTER DECODER
GAL16V8
ROM/ 0000-CFFF
RAM/ F000-FFFF
MSREQ/ D400-EFFF
MDAC/ D000-D3FF
SLVRAM/ E000-EFFF (0000-1FFF)
LEX/ D400-D7FF (2000-23FF)
U13
74HC04
U4
I/O DECODER
74HC138
ROWSEL
COLSEL
KEYSTAT/
CONTRAST/
VIDEO/
MSYNC/
LCDEN/
IRD/
U15
R77 5.1K
NOTE: CR16 AND R69 ARE CONNECTED TO +5V ON REV 2 AND 3 BOARDS. NOT PFAIL/!
CR16 1N4148
R69 10K
C65 22/25
C57 2.2/50
CR13 1N4148
SYSTEM RESET
74HC14
U39
R65 10K
CR17 BAR35
NOTE: CR17 IS NOT INSTALLED IN REV 2 AND 3 BOARDS
R59 1.0K
R57 1.0K
ZRST/
LRST/
MASTER RAM PROTECT
Q12 2N3904
Q11 2N3906
Q9 2N3904
R66 10K
R63 10K
R67 1.0K
C63 .1/50



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	PF/RS	
1	REVISED	RS 6/27/90 BACK-ANNO 7/16/90	
2	RELEASED FOR PRODUCTION	RW 10/25/90 AEJ 11/05/90	RW 10/25/90 AF 11/05/90
3	ADDED R77, CHANGED U12.5 FROM MMREQ/ TO MWR/, UPDATED DOC CTL BLOCK, CORRECTED Z LOCATORS, PER ECO 910117-00. ADDED R77 NOTE, PER ECO 910117-00-A.	RW 2/8/91 AEJ 2/8/91	RWH 2/8/91 AF 2/8/91
4	CHANGD R51 FROM 330 OHM, TO 100 OHM. R44 FROM 1K TO 75 OHM. UPDATED DOC CTL BLK, PER ECO 910415-00.	MF 5/7/91 RM 5/7/91	RWH 5/7/91 AF 5/8/91
5	DELETED R26. CHANGED C53 AND R6. ADDED NOTES 1 & 2 AND C71. CHANGED DOC CTL BLK PER ECO 910809-00. (SEE PAGE 5)	MF 10/8/91 AEJ 10/10/91	RWH 10/22/91 AF 10/22/91
6	MULTIPLE CHANGES PER ECO 911210-01	2/27/92 3/6/92	2/27/92 2/27/92
7	CHANGED SHEETS 4 & 7, UPDATED DOC CTL BLK PER ECO # 920421-00-A	5/1/92 5/7/92	5/1/92 6/30/92

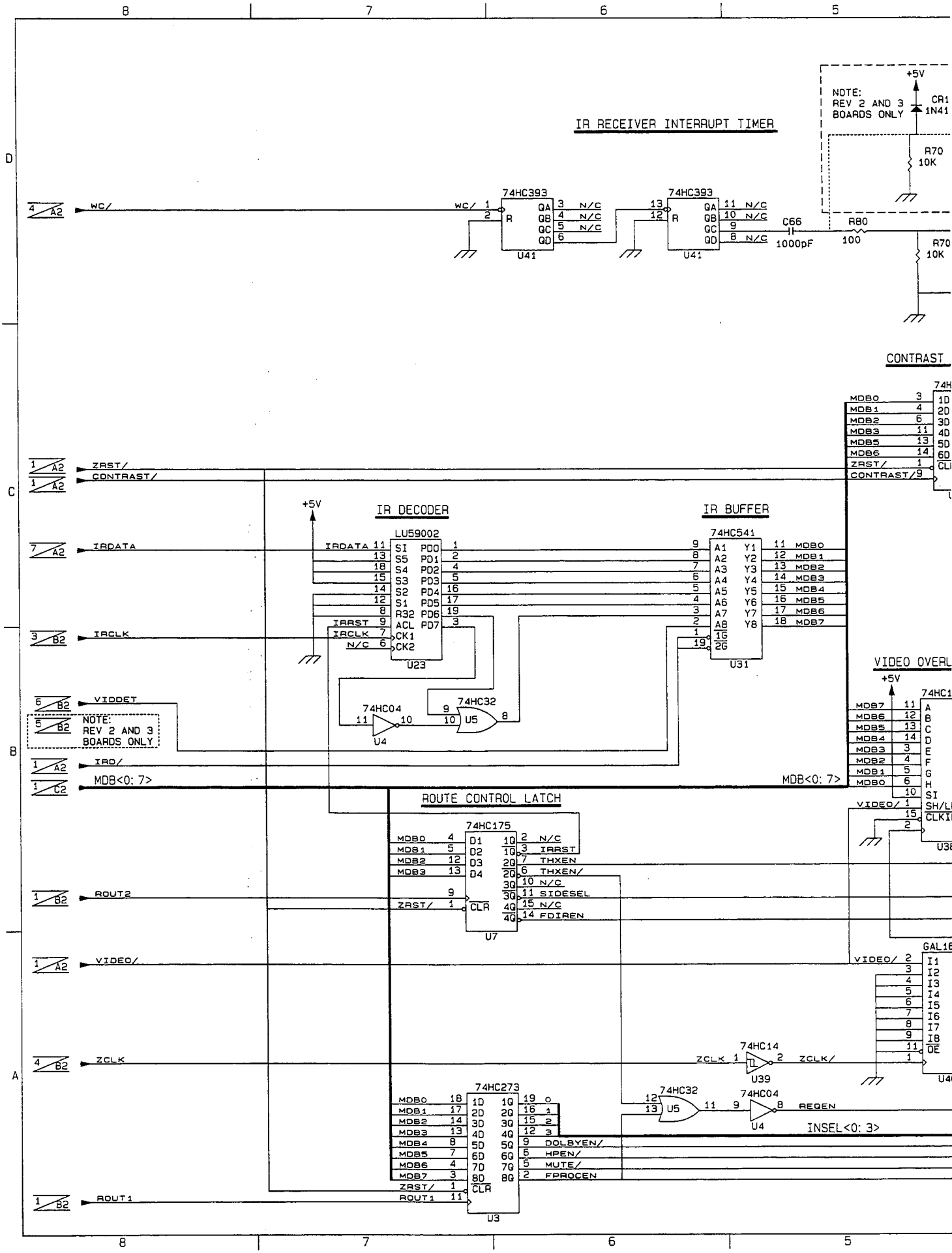
NOTES

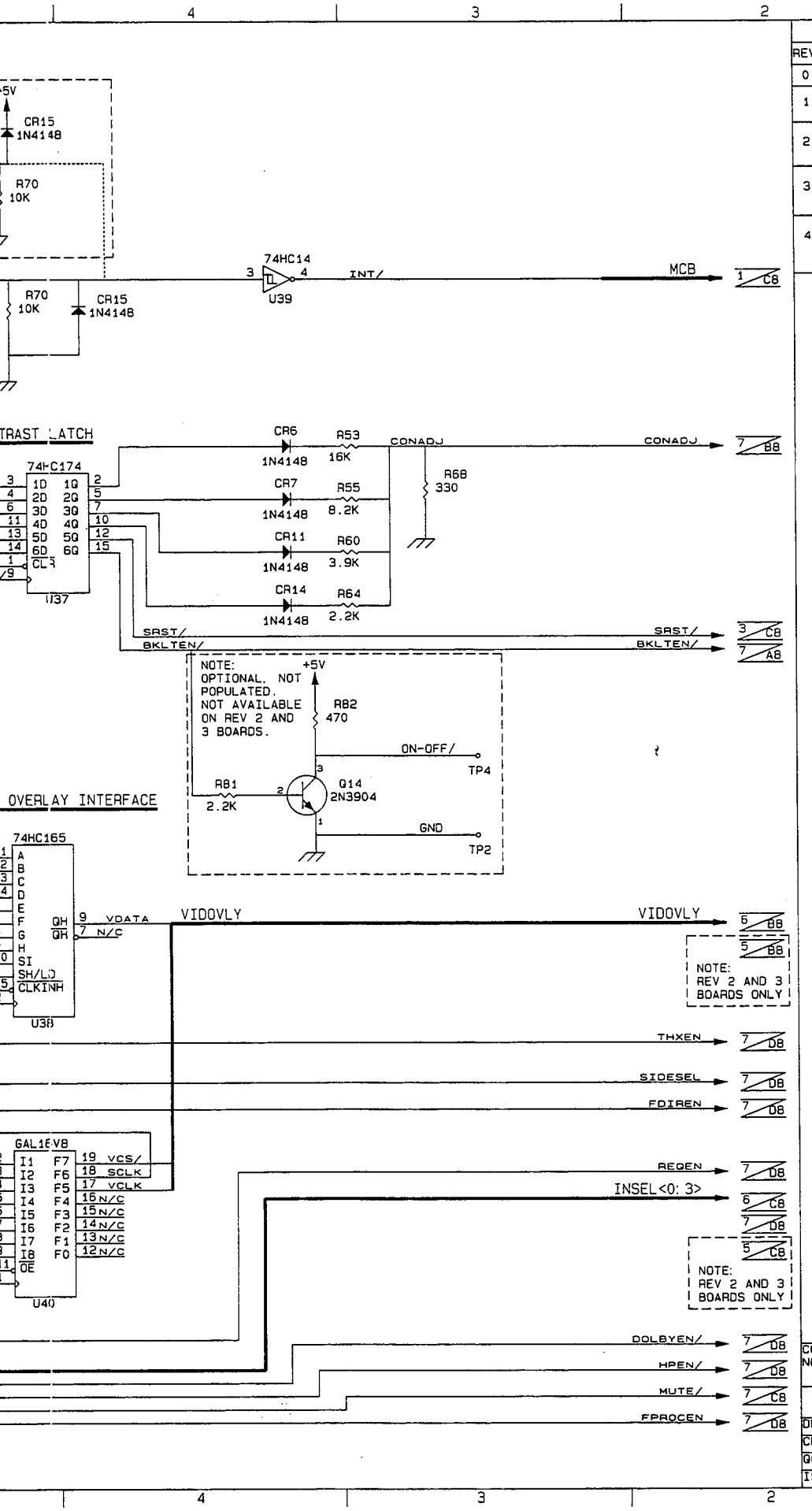
1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE uF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. VIDEO GROUND, DIGITAL GROUND, CHASSIS GROUND
5. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION
7. REFERENCE DESIGNATORS, LAST USED: C86, CR17, FB6, L3, Q14, R83, U40, J10, W3, TP4.
8. TO ENTER DIAGNOSTIC MODE, POWER DOWN, AND REMOVE W1, AND W2.

DOCUMENT CONTROL BLOCK: #060-08135

SHEET NUMBER	REVISION
1 OF 7	7
2 OF 7	4
3 OF 7	4
4 OF 7	5
5 OF 7	6
6 OF 7	0
7 OF 7	5

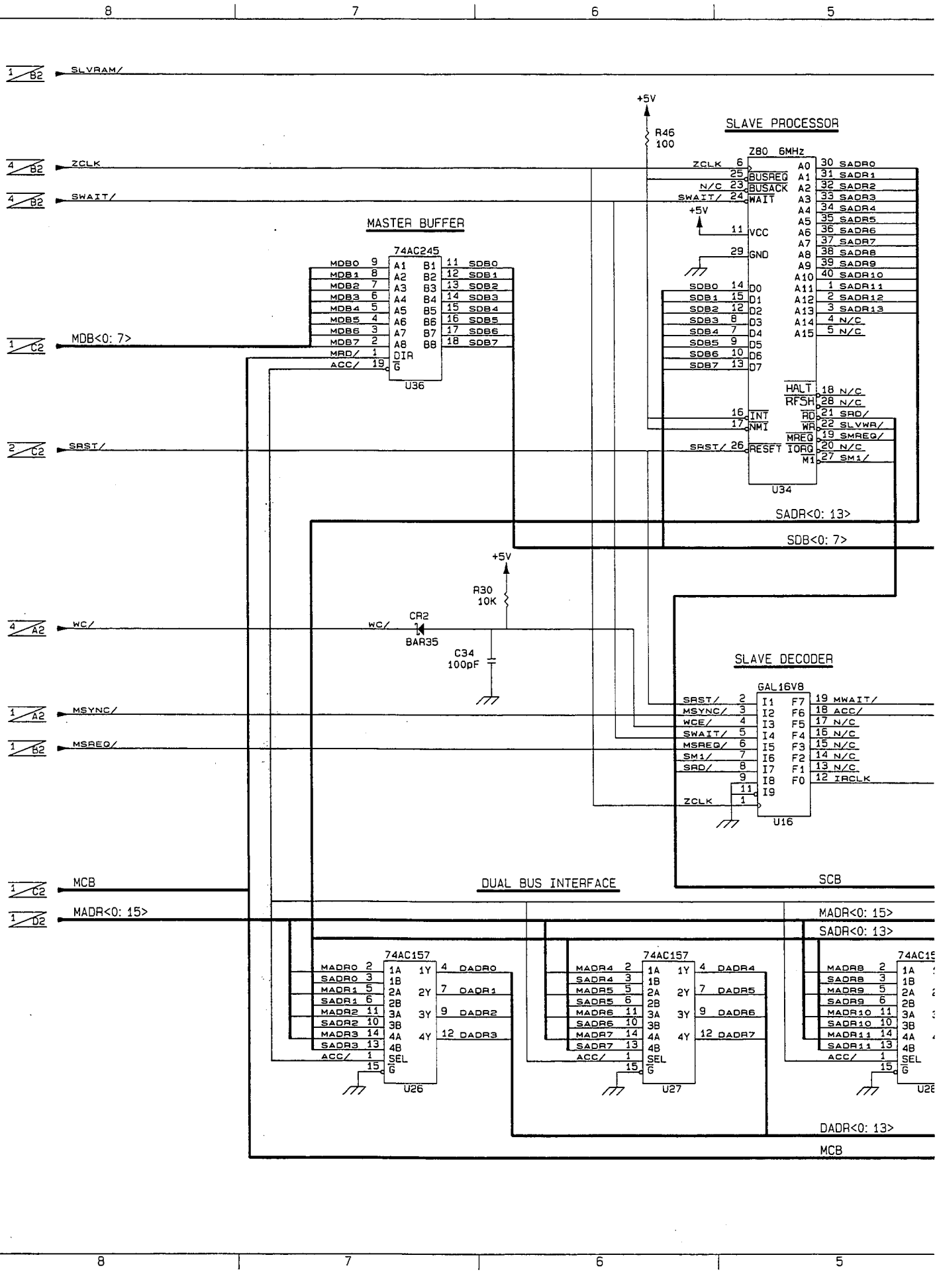
CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154			
APPROVALS	DATE	TITLE SCHEM, DIGITAL BD, CP-3 MASTER PROCESSOR		
DRAWN PF	02/05/90			
CHECKED AJ	11/5/90	SIZE: D	CODE:	NUMBER: 060-08135 REV: 7
Q.C. RW	10/25/90			
ISSUED AF	11/5/90	SHEET 1 OF 7		

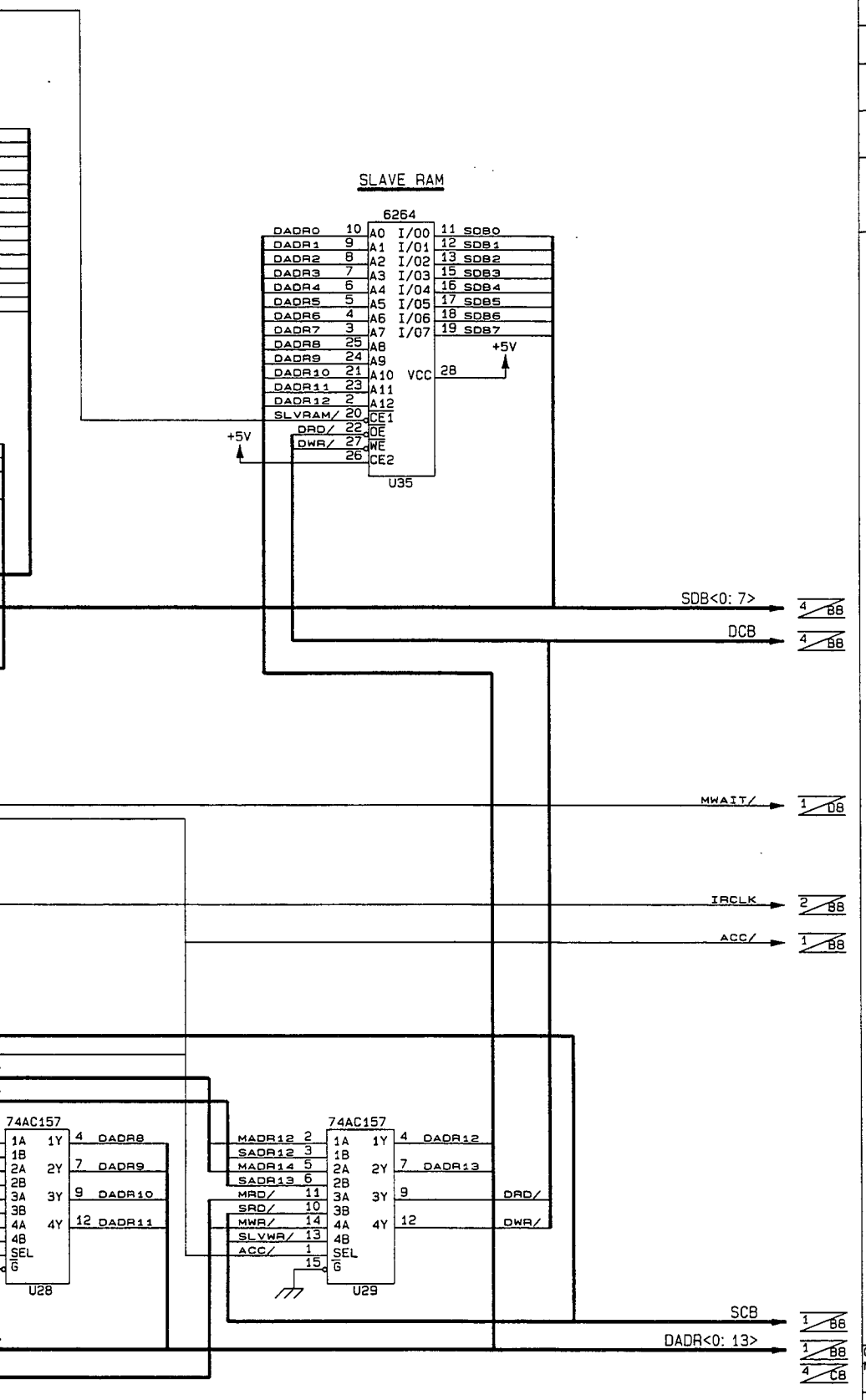

IR RECEIVER INTERRUPT TIMER
NOTE:
REV 2 AND 3
BOARDS ONLY
+5V
CR1
1N41
R70
10K
74HC393
U41
C66
1000pF
R80
100
CONTRAST
IR DECODER
LU59002
IR BUFFER
74HC541
VIDEO OVERL
74HC1
ROUTE CONTROL LATCH
74HC175
74HC273
74HC14
74HC32
74HC04
GAL16
WC/
ZRST/
CONTRAST/
IRDATA
IRCLK
VIDDET
IRD/
MDB<0: 7>
ROUT2
VIDEO/
ZCLK
ROUT1
IRRST
THXEN
THXEN/
SIDESEL
FDIREN
DOLBYEN/
HPEN/
MUTE/
FPROCEN
REGEN
INSEL<0: 3>
ZCLK/



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE		
1	REVISED	RS 6/27/90	
2	RELEASED FOR PRODUCTION	RW 10/25/90 AEJ 11/05/90	RW 11/05/90 AF 11/05/90
3	CORRECTED Z LOCATORS. PER ECO 910117-00.	RW 2/8/91 AEJ 2/8/91	RWH 2/8/91 AF 2/8/91
4	ADDED CIRCUIT FUNCTION LABELS. CHANGED INTERRUPT CIRCUITRY. ADDED ON OFF/ CIRCUITRY PER ECO 911210-01.	4/2/92 EJ 2/26/92	4/27/92 AF 2/27/92

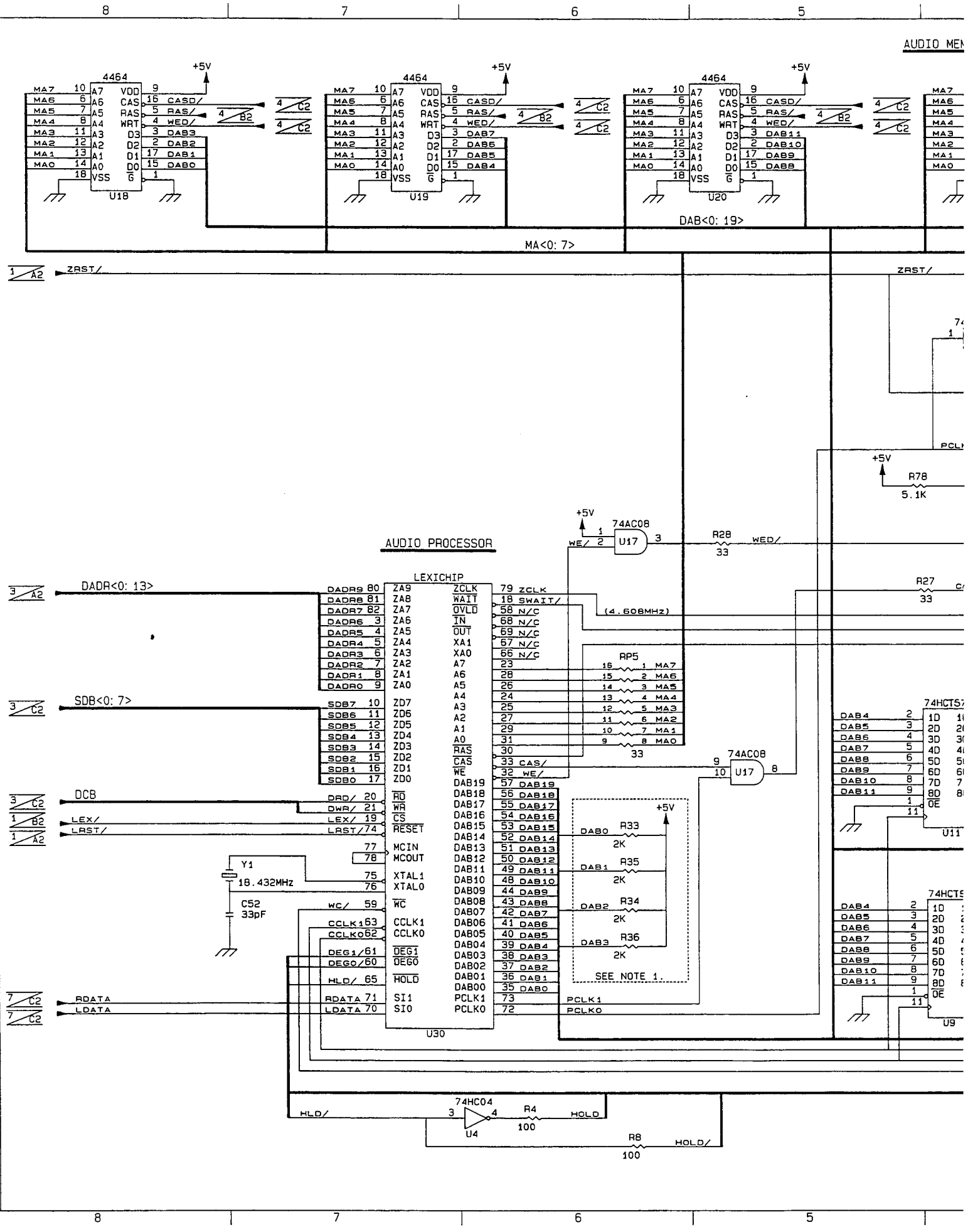
CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEM, DIGITAL BD, CP-3 PERIPHERAL DECODE
DRAWN PF	02/01/90	
CHECKED AJ	11/5/90	SIZE: D; CODE: ; NUMBER: 060-08135; REV.: 4
QC RW	10/25/90	
ISSUED AF	11/5/90	SHEET 2 OF 7


SLVRAM/
ZCLK
SWAIT/
MDB<0: 7>
SRST/
WC/
MSYNC/
MSREQ/
MCB
MADR<0: 15>
SLAVE PROCESSOR
Z80 6MHz
R46
100
+5V
MASTER BUFFER
74AC245
U36
U34
SADR<0: 13>
SDB<0: 7>
R30
10K
CR2
BAR35
C34
100pF
SLAVE DECODER
GAL16V8
U16
SCB
DUAL BUS INTERFACE
74AC157
U26
U27
U28
DADR<0: 13>
MCB

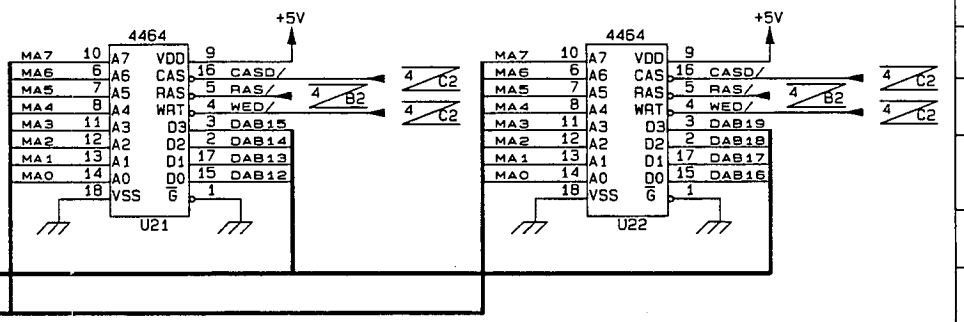


REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE		
1	REVISED	RS 6/27/90	
2	RELEASED FOR PRODUCTION	RW 10/25/90 AEJ 1105/90	RW 1105/90 AF 1105/90
3	CORRECTED Z LOCATOR'S. PER ECO NO. 910117-00.	RW 2/8/91 AEJ 2/8/91	RWH 2/8/91 AF 2/8/91
4	CHANGED U34.22 AND U29.13 FROM SWA/ TO SLVWR/. CORRECTED "Z" LOCATOR'S. U35 PIN NAMES AND CHANGED TOTAL SHEET NO. FROM 6 TO 7 PER ECO 911210-01	RWH 7/25/92 EJ 7/16/92	RWH AF 8/27/92

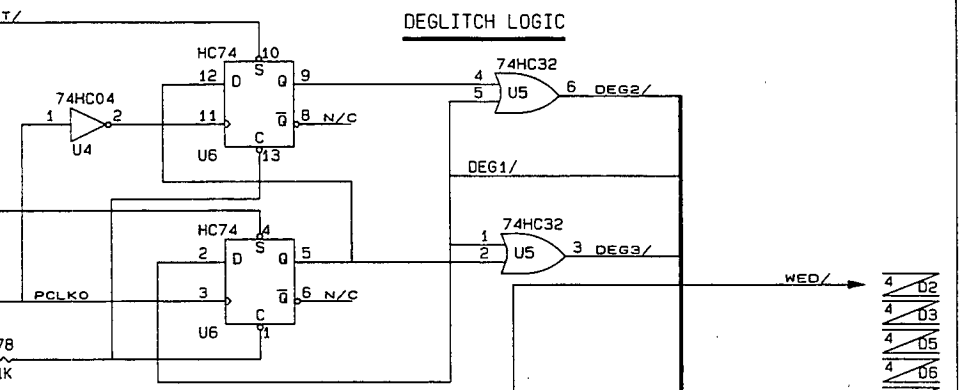
CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEMATIC, DIGITAL BD, CP-3 SLAVE PROCESSOR
DRAWN PF	02/01/90	
CHECKED AJ	11/5/90	SIZE: D; CODE: ; NUMBER: 060-08135; REV.: 4
G.C. RW	10/25/90	
ISSUED AF	11/5/90	SHEET 3 OF 7

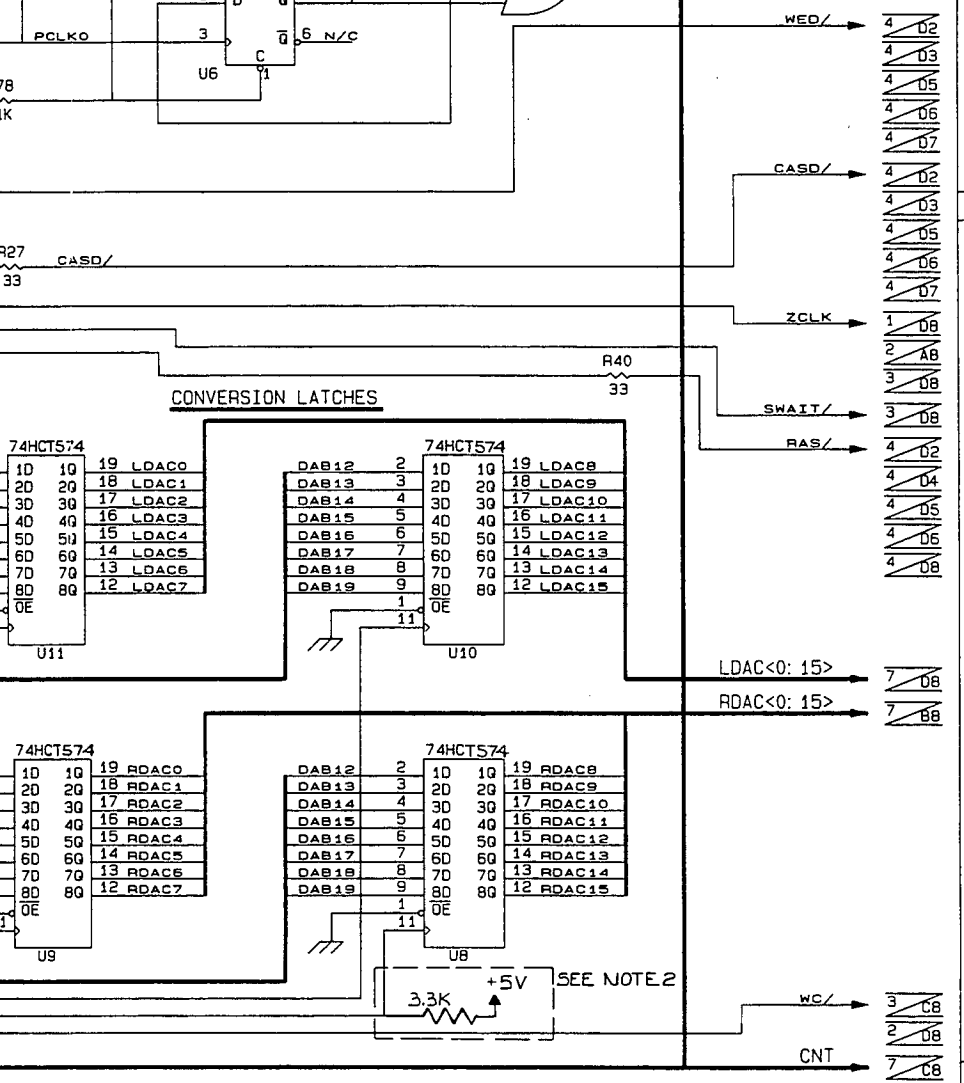

AUDIO MEM
4464
U18
U19
U20
+5V
MA<0: 7>
DAB<0: 19>
ZRST/
AUDIO PROCESSOR
LEXICHIP
U30
DADR<0: 13>
SDB<0: 7>
DCB
LEX/
LRST/
RDATA
LDATA
Y1
18.432MHz
C52
33pF
74AC08
U17
R28
33
WED/
WE/
R27
(4.608MHz)
RP5
R33
R35
R34
R36
2K
SEE NOTE 1.
R78
5.1K
74HCT574
U11
U9
74HC04
U4
R4
100
R8
HLD/
HOLD
HOLD/
PCLK1
PCLK0
SWAIT/
RAS
CAS
WE
RD
WR
CS
RESET
MCIN
MCOUT
XTAL1
XTAL0
WC/
CCLK1
CCLK0
DEG1/
DEG0/
SI1
SI0

DIO MEMORY

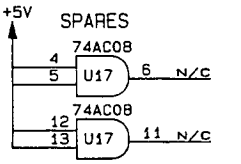


DEGLITCH LOGIC





CONVERSION LATCHES



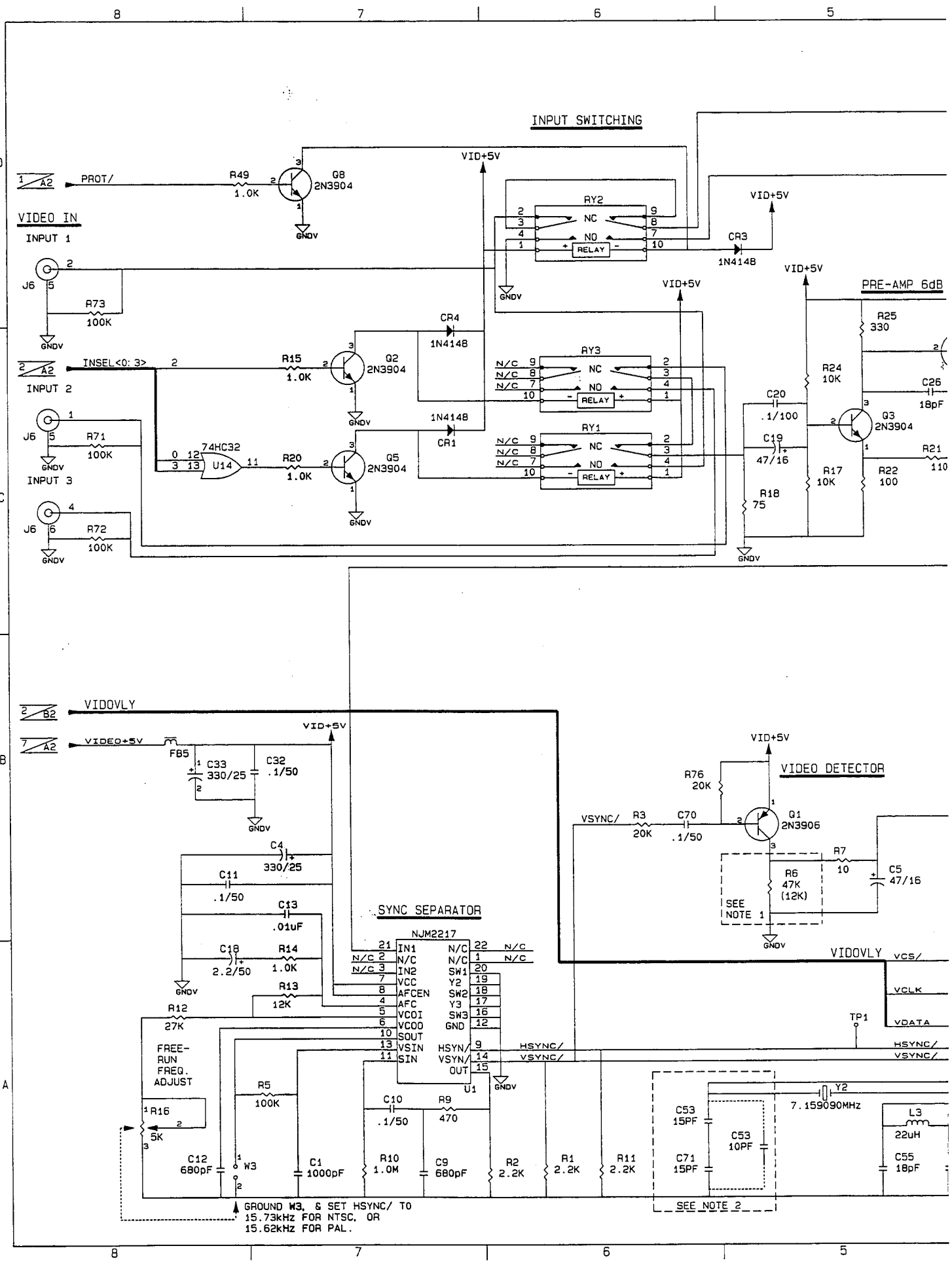
REVISIONS

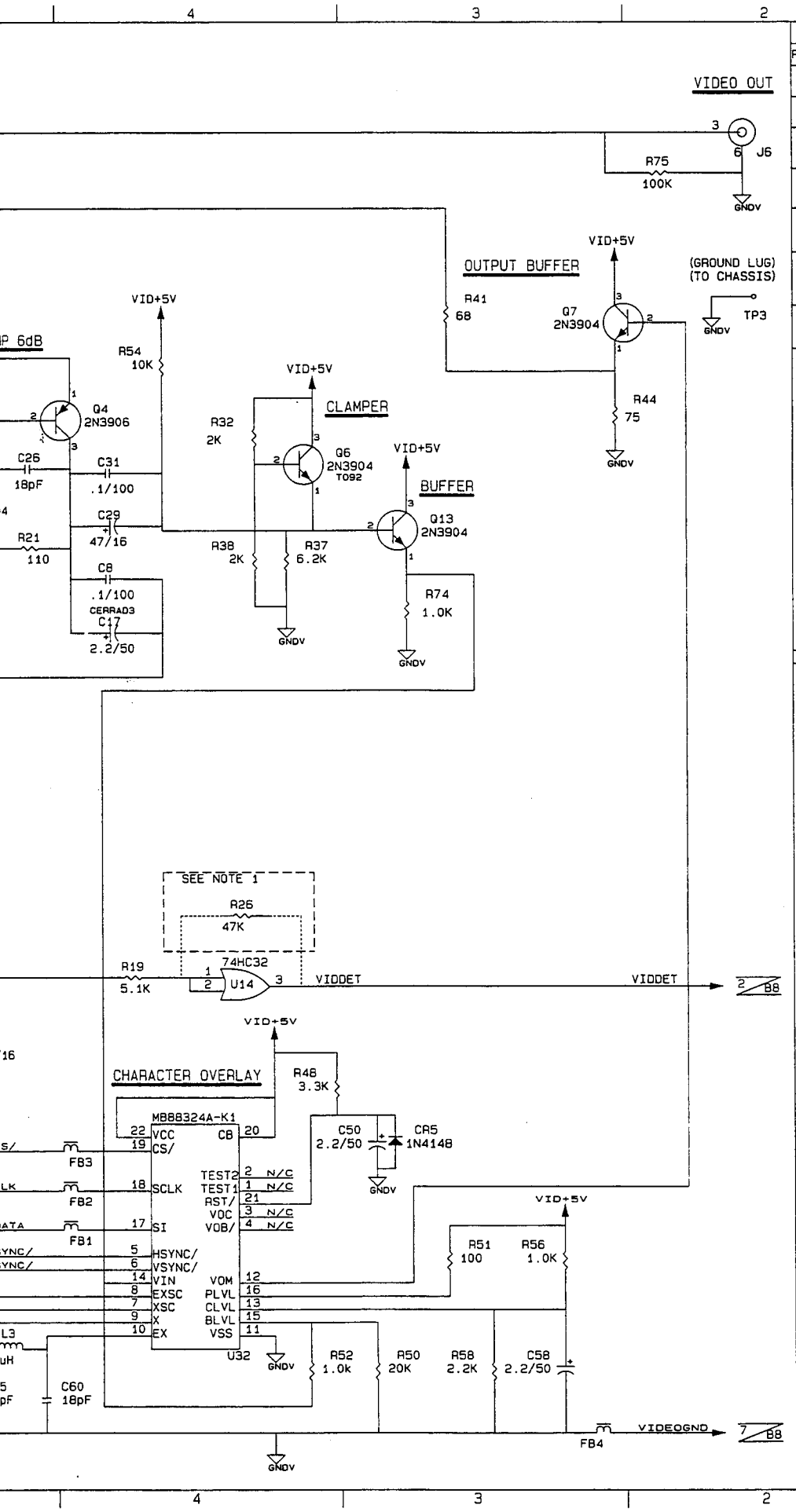
REV	DESCRIPTION	DRAFTER/ CHECKER	G.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	PF/RS	
1	REVISED	RS 6/27/90	
2	RELEASED FOR PRODUCTION	RW AEJ 11/05/90	RW 10/25/90 AF 11/05/90
3	ADDED R78. DISCONNECTED U6.1, 13 FROM THXEN CONNECTED TO R78. CORRECTED Z LOCATORS. PER ECO 910117-00.	RW 2/8/91 AEJ 2/8/91	RWH 2/8/91 AF 2/8/91
4	ADDED CIRCUIT FUNCTION LABELS AND CHANGED Z LOCATORS PER ECO 911210-01	5/26/92	2/27/92 AF 2/27/92
5	ADDED R84 NOTE2 AND CHANGE U8-U11 TO HCT PER ECO# 920421-00-A	5-7-92 6/11/92	6-4 6/3/92 AF 6/30/92

NOTES

1. R33-36 NOT INSTALLED.
2. R84 MAY BE ADDED IF 74HC574'S ARE INSTALLED AT U8-U11.

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEM, DIGITAL BD, CP-3 DRAM AND LEXICHIP
DRAWN PF	02/01/90	
CHECKED AJ	11/5/90	SIZE: D; CODE: ; NUMBER: 060-08135; REV.: 5
Q.C. RW	10/25/90	
ISSUED AF	11/5/90	SHEET 4 OF 7


INPUT SWITCHING
VIDEO IN
INPUT 1
INPUT 2
INPUT 3
PROT/
R49
1.0K
Q8
2N3904
VID+5V
RY2
RY3
RY1
NC
NO
RELAY
CR3
1N4148
CR4
CR1
J6
R73
100K
R71
R72
INSEL<0:3>
R15
R20
Q2
Q5
74HC32
U14
GNDV
PRE-AMP 6dB
R25
330
R24
10K
C26
18pF
C20
.1/100
C19
47/16
Q3
2N3904
R21
R22
100
R17
10K
R18
75
VIDOVLY
VIDEO+5V
FB5
C33
330/25
C32
.1/50
C4
330/25
C11
.1/50
C13
.01uF
C18
2.2/50
R14
1.0K
R13
12K
R12
27K
FREE-
RUN
FREQ.
ADJUST
R16
5K
SYNC SEPARATOR
NJM2217
IN1
IN2
VCC
AFCEN
AFC
VCOI
VCOO
SOUT
VSIN
SIN
N/C
SW1
SW2
SW3
Y2
Y3
GND
HSYN/
VSYN/
OUT
U1
HSYNC/
VSYNC/
VIDEO DETECTOR
R76
20K
VSYNC/
R3
20K
C70
.1/50
Q1
2N3906
R7
10
C5
47/16
R6
47K
(12K)
SEE
NOTE 1
VCS/
VCLK
VDATA
TP1
R5
100K
C10
.1/50
R9
470
Y2
7.159090MHz
L3
22uH
C53
15PF
C53
10PF
C71
15PF
C55
18pF
SEE NOTE 2
C12
680pF
W3
C1
1000pF
R10
1.0M
C9
680pF
R2
2.2K
R1
2.2K
R11
2.2K
GROUND W3, & SET HSYNC/ TO
15.73kHz FOR NTSC, OR
15.62kHz FOR PAL.

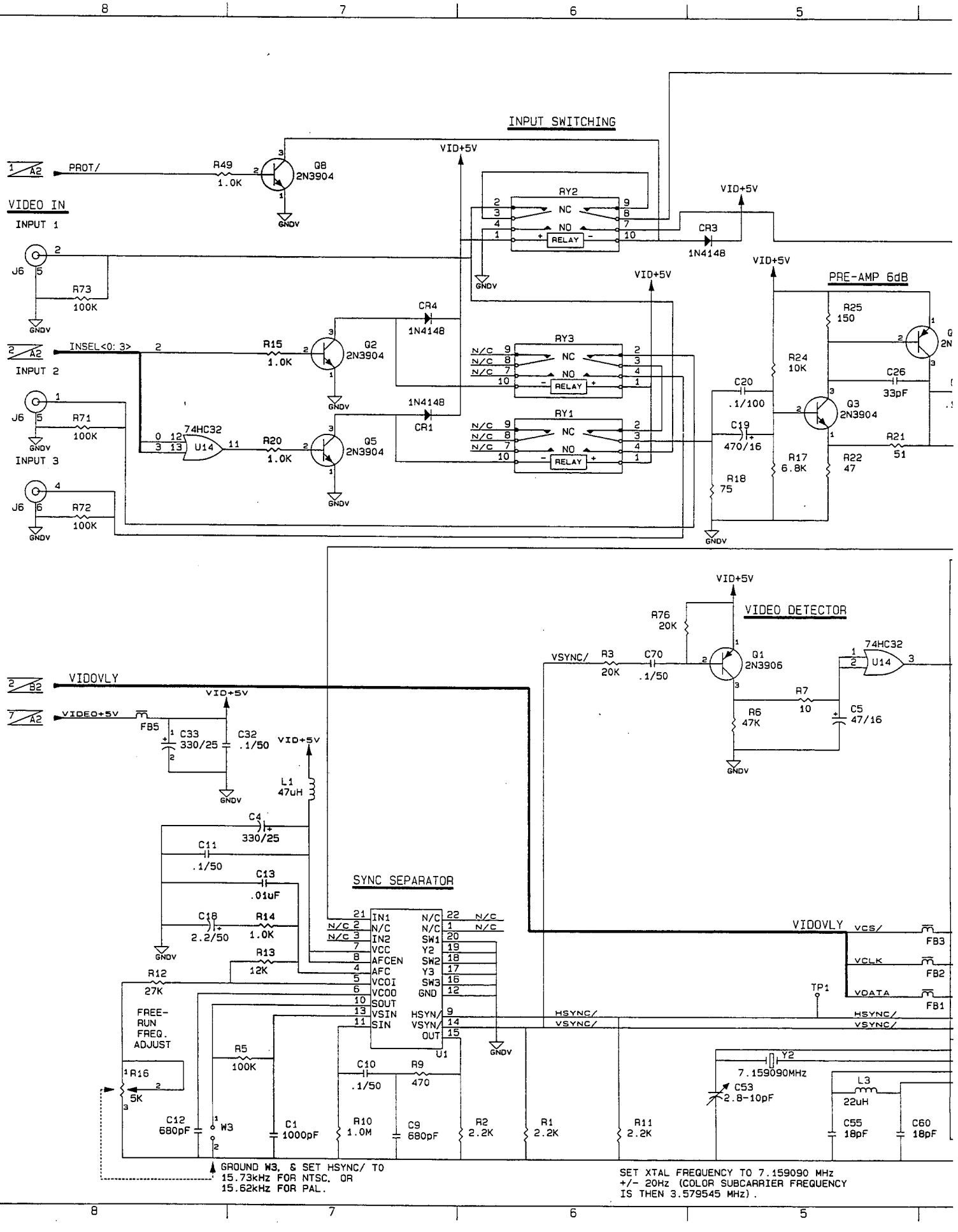


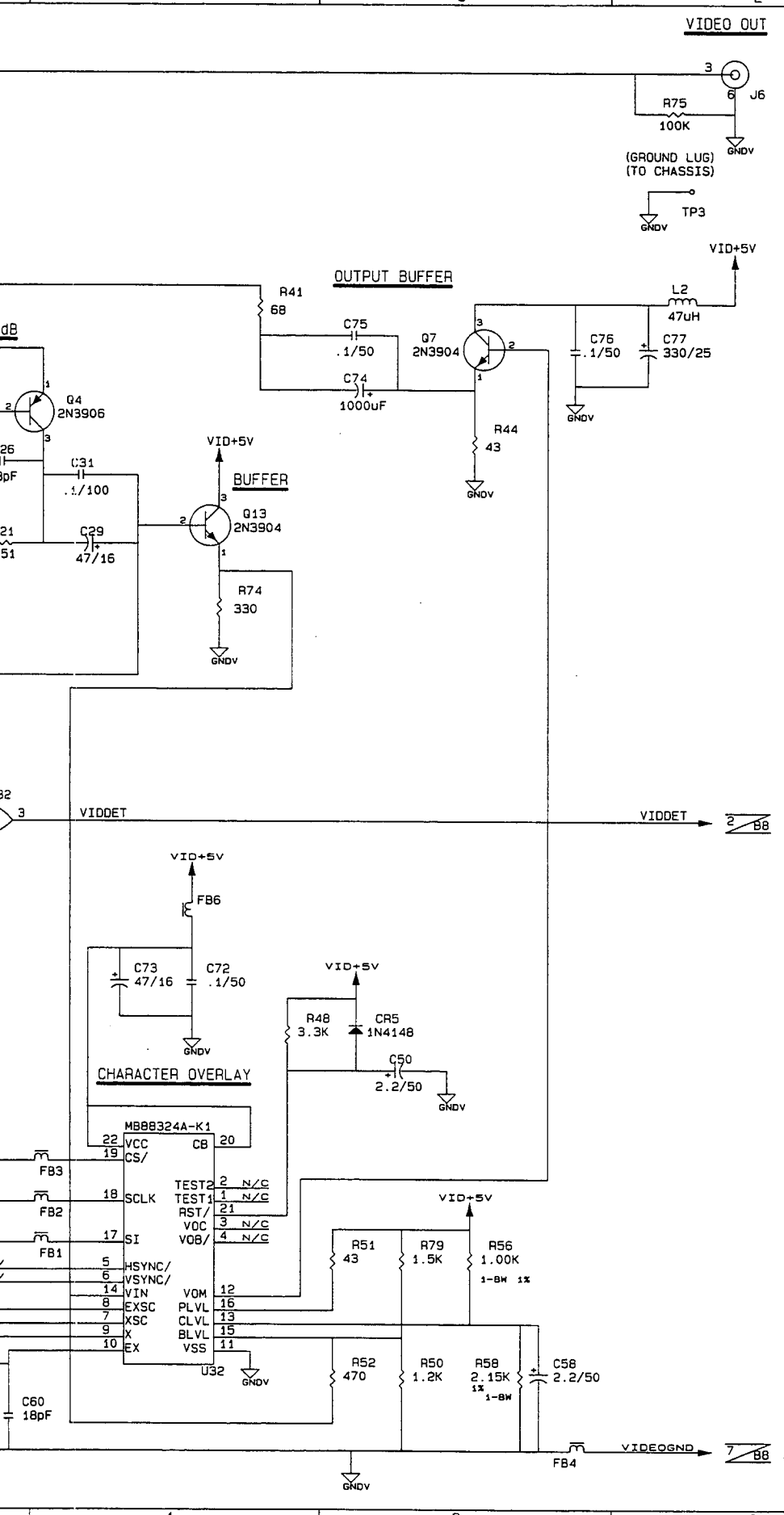
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE		
1	REVISED	RS 6/27/90	
2	RELEASE FOR PRODUCTION	RW 10/25/90 AEJ 11/05/90	RW 11/05/90 AF 11/05/90
3	CORRECTED Z LOCATORS, PER ECO 910117-00.	RW 2/8/91 AEJ 2/8/91	RWH 2/5/91 AF 2/8/91
4	CHANGED R51 FROM 330 OHM TO 100 OHM, R44 FROM 1K TO 75 OHM, PER ECO 910415-00	MF 5/7/91 RW 5/7/91	RWH 5/7/91 AF 5/8/91
5	DELETED R26, CHANGED C53 FROM 10pF TO 15pF, R6 FROM 12K TO 47K. ADDED NOTES 1, 2, AND C71 PER ECO 910809-00	MF 10/8/91 AEJ 10/9/91	RWH 10/22/91 AF 10/22/91
6	ADDED NOTE 3 AND CIRCUIT FUNCTION LABELS PER ECO 911210-01	RW 2/26/92 EJ 2/26/92	RW 2/27/92 AF 2/27/92

NOTES:

1. ON REV 3 DIGITAL BOARDS R26 MAY BE ELIMINATED AND THE VALUE OF R6 IS THEN 47K.
2. ON THE REV 3 DIGITAL BOARD SOME UNITS HAVE C53 10pF, OTHERS HAVE TWO 15pF (C53, C71) CAPS IN SERIES IN C53 LOCATION.
3. THIS SCHEMATIC APPLIES TO REV 2 AND 3 BOARDS ONLY.

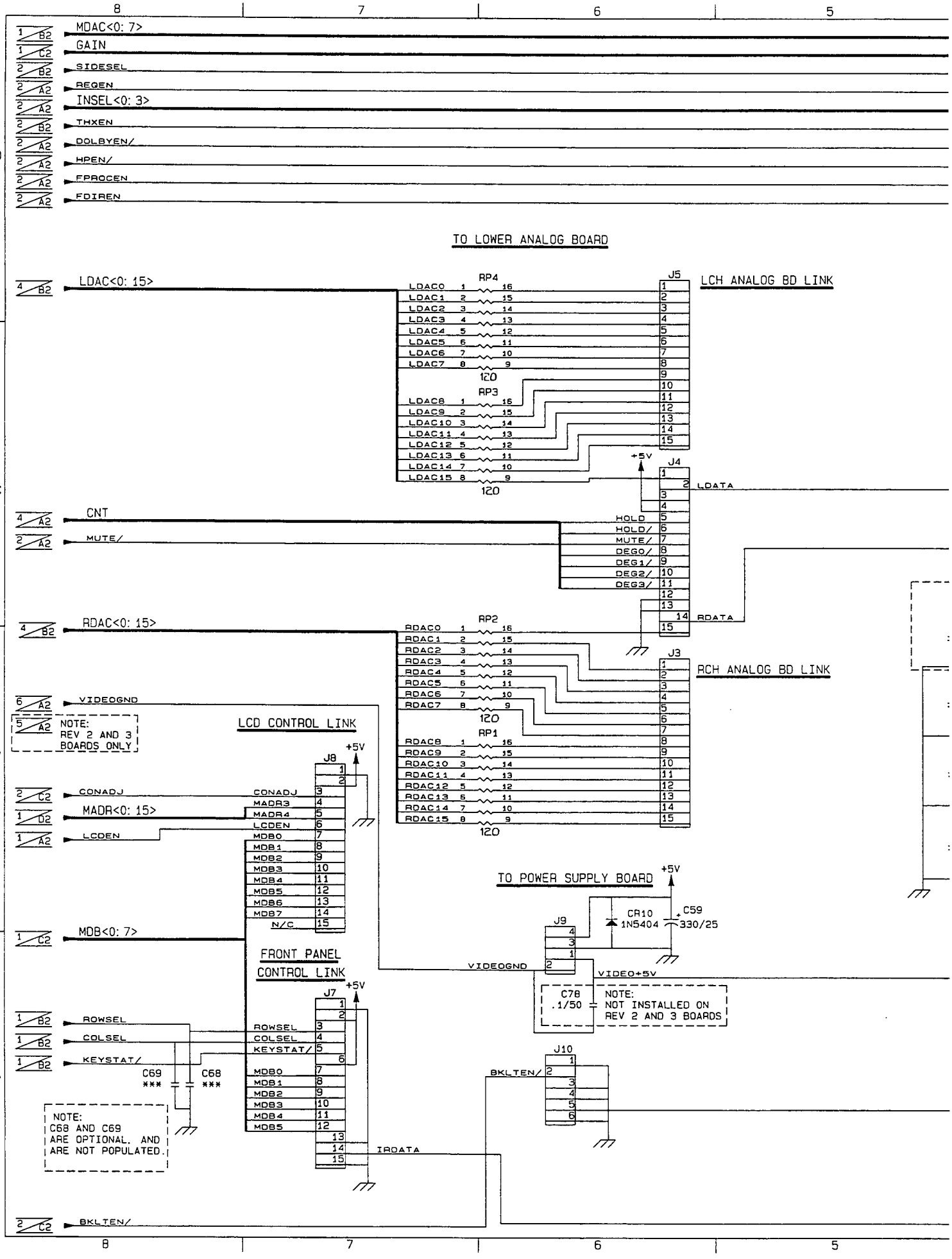
CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154				
APPROVALS	DATE	TITLE SCHEM, DIGITAL BD, CP-3 VIDEO OVERLAY			
DRAWN RS	6/14/89				
CHECKED AJ	11/5/90	SIZE	CODE	NUMBER	REV.
Q.C. RW	10/25/90	D		060-08135	6
ISSUED AF	11/5/90	SHEET 5 OF 7			

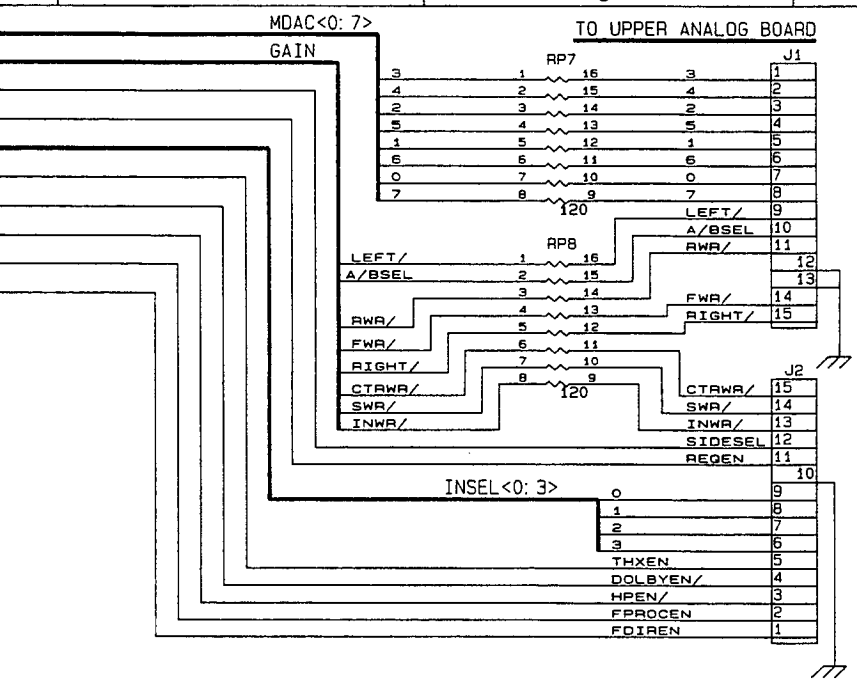

INPUT SWITCHING
VIDEO IN
INPUT 1
INPUT 2
INPUT 3
PROT/
INSEL<0:3>
VID+5V
GNDV
RELAY
NC
NO
PRE-AMP 6dB
VIDEO DETECTOR
VIDOVLY
VIDEO+5V
SYNC SEPARATOR
FREE-RUN FREQ. ADJUST
GROUND W3, & SET HSYNC/ TO 15.73kHz FOR NTSC, OR 15.62kHz FOR PAL.
SET XTAL FREQUENCY TO 7.159090 MHz +/- 20Hz (COLOR SUBCARRIER FREQUENCY IS THEN 3.579545 MHz).

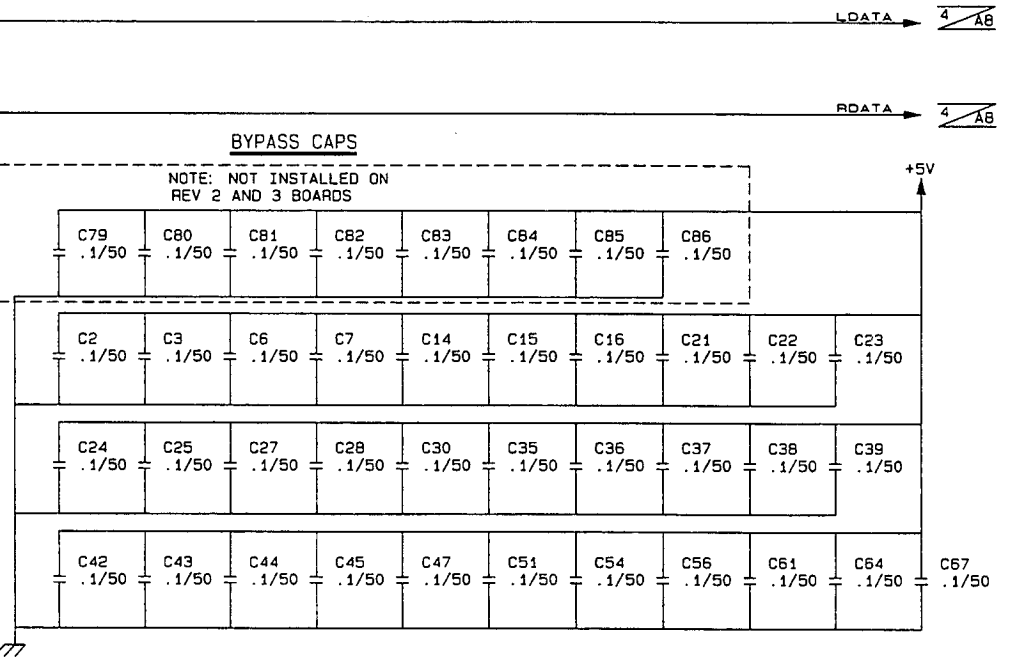


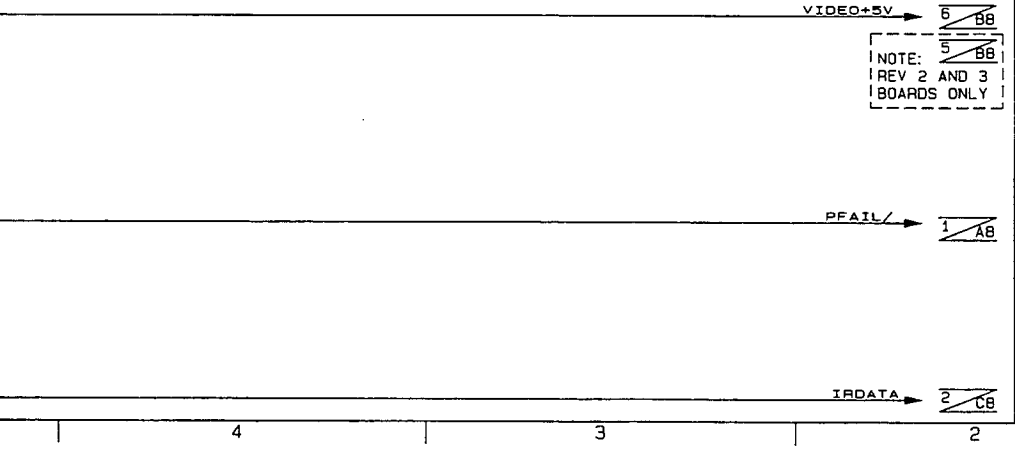
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	NEW PAGE CREATED FOR REV 4 BOARD PER ECO 911210-01	2/27/92 2/26/92	2/27/92 2/27/92

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE	SCHEM, DIGITAL BD, CP-3 VIDEO OVERLAY
DRAWN RW	2/25/92		
CHECKED EJ	2/26/92	SIZE D	CODE
Q.C. RW	2/27/92	NUMBER 060-08135	REV. 0
ISSUED F	2/27/92	SHEET 6 OF 7	

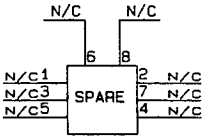

MDAC<0: 7>
GAIN
SIDESEL
REGEN
INSEL<0: 3>
THXEN
DOLBYEN/
HPEN/
FPROCEN
FDIREN
TO LOWER ANALOG BOARD
LDAC<0: 15>
RP4
RP3
J5
LCH ANALOG BD LINK
120
+5V
J4
LDATA
CNT
MUTE/
HOLD
HOLD/
MUTE/
DEG0/
DEG1/
DEG2/
DEG3/
RDATA
RDAC<0: 15>
RP2
RP1
J3
RCH ANALOG BD LINK
VIDEOGND
NOTE:
REV 2 AND 3
BOARDS ONLY
LCD CONTROL LINK
J8
CONADJ
MADR<0: 15>
LCDEN
MDB<0: 7>
N/C
TO POWER SUPPLY BOARD
J9
CR10
1N5404
C59
330/25
VIDEO+5V
C78
.1/50
NOTE:
NOT INSTALLED ON
REV 2 AND 3 BOARDS
FRONT PANEL
CONTROL LINK
J7
ROWSEL
COLSEL
KEYSTAT/
C69
***
C68
***
NOTE:
C68 AND C69
ARE OPTIONAL, AND
ARE NOT POPULATED.
J10
BKLTEN/
IRDATA
BKLTEN/





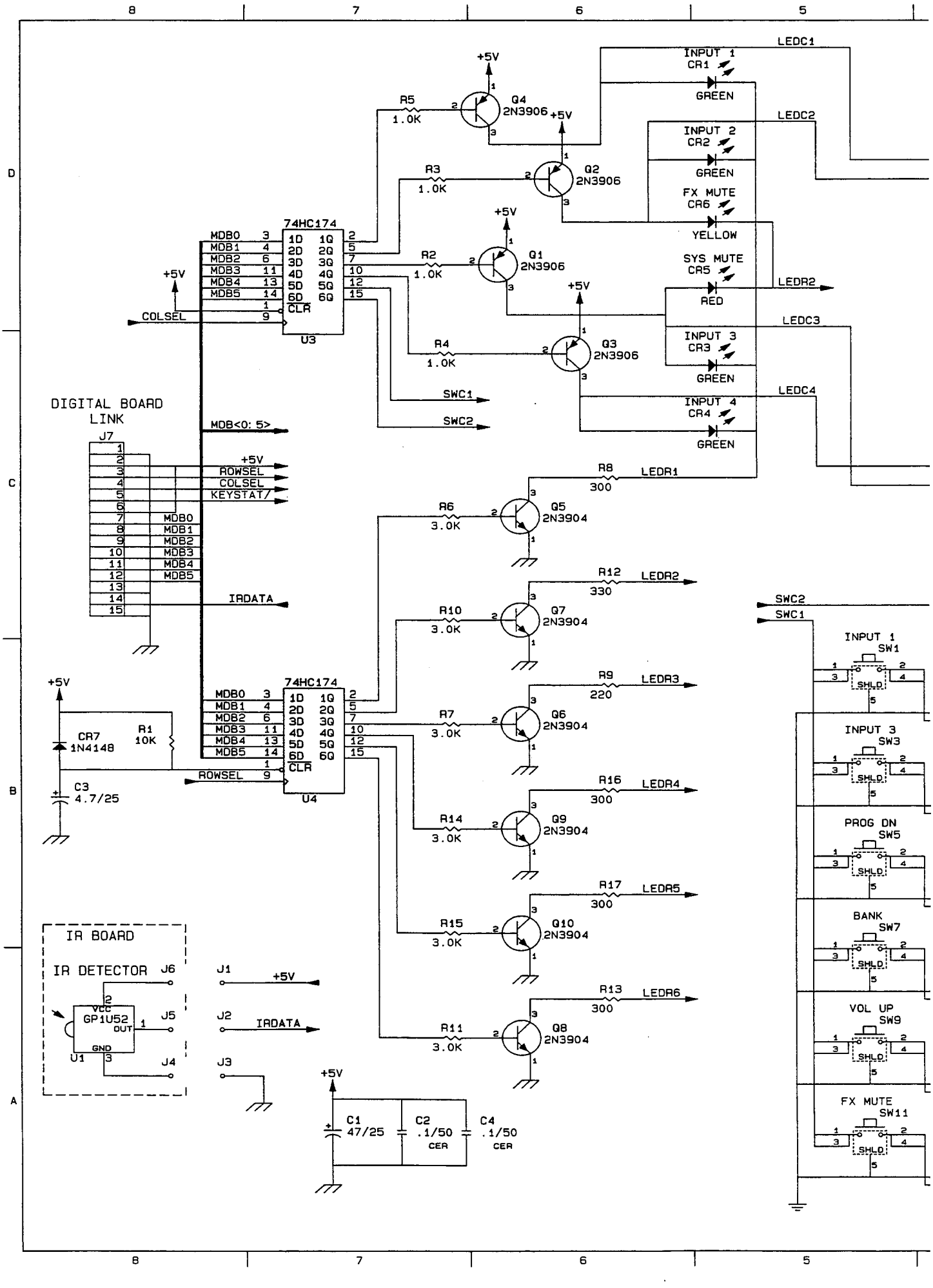


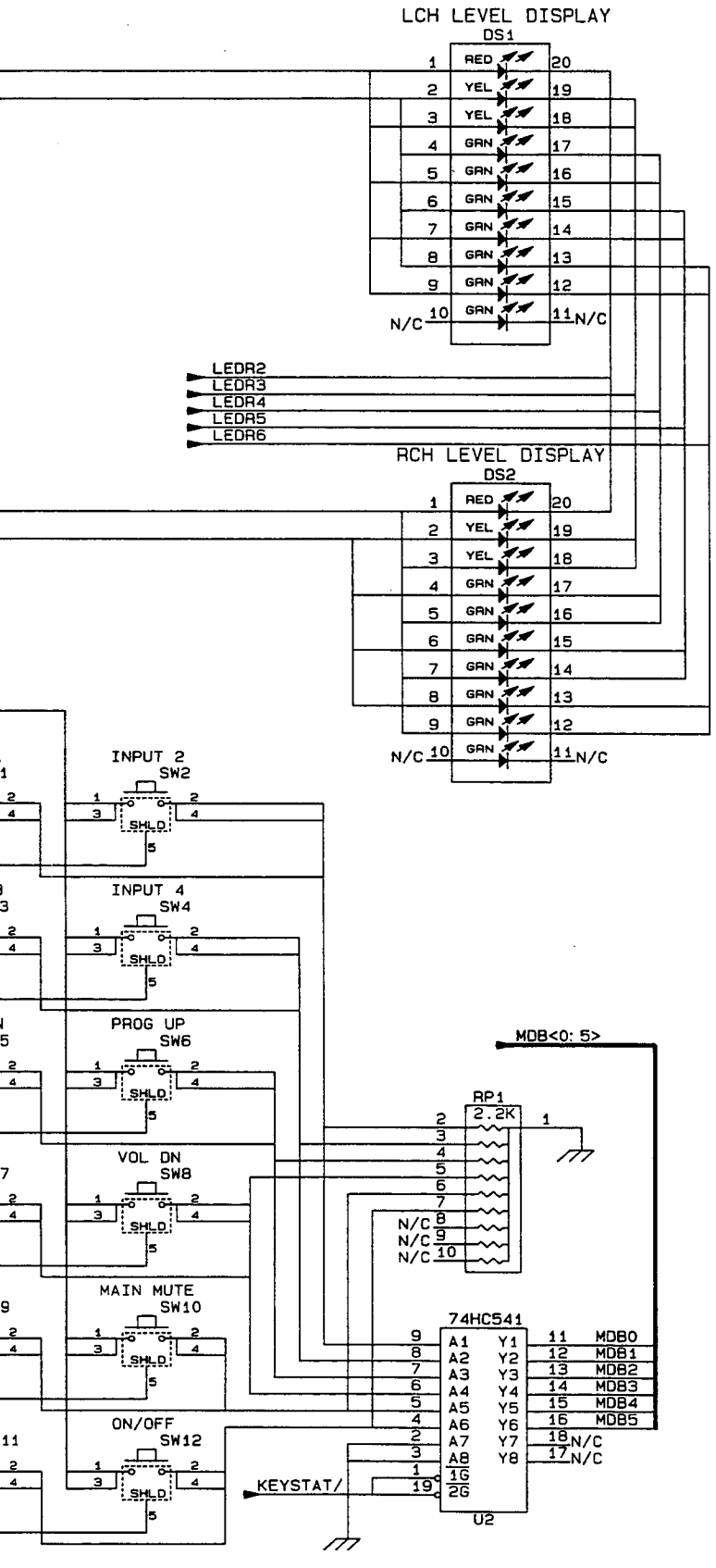
SPARE



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE		
1	REVISED	RS 6/28/90	
2	RELEASE FOR PRODUCTION	RW 10/25/90 AEJ 11/05/90	RW 10/25/90 AF 11/05/90
3	CHANGED RP7, AND RP8 FROM 150 TO 120, CORRECTED Z LOCATORS, DELETED NOTE. PER ECO 910117-00.	RW 2/8/91 AEJ 2/8/91	RWH 2/8/91 AF 2/8/91
4	ADDED CAPACITORS C78-C86, CHANGED SHEET NO. TO 7 AND CHANGED Z LOCATORS PER ECO 911210-01	2/19/92 2/26/92	2/27/92
5	CHANGES RP1-4 FROM 33 TO 120 PER ECO #920421-00-A	4/30/92 4/30/92	4/30/92 4/30/92

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154				
APPROVALS	DATE	TITLE SCHEM, DIGITAL BD, CP-3 BYPASS CAPS AND CONNECTORS			
DRAWN RS	09/01/89				
CHECKED AJ	11/5/90	SIZE D	CODE	NUMBER 060-08135	REV. 5
Q.C. RW	10/25/90				
ISSUED AF	11/5/90	SHEET 7 OF 7			


LEDC1
INPUT 1
CR1
GREEN
+5V
R5
1.0K
Q4
2N3906
LEDC2
INPUT 2
CR2
GREEN
+5V
R3
1.0K
Q2
2N3906
FX MUTE
CR6
YELLOW
74HC174
MDB0
MDB1
MDB2
MDB3
MDB4
MDB5
1D 1Q
2D 2Q
3D 3Q
4D 4Q
5D 5Q
6D 6Q
CLR
U3
+5V
R2
1.0K
Q1
2N3906
SYS MUTE
CR5
RED
LEDR2
+5V
COLSEL
R4
1.0K
Q3
2N3906
LEDC3
INPUT 3
CR3
GREEN
SWC1
SWC2
LEDC4
INPUT 4
CR4
GREEN
DIGITAL BOARD
LINK
J7
MDB<0:5>
+5V
ROWSEL
COLSEL
KEYSTAT/
MDB0
MDB1
MDB2
MDB3
MDB4
MDB5
IRDATA
R8
300
LEDR1
R6
3.0K
Q5
2N3904
R12
330
LEDR2
R10
3.0K
Q7
2N3904
R9
220
LEDR3
R7
3.0K
Q6
2N3904
R16
300
LEDR4
R14
3.0K
Q9
2N3904
R17
300
LEDR5
R15
3.0K
Q10
2N3904
R13
300
LEDR6
R11
3.0K
Q8
2N3904
74HC174
U4
+5V
CR7
1N4148
R1
10K
C3
4.7/25
ROWSEL
SWC2
SWC1
INPUT 1
SW1
INPUT 3
SW3
PROG DN
SW5
BANK
SW7
VOL UP
SW9
FX MUTE
SW11
SHLD
IR BOARD
IR DETECTOR
J6
VCC
GP1U52
OUT
GND
U1
J5
J4
J1
+5V
J2
IRDATA
J3
C1
47/25
C2
.1/50
CER
C4
.1/50
CER

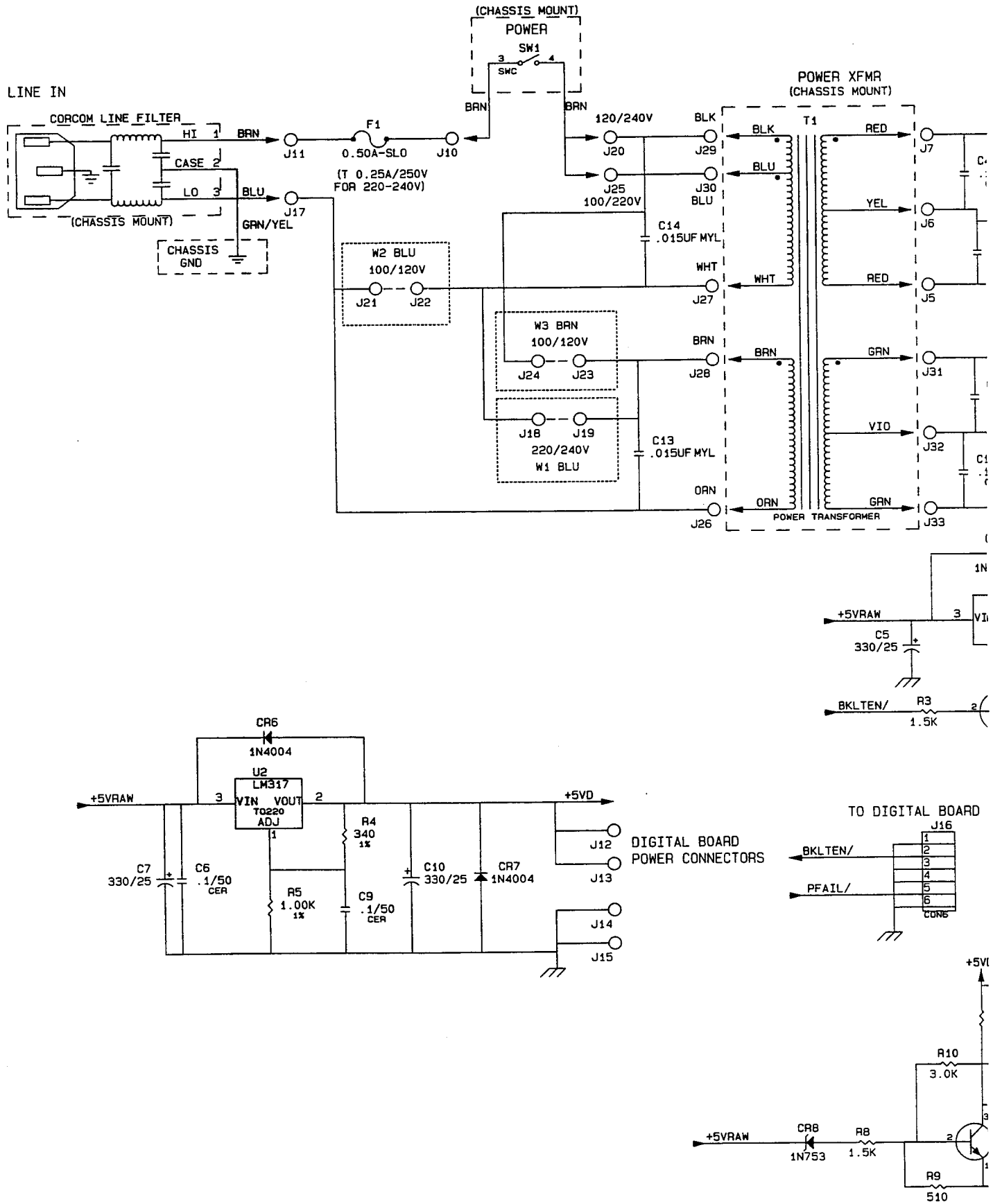


REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE		
1	REVISED	RS 6/20/90	
2	RELEASED FOR PRODUCTION	RS 10/25/90 AEJ 11/5/90	RW 10/25/90 AF 11/5/90

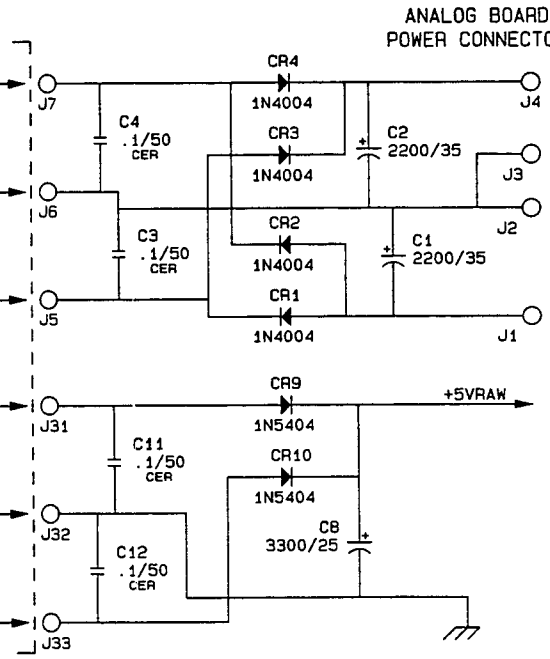
NOTES

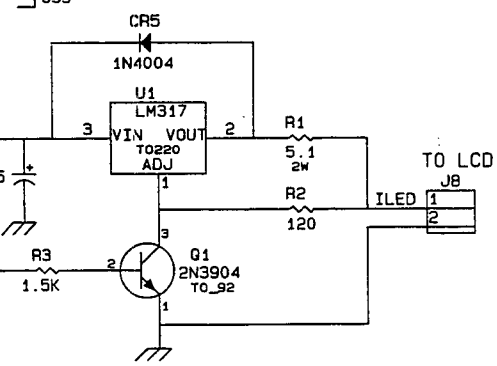
1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
5. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION
7. REFERENCE DESIGNATORS, LAST USED: C4, CR7, DS2, J7, Q10, R17, RP1, SW12, U4.

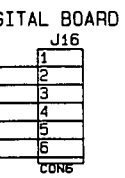
CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154				
APPROVALS	DATE	TITLE SCHEM, FRONT PANEL BD., CP-3			
DRAWN RS	02/07/90				
CHECKED AEJ	11/05/90	SIZE D	CODE	NUMBER 060-08149	REV. 2
Q.C. RW	10/25/90				
ISSUED AF	11/5/90	SHEET 1 OF 1			

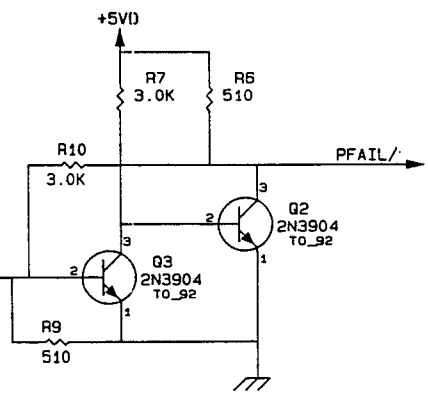

(CHASSIS MOUNT)
POWER
SW1
SWC
LINE IN
POWER XFMR
(CHASSIS MOUNT)
CORCOM LINE FILTER
HI 1
CASE 2
LO 3
(CHASSIS MOUNT)
BRN
BLU
GRN/YEL
J11
F1
0.50A-SLO
J10
(T 0.25A/250V
FOR 220-240V)
J17
CHASSIS
GND
120/240V
J20
J25
100/220V
BLK
J29
J30
BLU
T1
BLK
BLU
WHT
J27
RED
J7
YEL
J6
RED
J5
C14
.015UF MYL
W2 BLU
100/120V
J21
J22
W3 BRN
100/120V
J24
J23
BRN
J28
BRN
GRN
J31
VIO
J32
J18
J19
220/240V
W1 BLU
C13
.015UF MYL
ORN
J26
ORN
GRN
J33
POWER TRANSFORMER
+5VRAW
C5
330/25
BKLTEN/
R3
1.5K
CR6
1N4004
U2
LM317
VIN VOUT
TO220
ADJ
+5VRAW
+5VD
R4
340
1%
C7
330/25
C6
.1/50
CER
R5
1.00K
1%
C9
.1/50
CER
C10
330/25
CR7
1N4004
J12
J13
J14
J15
DIGITAL BOARD
POWER CONNECTORS
TO DIGITAL BOARD
J16
BKLTEN/
PFAIL/
CON6
R10
3.0K
+5VRAW
CR8
1N753
R8
1.5K
R9
510

REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE		
1	REVISED	RS 6/29/90 BACK-ANNO 7/16/90	
2	RELEASED FOR PRODUCTION	RS 10/11/90 AF 10/15/90	RW 10/21/90 DMB 10/24/90





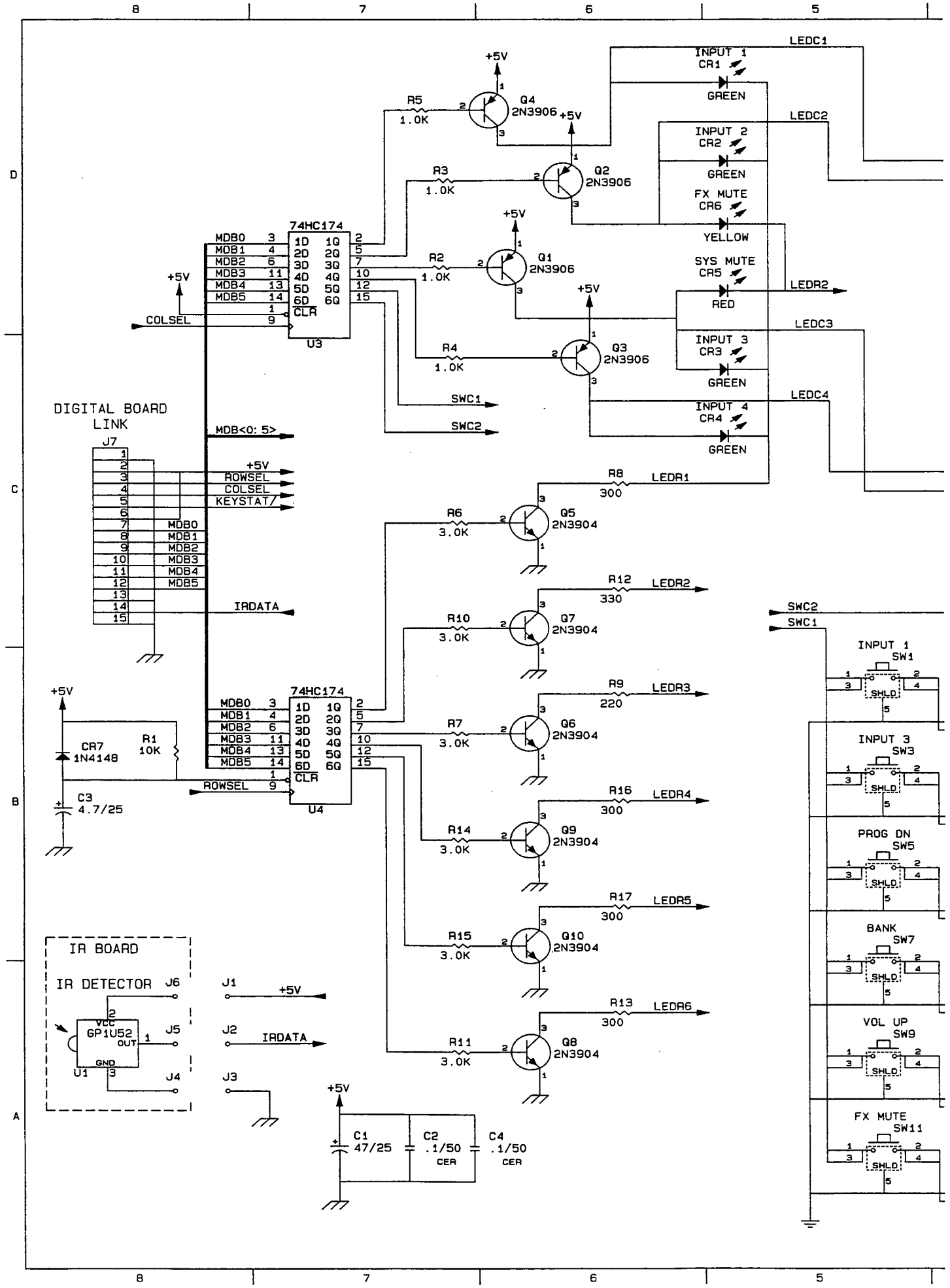


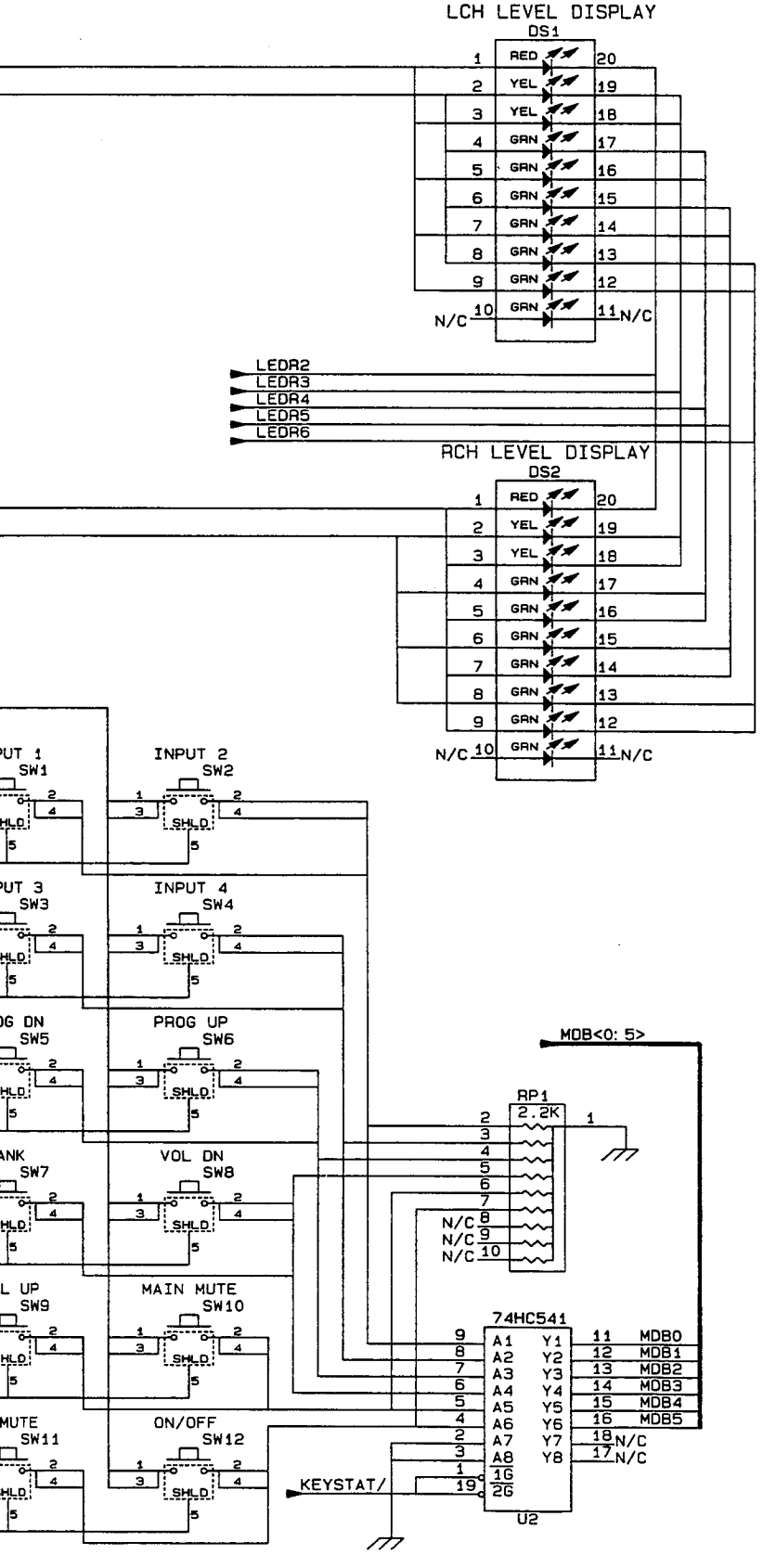


NOTES

1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
5. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION
7. REFERENCE DESIGNATORS, LAST USED: C23, CR22, J27, Q4, R14

CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA 02154				
APPROVALS	DATE	TITLE SCHEM, POWER SUPPLY BOARD, CP-3			
DRAWN RS	12/18/89				
CHECKED AF	10/15/90	SIZE D	CODE	NUMBER 060-08142	REV. 2
Q.C. RW	10/21/90				
ISSUED	DMB 10/24/90	SHEET 1 OF 1			


LEDC1
INPUT 1
CR1
GREEN
+5V
Q4
2N3906
R5
1.0K
LEDC2
INPUT 2
CR2
GREEN
+5V
Q2
2N3906
R3
1.0K
FX MUTE
CR6
YELLOW
74HC174
MDB0
MDB1
MDB2
MDB3
MDB4
MDB5
1D 1Q
2D 2Q
3D 3Q
4D 4Q
5D 5Q
6D 6Q
CLR
U3
+5V
Q1
2N3906
R2
1.0K
SYS MUTE
CR5
RED
LEDR2
COLSEL
+5V
Q3
2N3906
R4
1.0K
LEDC3
INPUT 3
CR3
GREEN
SWC1
SWC2
LEDC4
INPUT 4
CR4
GREEN
DIGITAL BOARD
LINK
J7
MDB<0:5>
+5V
ROWSEL
COLSEL
KEYSTAT/
IRDATA
R8
300
LEDR1
Q5
2N3904
R6
3.0K
R12
330
LEDR2
Q7
2N3904
R10
3.0K
SWC2
SWC1
INPUT 1
SW1
SHLD
INPUT 3
SW3
SHLD
PROG DN
SW5
SHLD
BANK
SW7
SHLD
VOL UP
SW9
SHLD
FX MUTE
SW11
SHLD
+5V
CR7
1N4148
R1
10K
C3
4.7/25
74HC174
MDB0
MDB1
MDB2
MDB3
MDB4
MDB5
1D 1Q
2D 2Q
3D 3Q
4D 4Q
5D 5Q
6D 6Q
CLR
ROWSEL
U4
R9
220
LEDR3
Q6
2N3904
R7
3.0K
R16
300
LEDR4
Q9
2N3904
R14
3.0K
R17
300
LEDR5
Q10
2N3904
R15
3.0K
R13
300
LEDR6
Q8
2N3904
R11
3.0K
IR BOARD
IR DETECTOR
J6
VCC
GP1U52
OUT
GND
U1
J5
J4
J1
+5V
J2
IRDATA
J3
+5V
C1
47/25
C2
.1/50
CER
C4
.1/50
CER

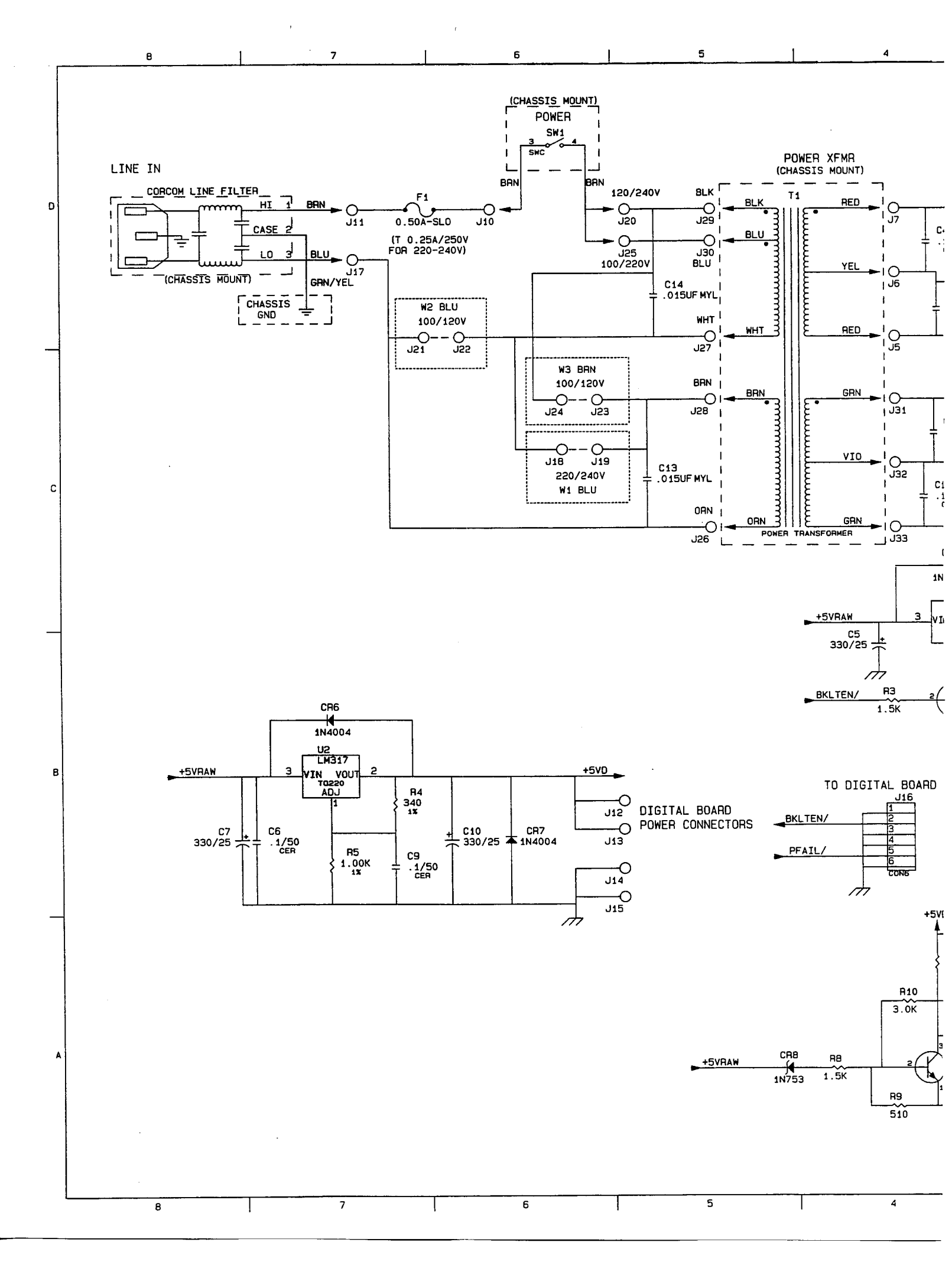


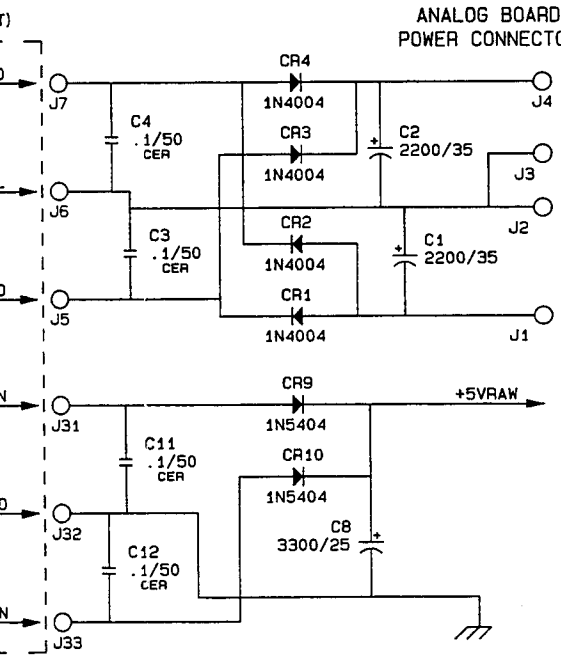
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE		
1	REVISED	RS 6/20/90	
2	RELEASED FOR PRODUCTION	10/25/90 AEJ 11/6/90	10/25/90 11/5/90

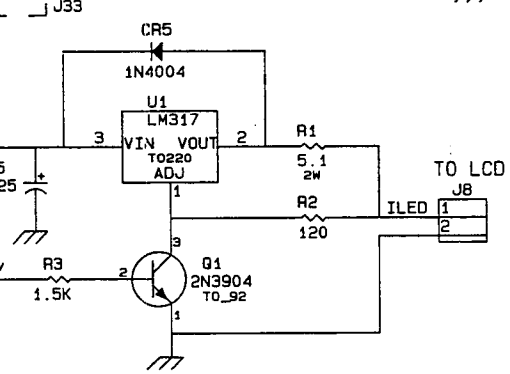
NOTES

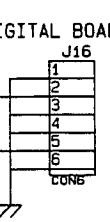
1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
5. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION
7. REFERENCE DESIGNATORS, LAST USED: C4, CR7, DS2, J7, Q10, R17, RP1, SW12, U4.

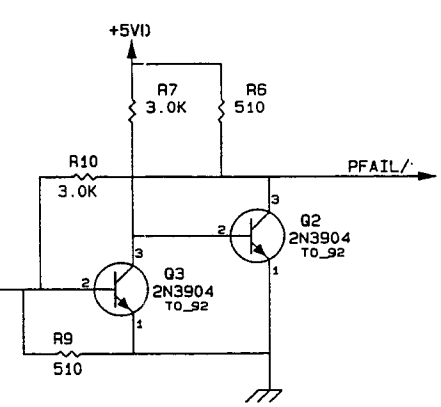
CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEM, FRONT PANEL BD., CP-3
DRAWN RS	02/07/90	
CHECKED AEJ	11/05/90	SIZE: D; CODE: ; NUMBER: 060-08149; REV.: 2
Q.C.	10/25/90	
ISSUED AF	11/5/90	SHEET 1 OF 1


LINE IN
CORCOM LINE FILTER
HI 1
CASE 2
LO 3
(CHASSIS MOUNT)
BRN
BLU
GRN/YEL
J11
J17
F1
0.50A-SLO
J10
(T 0.25A/250V
FOR 220-240V)
CHASSIS
GND
(CHASSIS MOUNT)
POWER
SW1
SWC
BRN
BRN
120/240V
J20
J25
100/220V
BLK
J29
BLU
J30
BLU
C14
.015UF MYL
WHT
J27
W2 BLU
100/120V
J21
J22
W3 BRN
100/120V
J24
J23
BRN
J28
J18
J19
220/240V
W1 BLU
C13
.015UF MYL
ORN
J26
POWER XFMR
(CHASSIS MOUNT)
T1
BLK
BLU
WHT
BRN
ORN
RED
YEL
RED
GRN
VIO
GRN
J7
J6
J5
J31
J32
J33
POWER TRANSFORMER
+5VRAW
C5
330/25
BKLTEN/
R3
1.5K
CR6
1N4004
U2
LM317
VIN VOUT
TO220
ADJ
+5VRAW
+5VD
R4
340
1%
R5
1.00K
1%
C7
330/25
C6
.1/50
CER
C9
.1/50
CER
C10
330/25
CR7
1N4004
J12
J13
J14
J15
DIGITAL BOARD
POWER CONNECTORS
TO DIGITAL BOARD
J16
BKLTEN/
PFAIL/
CON6
R10
3.0K
+5VRAW
CR8
1N753
R8
1.5K
R9
510









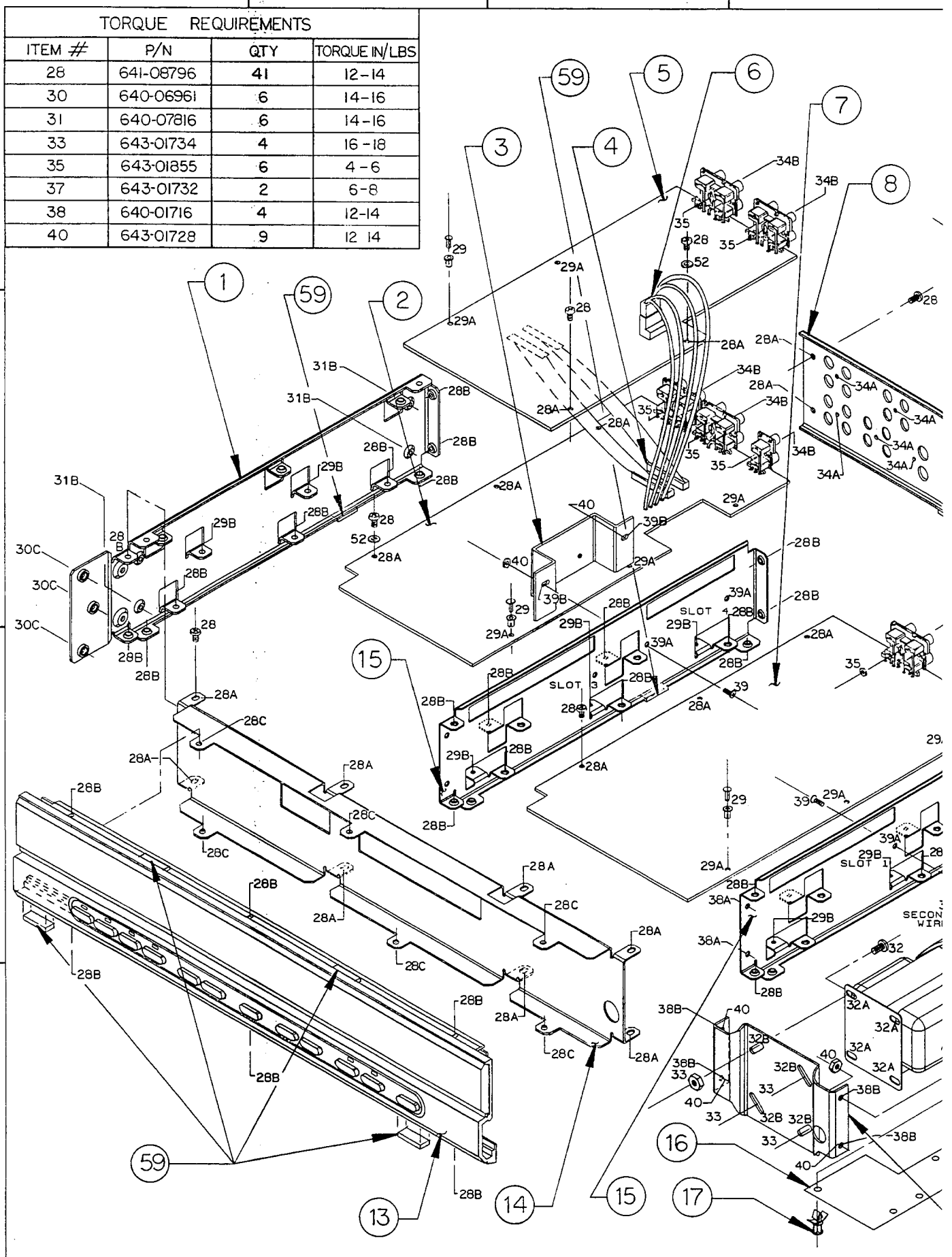
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE		
1	REVISED	RS 6/29/90 BACK-ANNO 7/16/90	
2	RELEASED FOR PRODUCTION	10/11/90 10/15/90	10/15/90 10/16/90

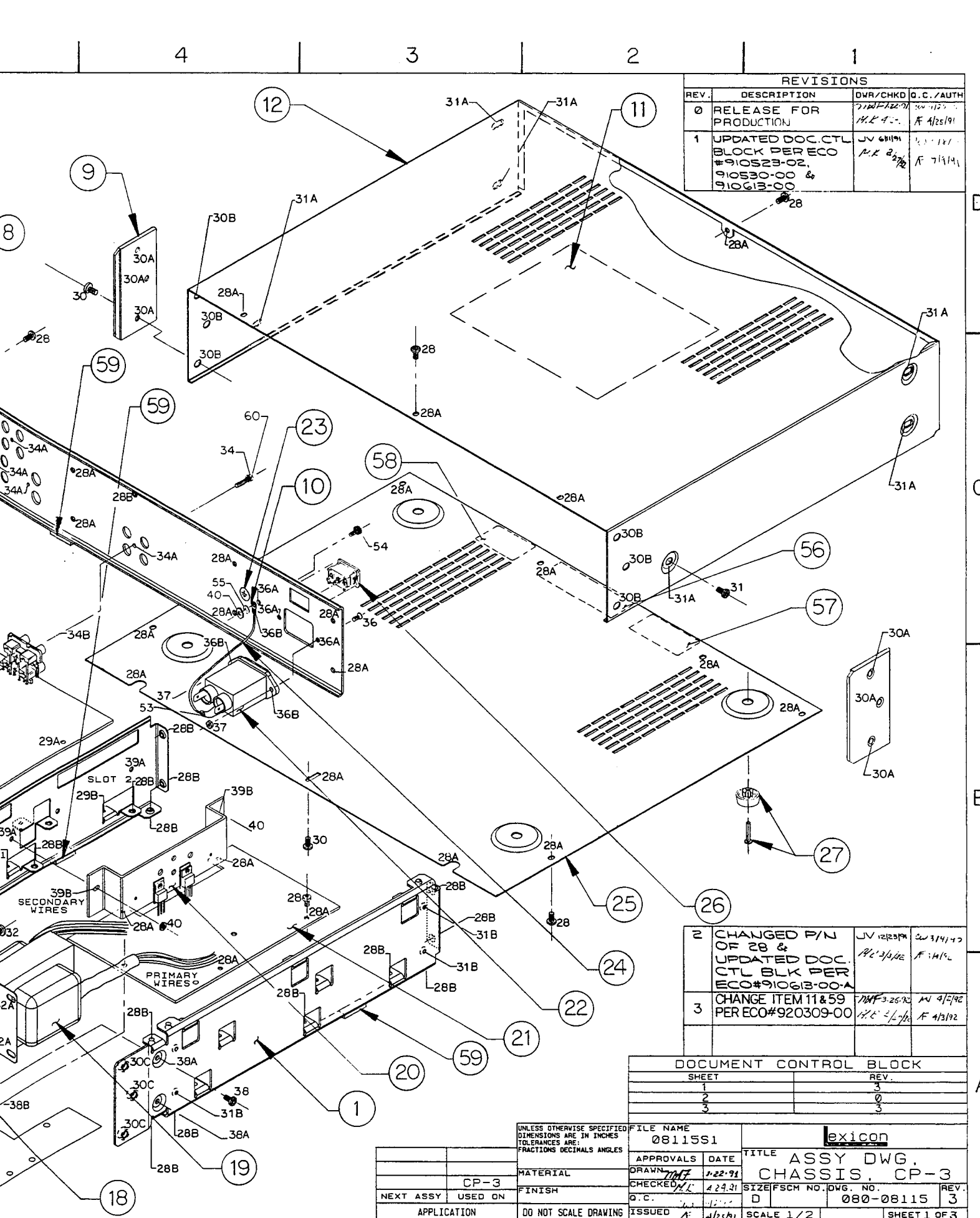
NOTES

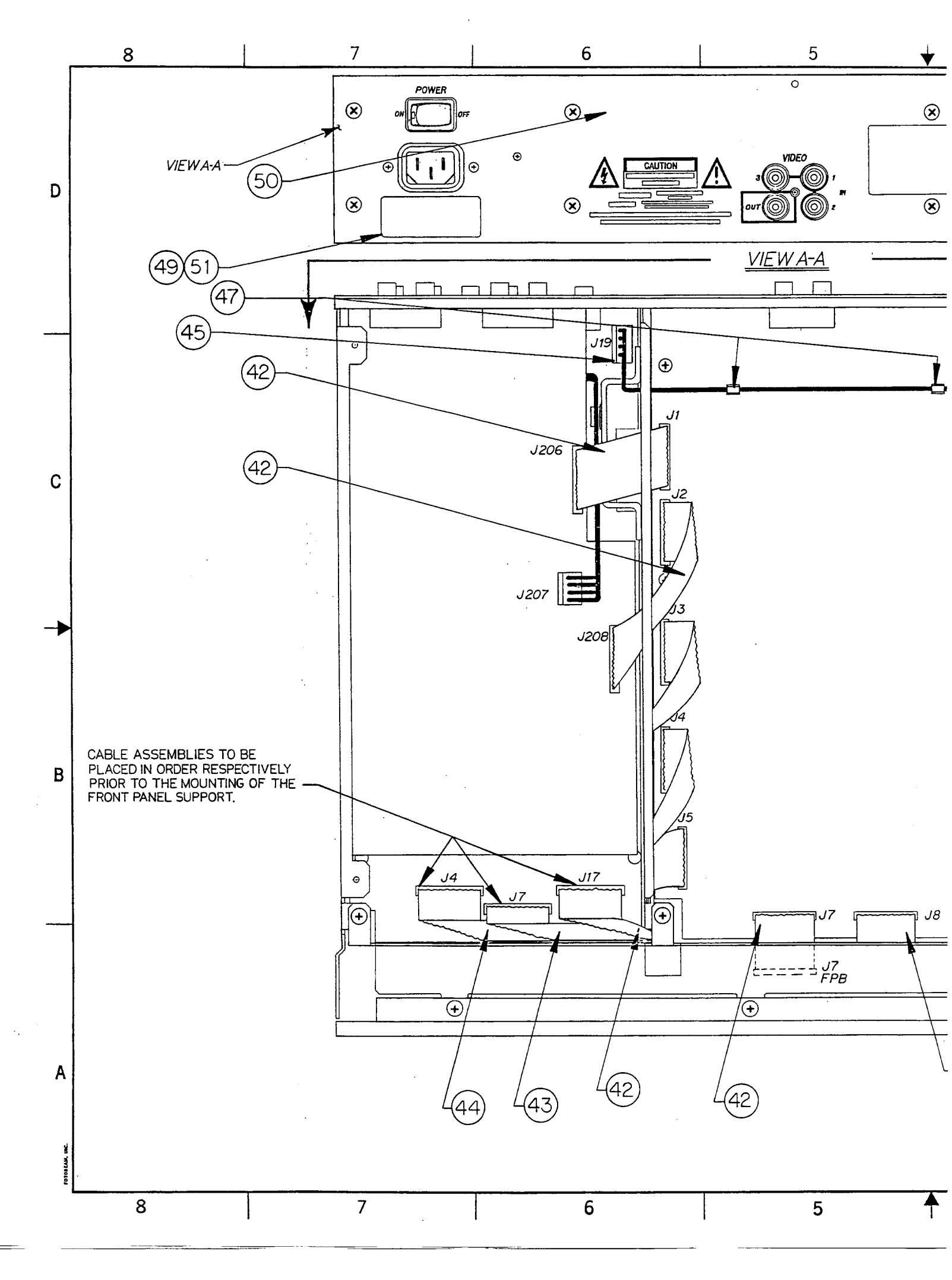
1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
5. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION
7. REFERENCE DESIGNATORS, LAST USED: C23, CR22, J27, Q4, R14

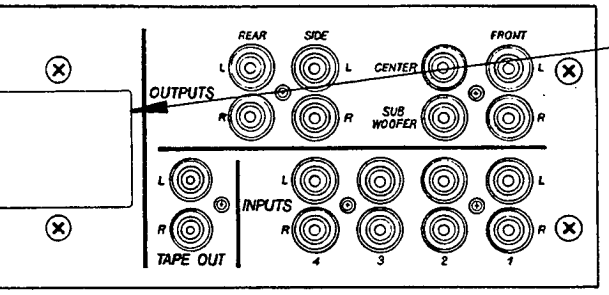
CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA 02154				
APPROVALS	DATE	TITLE SCHEM, POWER SUPPLY BOARD, CP-3			
DRAWN RS	12/18/89				
CHECKED AF	10/15/90	SIZE D	CODE	NUMBER 060-08142	REV. 2
Q.C. RW	10/21/90				
ISSUED	10/24/90	SHEET 1 OF 1			

TORQUE REQUIREMENTS			
ITEM #	P/N	QTY	TORQUE IN/LBS
28	641-08796	41	12-14
30	640-06961	6	14-16
31	640-07816	6	14-16
33	643-01734	4	16-18
35	643-01855	6	4-6
37	643-01732	2	6-8
38	640-01716	4	12-14
40	643-01728	9	12 14

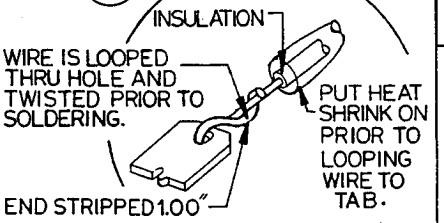



REVISIONS
REV. | DESCRIPTION | DWR/CHKD | Q.C./AUTH
0 | RELEASE FOR PRODUCTION | | AF 4/25/91
1 | UPDATED DOC.CTL BLOCK PER ECO #910523-02, 910530-00 & 910613-00 | JV 6/11/91 | AF 7/9/91
2 | CHANGED P/N OF 28 & UPDATED DOC. CTL BLK PER ECO#910613-00-A | JV 12/23/91 | AF 1/4/92
3 | CHANGE ITEM 11&59 PER ECO#920309-00 | 3.25.92 | AF 4/3/92
DOCUMENT CONTROL BLOCK
SHEET | REV.
1 | 3
2 | 0
3 | 3
SLOT 2
SECONDARY WIRES
PRIMARY WIRES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
DO NOT SCALE DRAWING
CP-3
NEXT ASSY | USED ON
APPLICATION
FILE NAME 08115S1
APPROVALS | DATE
DRAWN 1.22.91
CHECKED 4.29.91
Q.C.
ISSUED 4/25/91
Lexicon
TITLE ASSY DWG, CHASSIS, CP-3
SIZE D | FSCM NO. | DWG. NO. 080-08115 | REV. 3
SCALE 1/2
SHEET 1 OF 3


8
7
6
5
D
C
B
A
POWER
ON
OFF
VIEW A-A
50
CAUTION
VIDEO
3
1
OUT
IN
2
49
51
VIEW A-A
47
45
42
42
J19
J1
J206
J2
J207
J3
J208
J4
J5
J4
J17
J7
J7
J8
J7
FPB
CABLE ASSEMBLIES TO BE PLACED IN ORDER RESPECTIVELY PRIOR TO THE MOUNTING OF THE FRONT PANEL SUPPORT.
44
43
42
42
FOTOBEAM, INC.

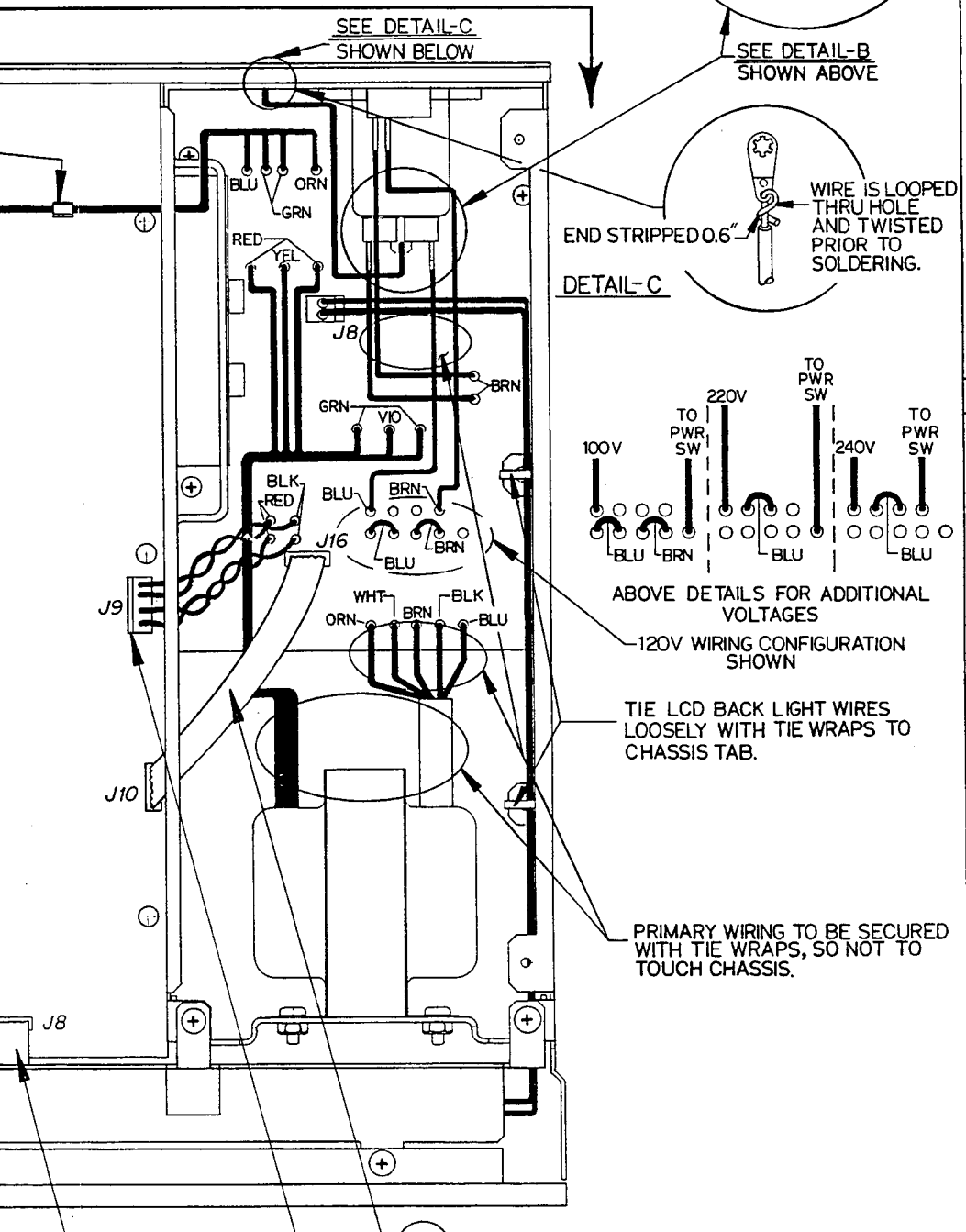


DETAIL-B



SEE DETAIL-C SHOWN BELOW

SEE DETAIL-B SHOWN ABOVE



DETAIL-C

ABOVE DETAILS FOR ADDITIONAL VOLTAGES

120V WIRING CONFIGURATION SHOWN

TIE LCD BACK LIGHT WIRES LOOSELY WITH TIE WRAPS TO CHASSIS TAB.

PRIMARY WIRING TO BE SECURED WITH TIE WRAPS, SO NOT TO TOUCH CHASSIS.

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	TMA 4-22-91 / M.C. 4/24/91	ccw 4/25/91 / AF 4/26/91

NOTES

1. PART NUMBER LISTING IS REFERENCE ONLY AND DOES NOT SUPERSEDE THE BILL OF MATERIALS 023-08331, 024-08325.
2. REFER TO DOCUMENT #080-08848 FOR ASSEMBLY NOTES.

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX	CONTRACT NO.
		MATERIAL	APPROVALS / DATE
	CP-3	FINISH	DRAWN TMA 4-22-91
NEXT ASSY	USED ON		CHECKED M.C. 4/24/91
APPLICATION		DO NOT SCALE DRAWING	Q.C. ccw 4/25/91
			ISSUED AF 4/26/91

lexicon

ASSY DWG, CHASSIS, CP-3

SIZE D | FSCM NO. | DWG. NO. 080-08115 | REV. 0

SCALE 1 : 1 | SHEET 2 OF 3

PARTS LIST
(SEE NOTE #1)

ITEM #	COMPONENT PART NUMBER	DESCRIPTION	QUANTITY PER ASSY	UNI
1.	701-08112	SUPPORT,SIDE,2UX13.43	2.00	EA
2.	024-08320	PL,ANLG BD ASSY,LOWER,CP-3	1.00	EA
3.	024-08323	PL,HS ASSY,ANLG,CP-3	1.00	EA
4.	680-06163	CABLE,079,SCKT/SCKT,15C,6.5"	2.00	EA
5.	024-08317	PL,ANLG BD ASSY,UPPER,CP-3	1.00	EA
6.	680-08176	CABLE/ASSY,4C,18G,6",SS/HSG	1.00	EA
7.	023-08327	PL,DIGITAL BD ASSY,CP-3	1.00	EA
8.	702-08105	PANEL,REAR,CP-3	1.00	EA
9.	700-08155	ENDCAP,CP-3	2.00	EA
10.	620-01999	LUG,SOLDER,LCKNG,#6,.020THK	1.00	EA
11.	702-09409	PANEL,DAMPING,5.0"X6.0"	1.00	EA
12.	700-08162	COVER,TOP,2UX13.51,CP-3	1.00	EA
13.	023-08306	PL,FP ASSY,CP-3	1.00	EA
14.	702-08104	PANEL,SUB,FRONT,CP-3	1.00	EA
15.	701-07482	SUPPORT,CENTER,M300	2.00	EA
16.	702-08341	COVER,PROTECTIVE,AC,CP-3	1.00	EA
17.	630-07846	SPCR,PCB/FOOT,.250,NYL	3.00	EA
18.	700-07563	BRACKET,MTG,XFORMER,M300	1.00	EA
19.	470-07508	TRANSFORMER,POWER,50VA	1.00	EA
20.	023-08332	PL,HS ASSY,PS,CP-3	1.00	EA
21.	023-08324	PL,PS BD ASSY,CP-3,120V	1.00	EA
	023-08693	PL,PS BD ASSY,CP-3,100V	1.00	EA
	023-08694	PL,PS BD ASSY,CP-3,220V	1.00	EA
	023-08695	PL,PS BD ASSY,CP-3,240V	1.00	EA
22.	490-00396	CONN,AC AND RFI FILTER	1.00	EA
23.	740-08556	LABEL,GROUND SYMBOL,0.5"DIA	1.00	EA
24.	675-08800	WIRE,18G,GRN/YEL,4.5",SSX2	1.00	EA
25.	702-08111	PLATE,BOTTOM,16.88X13.37	1.00	EA
26.	454-03900	SW,ROCKER,1P1T,QDC,INTL LINE	1.00	EA
27.	541-08184	BUMPER,FEET,.79DIAX.39,RVT MTG	4.00	EA
28.	641-08796	SCRW,TAP,6-32X5/16,THG,PD,BZ	41.0	EA
29.	650-07551	RVT,SNAP-IN,.16DIA,NYL	8.00	EA
30.	640-08874	SCRW,10-32X3/8,FH,PH,BLK	6.00	EA
31.	640-07816	SCRW,10-32X5/16,PNH,PH,SEMS,BK	6.00	EA
32.	640-01721	SCRW,8-32X3/8,PNH,PH,ZN	4.00	EA
33.	643-01734	NUT,8-32,KEP,ZN	4.00	EA
34.	640-08061	SCRW,2-56X3/4,PNH,PH,BLK	6.00	EA
35.	643-01855	NUT,2-56,HEX,ZN	6.00	EA
36.	640-02812	SCRW,4-40X3/8,PNH,PH,BLK	2.00	EA
37.	643-01732	NUT,4-40,KEP,ZN	2.00	EA
38.	640-01716	SCRW,6-32X3/8,PNH,PH,ZN	4.00	EA
39.	640-07774	SCRW,6-32X3/8,HWH,SL,ZN	4.00	EA
40.	643-01728	NUT,6-32,KEP,ZN	9.00	EA
41.	680-07764	CABLE,079,SCKT/SCKT,6C,8.5"	1.00	EA
42.	680-07767	CABLE,079,SCKT/SCKT,15C,5.5"	4.00	EA
43.	680-07768	CABLE,079,SCKT/SCKT,15C,8.0"	1.00	EA
44.	680-08542	CABLE,079,SCKT/SCKT,15C,12"	1.00	EA
45.	680-07759	CABLE ASSY,4C,18G,13",ST&T/HSG	1.00	EA
46.	680-08195	CABLE ASSY,4C,18G,7",TW/HSG	1.00	EA
47.	530-02486	TIE,CABLE,NYL,.1"X4"	7.00	EA
48.	740-08782	LABEL,PRODUCT ID,CP-3	1.00	EA
49.	740-06678	LABEL,CSA CERTIFIED,CONSUMER	1.00	EA
50.	740-08855	LABEL,UL CERTIFIED,CONSUMER	1.00	EA
51.	740-08558	LABEL,TUV CERTIFIED,BAYERN	1.00	EA
52.	630-00953	WSHR,FL,#6CLX3/80DX1/16,FBR	2.00	EA
53.	690-02060	SLEEVING,SHRINK,3/16X1/2LG,BLK	1.00	EA
54.	640-03087	SCRW,6-32X3/8,PNH,PH,SEMS,BLK	1.00	EA
55.	644-01735	WSHR,FL,#6CLX3/80DX1/32THK	1.00	EA
56.	740-08817	LABEL,DOLBY & THX LICENSE	1.00	EA
57.	740-08820	LABEL,WARNING,PERFORMANCE,GND	1.00	EA
58.	740-07166	LABEL,"RISK OF SHOCK"	1.00	EA
59.	720-08910	TAPE,FOAM,.062X.20X.84	9.00	EA
60.	644-06635	WSHR,INT STAR #2,ZN	6.00	EA

UNITS	REFERENCE INFORMATION
EA	–
EA	–
EA	–
EA	LO ANLG–J8 TO UP ANLG–J203;LO ANLG–J9 TO UP ANLG–J204
EA	–
EA	LO ANLG–J11–14 TO UP ANLG J207
EA	–
EA	–
EA	–
EA	REAR PANEL CHASSIS GND
EA	TOP COVER
EA	–
EA	–
EA	–
EA	–
EA	–
EA	PROT COV MTG
EA	–
EA	–
EA	–
EA	–
EA	–
EA	–
EA	–
EA	L1 (PS BD)
EA	REAR PANEL (INSIDE)
EA	AC CONN TO REAR PANEL CHASSIS GND
EA	–
EA	REAR PANEL
EA	–
EA	TOP COVER (4),BOTTOM PLATE (9) FRONT & REAR PANELS (8 EA);PCBS (12)
EA	DIG BD (3);ANLG UPPER (2);ANLG LOWER (3)
EA	END CAP MTG
EA	TOP COVER
EA	XFORMER
EA	XFORMER
EA	RCA JACKS
EA	RCA JACKS
EA	PWR
EA	PWR
EA	XFORMER BRACKET
EA	HEATSINK
EA	XFRMR BRKT (4);HEATSINK (4);REAR PAN CHAS GND (1)
EA	PS–J16 TO DIG–J10
EA	DIG–J1 TO UP ANLG–J206;DIG–J2 TO UP ANLG–J208; DIG–J5 TO LO ANLG–J17;DIG–J7 TO FP–J7
EA	DIG–J4 TO LO ANLG–J7
EA	DIG–J3 TO LO ANLG–J4
EA	PS TO ANALOG BD
EA	DIG–J9 TO PS (HARD WIRED)
EA	–
EA	REAR PANEL
EA	120V ONLY/REAR PANEL
EA	120V ONLY/REAR PANEL
EA	220V ONLY/REAR PANEL
EA	LOWER ANALOG (1);UPPER ANALOG (1)
EA	REAR PAN CHAS GND (1)
EA	REAR PAN CHAS GND (1)
EA	REAR PAN CHAS GND (1)
EA	BOTTOM PLATE
EA	BOTTOM PLATE (120V ONLY)
EA	BOTTOM PLATE (120V ONLY)
EA	SIDE SUPPORTS(2);CENTER SUPPORTS(2); FRONT PANEL(4);REAR PANEL(1)
EA	RCA JACKS

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	JV 4/19/91 MK 4/23/91	CW 4/25/91 AF 4/25/91
1	REVISED 49–51, PER ECO#910523–02. REVISED 30 PER ECO #910530–00. REVISED 28 PER ECO#910613–00	JV 6/11/91 AEJ 6/12/91 MK 7/3/91	CW 7/8/91 AF 7/9/91
2	CHANGED 28 PER ECO #910613–00–A	JV 12\23\91 MK 2\27\92	CW 3\4\92 AF 3\4\92
3	CHANGED 11 & 59 PER ECO#920309–00	MF 3\24\92 A.L. 3/30/92	MW 4/2/92 AF 4/3/92

NOTES

1. PART NUMBER LISTING IS REFERENCE ONLY AND DOES NOT SUPERSEDE THE BILL OF MATERIAL.
2. LETTERS DESIGNATE SCREW PATHS.
3. ALL SCREWS, NUTS, FASTENERS ETC., ARE LISTED AND SHOWN USING LONE NUMBERS. THE FASTENERS ASSEMBLY PATH THROUGH ADJOINING PIECES IS ILLUSTRATED BY MEANS OF NUMBERS USING CONSECUTIVE LETTER SUFFIXES, (I.E. 28A, 28B, 28C ETC).
4. DURING FINAL ASSEMBLY INSURE FRONT PANEL AND TOP COVER ARE MOUNTED FLUSH TO EACH OTHER.
5. USE FIXTURE TO INSURE DAMPING MATERIAL ITEM 11 IS INSTALLED IN BETWEEN CENTER RAILS.

	CP–3
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/–.010
.XXX +/–.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 10 FILE NAME 08115S3

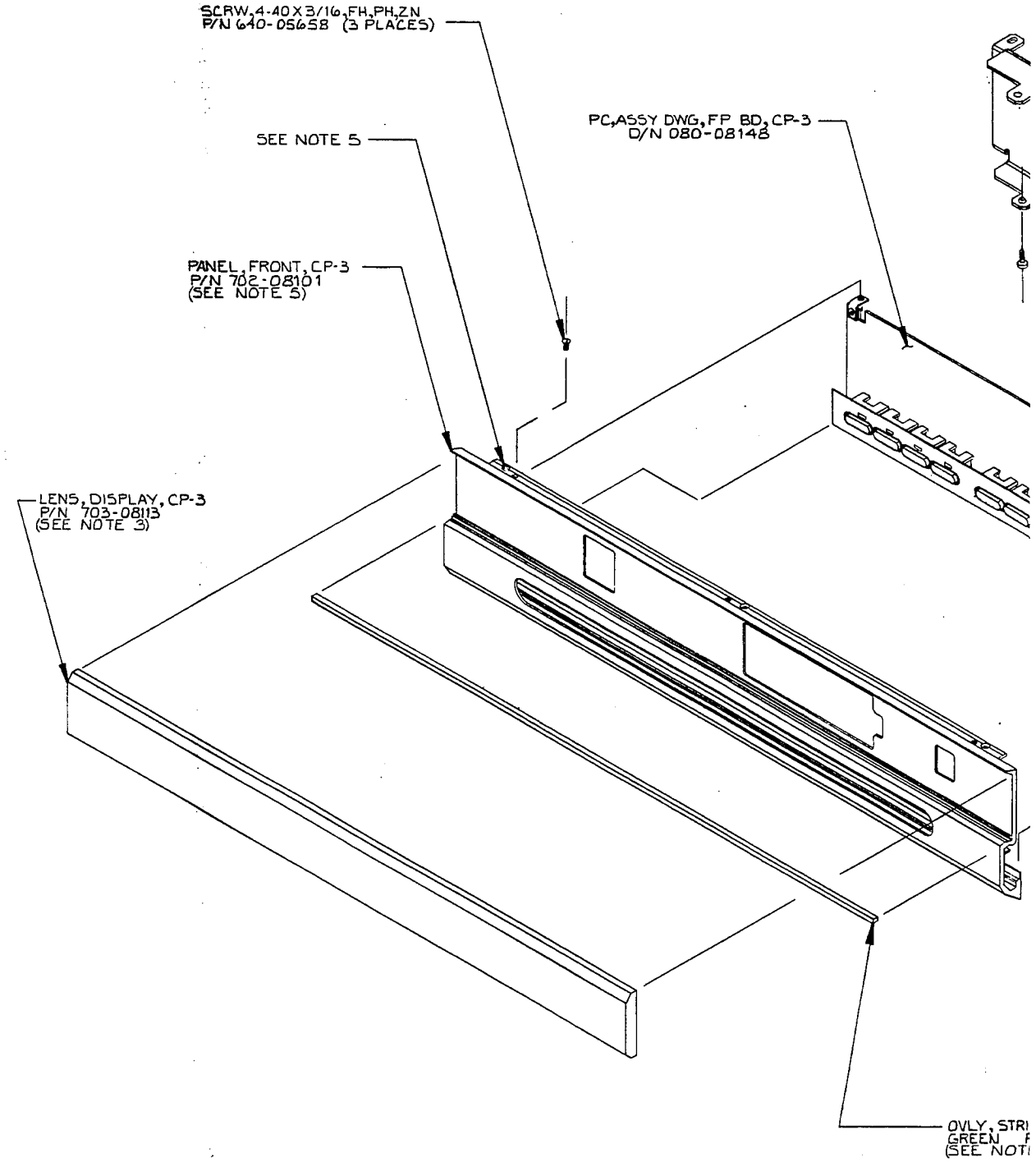
APPROVALS		DATE
DRAWN	JV	4/19/91
CHECKED	MK	4/24/91
Q.C.	CW	4/25/91
ISSUED	AF	4/25/91

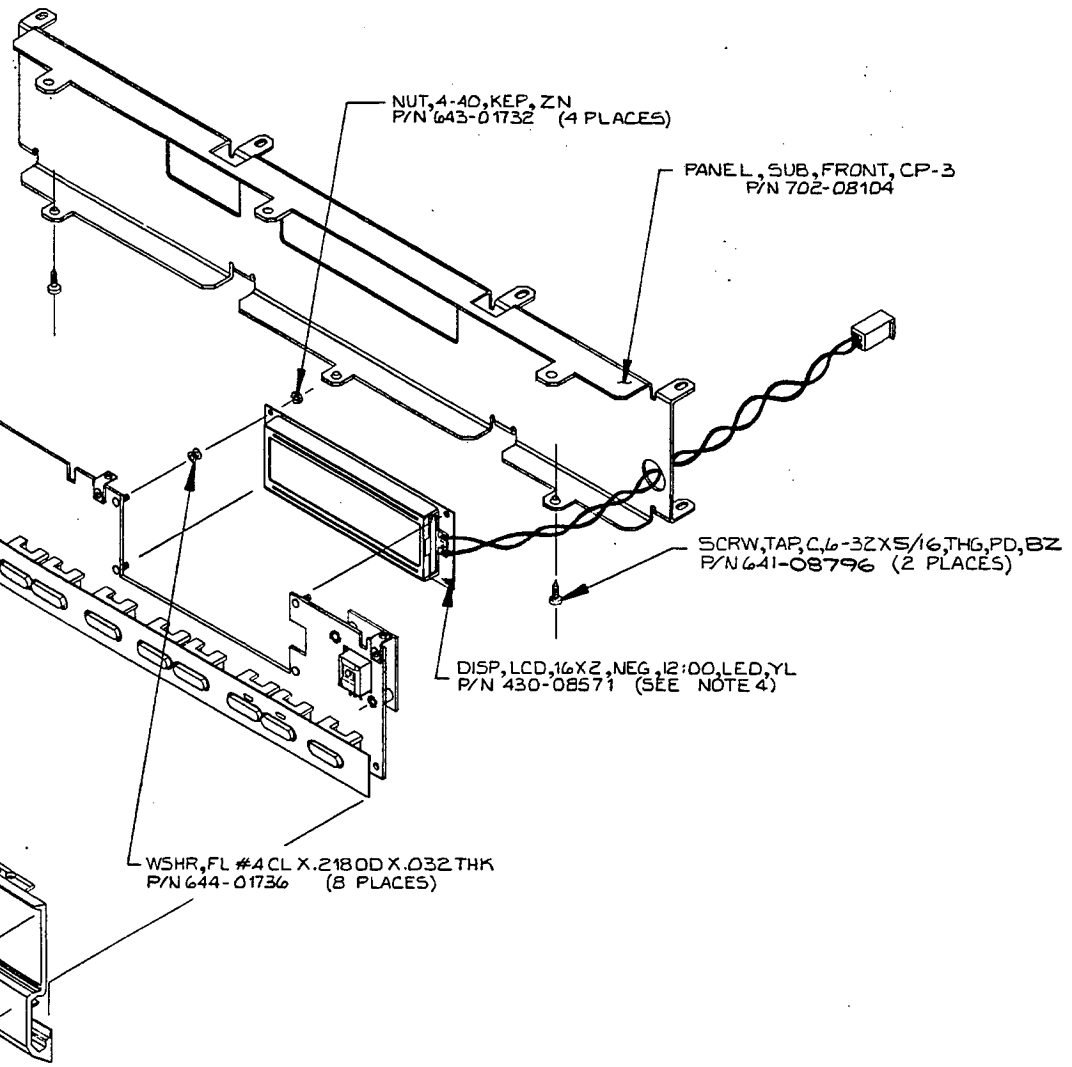
lexicon

TITLE ASSY DWG, CHASSIS,CP–3

SIZE	FSCM NO.	DWG. NO.	REV.
D		080–08115	3

SCALE 1/1 SHEET 3OF 3


SCRW,4-40X3/16,FH,PH,ZN
P/N 640-056S8 (3 PLACES)
SEE NOTE 5
PC,ASSY DWG,FP BD,CP-3
D/N 080-08148
PANEL,FRONT,CP-3
P/N 702-08101
(SEE NOTE 5)
LENS,DISPLAY,CP-3
P/N 703-08113
(SEE NOTE 3)



Y, STRIPE .125 X .062 X 17.26,
EN P/N 703-08114
NOTE 2)

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	TMA 11-28-90	CW 2/3/91 AF 2/20/91
1	DELETE (4) SUB PANEL SCREWS PER ECO # 910604-00. REVISE PER ECO # 910613-00	TMA 6-12-91 MK 7.03.91	CW 7/8/91 AF 7/9/91
2	CHANGED 641-09004 TO 641-08796 PER ECO#910613-00-A	JV 12/23/91 MK 2/27/92	CW 1/7/92 AF 3/4/92

NOTES

1. PART NUMBER LISTING IS REFERENCE ONLY AND DOES NOT SUPERSEDE THE BILL OF MATERIAL # 023-08306
2. USE PNEUMATIC SYRINGE WITH FINE NEEDLE TO FILL THE GROOVE IN THE FRONT PANEL WITH A SMOOTH EVEN HEAD OF BLACK SUPER WEATHER STRIP 3M#08008. INSERT GREEN STRIPE INTO GROOVE AND SLIDE FROM SIDE TO SIDE TO INSURE EVEN SPACING FROM ENDS. PRESS GREEN STRIPE INTO GROOVE TO INSURE GOOD CONTACT WITH ADHESIVE, WHILE EVENLY POSITIONING STRIPE TOP TO BOTTOM IN GROOVE. ALLOW 4 HOURS DRYING TIME BEFORE FURTHER ASSEMBLY.
3. REMOVE PAPER BACKING FROM REAR OF LENS, HOLD LENS AT EACH END AND PLACE ITS BOTTOM EDGE INTO GROOVE SLIDE LENS IN GROOVE TO INSURE EVEN SPACING WITH ENDS OF FRONT PANEL. PRESS LENS INTO PLACE AND WIPE OFF ANY DIRT OR FINGERPRINTS WITH SOFT CLOTH.
4. REMOVE PAPER BACKING AND USING SOFT CLOTH, WIPE OFF ANY DIRT OR FINGER-PRINTS FROM LCD PRIOR TO INSTALLATION
5. REMOVE PAINT FROM THREE COUNTERSINK HOLES FOR GROUND PURPOSES.

	CP-3
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/-.010
.XXX +/-.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

FILE NAME 08116S1

APPROVALS	DATE
DRAWN TMA	11-28-90
CHECKED	
D.C.	
ISSUED AF	2/20/91

lexicon

TITLE ASSY DWG, FP MECH, CP-3

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-08116	2

SCALE 1/2 SHEET 1 OF 1