

Power Supply Considerations for AV Receivers

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ABSTRACT

Requirements for a power supply for a Class D amplifier without feedback is different from a power supply for a conventional Class AB amplifier. Parameters like power supply output impedance and peak current limitation level becomes important for this application.

This document describes power supply and system considerations, which needs to be taken into account when designing a Class D BD-mode amplifier without feedback for high performance AV receivers. TDAA audio amplifier technology that gives high-end amplifiers consists of devices like the modulator TAS5036 or TAS5076 and the TAS5182 for output stage. Both modulators use BD mode modulation.

Topics covered are:

- Calculating required power supply voltage
- Calculating peak versus average power requirements
- Optimizing power supply for low THD+N

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1 Introduction

TDAA audio amplifier technology is a direct PCM-to-PWM converter without feedback; this requires good decoupling and a good power supply. The power supply voltage needs to be regulated because the H-bridge is switching the supply level directly to the outputs via the output reconstruction filter. The power supply in a non-feedback audio amplifier can be regarded as a voltage reference for a DAC.

Modulators like the TAS5036 and TAS5076, together with output stages like the TAS5182, can give high-end audio performance. In order to get the highest achievable performance, all corners of the system must be optimized. Both the TAS5036 and the TAS5076 use BD mode modulation. BD mode modulation is sensitive to power supply output impedance. However, the BD mode can give a good audio performance with respect to dynamic range and harmonic distortion.

For a 1-2% THD+N design, no special attention to system optimization is required. Power supply output impedance can be 0.14 Ω to 0.28 Ω . Also, PWM timing errors such as dead time and timing between channels doesn't need to be optimized to get this performance.

For a design where THD+N less than 0.15% is wanted, every parameter needs to be optimized to get low THD+N. Configuration of IC's, PCB layout, and system architecture needs to be correct before good measured audio performance is reachable.

2 Supply Voltage

The voltage required for the H-bridge can be calculated using following equation:

$$V_{PVDD} = \frac{(Z_{LOAD} + 2R_{DMOS,ON} + 2R_{INDUCTOR}) \cdot \sqrt{2P_{MAX} / Z_{LOAD}}}{M}$$

P_{MAX} is the maximum output power per channel, Z_{LOAD} is the load impedance, $R_{DMOS,ON}$ is the on-state resistance of switching transistors, $R_{INDUCTOR}$ is the resistance of the output inductor, and M is the maximum modulation. For the TAS5036B and TAS5076, the maximum modulation is 0.93.

In addition to this calculated voltage, headroom must be added to compensate for power supply tolerance and the voltage drop in the interface, e.g. connectors and wires.

For a typical system using the TAS5182 and an output requirement of 100 W at 6 Ω , a supply voltage of 40.5 V nominal and 41 V maximum is required.

3 Current Limitation Level

Peak power, P_{TM} , must be taken into consideration when current limitation level is determined. When delivering power to a load sinusoidal, the peak power is actually twice the average (RMS) power. This gives the following formula for output peak power.

$$P_{TM} = \frac{2 \cdot P_{OUT}}{\eta}$$

Where P_{OUT} is the total output power for all channels that are to be driven simultaneously at full power and η is the output stage efficiency, approx 0.93.

The current limitation level of the power supply must be set above P_{TM} . In case the limitation level is lower than the peak power, the amplifier will *clip* the output signal, resulting in high distortion. Limitation current can be calculated as:

$$I_{LIM} = \frac{P_{TM}}{V_{PVDD}}$$

If 2x 100 W at 6 Ω are to be driven following current limitation is needed:

$$P_{TM,2CH} = \frac{2 \cdot 2 \cdot 100W}{0.93} = 430W$$

$$I_{LIM,2CH} > \frac{430W}{40.5V} = 10.6A$$

If 6x 100 W at 6 Ω is to be driven, the current limitation level must be set to:

$$P_{TM,6CH} = \frac{6 \cdot 2 \cdot 100W}{0.93} = 1290W$$

$$I_{LIM,6CH} > \frac{1290W}{40.5V} = 31.9A$$

Normally, audio does not require full power in all channels, continuously. For most multi-channel applications, adequate power is derived from the two front channels driven at full scale, continuously. Hence, the maximum power to be delivered from the power supply is 430 W, giving a minimum current limitation level at 10.6 A.

4 Power Supply Output Impedance

Because TDAA is a non-feedback system, all components that affect THD+N must be considered separately to get high audio performance. For the power supply output, this means that the voltage must be as ideal as possible. In its simplest form, the output signal at a given moment can be expressed as:

$$V_{OUT} = D \cdot V_{PVDD}$$

Where D is the duty cycle and V_{PVDD} is the power supply output voltage. The duty cycle varies over time according to the audio signal. Any error in the duty cycle or V_{PVDD} results in distortion of the output signal.

Errors in the duty cycle are unwanted changes in the PWM timing. Changes in the PWM can be caused by the following factors: dead time, gate drive strength, and waveform distortion caused by the circuit. Some of the waveform distortion can be compensated for by use of ABD and TC registers in the TAS5036B and TAS5076. However, PWM timing errors mainly affects THD+N at low and midrange power levels. Errors in PWM timing will not be covered any further in this document.

Changes in supply voltage are caused by the output impedance of the power supply or by current limitation of the power supply. Errors due to output impedance can not be compensated because power supply output impedance is not constant over the audio band and no feedback is used. Therefore, it is important to optimize the power supply for low output impedance to get low THD+N.

Output impedance affects THD+N mainly at high output levels. At high output power levels, high currents are drawn from the power supply. Hence, a voltage change in V_{PVDD} becomes dominating.

4.1 Output Impedance vs THD+N

The output impedance contribution to THD+N in a BD mode true digital amplifier can be estimated to:

$$THD = \frac{R_{PSU} \cdot M^2}{4 \cdot Z_{LOAD}}$$

Where M is maximum modulation; Z_{LOAD} is total load impedance, e.g. two channels of 6- Ω loads gives a total load impedance of 3 Ω . Note that contribution due to PWM timing error must be added. See reference 3 for more details.

Also note that the supply voltage is not a part of the formula, only load impedance and power supply impedance. Therefore, the impedance requirement for a 50-W system and a 100-W system is identical with respect to output impedance.

Calculating the maximum allowable impedance for two 6- Ω loads gives 14 m Ω for 0.1% THD+N. Note that when PWM timing errors are added, THD+N at full scale can be up to 0.15%.

Power supply impedance less than 14 m Ω means that output impedance plus PCB tracks plus wires and connectors must be less than 14 m Ω to have a system with THD+N at 0.1%, excluding PWM timing error contribution. Note that PWM-timing errors also need to be optimized to get low THD+N. Section 4.2 describes ways to achieve low output impedance.

4.2 Power Supply Output Impedance Origins

Output impedance comes from various sources. All of these sources must be considered to reach the required output impedance.

- Power supply capacitors on the PSU and AMP boards
- Connectors and wire impedance
- PCB track impedance
- Power supply loop gain
- Voltage sense point

4.2.1 Power Supply Capacitors

Capacitance on the power supply output, including the capacitors placed at the amplifier board, determines the impedance at high frequencies. Above the power supply control loop bandwidth, the output capacitors take over the current supply. Therefore, it is obvious that the more capacitance present at the power supply output, the lower the impedance will be at high frequencies.

In order to get minimum disturbance in the H-bridge between A-side and B-side, it is good to split the power track after the capacitor. Figure 1 shows this split of the PVDD supply track for one channel. Note that the track splits at the positive capacitor node. Currents to each side of the H-bridge then give minimum disturbance to the other side.

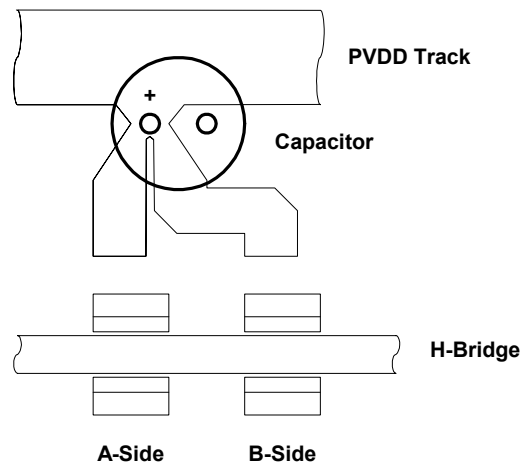


Figure 1. Capacitor Placement on the PCB

For actual PCB layout, see the layout for the device relevant EVM board.

4.2.2 Connector and Wire Impedance

Interfacing wires and connectors have high resistance. Only using 1 pin and 1 wire gives a resistance of $>20\text{ m}\Omega$, depending on the wire and connector type. This is too high for a high power system. Using remote voltage sense can compensate for the added resistance, but the added resistance reduces PSU control loop capability.

It is recommended to use two or more wires and pins in parallel between the PSU and the AMP board.

4.2.3 PCB Track Impedance

As for connector and wire impedance, impedance in the PCB track has an impact on power supply output impedance; especially on the AMP board after the voltage sense point PCB track impedance will be significant.

A track of 8 mm width x 160 mm length in 1-oz. copper has an impedance of 13 m Ω .

This leaves little room for the power supply control loop impedance. To lower the impedance, the following is recommended:

- Use a wider track
- Use a 2-oz. copper (70 μm CU)
- Place a power supply connector on the middle of the AMP board. This reduces the distance from the connector to all channels, hence lowering the impedance from the connector to all channels.

However, this only lowers the impedance from the AMP board connectors to the different output channels. The optimization is needed regardless of the power supply configuration.

Figure 2 shows a good placement of the power connector. The connector is placed so the track will only carry the current for three channels. This gives low cross coupling between channels. Furthermore, impedance in the track is kept at a minimum for all channels. It is important to have an unbroken GND plane on the solder side. This ensures that the current has a good return path. Sense is also placed at the middle of all channels which gives the best cross coupling between channels.

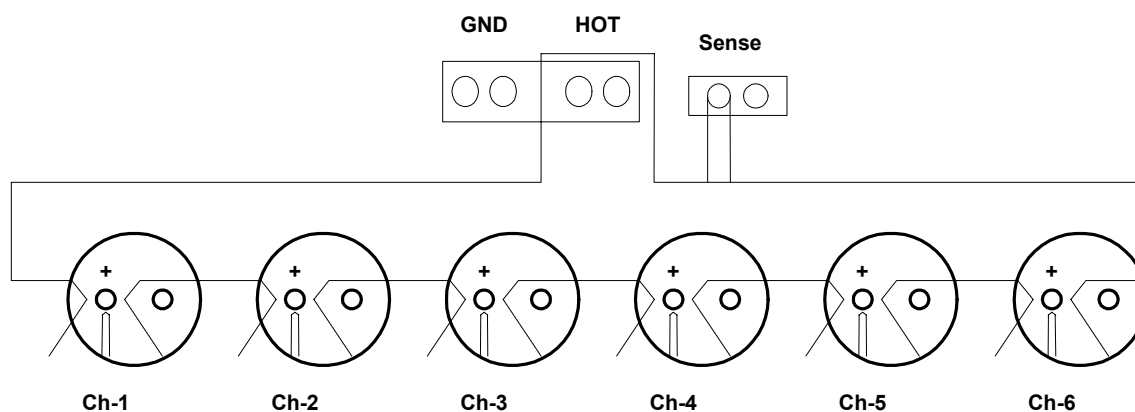


Figure 2. Example of Good PSU Connector Placement

4.2.4 Power Supply Loop Gain

A voltage control loop using integrating feedback will have an output impedance at dc of $0\ \Omega$, measured at the voltage sense point. However, at a few Hz the impedance increases until it reaches the maximum impedance at 0-dB crossover frequency. This frequency is also known as the control loop bandwidth.

When designing the control loop, care must be taken to get adequate impedance at 400 Hz – 1500 Hz, where capacitor impedance takes over.

4.2.5 Voltage Sense Point

The control loop can compensate for voltage drops up to the sense point, but from the sense point and beyond the control loop will not correct anything. Impedances in wires, connectors, and PCB tracks after sense point will be added linearly to the impedance.

Figure 3 shows how a power supply is sensing the output voltage in a typical application. The error amplifier compensates for all errors inside the power supply. The voltage on the output nodes of the power supply is then precise and the output impedance is low. But because of the wires and connectors used to interface the two PCB's, the impedance to the H-bridge increases.

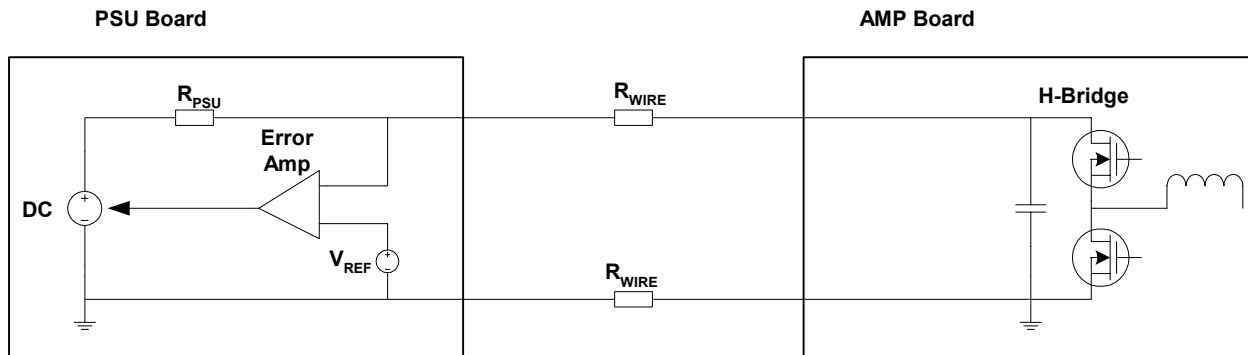


Figure 3. Standard Voltage Sense for a PSU

Based on that, the best sense point will be as close to the amplifier H-bridge as possible. This means that use of remote sense on the AMP board compensates for impedances in wires and connectors. For a multi-channel system, the optimum sense point is in the middle of the channels.

If the PSU and amplifier are two different boards using wires and connectors to interface, both HOT and GND sense must be considered. Using only HOT sense only compensates for impedance in HOT wire; leaving the entire GND wire resistance uncompensated.

HOT and GND sense can be implemented by either having a differential voltage sense amplifier on the PSU board or placing the voltage error amplifier on the AMP board only transferring the control signal to the PSU.

Using a differential input to the error amplifier compensates for impedance in both HOT and GND wire. Figure 4 shows a PSU using a differential error amplifier. The voltage is sensed as close to H-bridge as possible. The power supply impedance is then compensated for both internal resistance, R_{PSU} , and resistances in connectors and wires, R_{WIRE} .

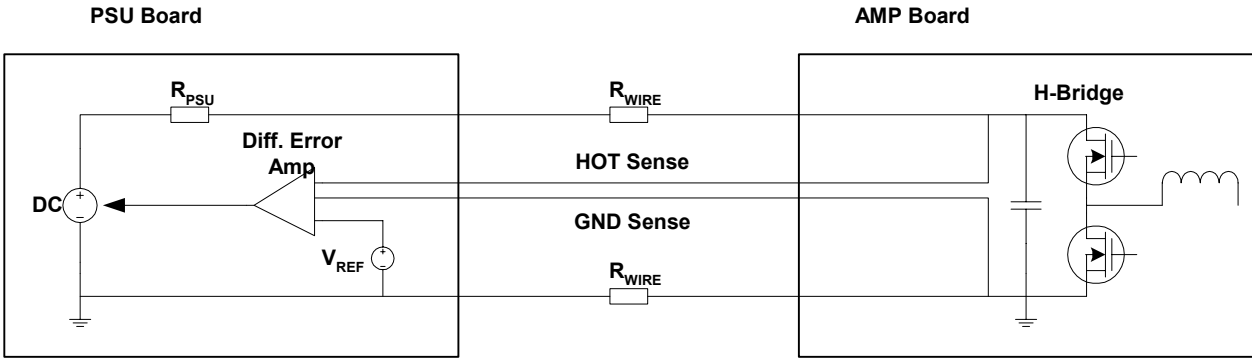


Figure 4. Remote Sensing Using Differential Voltage Sense

Implementing differential voltage sensing can be difficult. The differential error amplifier needs to be perfectly balanced in order to get good performance. An easier solution is shown in Figure 5. In this configuration, a standard error amplifier is placed on the AMP board instead of the PSU board. The control signal from the error amplifier is then sent back to the PSU board to control the power supply.

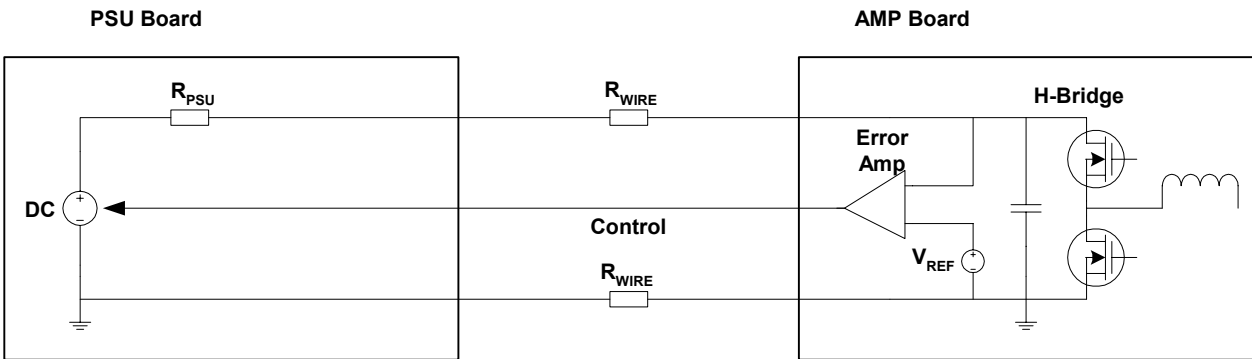
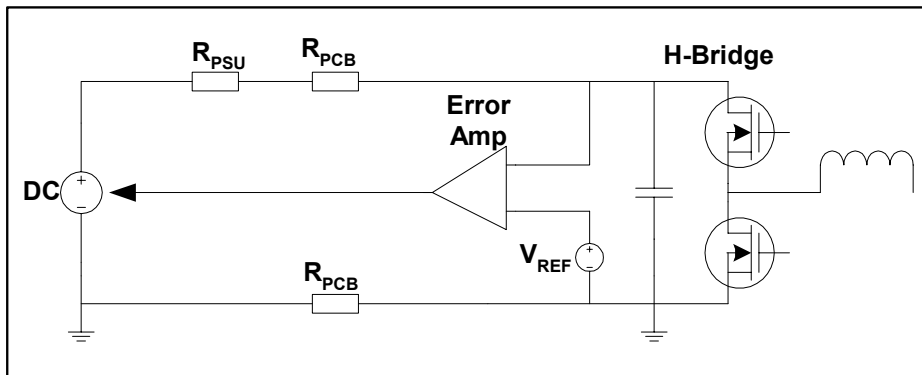


Figure 5. Remote Sensing Using ERR-AMP on the AMP Board

In this configuration, the error amplifier still compensates for resistance in both HOT and GND wire. Note that this configuration does not add extra components to the system, but only moves components from one board to the other.

The best performance is achieved if the power supply and amplifier are built on same the PCB. Figure 6 shows this system.

PSU +AMP Board**Figure 6. PSU and AMP on the Same Board**

Resistance from wires and connectors interfacing the two PCB's is no longer there; however they are replaced with PCB track impedance, R_{PCB} , instead. The PCB track impedance is much smaller than impedance in wires and resistance, which in it self improves the power supply impedance. The best performance is obtained when the voltage is sensed close to the H-bridge.

5 Measurement of Power Supply Output Impedance

The impedance of a power supply can be measured using an Audio Precision Analyzer. Since the amplifier board contains several capacitors, this measurement must be done with the amplifier board connected to the power supply. Use the same wires and connector between the power supply board and the amplifier board as will be used in the end application. The impedance is then measured including wires and connectors and the result is the impedance that the amplifier will be affected by during operation.

Connect the power supply amplifier board and audio precision as shown in Figure 7.

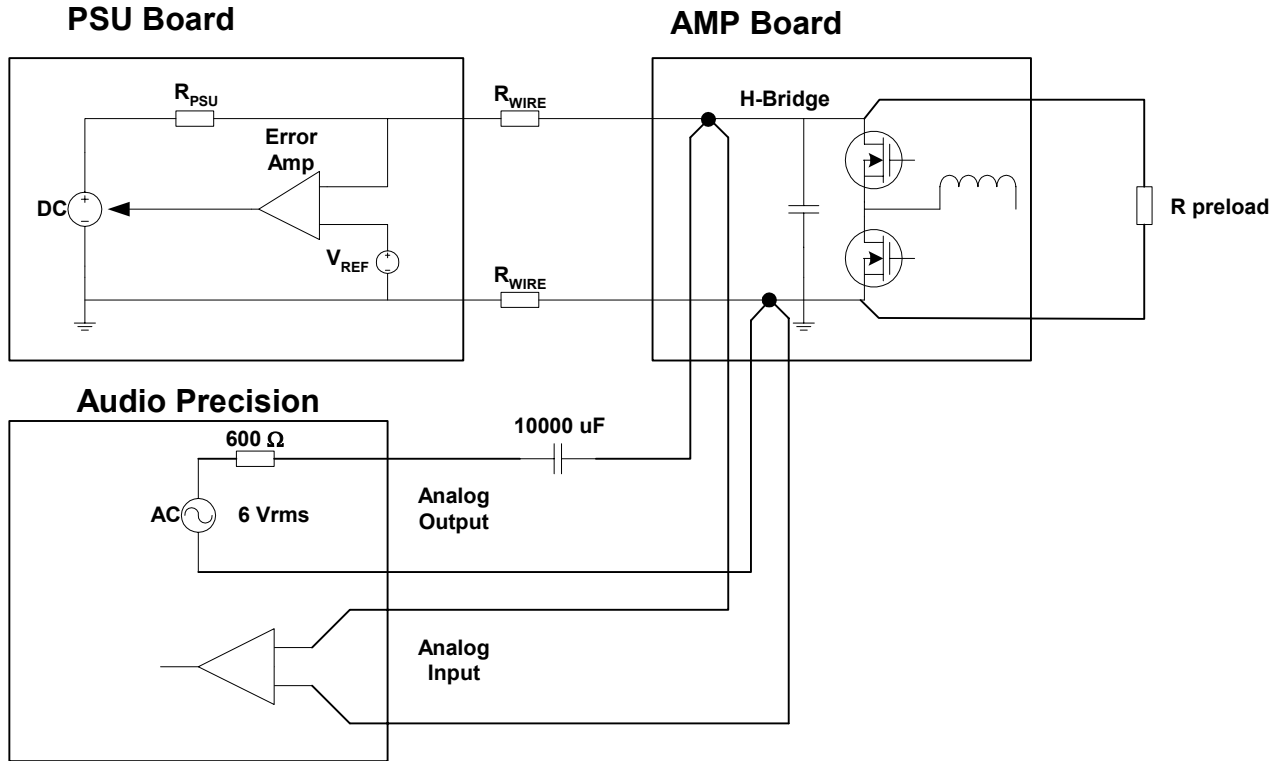


Figure 7. Impedance Measurement Setup

- Connect the power supply board to amplifier board as done in the end application.
- On the H-bridge power rail on the amplifier board, connect a preload resistor. The preload resistor is used to load the power supply at maximum operating point. The value of the preload resistor is defined as $R_{PRELOAD} = \frac{V_{H-BRIDGE}^2}{P_{MAX}}$. For a 2x 105-W system the resistor value is $R_{PRELOAD} = \frac{40.5V^2}{2 \cdot 105W} \approx 8\Omega$.
- The AP analog output is set to 600-Ω output impedance.
- Connect the AP analog output to H-bridge through a 10000-μF capacitor.
- The analog input is connected to H-bridge.
- Note that to get accurate measurements, the AP connections to the H-bridge must be made as a four terminal measurement as shown in Figure 7.

CAUTION:

Before turning the power supply on/off the AP analog output **MUST** be bypassed with a 10-Ω resistor. When the H-bridge voltage is changed, the 10000 μF capacitor will be recharged. This creates a charge current that may harm the Audio Precision if not bypassed by a resistor.

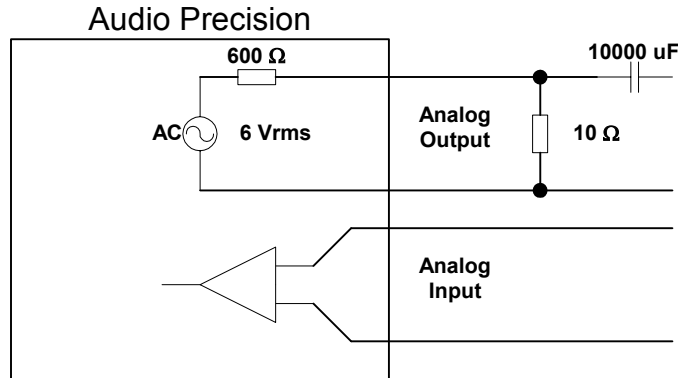


Figure 8. Resistor Placement During PSU Voltage Change

- Apply a 10-Ω resistor to the analog output and turn on the power supply.
- When the power supply voltage is stable, remove the 10-Ω resistor.
- Do not apply an audio signal to the amplifier input. Keep all audio channels muted.
- Set the AP analog output to 6 V_{RMS}. This generates a 10-mA current, which is injected into the power supply.
- Sweep from 20 Hz to 20 kHz, measuring ac voltage on the analog input.
- Power supply output impedance is then calculated as $R_{PSU} = \frac{V_{ANALOG_INPUT}}{10mA}$.

6 Example Applications Measurements

Data shown is measurements on the TAS5036REF and TAS5182C6REF. Two power supplies are tested for comparison. Tested power supplies are Delta SM70-22 power supply and a dedicated dc/dc converter (A706) to show a high-end power supply.

Delta SM70-22 is a LAB supply 70 V 22 A. Its output performance is as a typical power supply could be in an application without any of the recommended features. The control loop is implemented without particular attention to the output impedance and no remote sensing is used.

The control loop for the dc/dc converter is optimized to give low output impedance up to 800 Hz. Above 800 Hz, the decoupling capacitors are keeping the impedance low. It can be configured to use remote sense on HOT wire only. Hence, the GND wire resistance is not compensated for in this application.

Both power supplies are tested at 40.5 V and amplifier is loaded with 105 W / 6 Ω.

Figure 9 shows output impedance of the Delta SM 70-22 power supply. At 20-Hz output, impedance is 38 mΩ. This high impedance is due to long wires (more than 10 cm) between power supply and amplifier board, which this power supply do not compensate for. Output impedance peaks at 350 Hz, where the impedance is 55 mΩ. This peak is caused by the control loop, which is not optimized for low output impedance. At higher frequencies, >350 Hz, output impedance is controlled by capacitors on amplifier board.

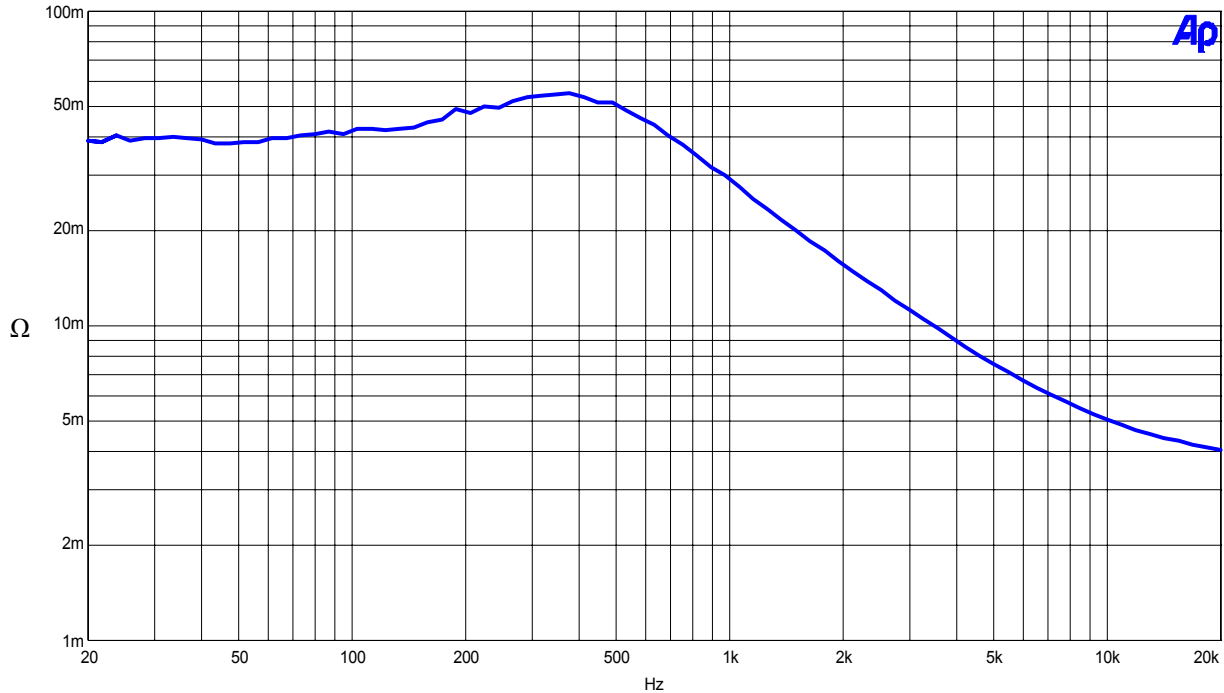


Figure 9. Rout Delta SM70-22 PSU

Resulting THD+N versus frequency is shown in Figure 10. At low frequencies, there is high THD+N. This is because of the wire resistance between power supply and amplifier board. THD+N peaks at 170 Hz. Note that this is half the frequency, at which the output impedance peak. The reason for this is that an output signal at 175 Hz causes a supply current at 350 Hz.

At higher frequencies the THD+N curve is getting flat, about 5 kHz. At this point, the power supply is no longer dominating THD+N. It is then PWM-timing errors that give the main contribution.

At 7 kHz, THD+N is suddenly dropping fast. Dominating THD+N in BD-mode modulation is third order harmonics. This means that the 7-kHz output signal gives third order harmonic at 21 kHz. This is outside the audio bandwidth and is then no longer part of the measurement when using an AES17 filter that cuts off all frequencies above 20 kHz.

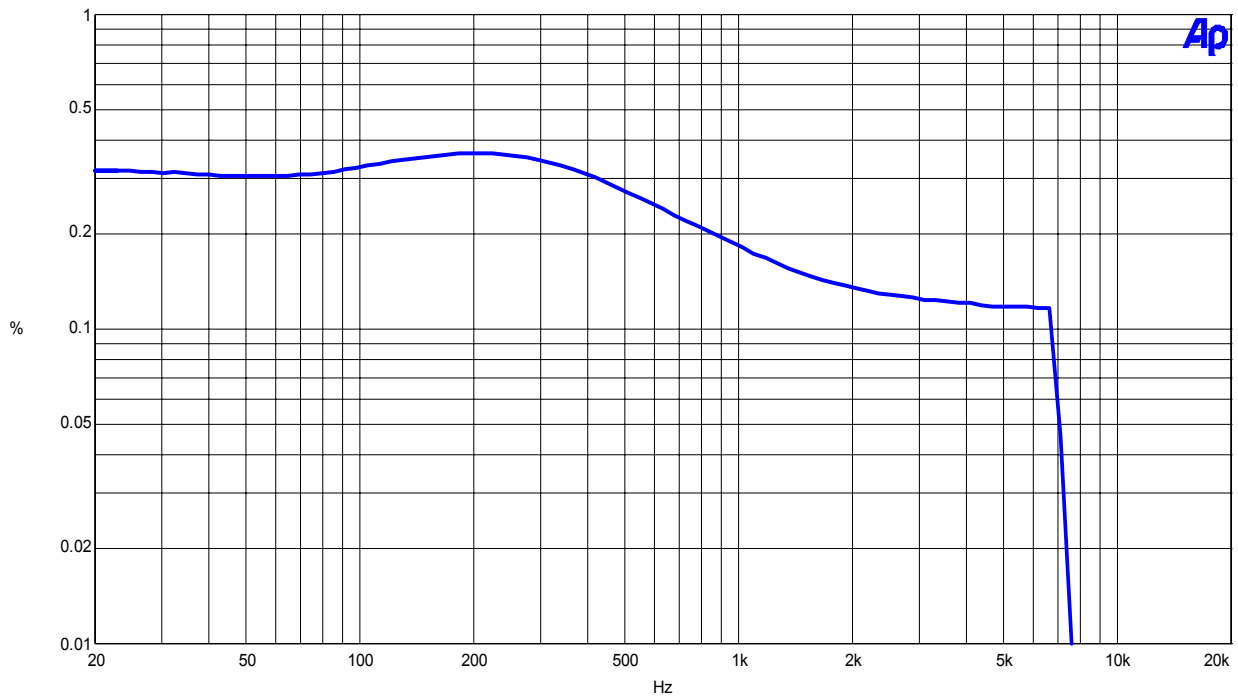


Figure 10. THD+N Performance Delta SM70-22 PSU

Not using remote sensing results in an impedance of 22 mΩ, as it can be seen in Figure 11. The dc/dc converter is optimized for low output impedance, so peak impedance is not visual in this measurement. The output impedance is mainly coming from wires and connectors.

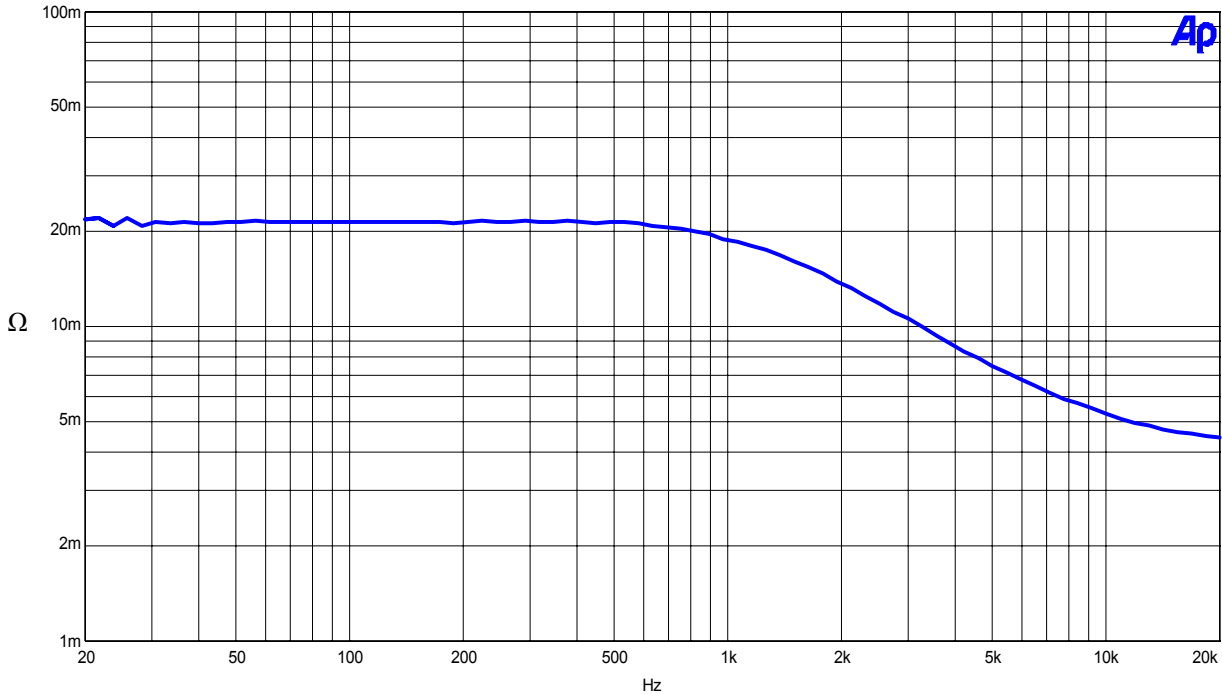


Figure 11. Rout for DC/DC Converter (A706) Without Remote Sensing

However, 22 mΩ is too high to give good THD+N performance versus frequency. This can be seen in Figure 12. THD+N at low frequencies is 0.14%. Above approx 400 Hz, the onboard capacitors becomes dominating and THD+N drop to its final value of 0.11%, where PWM-timing related THD+N is dominating.

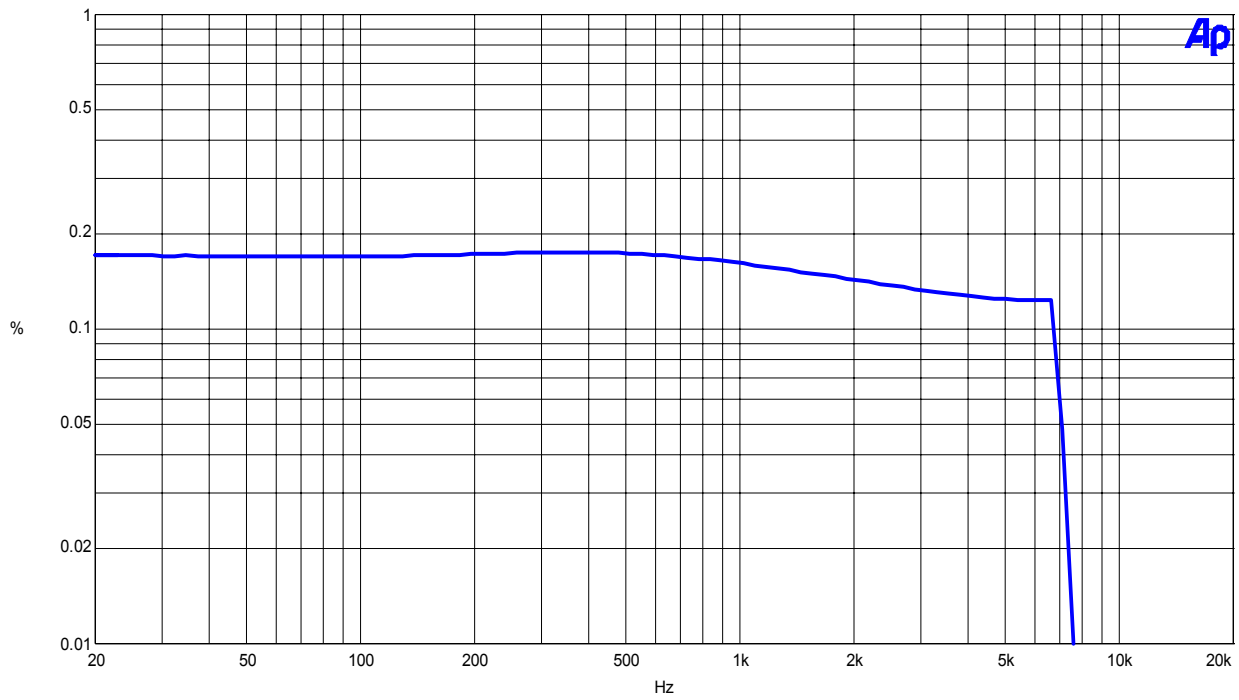


Figure 12. THD+N Performance for DC/DC Converter (A706) Without Remote Sensing

THD+N at low frequencies can be optimized using remote sensing. Remote sensing eliminates resistance in wires and connectors.

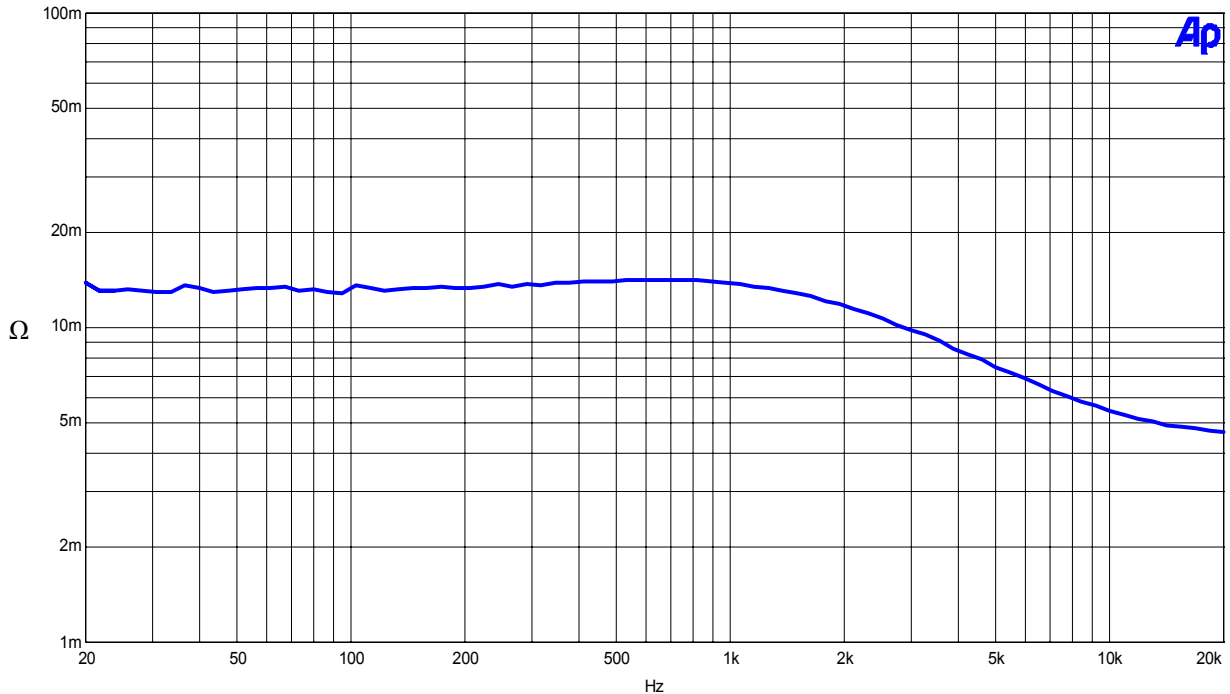


Figure 13. Rout for DC/DC Converter (A706) With HOT Remote Sensing

Output impedance from dc/dc converter A706 is seen in Figure 13. Using remote sense, resistance in HOT wire and connector becomes eliminated by the control loop. At 20-Hz, impedance is measured to 13 mΩ, rising to 14 mΩ at 800 Hz. This increase is coming from the control loop, as seen on Delta SM70-22, it is just much smaller.

Above 800 Hz, decoupling capacitors result in low impedance.

Using remote sensing on HOT wire reduces impedance from 22 mΩ to 14 mΩ. Impedance in the HOT wire and connector can then be calculated to be 8 mΩ. It can then be expected that having remote sensing in HOT and GND reduces the impedance even further by 8 mΩ. It will not be possible to reduce the impedance further due to finite control loop gain, but this is not necessary, being below 14 mΩ is acceptable for most applications. Below 14 mΩ, timing errors becomes dominant.

When using remote sensing THD+N versus frequency curve becomes almost flat from 20 Hz to 7 kHz, see Figure 14. When the THD+N curve is flat over frequency, the power supply is optimized to best performance for the application. Improving the power supply impedance further will not benefit audio performance, but only increase cost. At this point, the dominant factor with respect to THD+N is PWM-timing errors.

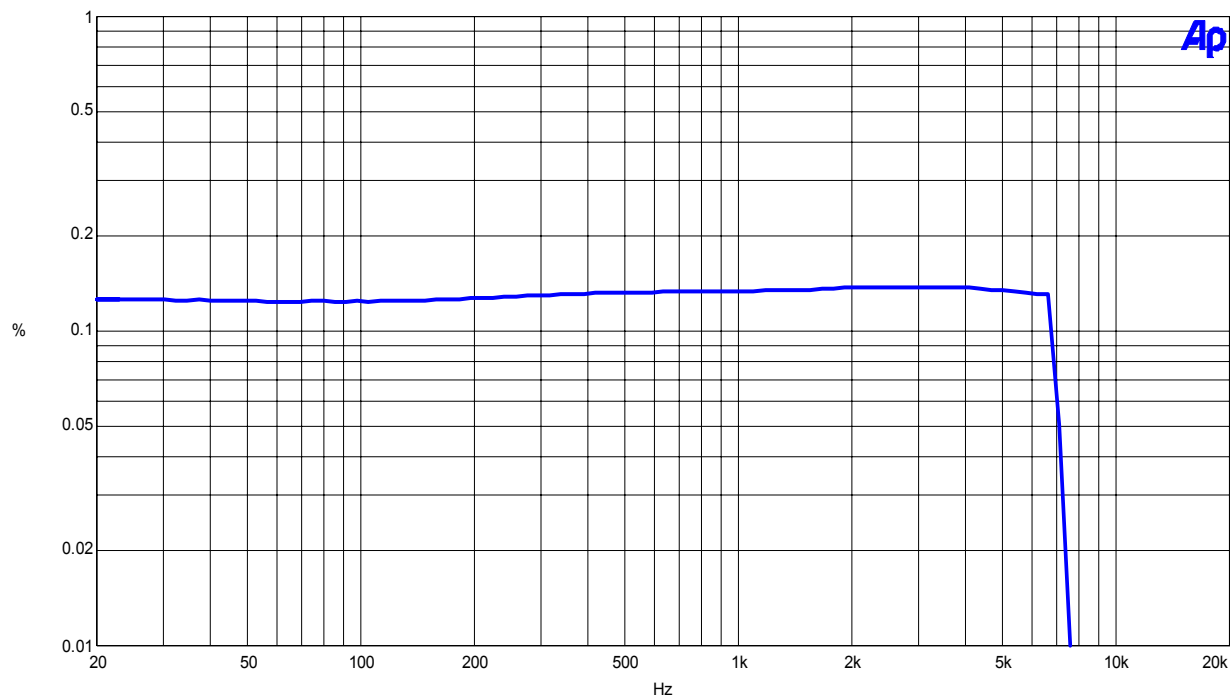


Figure 14. THD+N Performance for DC/DC Converter (A706) With HOT Remote Sensing

The conclusion for this application is that use of a dc/dc converter with optimized control loop and use of remote sensing in HOT wire is adequate to give optimum performance.

In case that the wire impedance between the power supply and amplifier board had been higher, use of both HOT and GND wire remote sensing would have been necessary.

References

1. *Digital Audio Measurements* (SLAA114)
2. *System Design Considerations for True Digital Audio Power Amplifiers* (SLAA117)
3. *Performance of an All-Digital Power Amplification System* (AES-104, May 98)

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