Technical Article

Understanding Class D Amplifier Non-Idealities: Reactive Loads and Parasitic Capacitances

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In this article, we'll learn about two important non-idealities of Class D power amplifiers and how they affect performance.

As we know from earlier articles, the switching frequency of a practical Class D amplifier doesn't always match its resonant frequency. This mismatch can result either from component non-idealities or the intentional operation of the amplifier at a slightly different frequency. In both cases, the mistuned LC circuit produces a reactive load.

In this article, we'll examine how the performance of a Class D amplifier is affected when its load network has a reactive component. We'll also explore the impact of parasitic capacitances at the input of the tuned circuit. The discussion of each non-ideality will conclude with an example problem.

Power Loss Due to Reactive Loads

Figure 1 shows the complementary voltage-switching Class D amplifier that we've been exploring over the past few articles.

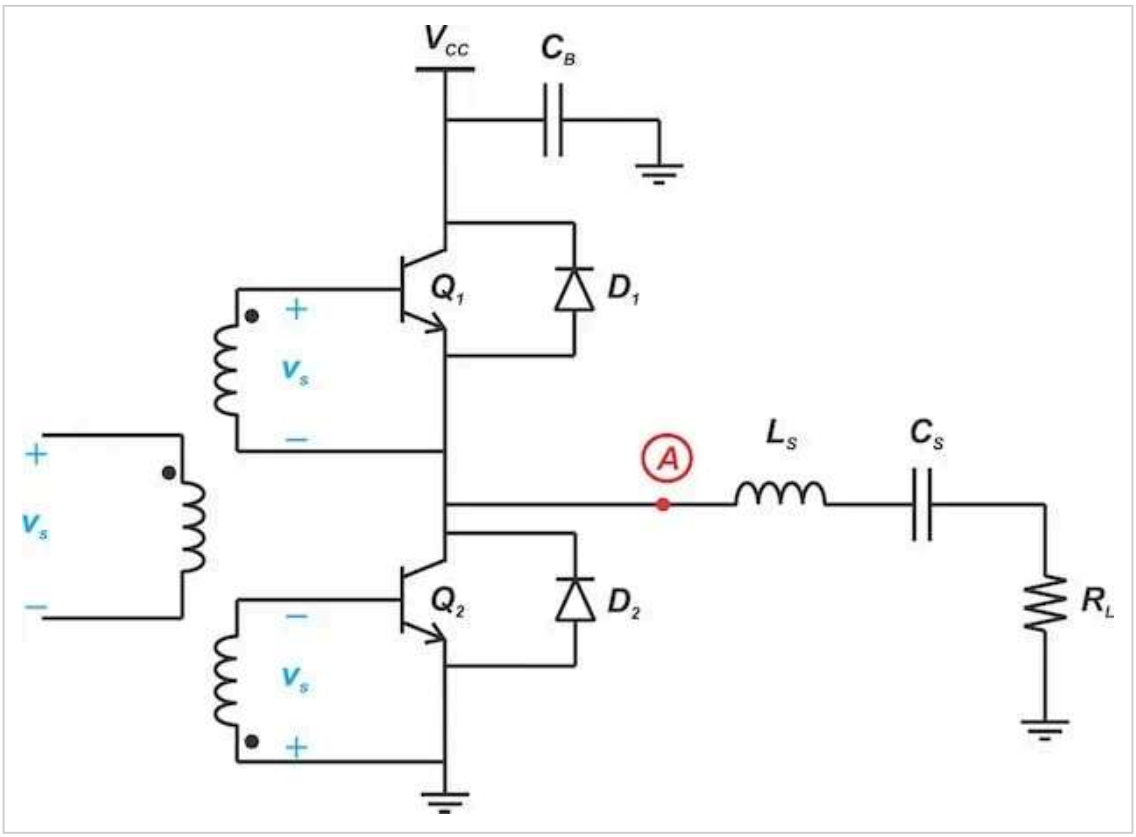

Figure 1. Complementary voltage-switching Class D configuration.

For the above amplifier, the ideal inductance value is L_S. The ideal capacitance is C_S. Together, L_S and C_S give us an ideal resonant circuit tuned to the switching frequency.

However, suppose that the inductance is actually $(L_S + L_a)$ because of component non-idealities. As illustrated in Figure 2, we now have an additional inductance in series with the ideal tuned circuit.

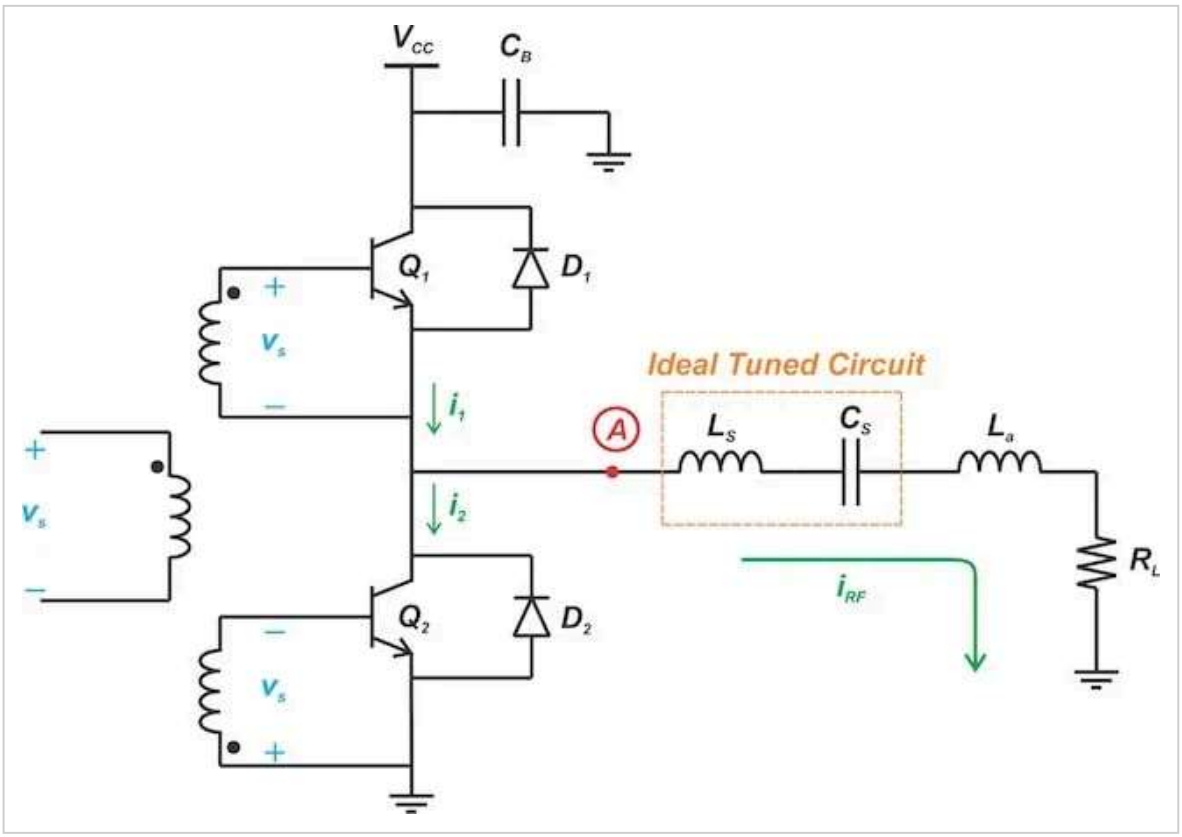

Figure 2. A Class D amplifier with a mistuned LC circuit due to component non-idealities.

The ideal tuned circuit in the orange box acts as a short at the switching frequency. The remaining load network comprises the series connection of L_a and R_L. Since the load is inductive, we see in Figure 3 that the output current (i_{RF}) lags behind the fundamental component of the square wave at node A (V_A).

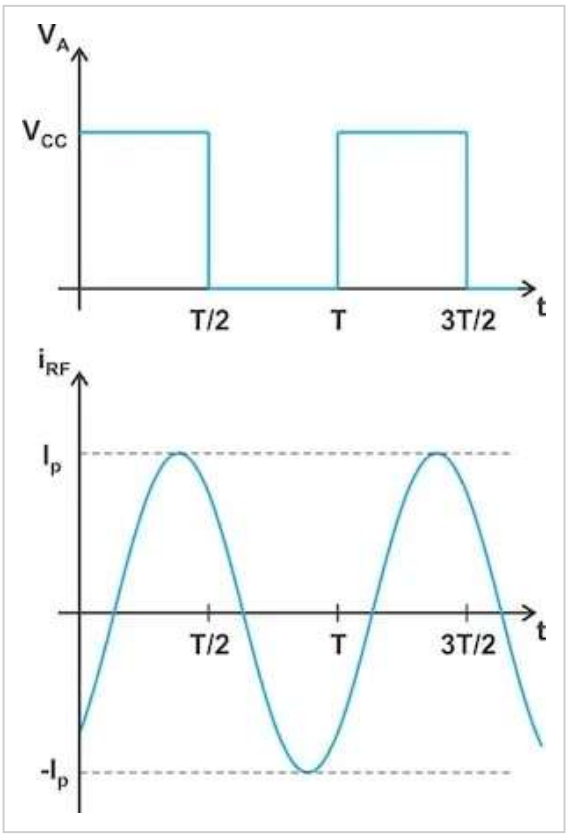

Figure 3. Above the resonant frequency, the current lags the fundamental component of the square wave voltage.

From our first discussion of Class D operation, we know that an ideal Class D amplifier has a theoretical 100% efficiency and an output power of $P_L = 2V_{CC}^2/\pi^2 R_L$. Let's see how the phase difference in Figure 3 influences these parameters.

The Effect of a Reactive Load on Output Power

We need to know the load current's peak value (I_p) to calculate the power delivered to the load. The load current is produced by the fundamental component of V_A. Using the Fourier series representation to express V_A in terms of its constituent frequency components, we get:

$$V_A = \frac{V_{CC}}{2} + \frac{2V_{CC}}{\pi} \sum_{n=1}^{\infty} \frac{\sin((2n-1)\omega_0 t)}{2n-1}$$

Equation 1.

where ω_0 is the angular fundamental frequency of the square wave.

From Equation 1, we see that the fundamental component of V_A has a peak value of $2V_{CC}/\pi$. Both the equation and its result are unchanged from when we discussed the ideal Class D amplifier.

The same can't be said of Equation 2. The load impedance (Z_L) at the switching frequency (ω_0) is no longer simply equal to R_L. Instead, it consists of the series connection of L_a and R_L, giving us an impedance of:

$$Z_L = R_L + jL_a\omega_0 = R_L + jX_L$$

Equation 2.

where X_L is the inductive reactance. Using Ohm's law, the current flowing through the load is:

$$i_{RF} = \frac{V_{A,\ fundamental}}{Z_L} \Rightarrow i_{RF}(t) = \frac{2V_{CC}}{\pi|Z_L|}\sin\left(\omega_0 t - \arctan(\frac{X_L}{R_L})\right)$$

Equation 3.

From Equation 3, the peak value of i_{RF} is $I_p = \frac{2V_{CC}}{\pi|Z_L|}$. Recalling that i_{rms} is equal to $I_p/\sqrt{2}$, we can now calculate the average power delivered to the load:

$$P_L = R_L i_{rms}^2 = \frac{2V_{CC}^2}{\pi^2|Z_L|^2} \times R_L$$

Equation 4.

This equation can be rewritten as:

$$P_L = \left(\frac{2V_{CC}^2}{\pi^2 R_L}\right) \times \rho^2$$

Equation 5.

where:

$\frac{2V_{CC}^2}{\pi^2 R_L}$ is the power that would be delivered to a purely resistive (X_L = 0) load

ρ = $R_L/|Z_L|$

Since the load impedance includes a reactive component, ρ is less than unity. The product of Equation 5 is therefore less than the ideal load power.

It's not surprising that adding a reactive component reduces the load power—it's easy to see from Equation 2 that a reactive term increases the magnitude of the load impedance ($|Z_L|$), which reduces the output current.

The Effect of a Reactive Load on Efficiency

In the previous section, we calculated the output power. To find the efficiency, we also need to determine the input power provided by the supply. The input power is equal to the supply voltage multiplied by the average value of the current drawn from the supply.

In Figure 3's waveforms, the current is drawn from the supply during the first half-cycle of the switching period (from $t = 0$ to $t = T/2$), which is when the upper switch is ON. In the second half-cycle, the upper switch is open and no current can be drawn from the supply. During this half of the cycle, the energy stored in the LC circuit circulates through the load and the lower switch. Therefore, the DC component of the supply current is:

$$\begin{aligned} I_{dc} &= \frac{1}{T}\int_0^{T/2} i_{RF}(t)\,dt \\ &= \frac{1}{T}\int_0^{T/2} \frac{2V_{CC}}{\pi|Z_L|}\sin\left(\omega_0 t - \arctan(\frac{X_L}{R_L})\right)\,dt \end{aligned}$$

Equation 6.

Note that the integral is taken over the time interval when the upper switch is ON.

The seemingly intimidating equation above simplifies to:

$$I_{dc} = \frac{2V_{CC}}{\pi^2|Z_L|^2} \times R_L$$

Equation 7.

Multiplying Equation 7 by V_{CC}, we find the input power:

$$P_{CC} = \frac{2V_{CC}^2}{\pi^2|Z_L|^2} \times R_L$$

Equation 8.

This is equal to the output power (Equation 4), resulting in an ideal efficiency of 100%. Even though a reactive load reduces the output power, it doesn't degrade the amplifier's efficiency.

Example: Power Reduction Caused by a Reactive Load

When discussing the ideal Class D amplifier, we designed a complementary voltage-switching Class D amplifier to deliver 20 W to a purely resistive 50 Ω load. We saw that this requires a supply voltage of V_{CC} = 70.2 V and transistors that can safely conduct a maximum current of 0.89 A. You can verify these numbers by substituting R_L = 50 Ω and X_L = 0 into Equations 3 and 5 of this article, as the purely resistive load is a special case of the analysis we provided above.

This time, let's assume that a reactance of 50 Ω appears in series with R_L = 50 Ω. What would the output power and maximum collector current be?

First, let's find ρ. With R_L = 50 Ω and X_L = 50 Ω, we have:

$$\rho = \frac{R_L}{|Z_L|} = \frac{50}{\sqrt{50^2 + 50^2}} = \frac{1}{\sqrt{2}}$$

Equation 9.

Plugging this value of ρ into Equation 5, we observe that the output power is halved because of the reactive component of the load network. The output power with a resistive load was 20 W, so the new output power is 0.5 × 20 = 10 W.

In Equation 3, we saw that the maximum current is $I_p = \frac{2V_{CC}}{\pi|Z_L|}$. $|Z_L|$ is equal to R_L/ρ, and V_{CC} is given as 70.2 V at the start of the example. We therefore have a peak current of:

$$I_p = \frac{2V_{CC}}{\pi|Z_L|} = \frac{2 \times 70.2}{\pi \times 50 \times \sqrt{2}} = 0.63 \text{ A}$$

Equation 10.

The maximum current passing through the transistor reduces from 0.89 A (in the ideal amplifier) to 0.63 A. As stated above, the output power halves from 20 W to 10 W.

Power Loss Due to Parasitic Capacitances

Figure 4 shows another important non-ideality of Class D amplifiers: parasitic capacitances.

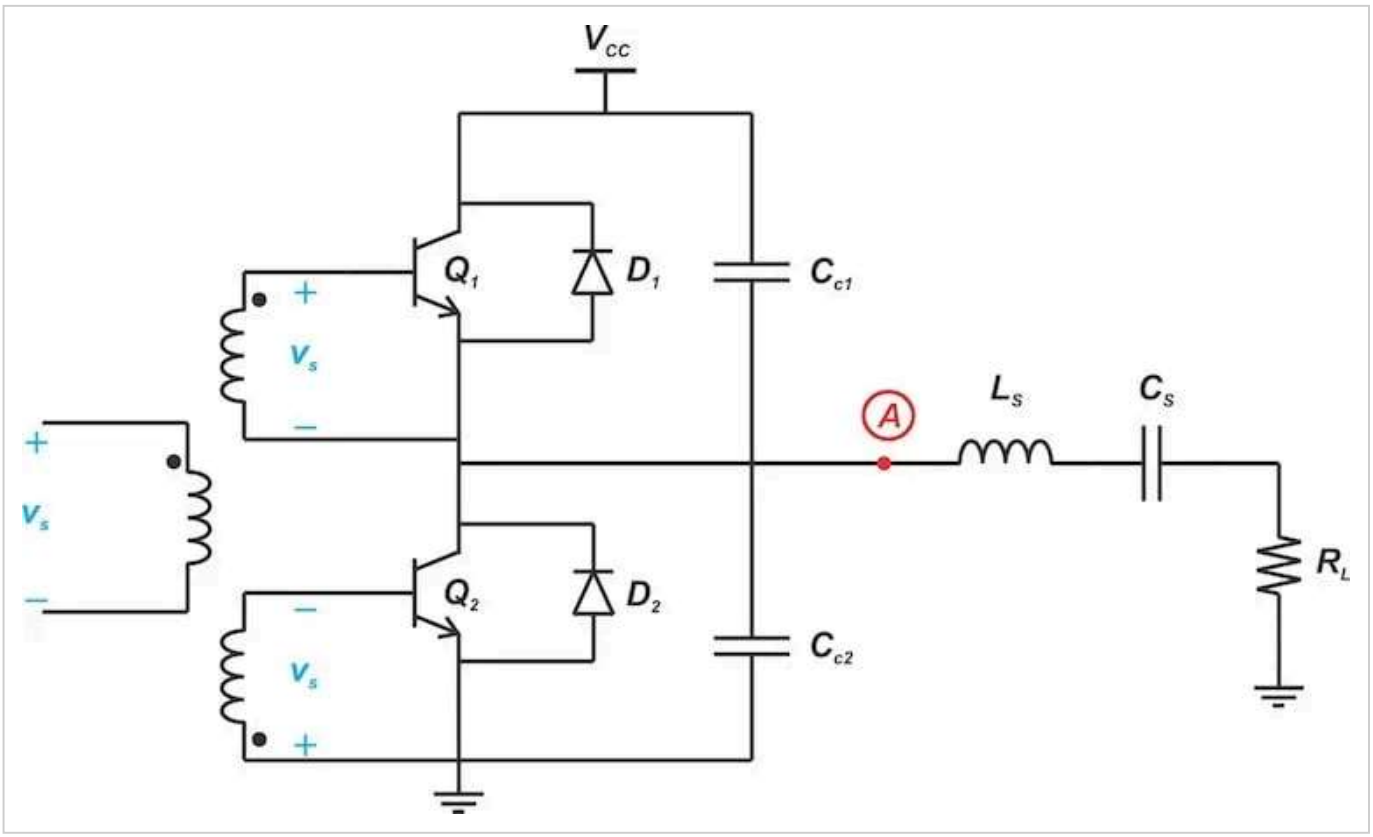

Figure 4. **C_{c1}** ***and*** **C_{c2}** ***model the parasitic capacitances that exist between node A and the supply rails.***

In the above figure, C_{c1} and C_{c2} are the equivalent parasitic capacitances that appear in parallel with Q_1 and Q_2. When the square wave transitions between the supply rails, the capacitances cause power loss at node A. Let's see how this affects the amplifier's performance.

Figure 5(a) provides a simplified model of the circuit during the first half-cycle of operation. Figure 5(b) does the same for the second half-cycle. The voltages at C_{c1} and C_{c2} for each half-cycle are indicated in green.

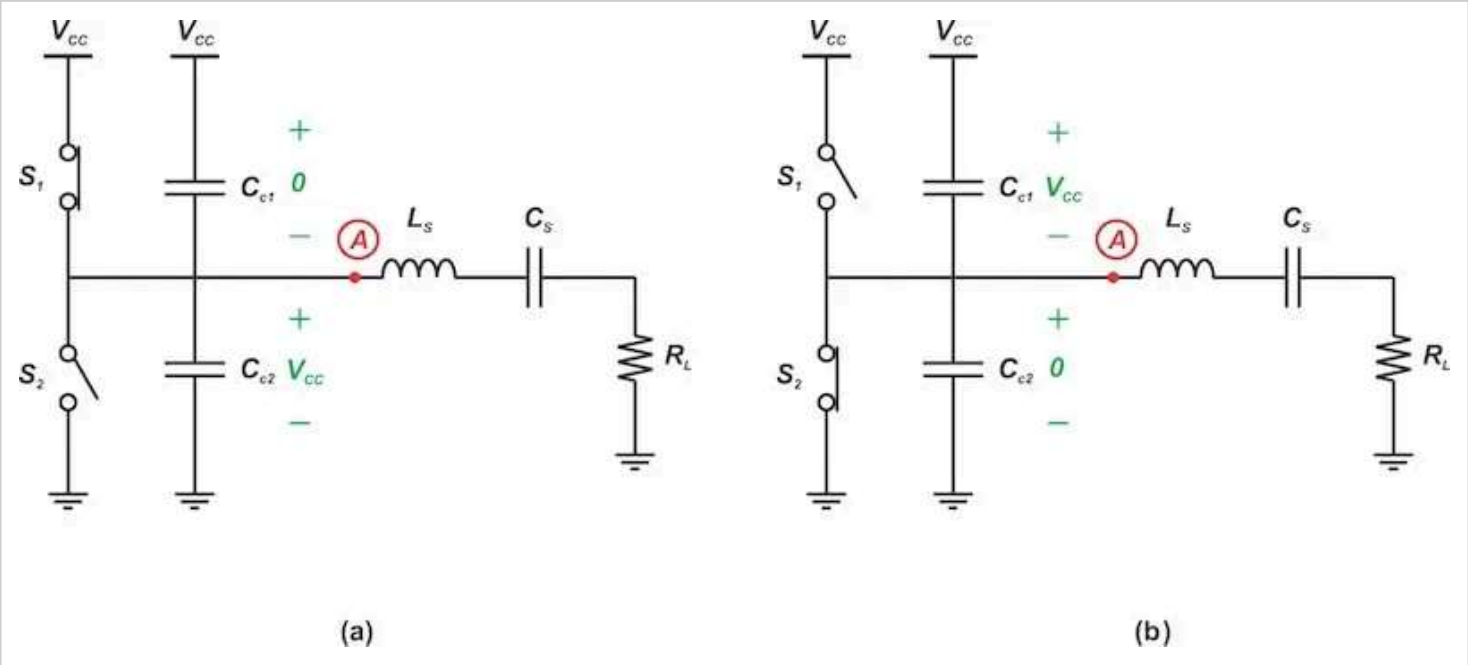

Figure 5. Voltages at C_{c1} and C_{c2} when node A is driven to V_{CC} (a) and ground (b).

In the first half of the cycle, the upper switch (S_1) is closed and the lower switch (S_2) is open. The square wave at node A is therefore driven to V_{CC}. Because both of its terminals are at the same potential, C_{c1} has no charge. Meanwhile, C_{c2} is charged to V_{CC}.

At the beginning of the second half-cycle, S_2 closes and S_1 opens. The voltage at node A is driven—ideally instantly—to ground. When this transition occurs, S_2 charges C_{c1} to V_{CC} and discharges C_{c2} from V_{CC} to 0 V. The energy that was initially stored in C_{c2} is therefore lost.

Using the formula for energy storage in a capacitor, we can calculate the initial energy of C_{c2}:

$$U_1 = \frac{1}{2} C_{c2} V_{CC}^2$$

Equation 11.

This energy is dissipated as heat in S_2 when it closes. At the same time, C_{c1} is charged to V_{CC}. Denoting the energy that gets stored in C_{c1} as U_2, we have:

$$U_2 = \frac{1}{2} C_{c1} V_{CC}^2$$

Equation 12.

To understand how this affects power loss, we need to review the behavior of the simple RC circuit in Figure 6.

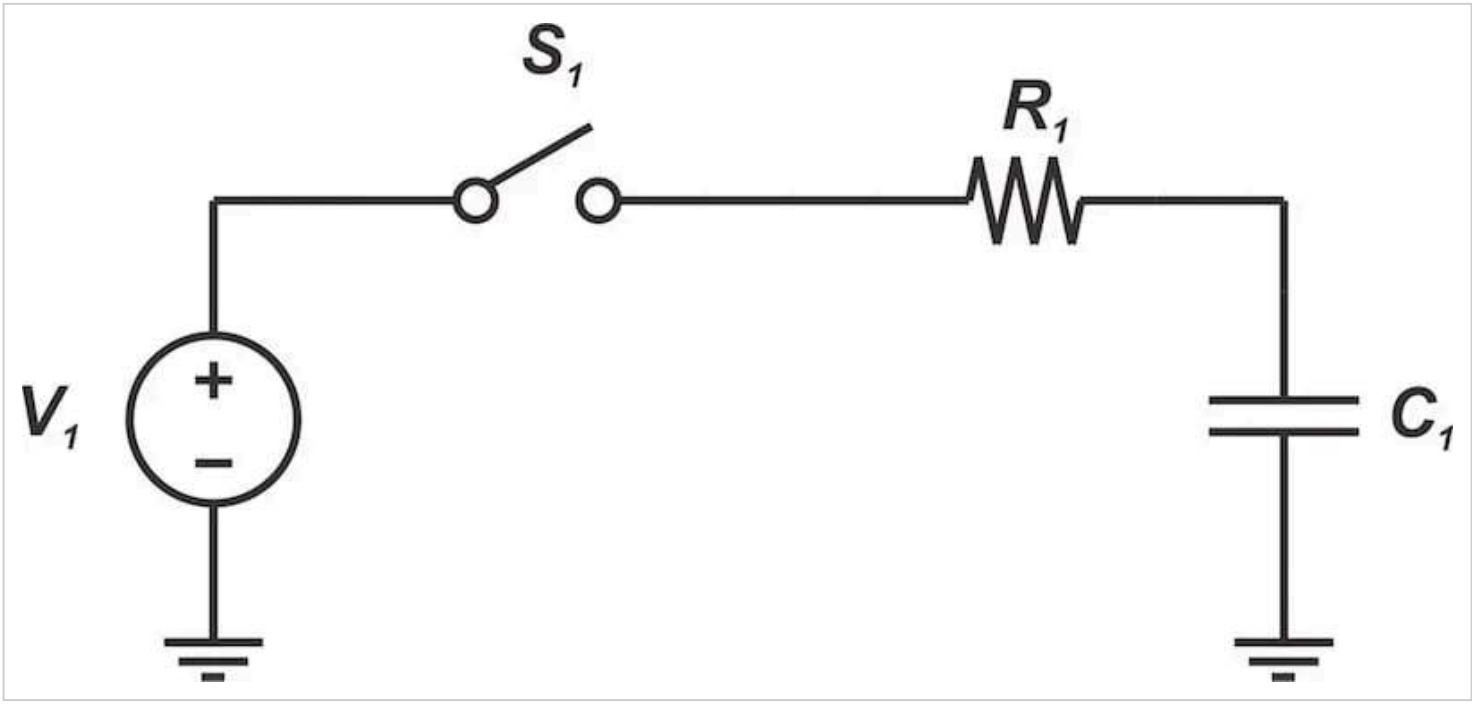

Figure 6. An RC circuit to charge a capacitor.

When we close the switch in this circuit, the voltage source supplies the energy to charge the capacitor. However, it can be shown that only half of the energy supplied by the battery is stored in the capacitor. The other half is dissipated as heat in the resistor.

Interestingly, the energy dissipated in the resistor is independent of the resistance value. In the Class D amplifier, this means that an amount of energy equal to U_2 is dissipated in the switch-on resistance when S_2 closes and charges C_{c1}. Therefore, the total energy dissipated in S_2 is $U_1 + U_2$.

A similar sequence of events happens at the beginning of the next half-cycle, when node A is driven back to V_{CC}. At this instant, the switch S_1 closes to discharge C_{c1} to 0 V and charge C_{c2} to V_{CC}. This leads to another energy loss of $U_1 + U_2$. Therefore, the total energy lost due to the parasitic capacitances over a full cycle is:

$$U_{total} = 2(U_1 + U_2) = (C_{c1} + C_{c2})V_{CC}^2$$

Equation 13.

Since this amount of energy is lost in every RF cycle, the power dissipated is:

$$P_{dissipated} = (C_{c1} + C_{c2})V_{CC}^2 f$$

Equation 14.

where f is the switching frequency.

Because this power is dissipated in the switches, there's no effect on the amplifier's output power—only on its efficiency.

Example: Efficiency Reduction Caused by Parasitic Capacitances

A complementary voltage-switching Class D amplifier powered by V_{CC} = 70.2 V delivers 20 W to a 50 Ω load. However, two 20 pF parasitic capacitances (C_{c1} = C_{c2} = 20 pF) exist at the input of its tuned circuit. If the switching frequency is 10 MHz, how much power is lost due to the parasitic capacitors? What is the efficiency of the amplifier?

Plugging the numbers into Equation 14, we obtain:

$$\begin{aligned} P_{dissipated} &= (C_{c1} + C_{c2})V_{CC}^2 f \\ &= (20 + 20) \times 10^{-12} \times 70.2^2 \times 10 \times 10^6 \\ &= 1.97 \text{ W} \end{aligned}$$

Equation 15.

The capacitances cause 1.97 W of power loss.

As we saw above, power losses due to parasitic capacitances don't affect the output power. They only increase the power provided by the supply. Therefore, efficiency can be calculated as:

$$\eta = \frac{P_{out,ideal}}{P_{out,ideal} + P_{dissipated}} = \frac{20}{20 + 1.97} = 91\%$$

Equation 16.

Because of the parasitic capacitances, the Class D amplifier has an efficiency of 91%, whereas the idealized Class D amplifier had a theoretical efficiency of 100%.

Wrapping Up

In this article, we learned about two non-idealities—reactive load components and parasitic capacitances—that affect Class D amplifiers. We saw that a reactive load reduces the amplifier's output power but not its efficiency; the parasitic capacitances, on the other hand, reduce efficiency but not output power.

As in the preceding articles about the Class D amplifier, our discussion was based on the complementary voltage-switching configuration. In the next article, we'll introduce a different configuration: the transformer-coupled voltage-switching Class D amplifier.

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