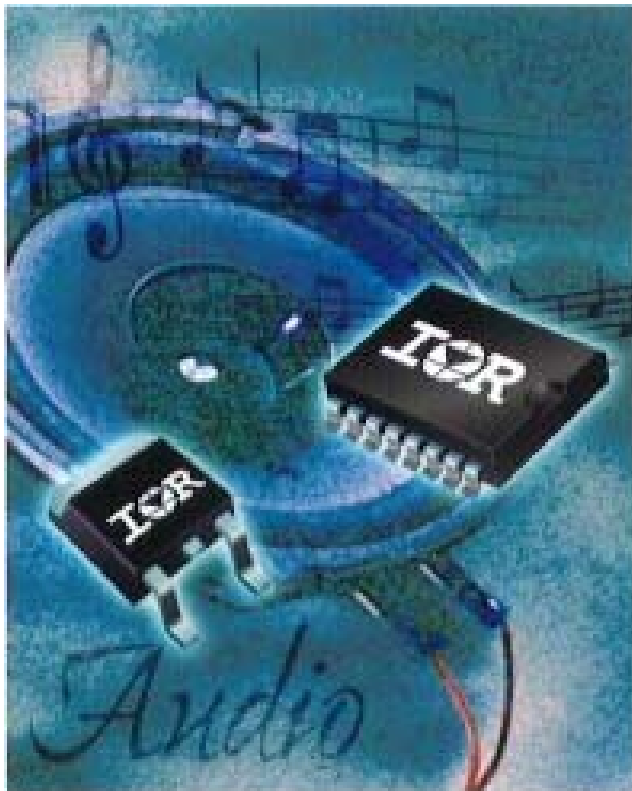


## Class D Audio Amplifier Design



- **Class D Amplifier Introduction**

Theory of Class D operation, topology comparison

- **Gate Driver**

How to drive the gate, key parameters in gate drive stage

- **MOSFET**

How to choose, tradeoff relationships, loss calculation

- **Package**

Importance of layout and package, new packaging technology

- **Design Example**

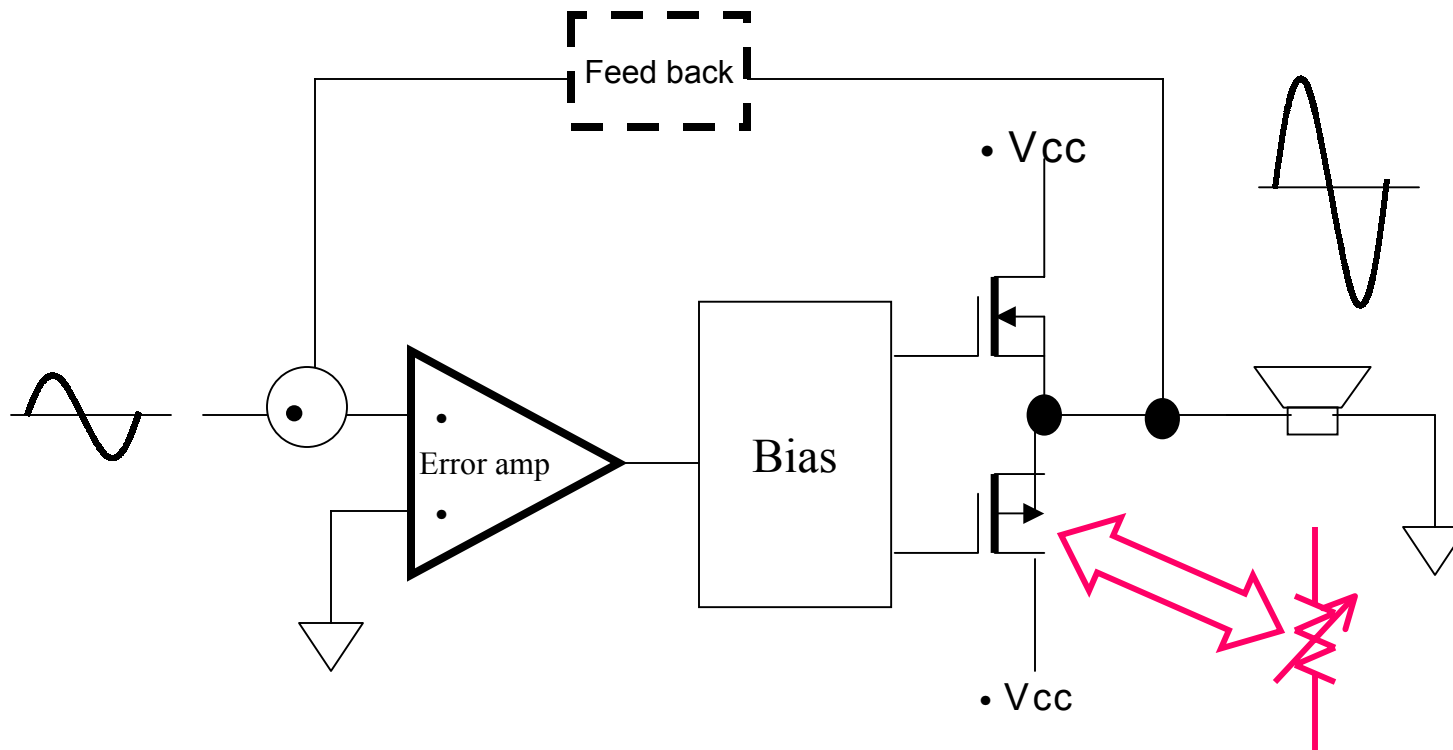
200W+200W stereo Class D amplifier

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## Trend in Class D Amplifiers

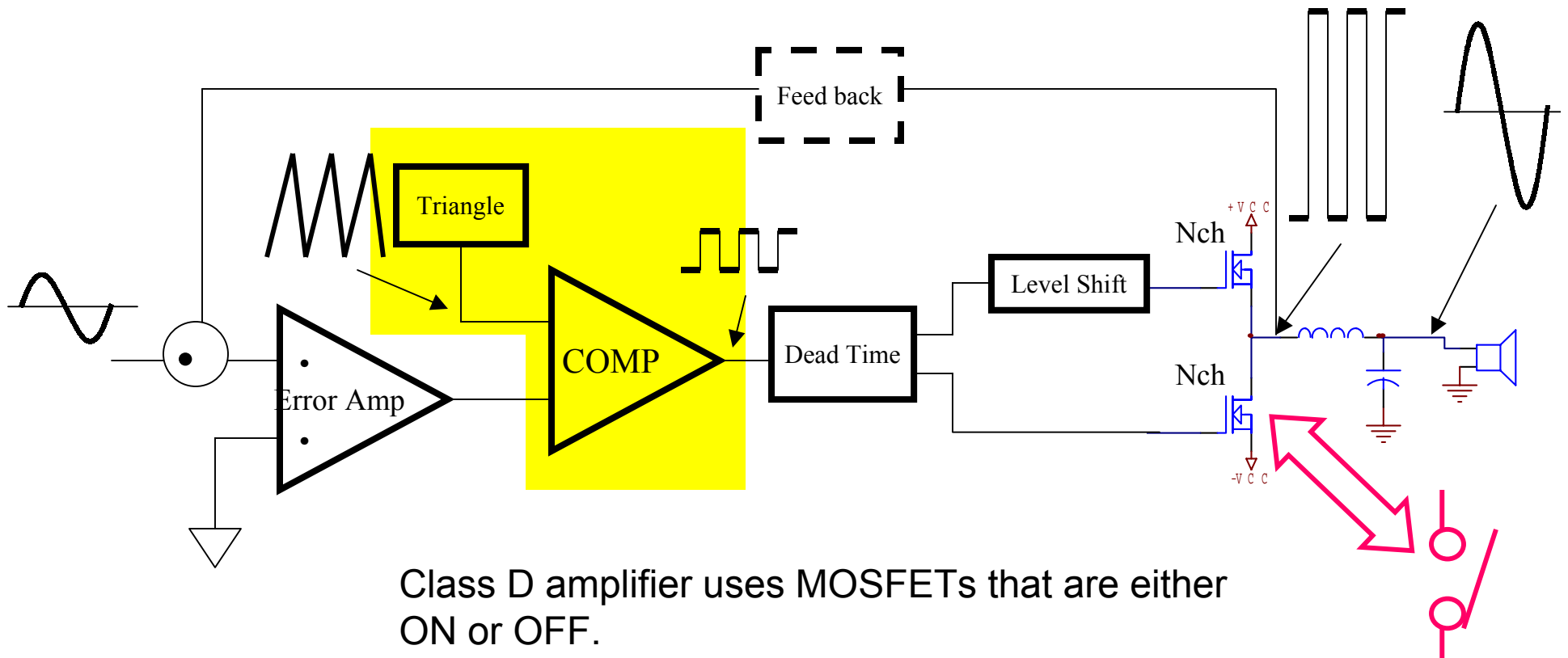
- **Make it smaller!**
  - higher efficiency
  - smaller package
  - Half Bridge
- **Make it sound better!**
  - THD improvement
  - fully digitally processed modulator

## Traditional Linear Amplifier



Class AB amplifier uses linear regulating transistors to modulate output voltage.  $\eta = 30\%$  at temp rise test condition.

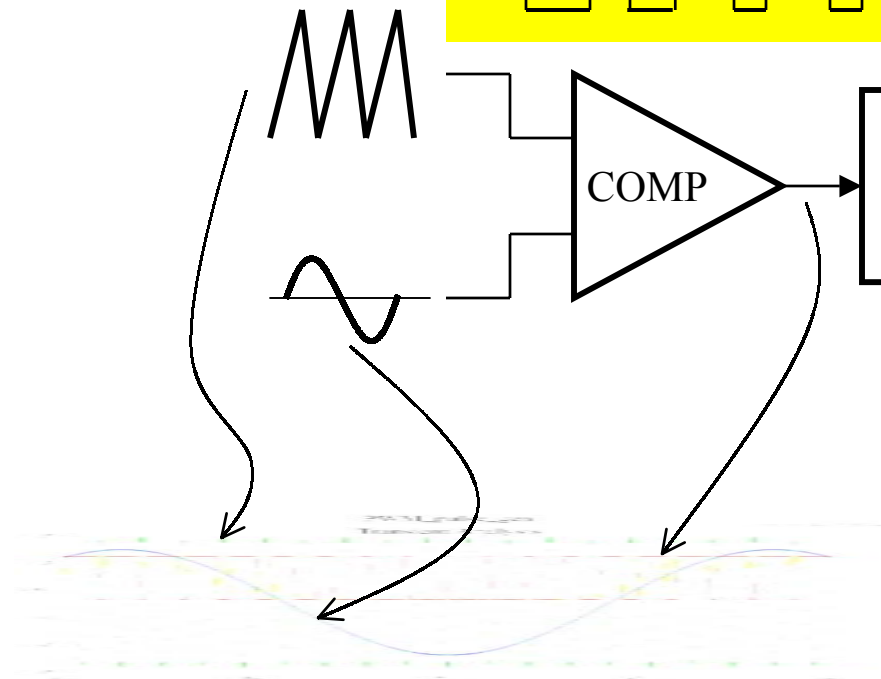
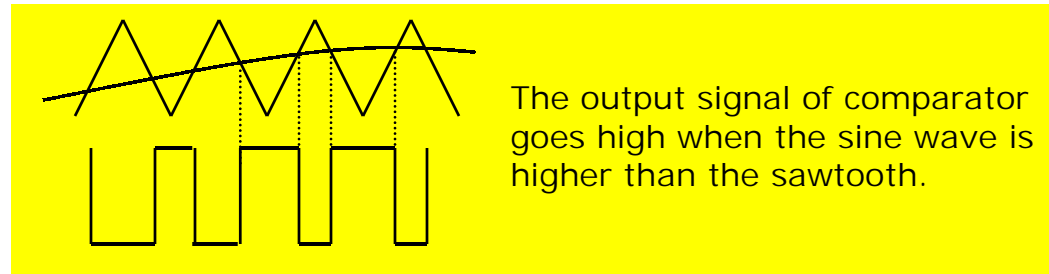
## How a Class D Amplifier Works



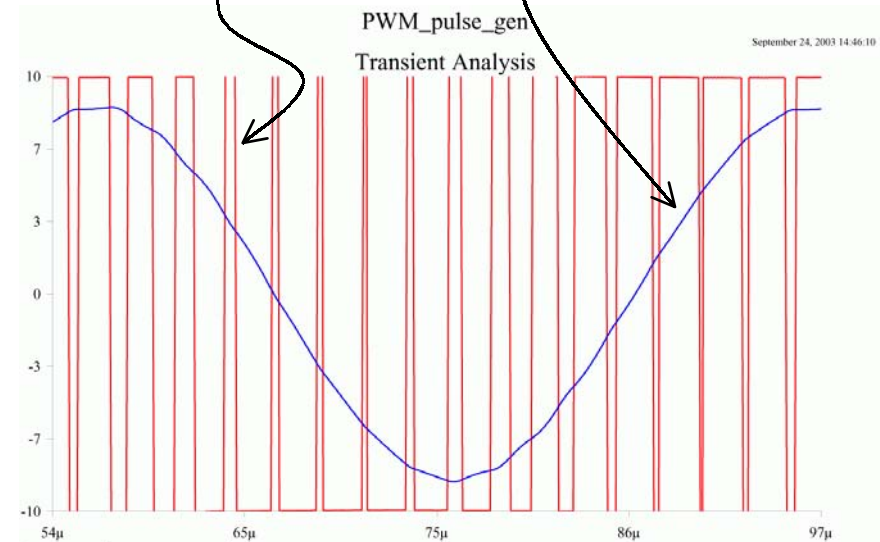
Class D amplifier uses MOSFETs that are either ON or OFF.

PWM technique is used to express analog audio signals with ON or OFF states in output devices. [www.irf.com](http://www.irf.com)

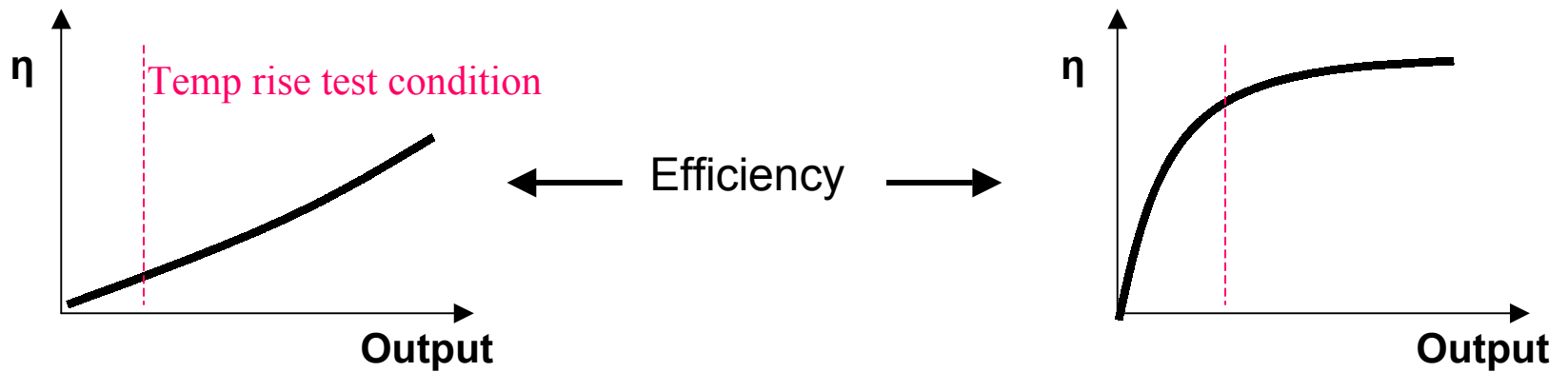
## Basic PWM Operation



Using  $f_{PWM}=400\text{KHz}$  to modulate  $25\text{KHz}$  sinusoidal waveform



# Topology Comparison: Class AB vs Class D



Constant over  $V_{bus}$  ←

Gain

→

Proportional to  $V_{bus}$

Good ←

PSRR

→

0 dB

Always from supply to load ←

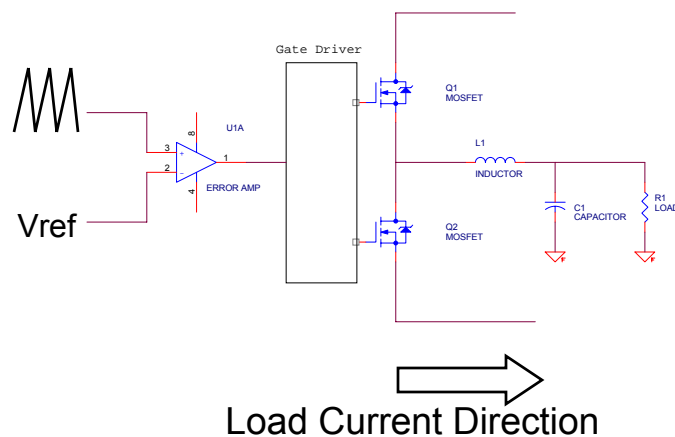
Direction of energy flow

→

Both way  
Creates  $V_{bus}$  pumping phenomena

## Analogy to Buck DC-DC Converter

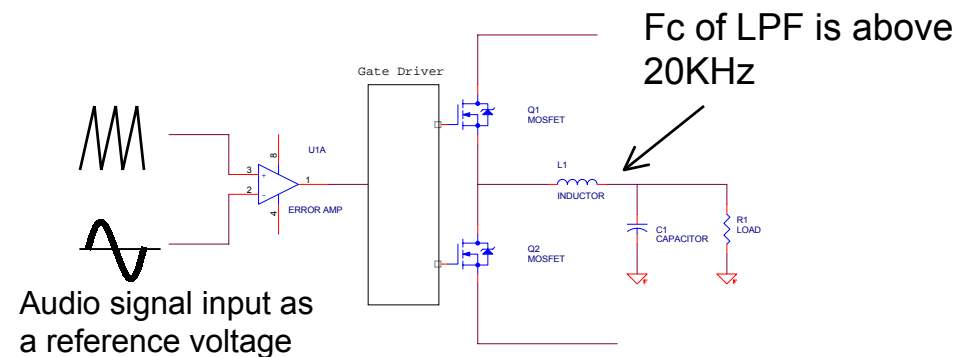
### Buck Converter



Duty ratio is fixed

- Independent optimization for HS/LS
- Low  $R_{DS(ON)}$  for longer duty, low Qg for shorter duty

### Class D Amplifier



Audio signal input as a reference voltage

Both current directions

- Influence of dead time is different
- Dead time needs to be very tight

Duty varies but average is 50%

- Same optimization for both MOSFETs
- Same  $R_{DS(ON)}$  required for both sides

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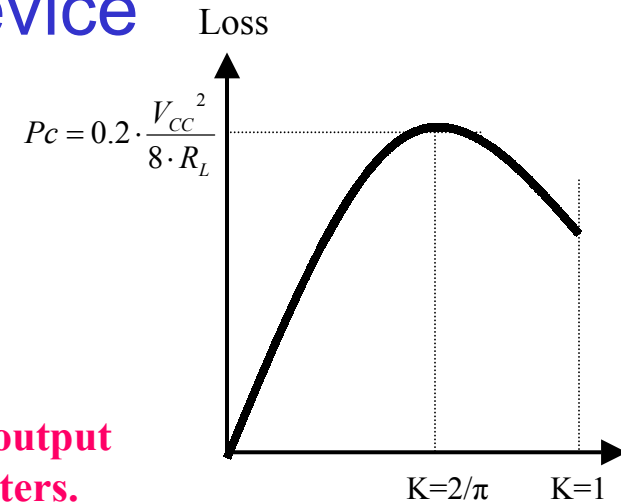
## Loss in Power Device

### Loss in class AB

$$P_C = \frac{1}{2 \cdot \pi} \cdot \int_0^\pi \frac{V_{CC}}{2} (1 - K \sin \omega \cdot t) \frac{V_{CC}}{2 \cdot R_L} K \sin \omega \cdot t \cdot d\omega \cdot t$$

$$= \frac{V_{CC}^2}{8\pi \cdot R_L} \cdot \left( \frac{2K}{\pi} - \frac{K^2}{2} \right)$$

← **Regardless of output device parameters.**

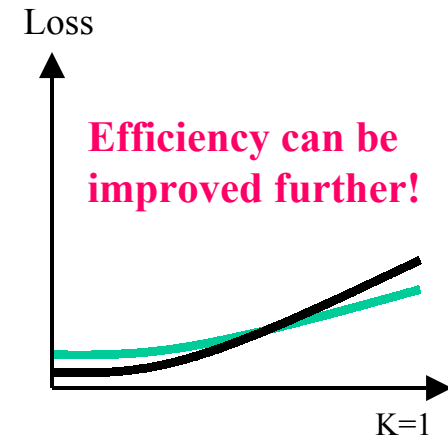


### Loss in Class D

$$P_{TOTAL} = P_{SW} + P_{cond} + P_{gd}$$

$$P_{cond} = \frac{R_{DS(ON)}}{R_L} \cdot P_O \quad P_{gd} = 2 \cdot Q_g \cdot V_{gs} \cdot f_{PWM}$$

$$P_{SW} = C_{OSS} \cdot V_{BUS}^2 \cdot f_{PWM} + I_D \cdot V_{DS} \cdot t_f \cdot f_{PWM}$$



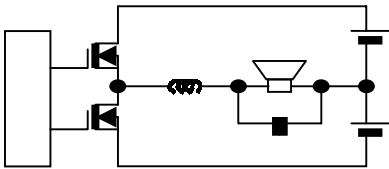
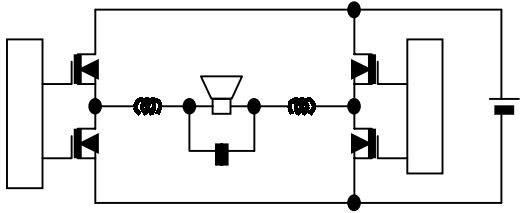
**Efficiency can be improved further!**

K is a ratio of Vbus and output voltage.



System → Gate Drive → MOSFET → Design Example

### Half Bridge vs Full Bridge

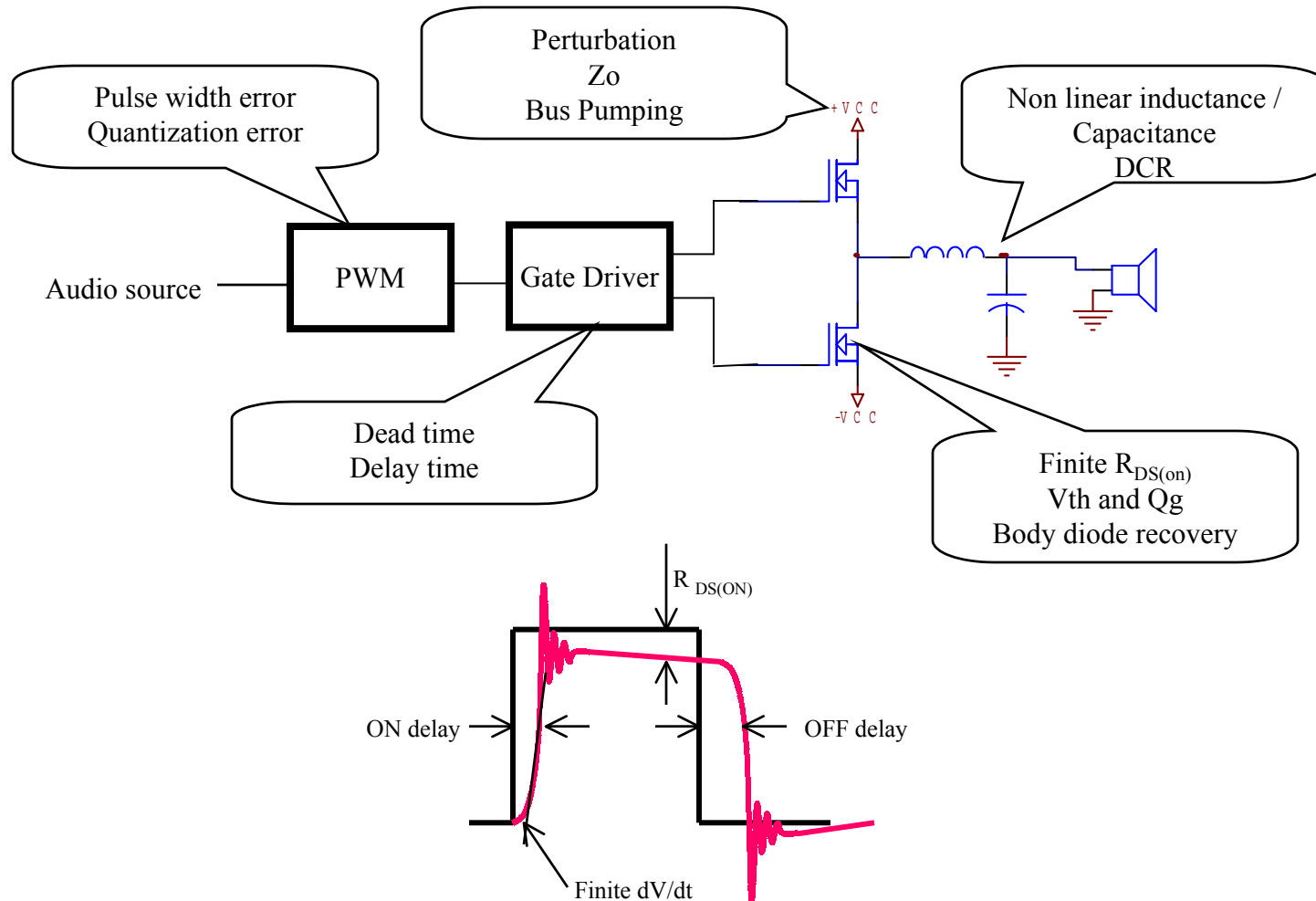
<b>Supply voltage</b>	0.5 x 2ch	1
<b>Current ratings</b>	1	2
<b>MOSFET</b>	2 MOSFETs/CH	4 MOSFETs/CH
<b>Gate Driver</b>	1 Gate Driver/CH	2 Gate Drivers/CH
<b>Linearity</b>		Superior (No even order HD)
<b>DC Offset</b>	Adjustment is needed	Can be cancelled out
<b>PWM pattern</b>	2 level	3 level PWM can be implemented
<b>Notes</b>	<p>Pumping effect Need a help of feed back</p> 	

Superior (No even order HD)  
Can be cancelled out  
3 level PWM can be implemented

→ Suitable for open loop design

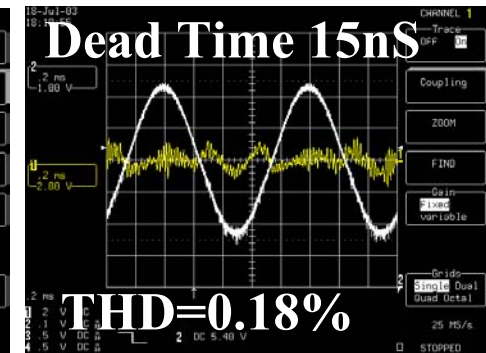
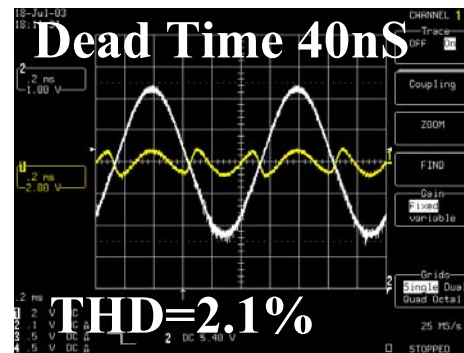
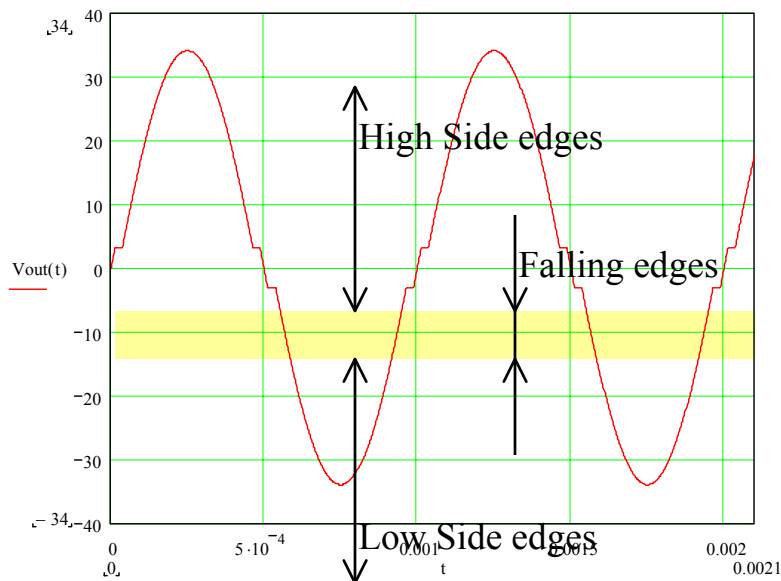
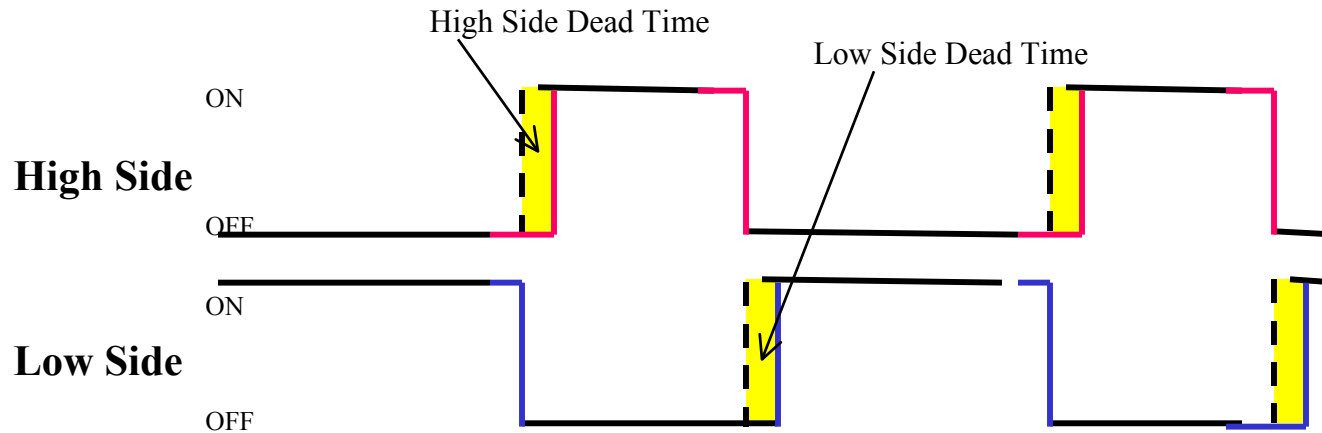
System → Gate Drive → MOSFET → Design Example

## Major Cause of Imperfection



System → Gate Drive → MOSFET → Design Example

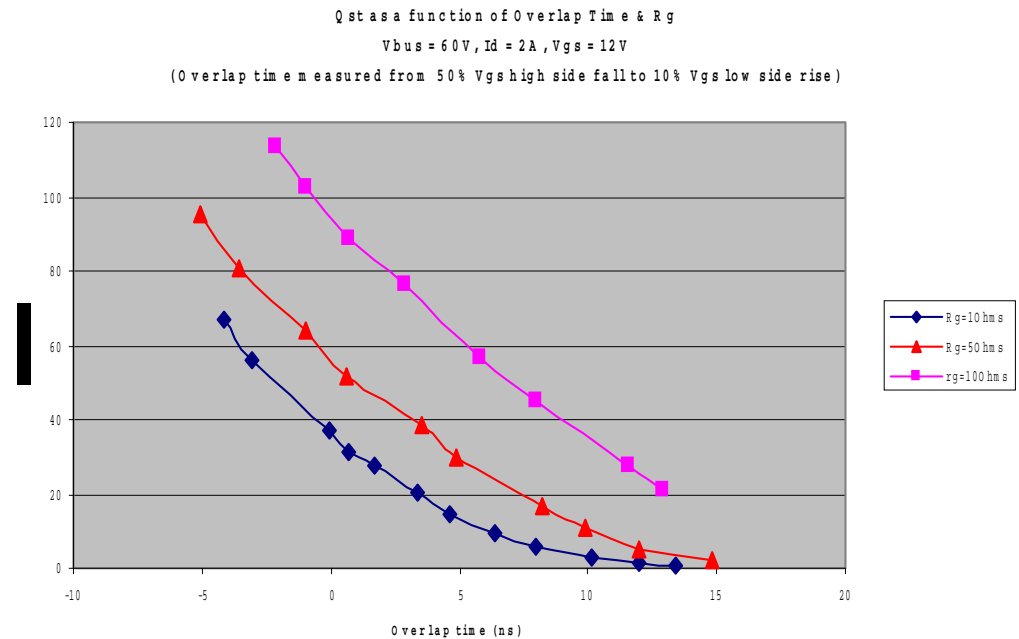
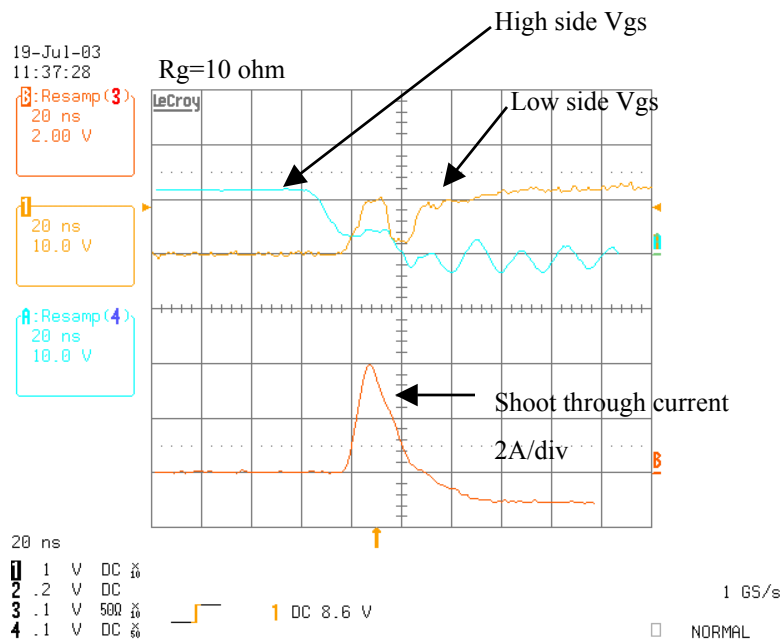
## THD and Dead Time



Note: THD (Total Harmonic Distortion) is a means to measure linearity with sinusoidal signal.

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \dots}}{V_{fundamental}}$$

## Shoot Through and Dead Time

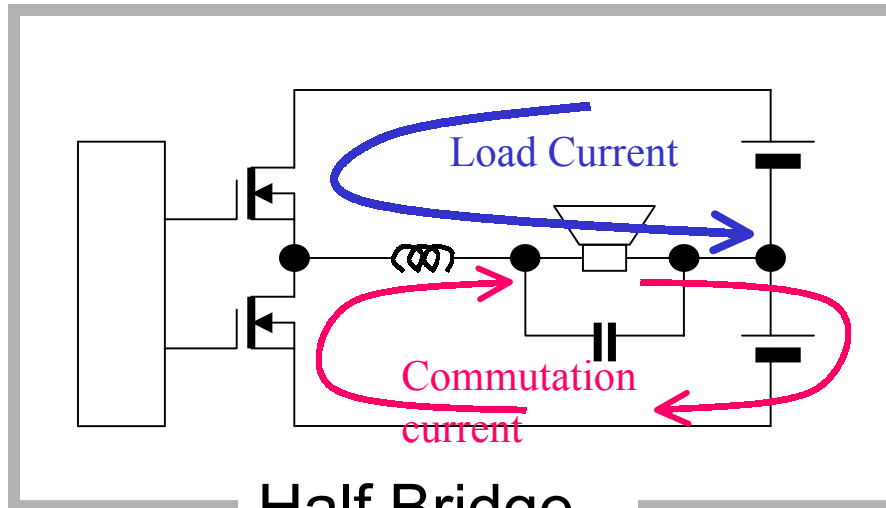


-Shoot through charge increases rapidly as dead time gets shorter.

-Need to consider manufacturing tolerances and temperature characteristics.

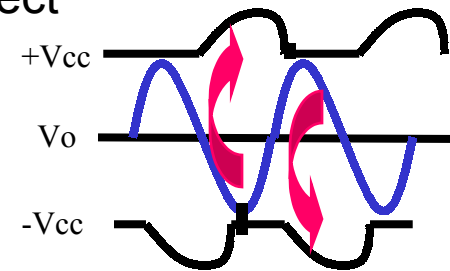
System → Gate Drive → MOSFET → Design Example

## Power Supply Pumping



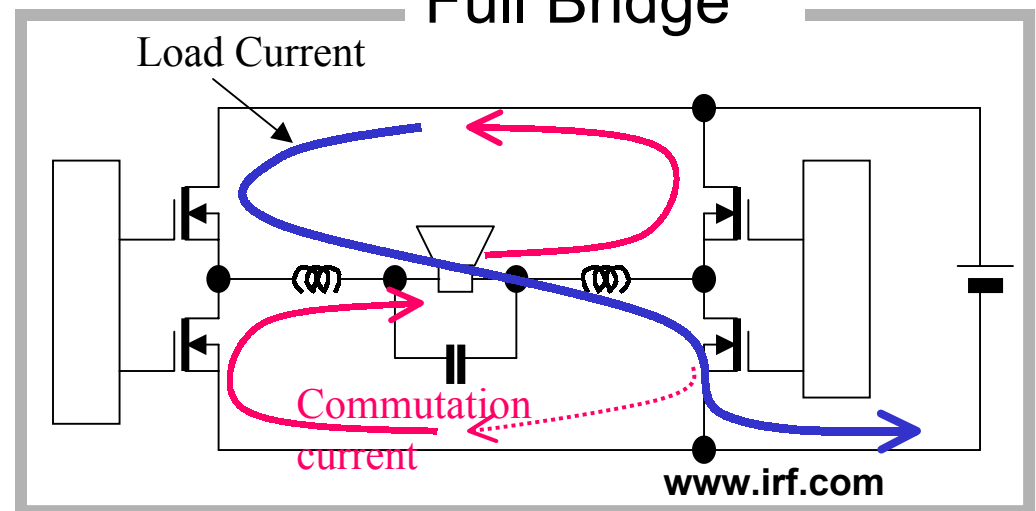
Half Bridge

Supply voltage Pumping effect



$$\Delta V_{BUS} \max = \frac{V_{BUS}}{8 \cdot \pi \cdot f_{PWM} \cdot R_{LOAD} \cdot C_{BUS}}$$

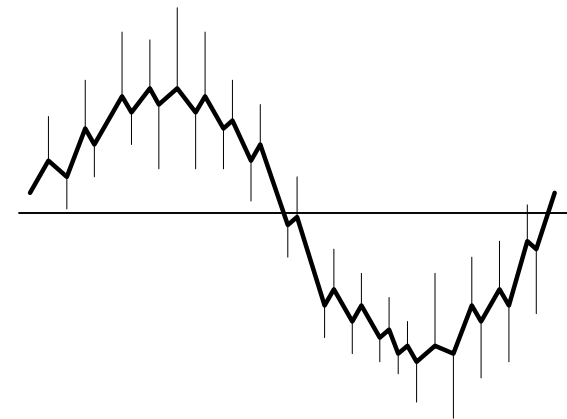
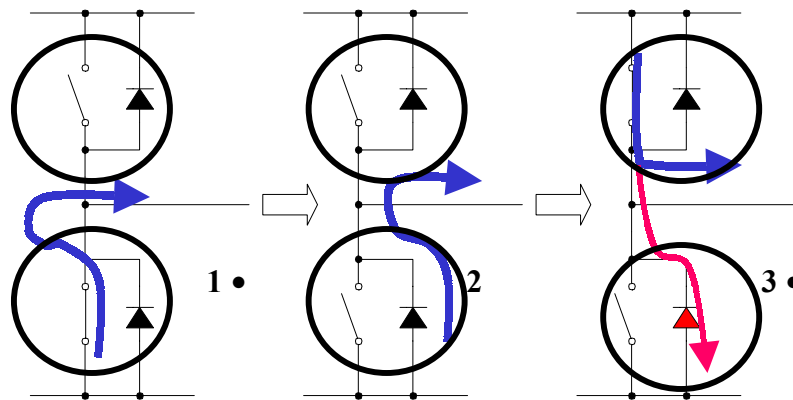
Full Bridge



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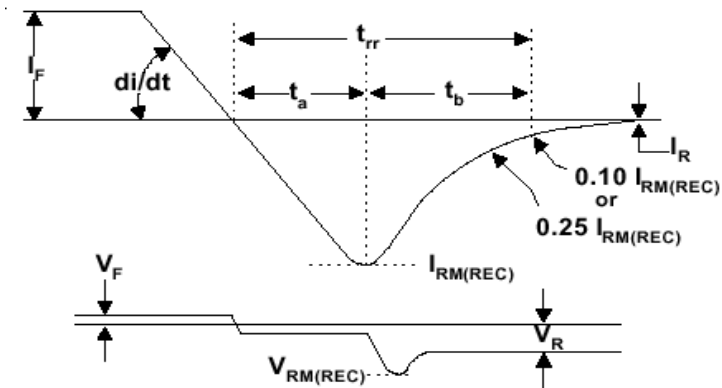
- Significant at low frequency output
- Significant at low load impedance
- Significant at small bus capacitors
- Largest at duty = 25%, and 75%

## EMI consideration: Qrr in Body Diode



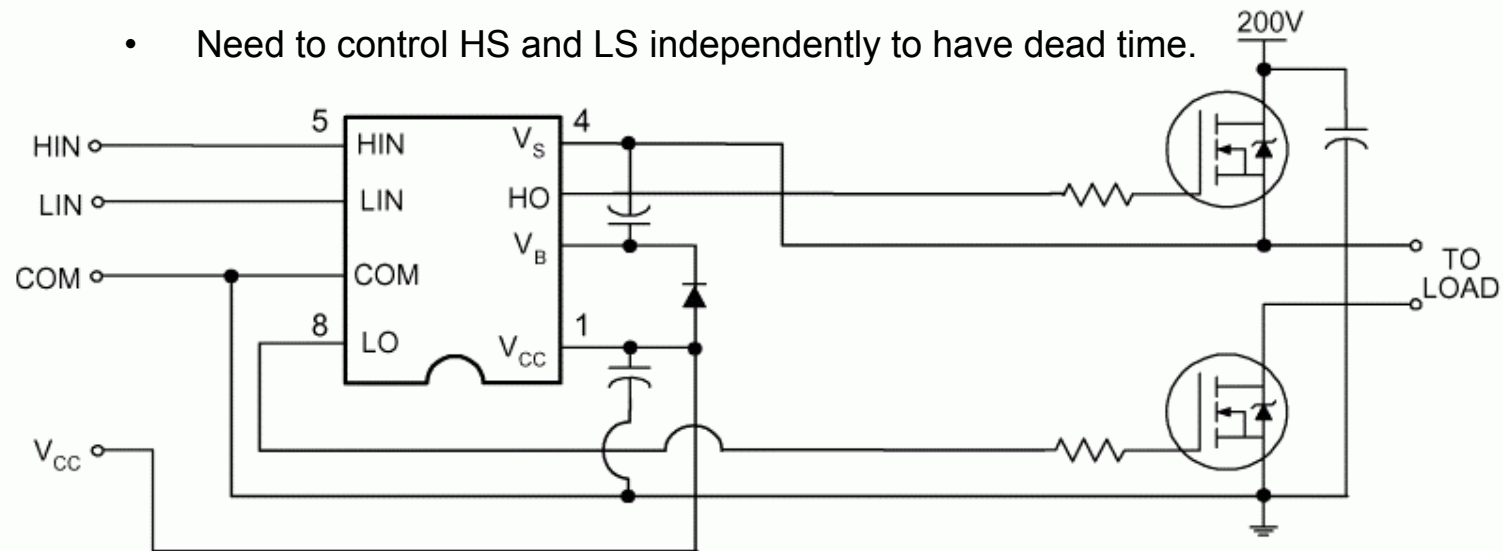
1. Low side drains inductor current
2. During dead time body diode of low side conducts and keep inductor current flow
3. At the moment high side is turned ON after dead time, the body diode is still conducting to wipe away minority carrier charge stored in the duration of forward conduction.

→ This current generates large high frequency current waveform and causes EMI noises.



### Gate Driver: Why is it Needed?

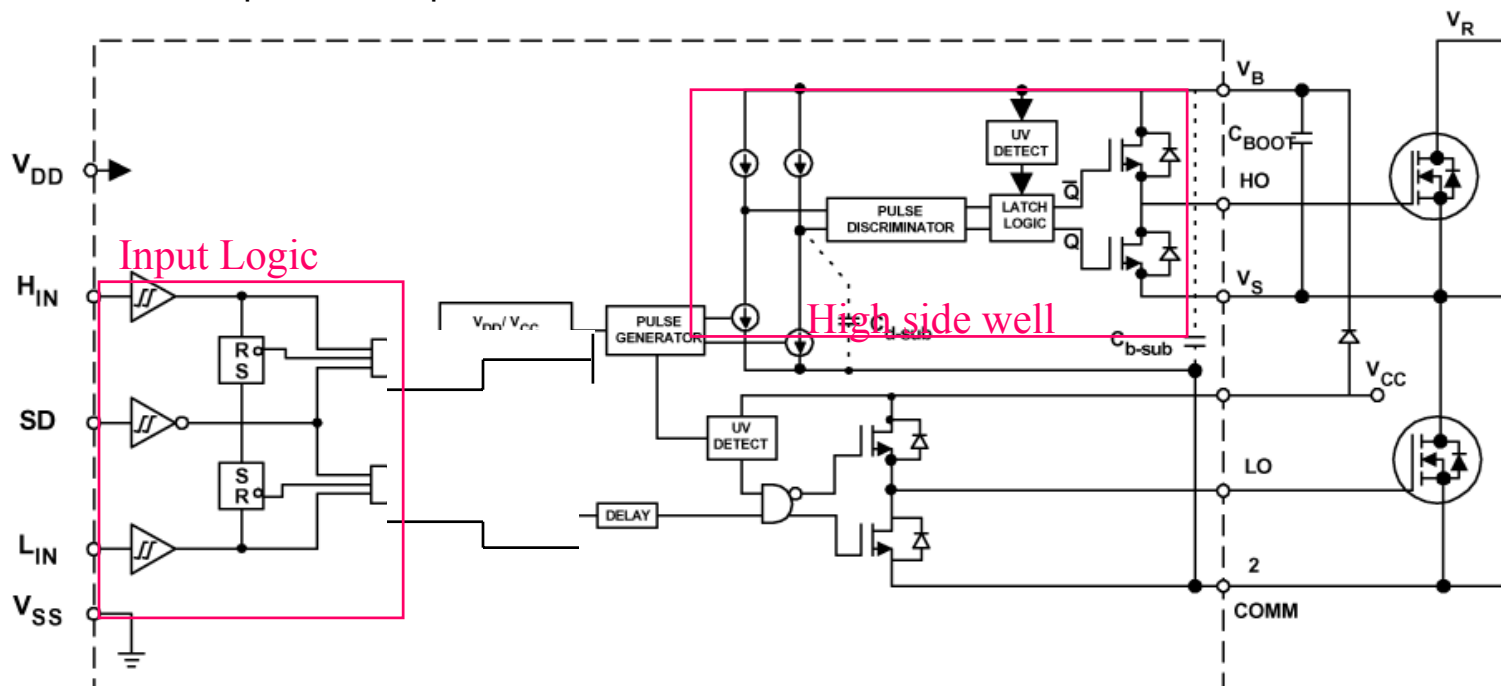
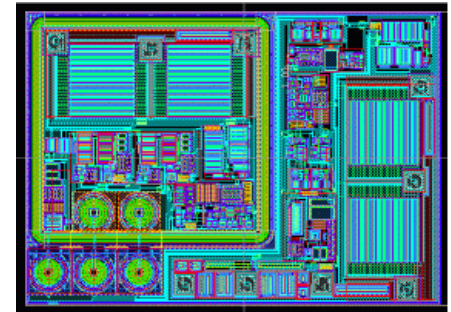
- Gate of MOSFET is a capacitor to be charged and discharged. Typical effective capacitance is 2nF.
- High side needs to have a gate voltage referenced to it's Source.
- Gate voltage must be 10-15V higher than the drain voltage.
- Need to control HS and LS independently to have dead time.



## Functional Block Diagram Inside Gate Driver

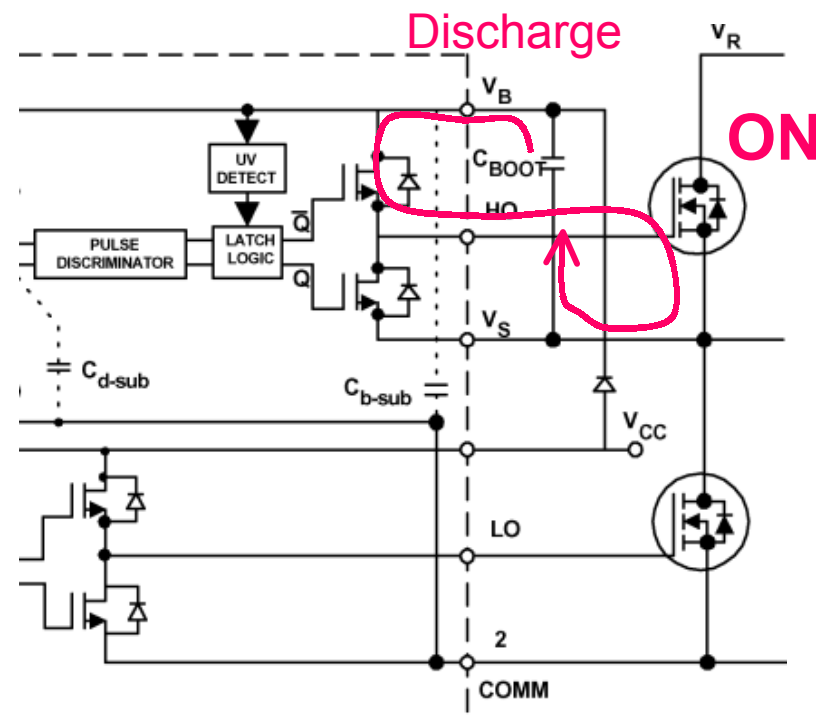
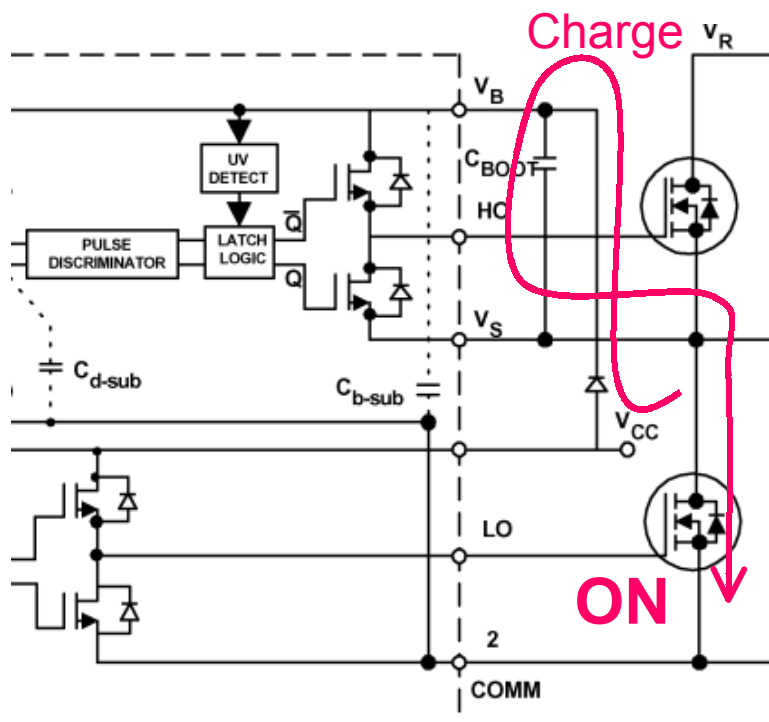
International Rectifier's family of MOS gate drivers integrate most of the functions required to drive one high side and one low side power MOSFET in a compact package.

With the addition of few components, they provide very fast switching speeds and low power dissipation.





## Boot Strap High Side Power Supply



When  $V_S$  is pulled down to ground through the low side FET, the bootstrap capacitor ( $C_{BOOT}$ ) charges through the bootstrap diode ( $D_b$ ) from the  $V_{CC}$  supply, thus providing a supply to  $V_B$ .

## Boot Strap High Side Power Supply (Cont'd)

- Boot Strap Capacitor Selection**

$$C \geq \frac{2 \left[ 2Q_g + \frac{I_{qbs(max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f} \right]}{V_{cc} - V_f - V_{LS} - V_{Min}} \quad \text{EQ(2)}$$

Where:

$V_f$  = Forward voltage drop across the bootstrap diode       $V_{LS}$  = Voltage drop across FET  
 (or load for a high side driver)

$V_{Min}$  = Minimum voltage between  $V_B$  and  $V_S$

To minimize the risk of overcharging and further reduce ripple on the  $V_{bs}$  voltage the  $C_{bs}$  value obtained from the above equation should be multiplied by a factor of 15 (rule of thumb).

- Boot Strap Diode Selection**

The bootstrap diode ( $D_{bs}$ ) needs to be able to block the full power rail voltage, which is seen when the high side device is switched on. It must be a fast recovery device to minimize the amount of charge fed back from the bootstrap capacitor into the  $V_{cc}$  supply.

$VRRM$  = Power rail voltage,  $\max t_{rr} = 100\text{ns}$ ,  $I_F > Q_{bs} \times f$

For more details on boot strap refer to DT98-2

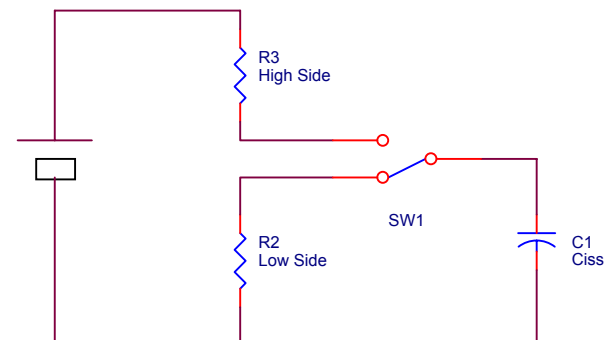
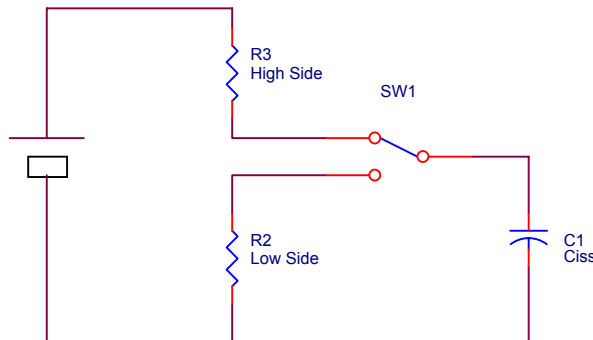
### Power Dissipation in Gate Driver

- Whenever a capacitor is charged or discharged through a resistor, half of energy that goes into the capacitance is dissipated in the resistor. Thus, the losses in the gate drive resistance, internal and external to the MGD, for one complete cycle is the following:

$$P_G = V \cdot f_{SW} \cdot Q_G$$

For two IRF540 HEXFET® MOSFETs operated at 400kHz with  $V_{gs} = 12V$ , we have:

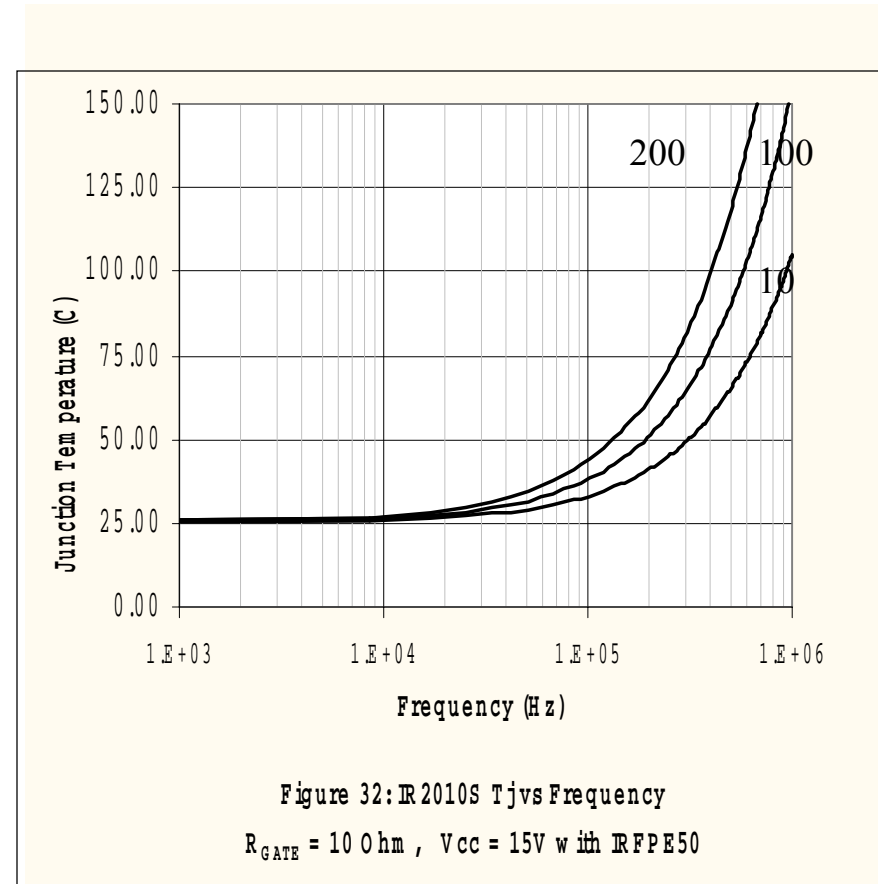
$$P_G = 2 \cdot 12 \cdot 37 \cdot 10^{-9} \cdot 400 \cdot 10^3 = 0.36W$$



For more details on gate driver ICs, refer to AN978

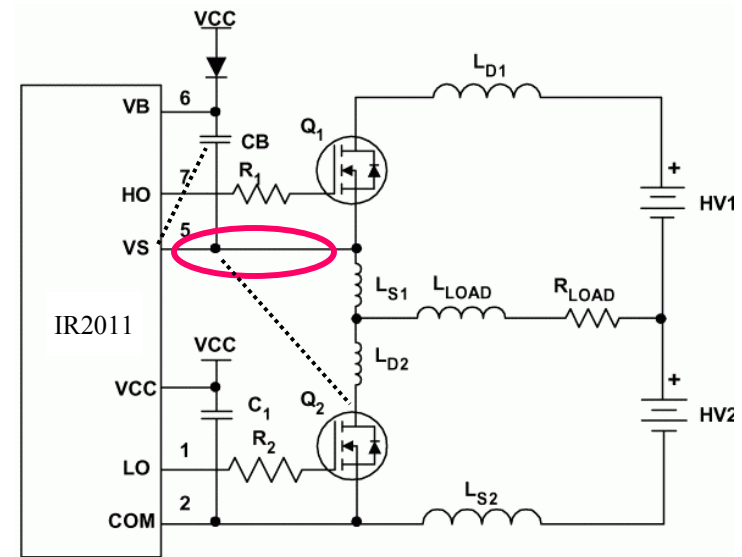
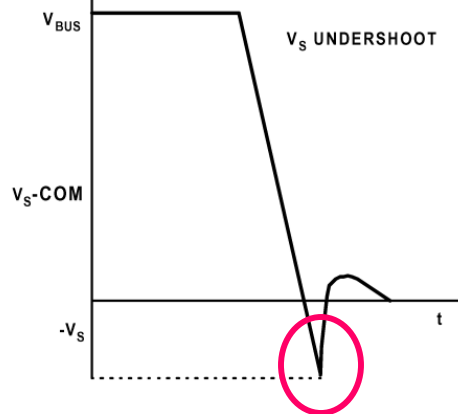
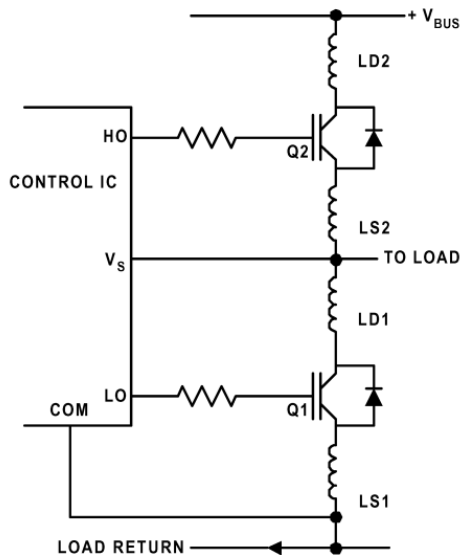
### Power Dissipation in Gate Driver (Cont'd)

- The use of gate resistors reduces the amount of gate drive power that is dissipated inside the MGD by the ratio of the respective resistances.
- These losses are not temperature dependent.



## Layout Considerations

- Stray inductance LD1+LS1 contribute to undershoot of the Vs node beyond the ground



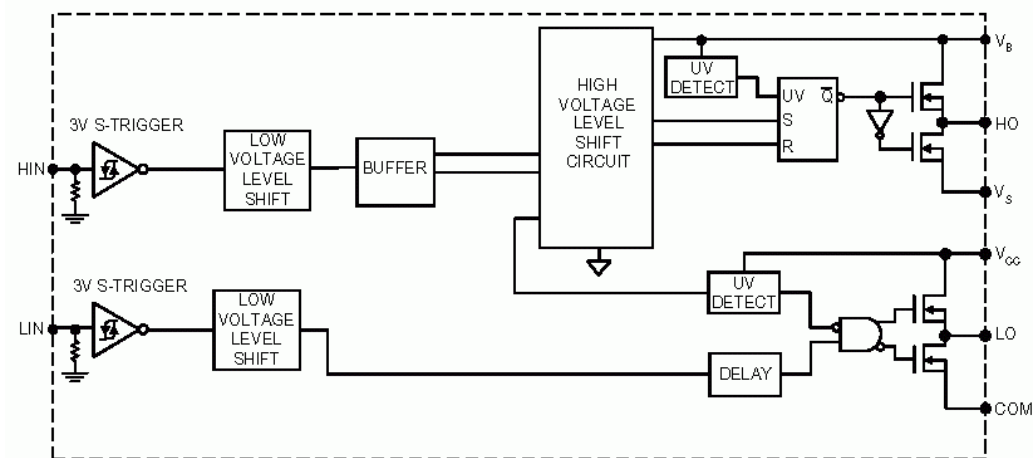
As with any CMOS device, driving any of parasitic diodes into forward conduction or reverse breakdown may cause parasitic SCR latch up.

## Gate Driver for Class D Applications

### IR2011(S)

#### Key Specs

$V_{OFFSET}$	200V max.
$I_{O+/-}$	1.0A /1.0A typ.
$V_{OUT}$	10 - 20V
$t_{on/off}$	80 & 60 ns typ.
Delay Matching	20 ns max.

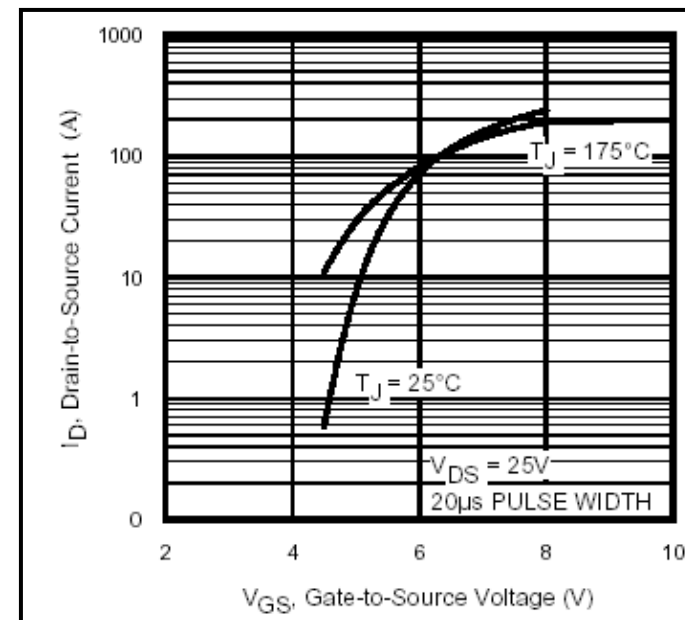
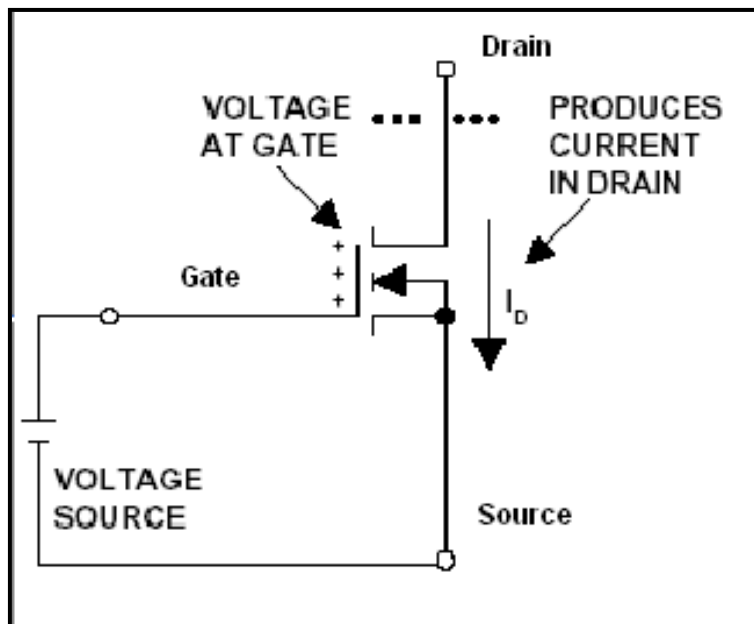


- Fully operational up to +200V
- Low power dissipation at high switching frequency
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Tolerant to negative transient voltage, dV/dt immune
- SO-8/DIP-8 Package



## How MOSFETs Work

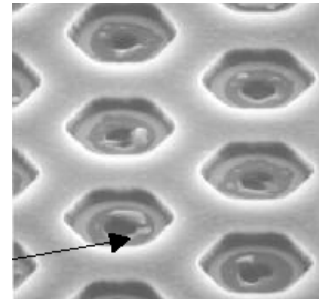
- A MOSFET is a voltage-controlled power switch. A voltage must be applied between Gate and Source terminals to produce a flow of current in the Drain.



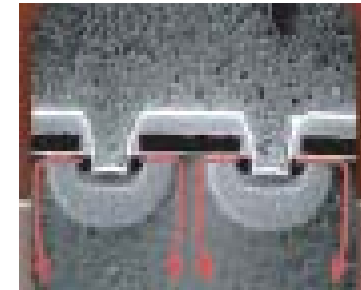
## MOSFET Technologies (1)

- IR is striving to continuously improve the power MOSFET to enhance the performance, quality and reliability.

- Hexagonal Cell Technology



- Planar Stripe Technology



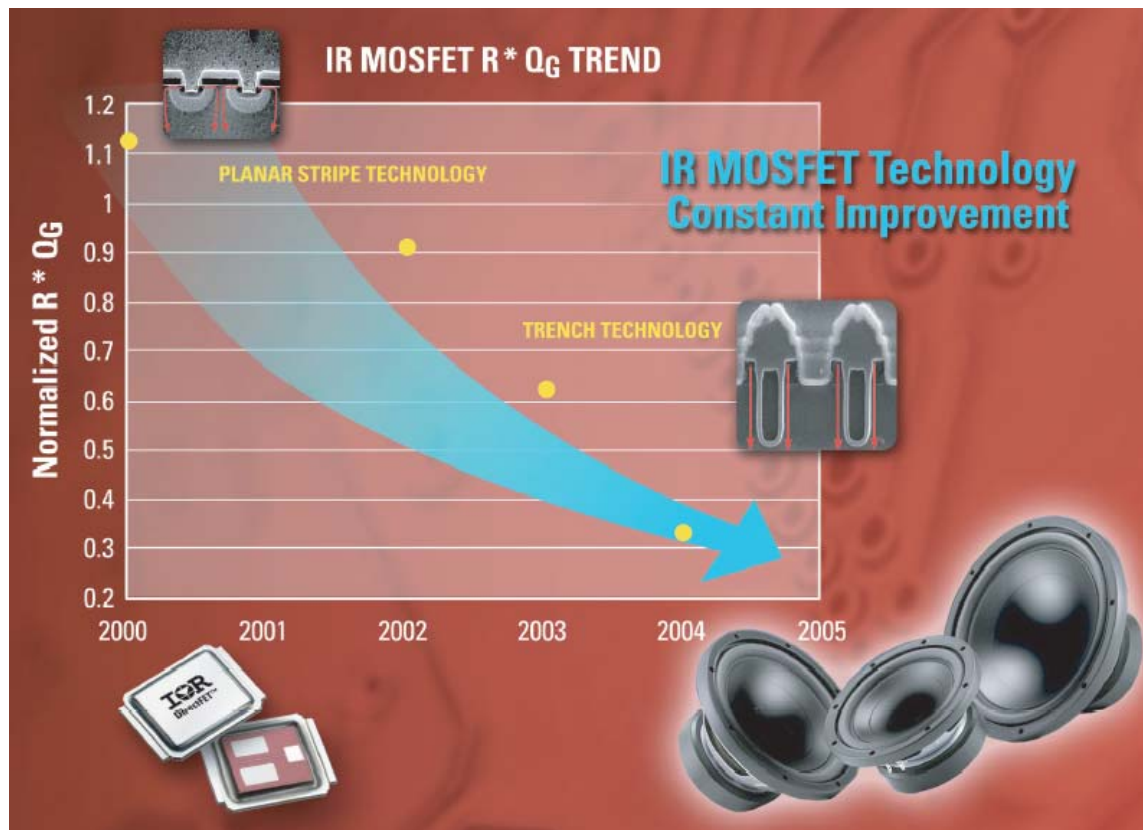
- Trench Technology





## MOSFET Technologies (2)

- Power MOSFET FOMs ( $R \cdot Q_g$ ) have significantly improved between the released IR MOSFET technologies



## Key Parameters of MOSFETs (1)

- **Voltage Rating,  $BV_{DSS}$**

**This is the drain-source breakdown voltage (with  $V_{GS} = 0$ ).  $BV_{DSS}$  should be greater than or equal to the rated voltage of the device, at the specified leakage current, normally measured at  $I_d = 250\mu A$ .**

**This parameter is temperature-dependent and frequently  $\Delta BV_{DSS} / \Delta T_j$  ( $V/^\circ C$ ) is specified on datasheets.**

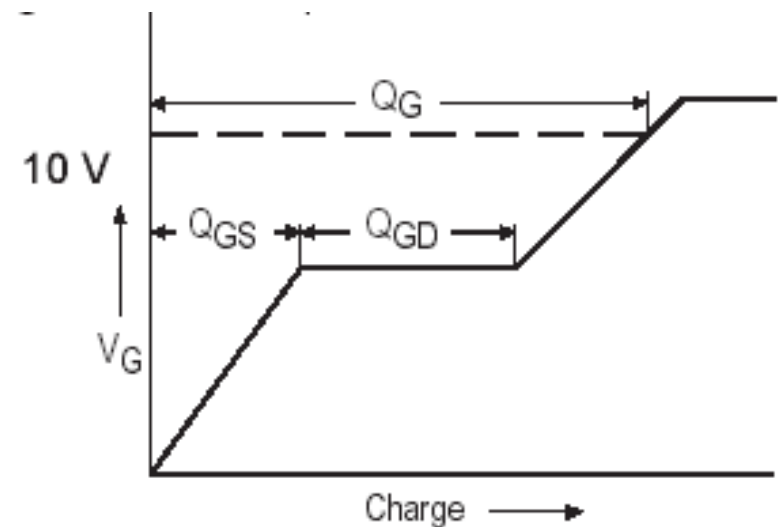
**$BV_{DSS}$  MOSFET voltages are available from tens to thousand volts.**

## Key Parameters of MOSFETs (2)

- Gate Charge,  $Q_g$

This parameter is directly related to the MOSFET speed and is temperature-independent. Lower  $Q_g$  results in faster switching speeds and consequently lower switching losses.

The total gate charge has two main components: the gate-source charge,  $Q_{gs}$  and, the gate-drain charge,  $Q_{gd}$  (often called the Miller charge).



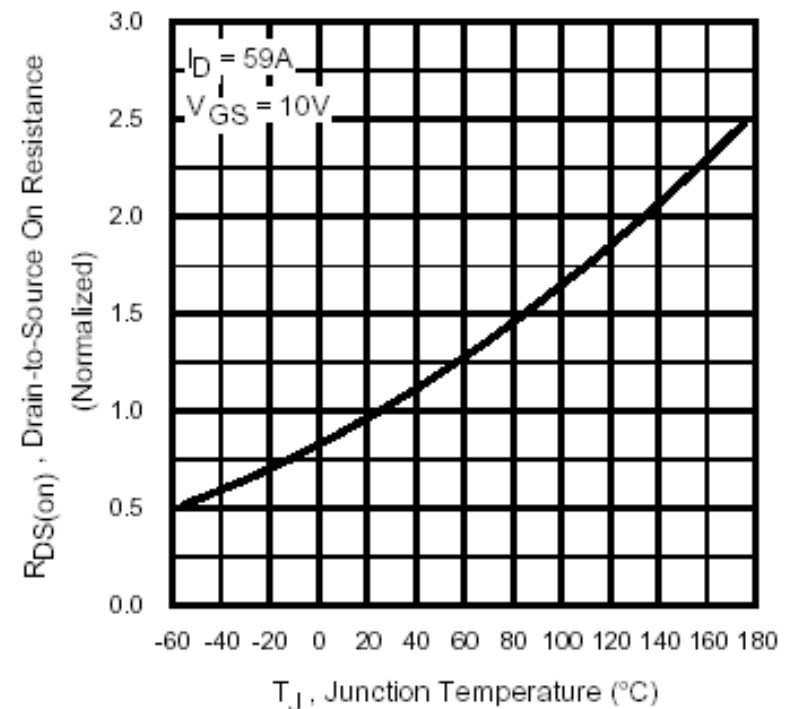
Basic Gate Charge Waveform

## Key Parameters of MOSFETs (3)

- **Static Drain-to-Source On-Resistance,  $R_{DS(ON)}$**

This is the drain-source resistance, typically specified on data sheet at  $25^{\circ}\text{C}$  with  $V_{GS} = 10\text{V}$ .

$R_{DS(ON)}$  parameter is temperature-dependent, and is directly related to the MOSFET conduction losses. lower  $R_{DS(ON)}$  results in lower conduction losses.



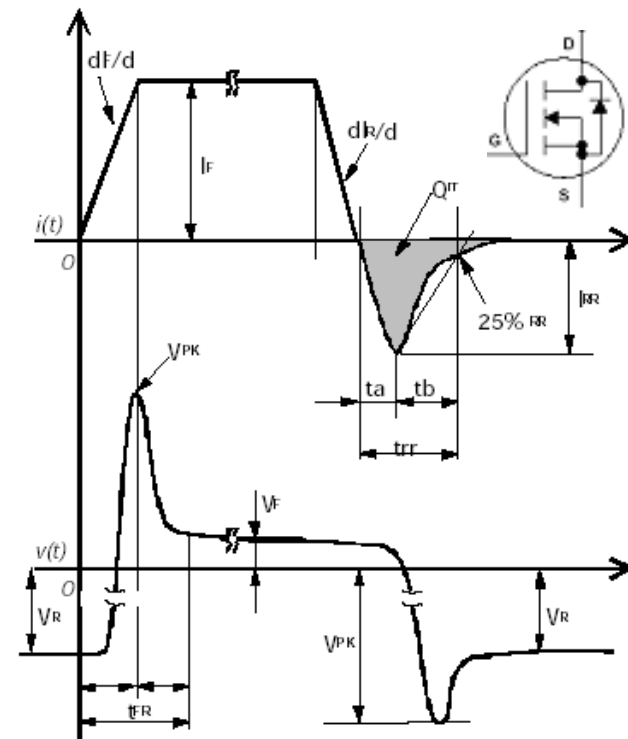
Normalized On-Resistance vs. Temperature

## Key Parameters of MOSFETs (4)

- **Body Diode Reverse Recovery Characteristics,  $Q_{rr}$ ,  $t_{rr}$ ,  $I_{rr}$  and S factor.**

Power MOSFETs inherently have an integral reverse body-drain diode. This body diode exhibits reverse recovery characteristics. Reverse Recovery Charge  $Q_{rr}$ , Reverse Recovery Time  $t_{rr}$ , Reverse Recovery Current  $I_{rr}$  and Softness factor ( $S = t_b/t_a$ ), are typically specified on data sheets at  $25^\circ\text{C}$  and  $di/dt = 100\text{A}/\mu\text{s}$ .

Reverse recovery characteristics are temperature-dependent and lower  $t_{rr}$ ,  $I_{rr}$  and  $Q_{rr}$  improves THD, EMI and Efficiency  $\eta$ .



**Typical Voltage –Current Waveforms for a MOSFET Body Diode**

[www.irf.com](http://www.irf.com)

## Key Parameters of MOSFETs (5)

- **Package**

MOSFET devices are available in several packages as SO-8, TO-220, D-Pak, I-Pak, TO-262, DirectFET™, etc.

The selection of a MOSFET package for a specific application depends on the package characteristics such as dimensions, power dissipation capability, current capability, internal inductance, internal resistance, electrical isolation and mounting process.



### Choosing the MOSFET Voltage Rating for Class D applications (1)

- **MOSFET voltage rating for a Class D amplifier is determined by:**
  - **Desired  $P_{OUT}$  and load impedance (i.e. 250W on 4Ω)**
  - **Topology (Full Bridge or Half Bridge)**
  - **Modulation Factor M (80-90%)**

$$V_{B_{DSS\ min}} = \sqrt{\frac{2 * P_{OUT} * R_{LOAD}}{M}} * 1.5$$

*Typical additional factor due to stray resistance, power supply fluctuations and MOSFET Turn-Off peak voltage*

### Choosing the MOSFET Voltage Rating for Class D Applications (2)

- Full-Bridge Topology Class D amplifier**

Output Power (W)	BVDSS Minimum				
	Load (Ohms)				
	1	2	4	6	8
100	25.0	35.3	49.9	61.1	70.6
150	30.6	43.2	61.1	74.9	86.5
200	35.3	49.9	70.6	86.5	99.8
500	55.8	78.9	111.6	136.7	157.8
1000	78.9	111.6	157.8	193.3	223.2

Corresponding IR MosFET BVDSS					
Load (Ohms)					
1	2	4	6	8	
30	40	55	75	75	
40	55	75	75	100	
40	55	75	100	100	
75	100	150	150	200	
100	150	200	200	250	

- Half-Bridge Configuration Class D amplifier**

Output Power (W)	VBDSS Minimum				
	Load (Ohms)				
	1	2	4	6	8
100	49.9	70.6	99.8	122.3	141.2
150	61.1	86.5	122.3	149.7	172.9
200	70.6	99.8	141.2	172.9	199.7
500	111.6	157.8	223.2	273.4	315.7
1000	157.8	223.2	315.7	386.6	446.4

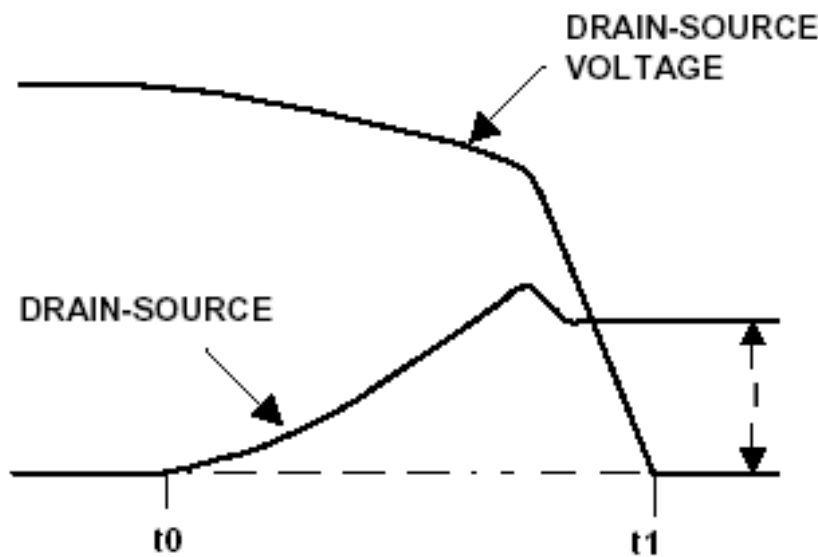
Corresponding IR MosFET BVDSS					
Load (Ohms)					
1	2	4	6	8	
55	75	100	150	150	
75	100	150	150	200	
75	100	150	200	200	
150	200	250	300	400	
200	250	400	400	450	

Note 1. Modulation Factor M = 85%

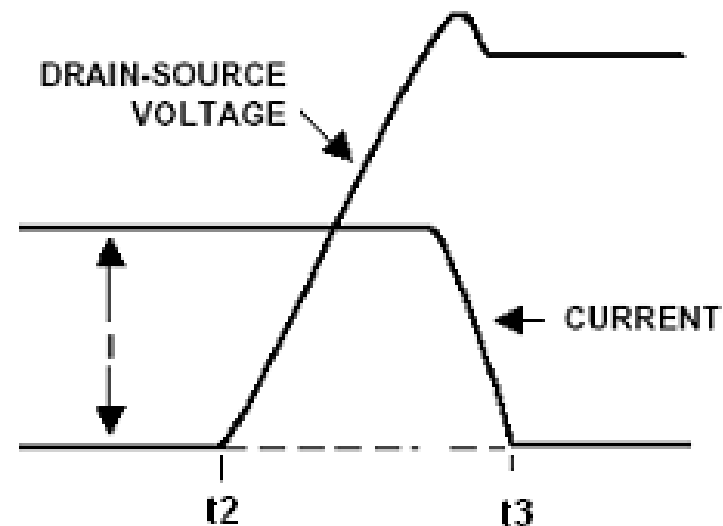


## Calculation of Switching Loss (1)

- **Switching Losses are the result of turn-on and turn-off switching times**



MOSFET Turn-On



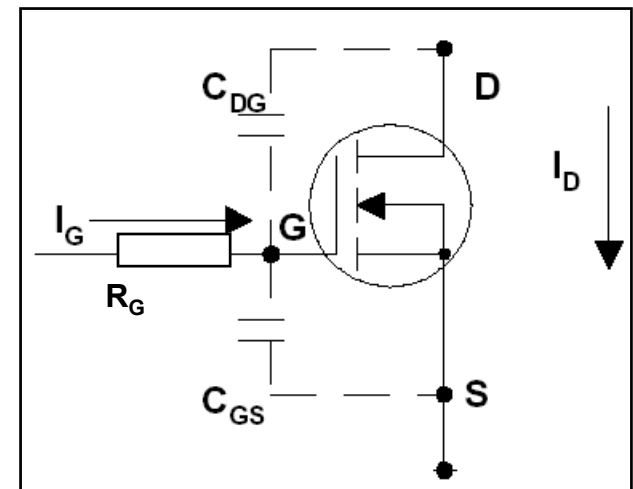
MOSFET Turn-Off

## Calculation of Switching Loss (2)

- Gate resistance  $R_g$ , and gate charge  $Q_g$ , have a significant influence on turn-on and turn-off switching times

$\uparrow R_g \Rightarrow \downarrow I_g \Rightarrow \uparrow t_{\text{SWITCHING}} \Rightarrow \uparrow P_{\text{SWITCHING}}$

$\uparrow Q_g \Rightarrow \uparrow t_{\text{SWITCHING}} \Rightarrow \uparrow P_{\text{SWITCHING}}$



## Estimation of Switching Losses (1)

- **Switching losses can be obtained by calculating the switching energy dissipated in the MOSFET**

$$E_{sw} = \int_0^t V_{DS}(t) * I_D(t) dt$$

**Where t is the length of the switching pulse.**

- **Switching losses can be obtained by multiplying switching energy with switching frequency.**

$$P_{SWITCHING} = E_{sw} * F_{sw}$$

## Estimation of Conduction Loss (2)

- **Conduction losses can be calculated using  $R_{DS(ON)}$  @  $T_j$  max and  $I_{D RMS}$  current of MOSFET**

$$P_{CONDUCTION} = (I_{D RMS})^2 * R_{DS(ON)}$$

**$I_{D RMS}$  is determined using amplifier specifications:**

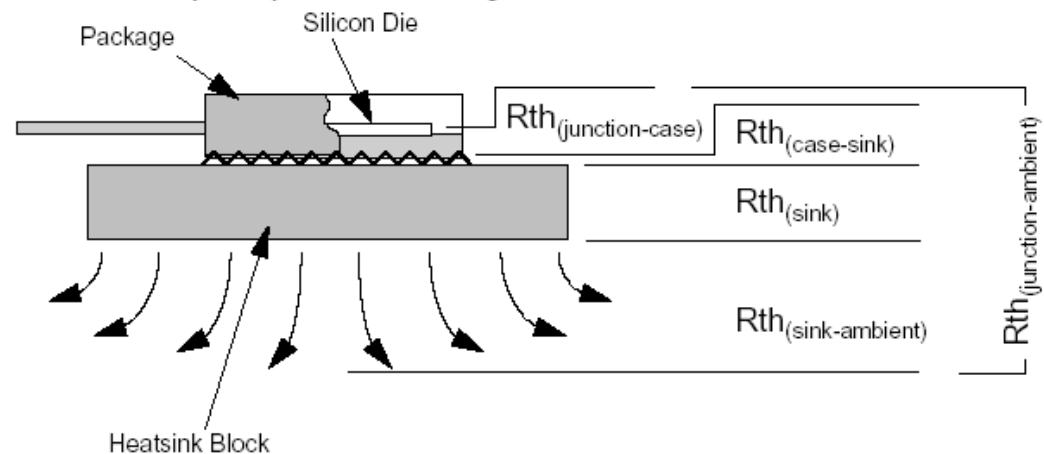
$$I_{D RMS} = \sqrt{\frac{P_{OUT}}{R_{LOAD}}}$$

**$R_{DS(ON)}$  data can be obtained from the MOSFET data sheet.**

### Thermal Design

- Maximum allowed power dissipation for a MOSFET mounted on a heat sink:

$$P_{\max} = \Delta T_j / R_{\text{thja max}}$$



$$P_{\max} = (T_{\text{amb}} - T_{j_{\max}}) / (R_{\text{thjc max}} + R_{\text{thcs max}} + R_{\text{ths max}} + R_{\text{thsa max}})$$

Where:  $T_{\text{amb}}$  = Ambient Temperature

$T_{j_{\max}}$  = Max. Junction Temperature

$R_{\text{thjc max}}$  = Max. Thermal Resistance Junction to Case

$R_{\text{thcs max}}$  = Max. Thermal Resistance Case to Heatsink

$R_{\text{ths max}}$  = Max. Thermal Resistance of Heatsink

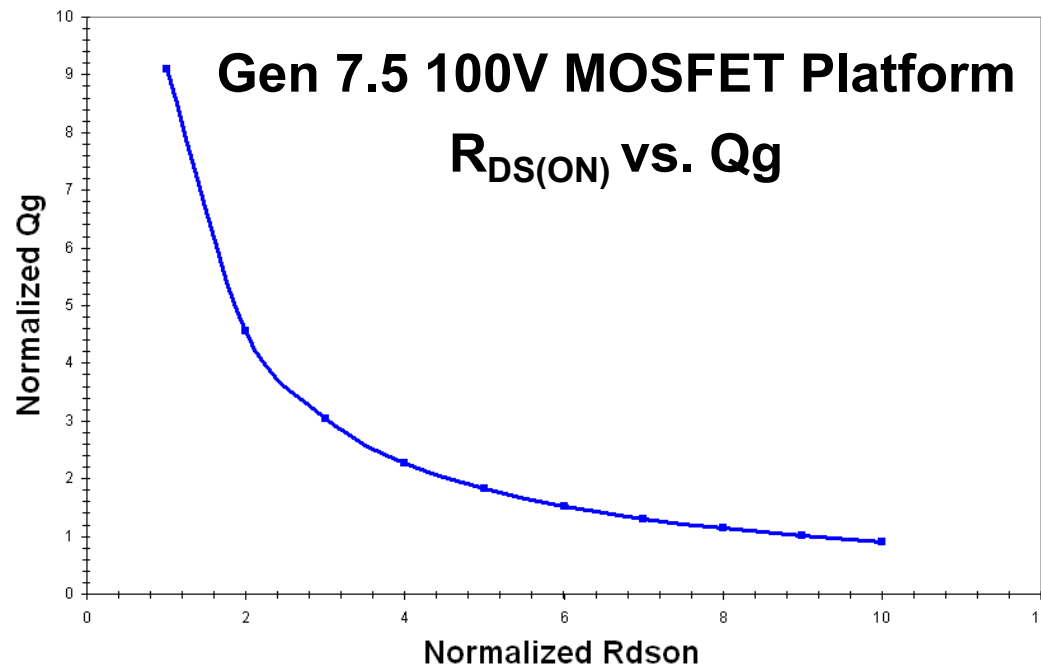
$R_{\text{thsa max}}$  = Max. Thermal Resistance Heatsink to Ambient

### $R_{DS(ON)}$ vs $Q_g$

- There is tradeoff between Static Drain-to-Source On-Resistance,  $R_{DS(ON)}$  and Gate charge,  $Q_g$

Higher  $R_{DS(ON)} \Rightarrow$  Lower  $Q_g \Rightarrow$  Higher  $P_{CONDUCTION}$  & Lower  $P_{SWITCHING}$

Lower  $R_{DS(ON)} \Rightarrow$  Higher  $Q_g \Rightarrow$  Higher  $P_{SWITCHING}$  & Lower  $P_{CONDUCTION}$

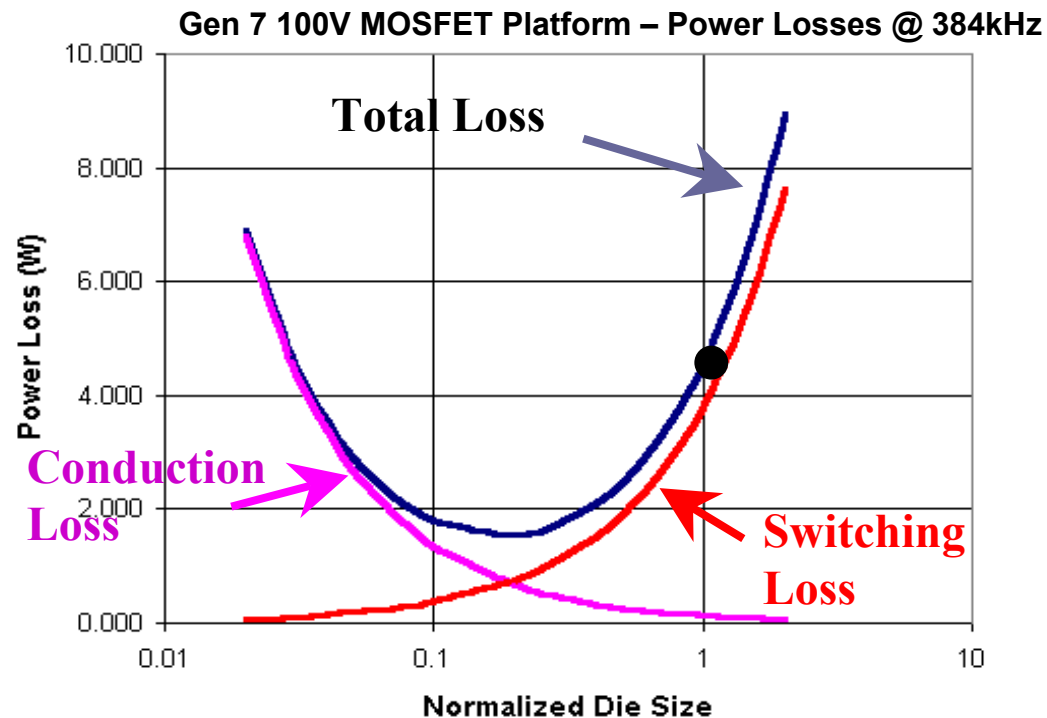


### Die Size vs Power Loss (1)

- Die size has a significant influence on MOSFET power losses

Smaller Die ⇒ Higher  $P_{\text{CONDUCTION}}$  & Lower  $P_{\text{SWITCHING}}$

Bigger Die ⇒ Higher  $P_{\text{SWITCHING}}$  & Lower  $P_{\text{CONDUCTION}}$

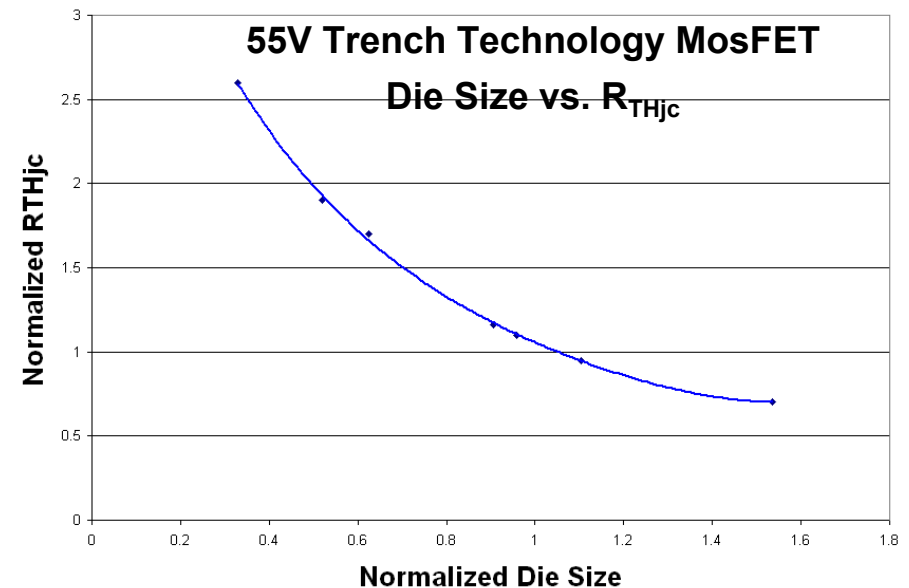
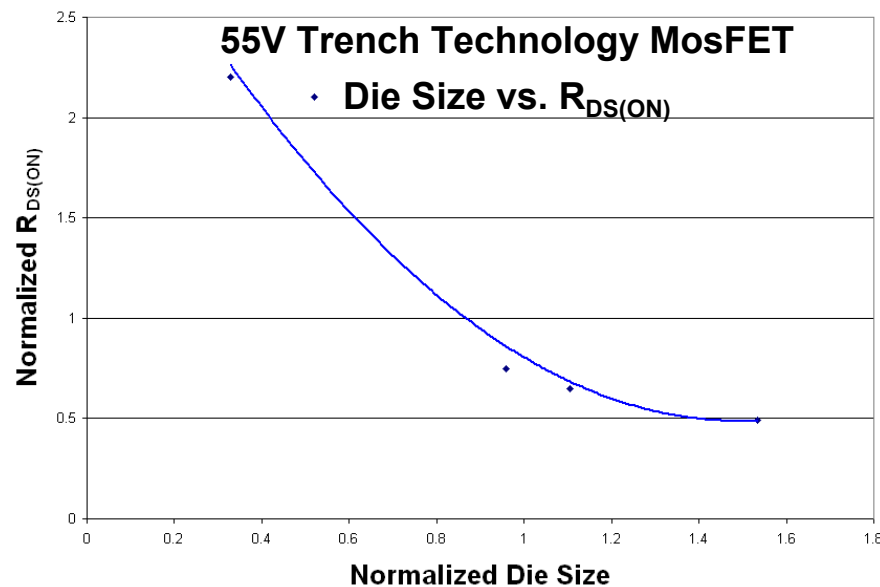


### Die Size vs Power Loss (2)

- Die size is directly related with  $R_{DS(ON)}$  and  $R_{THjc}$  of the MOSFET

Smaller Die ⇒ Higher  $R_{DS(ON)}$  and Higher  $R_{THjc}$

Bigger Die ⇒ Lower  $R_{DS(ON)}$  and Lower  $R_{THjc}$





## Choosing the Right MOSFET for Class D Applications (1)

- **The criteria to select the right MOSFET for a Class D amplifier application are:**
  - $V_{B_{DSS}}$  should be selected according to amplifier operating voltage, and it should be large enough to avoid avalanche condition during operation
  - Efficiency  $\eta$  is related to static drain-to-source on-resistance,  $R_{DS(ON)}$ . smaller  $R_{DS(ON)}$  improves efficiency  $\eta$ .  $R_{DS(ON)}$  is recommended to be smaller than 200m $\Omega$  for mid and high-end power, full-bandwidth amplifiers
  - Low gate charge,  $Q_g$ , improves THD and efficiency  $\eta$ .  $Q_g$  is recommended to be smaller than 20nC for mid and high-end power, full-bandwidth amplifiers

## Choosing the Right MOSFET for Class D Application (2)

- Amplifier performance such as THD, EMI and efficiency  $\eta$  are also related to MOSFET reverse recovery characteristics. Lower  $t_{rr}$ ,  $I_{rr}$  and  $Q_{rr}$  improves THD, EMI and efficiency  $\eta$
- $R_{thjc}$  should be small enough to dissipate MOSFET power losses and keep  $T_j < \text{limit}$
- Better reliability and lower cost are achieved with higher MOSFET  $T_j \text{ max}$
- Finally, selection of device package determines the dimensions, electrical isolation and mounting process. These factors should be considered in package selection. Because cost, size and amplifier performance depend on it.

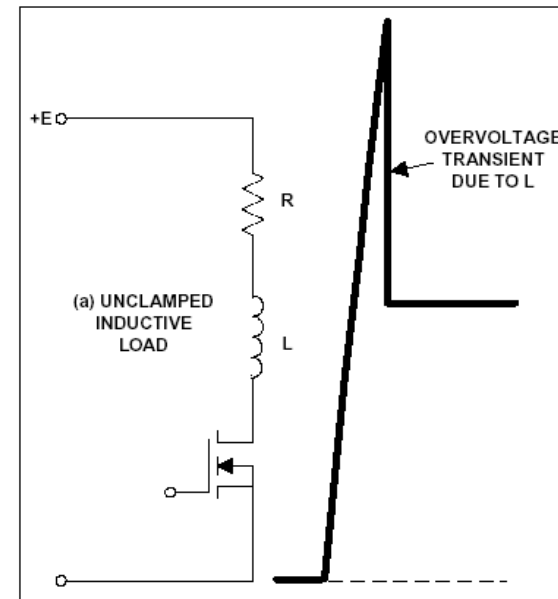
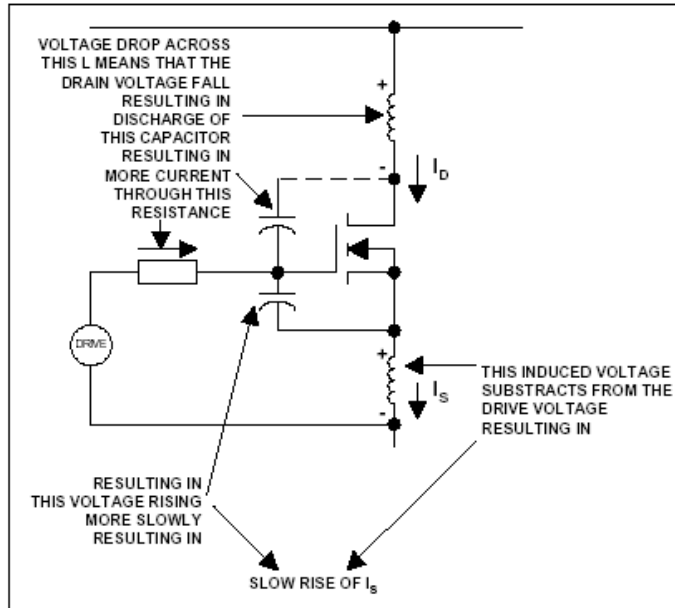
## Development of Class D Dedicated Devices

- **Performance of the Class D amplifying stage strongly depends on the characteristics of MOSFETs and ICs.**
- **Designers of driver IC and MOSFET silicon need to keep the special requirements of the Class D application in mind.**

## Influences of Stray Inductance

- **PCB layout and the MOSFET internal package inductances contribute to the stray inductance ( $L_s$ ) in the circuit.**
- **Stray inductances affect the MOSFET performance and EMI of the system.**

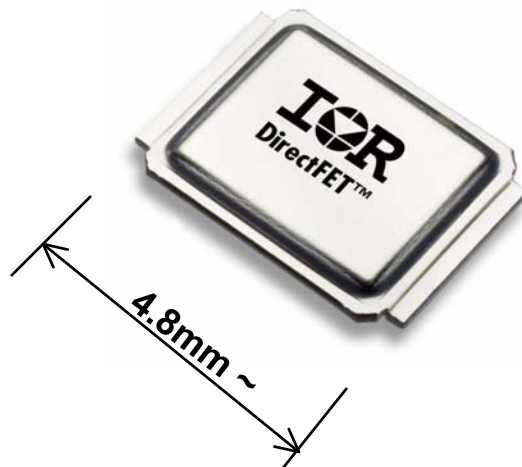
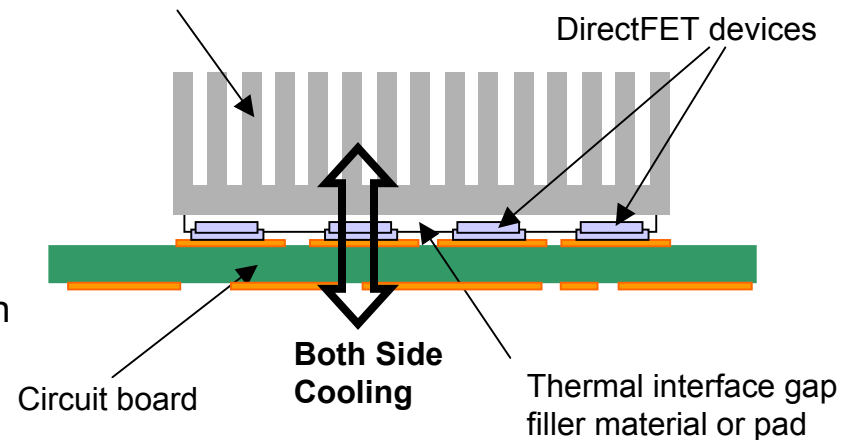
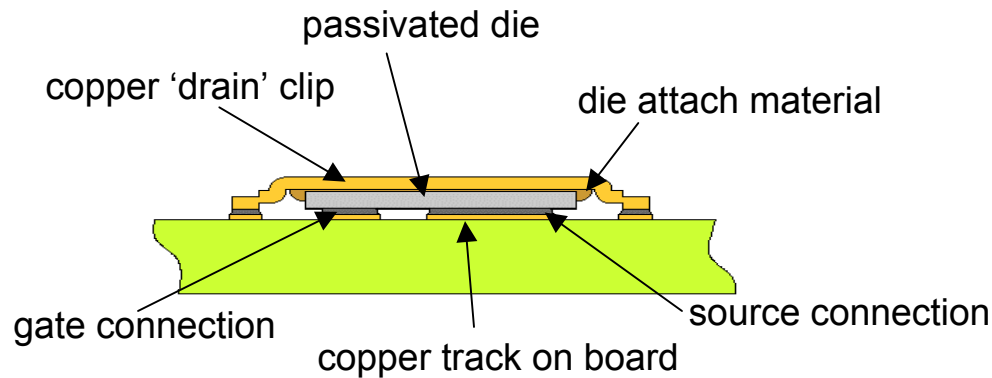
## Influences of Stray Inductance



- Drain and source stray inductances reduces the gate voltage during turn-on resulting in longer switching time.
- Also during turn-off, drain and source stray inductances generate a large voltage drop due to  $dI_D/dt$ , producing drain to source over-voltage transients.

### DirectFET™ Packaging

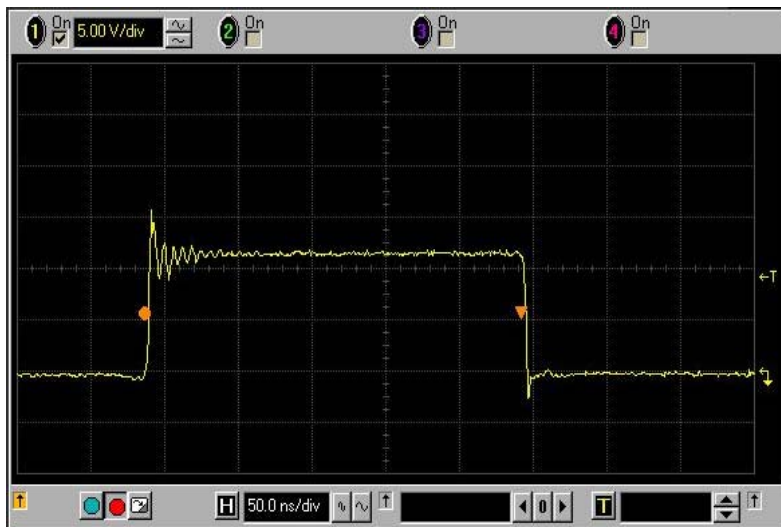
Use a single multiple-finned heat sink to dissipate heat from devices



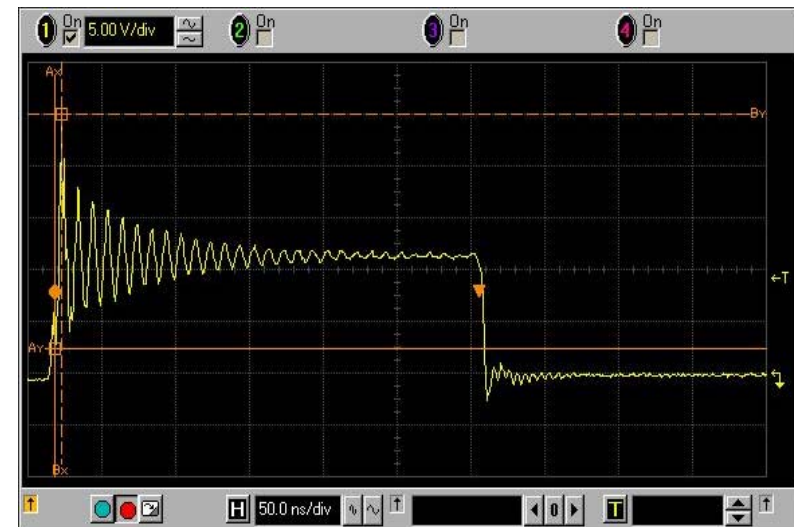
- Remove wirebonds from package and replace with large area solder contacts
- Reduced package inductance and resistance
- Copper can enables **dual sided cooling**

### DirectFET™ Packaging

**DirectFET waveform**



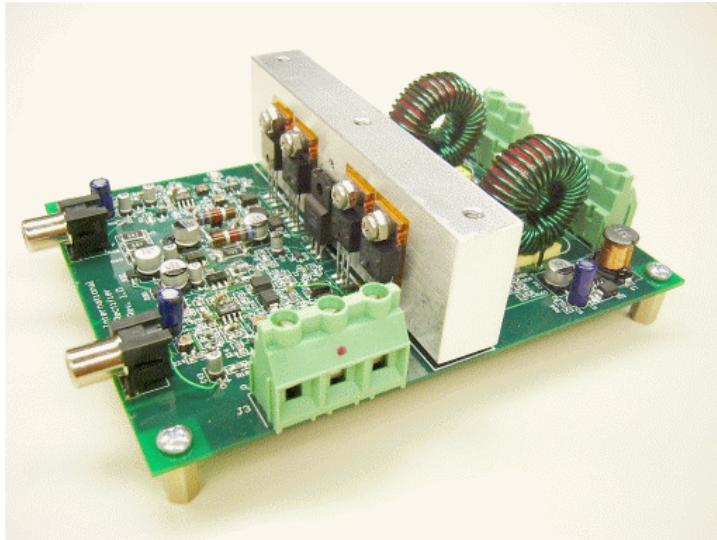
**SO-8 waveform**



- 30A VRM output current
- 500 kHz per phase
- Silicon of the near identical active area, voltage and generation used in both packages
- Inductance related ringing greater in case of SO-8

## Class D Amp Reference Design

- **Specs**



**Topology:** Half Bridge

**IR Devices:** IR2011S, IRFB23N15D

**Switching frequency:** 400kHz (Adjustable)

**Rated Output Power:** 200W+200W / 4 ohm

**THD:** 0.03% @1kHz, Half Power

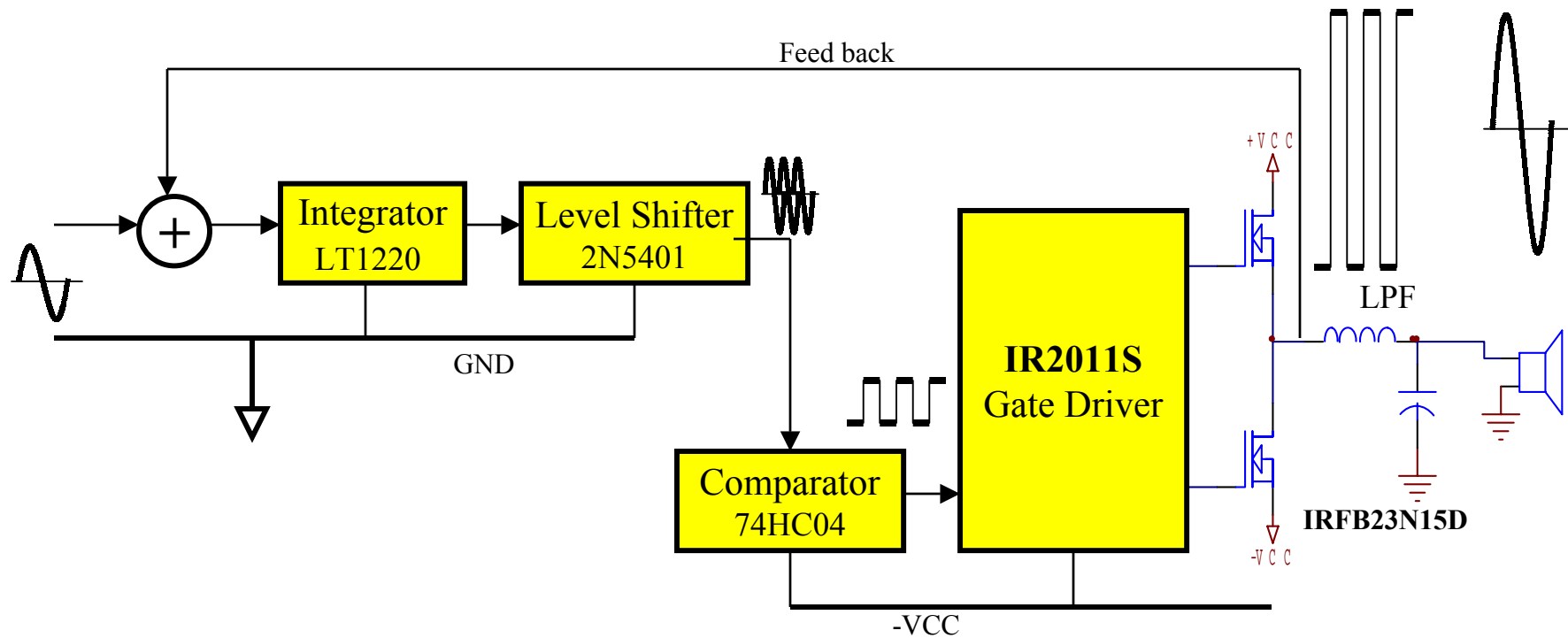
**Frequency Response:** 5Hz to 40kHz (-3dB)

**Power Supply:** ~ ±50V

**Size:** 4.0" x 5.5"



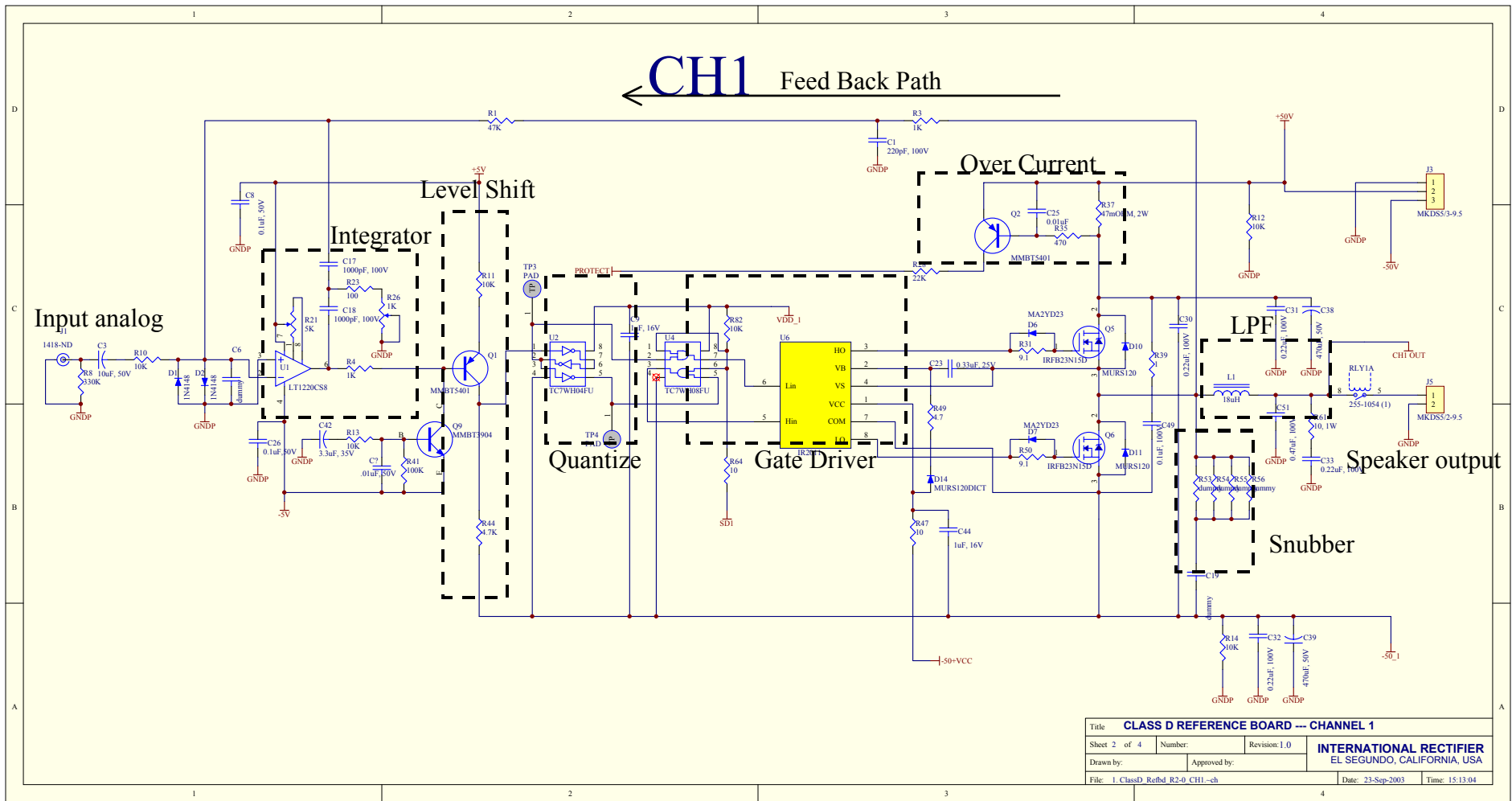
## Class D Amp Reference Board: Block Diagram



System → Gate Drive → MOSFET → Design Example

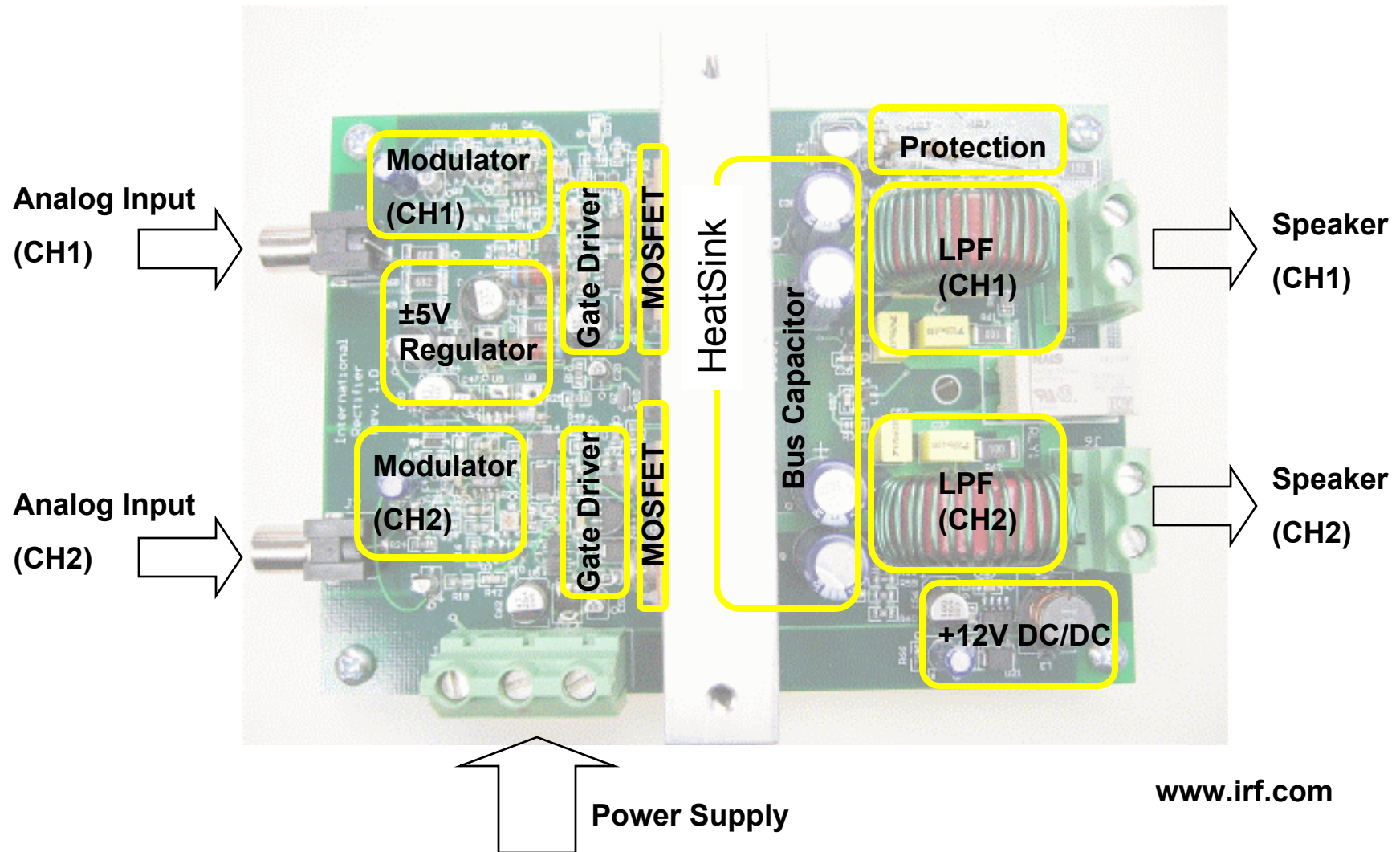
## Circuit Diagram

← CH1 Feed Back Path



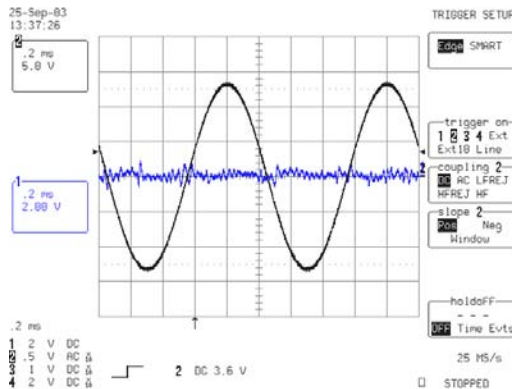
Title <b>CLASS D REFERENCE BOARD --- CHANNEL 1</b>			
Sheet 2 of 4	Number:	Revision: 1.0	<b>INTERNATIONAL RECTIFIER</b> EL SEGUNDO, CALIFORNIA, USA
Drawn by:	Approved by:		
File: 1_ClassD_RefBd_R2-0_CH1--ch			Date: 23-Sep-2003 Time: 15:13:04

# Class D Amp Reference Board: Layout

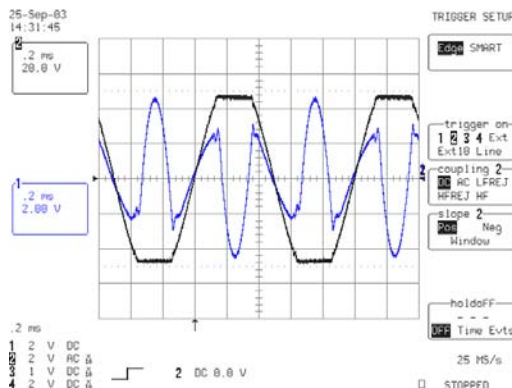


## Performance

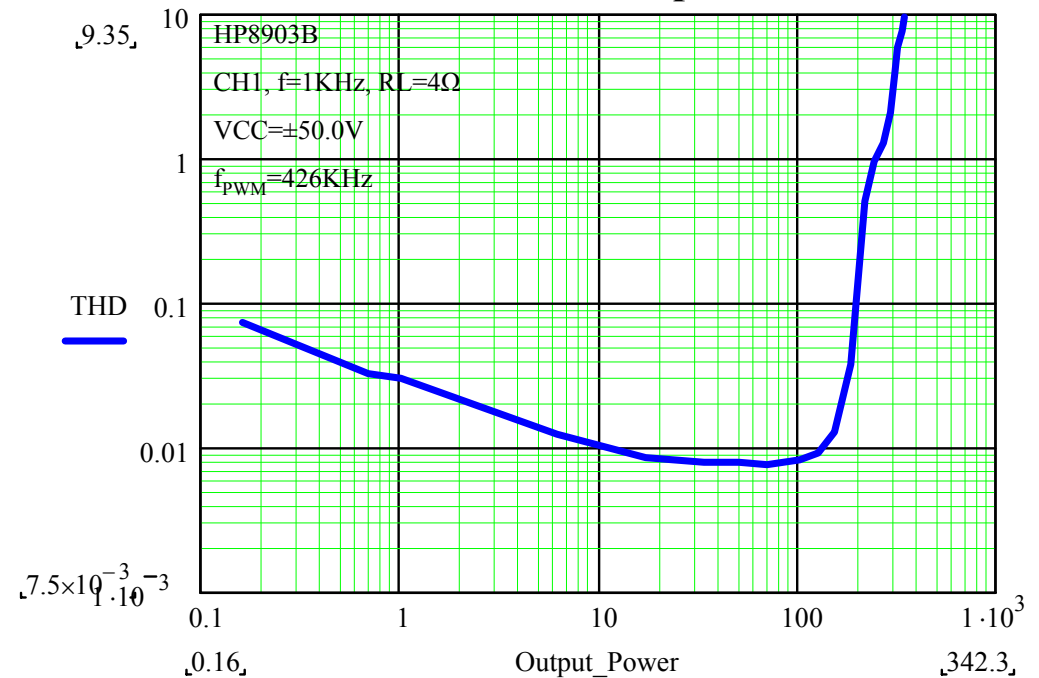
**50W / 4Ω, 1KHz, THD+N=0.0078%**



**342W / 4Ω, 1KHz, THD+N=10%**



**THD+N v.s. Output Power**



•Peak Output Power (f=1KHz)

120W / 8Ω / ch, THD=1%

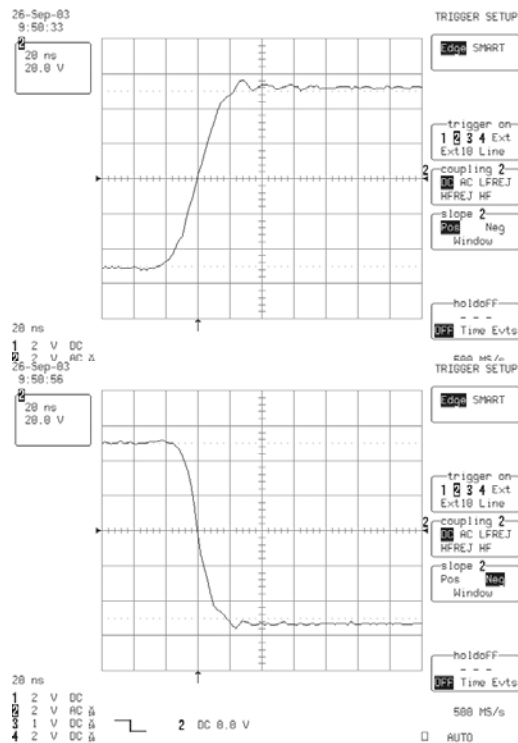
180W / 8Ω / ch, THD=10%

245W / 4Ω / ch, THD=1%

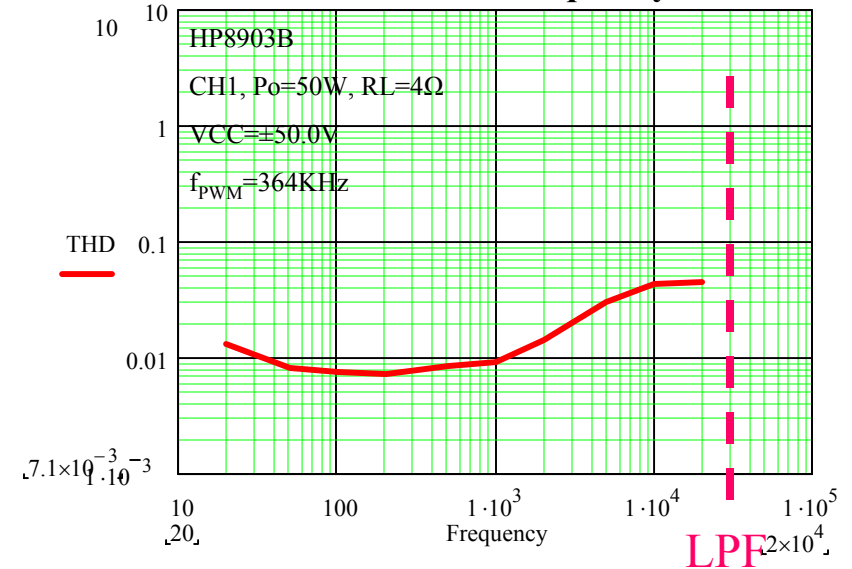
344W / 4Ω / ch, THD=10%

## Performance (Cont'd)

Switching waveform



THD+N v.s. Frequency



Residual Noise: 62.5μVrms, A-Weighted,  
30KHz-LPF

## Conclusion

- Highly efficient Class D amplifiers now provide similar performance to conventional Class AB amplifiers -  
If key components are carefully selected and the layout takes into account the subtle, yet significant impact due to parasitic components.

Constant innovation in semiconductor technologies helps the growing Class D amplifiers usage due to improvements in higher efficiency, increased power density and better audio performance.